AT91SAM9XE Microcontroller Series Schematic Check List

1. Introduction

This application note is a schematic review check list for systems embedding Atmel's AT91SAM9XE series of ARM® Thumb®-based microcontrollers.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the AT91SAM9XE Series. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.

AT91 ARM Thumb-based Microcontrollers

Application Note

6420C–ATARM–01-Oct-09

2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the AT91SAM9XE Series Microcontrollers on Atmel's Web site.

Table 2-1 gives the associated documentation needed to support full understanding of this application note.

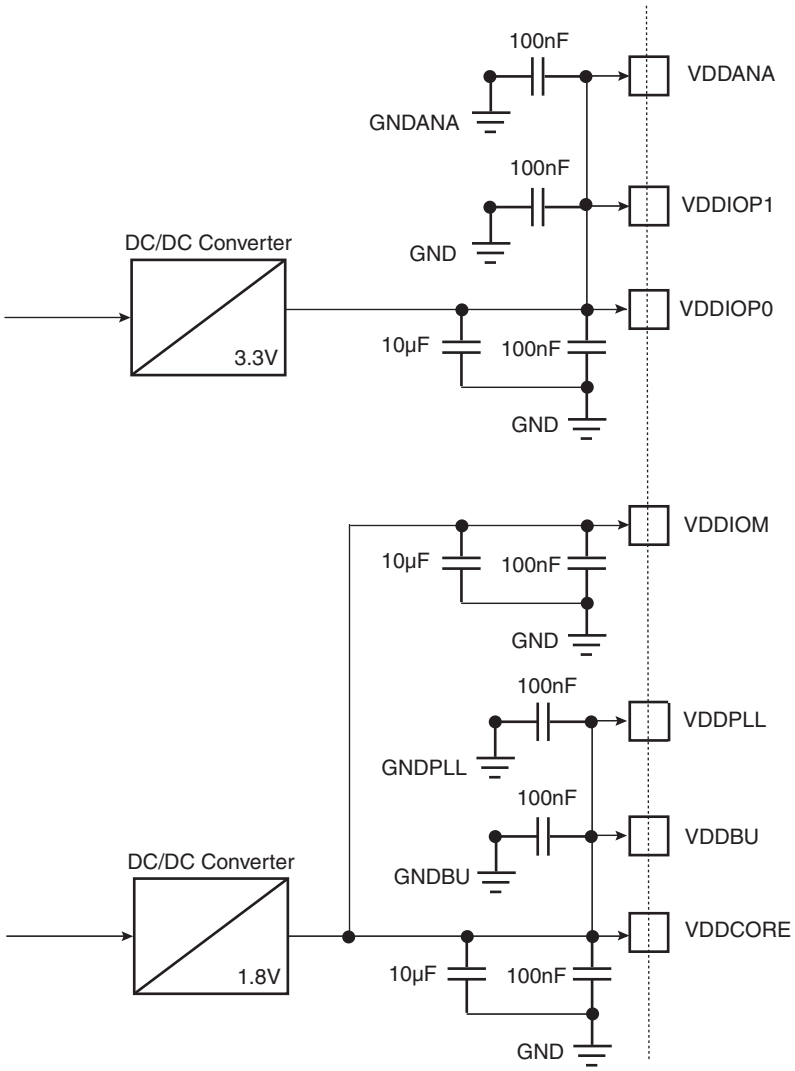
Table 2-1. Associated Documentation

Information	Document Title
User Manual Electrical/Mechanical Characteristics Ordering Information Errata	AT91SAM9XE Series Product Datasheet
Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM9EJ-S™ Technical Reference Manual ARM926EJ-S™ Technical Reference Manual
Evaluation Kit User Guide	AT91SAM9XE-EK Evaluation Board User Guide
Using SDRAM on AT91SAM9 Microcontrollers	Using SDRAM on AT91SAM9 Microcontrollers
NAND Flash Support in AT91SAM9 Microcontrollers	NAND Flash Support in AT91SAM9 Microcontrollers

3. Schematic Check List

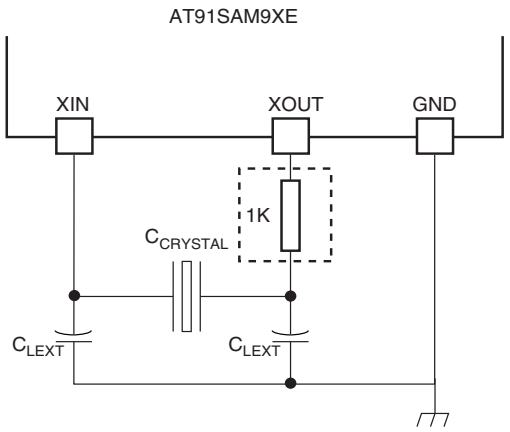
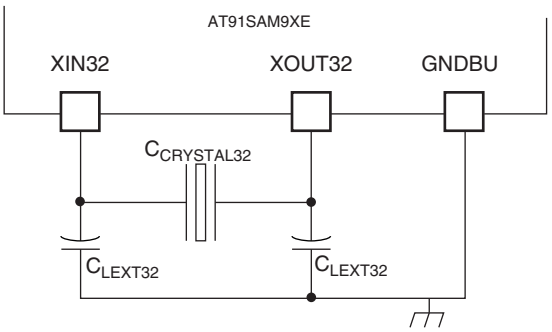
CAUTION: The AT91SAM9 board design must comply with the power-up and power-down sequence guidelines provided in the Electrical Characteristics section in the datasheet to guarantee reliable operation of the device.

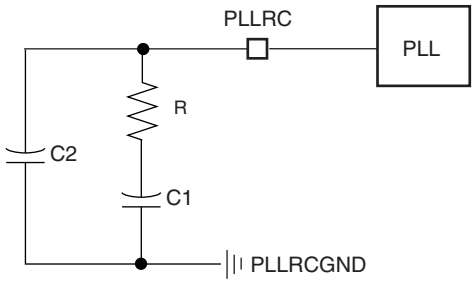
1.8V and 3.3V Dual Power Supply Schematic Example



1.8V and 3.3V Dual Power Supply Schematic Example

☑	Signal Name	Recommended Pin Connection	Description
	VDDCORE	1.65V to 1.95V (1.8V nominal) Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers the device. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDBU	1.65V to 1.95V (1.8V nominal) Decoupling capacitor (100 nF)[1][2]	Powers the Slow Clock oscillator and a part of the System Controller.
	VDDIOM[3]	1.65V to 1.95V or 3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers External Bus Interface I/O lines. Dual voltage range supported. The voltage ranges are selected by programming the VDDIOMSEL bit in the EBI_CSA register. At power-up, the selected voltage is 3.3V nominal, and power supply pins can accept either 1.8V or 3.3V. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIOP0[3][4]	3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers Peripheral I/O lines. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIOP1[3][4]	1.65V to 3.6V (1.8V, 2.5V, 3V or 3.3V nominal) Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers Peripheral I/O lines. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDPLL	1.65V to 1.95V (1.8V nominal) Decoupling capacitor (100 nF)[1][2]	Powers the PLL cell.
	VDDANA	3.0V to 3.6V Decoupling capacitor (100 nF)[1][2]	Powers the ADC cell.
	GND	Ground	GND pins are common to VDDCORE, VDDIOM, VDDIOP0 and VDDIOP1 pins. GND pins should be connected as shortly as possible to the system ground plane.
	GNDPLL	PLL ground	GNDPLL pin is provided for VDDPLL pin. GNDPLL pin should be connected as shortly as possible to the system ground plane.
	GNDANA	ADC analog ground	GNDANA pin is provided for VDDANA pin. GNDANA pin should be connected as shortly as possible to the system ground plane.
	GNDBU	Backup ground	GNDBU pin is provided for VDDBU pin. GNDBU pin should be connected as shortly as possible to the system ground plane.

☑	Signal Name	Recommended Pin Connection	Description
Clock, Oscillator and PLL			
	XIN XOUT Main Oscillator in Normal Mode	3 to 20MHz crystal Capacitors on XIN and XOUT (crystal load capacitance dependent) 1 kOhm resistor on XOUT only required for crystals with frequencies lower than 8 MHz.	Crystal Load Capacitance to check  Example: for an 18.432 MHz crystal with a load capacitance of $C_{CRYSTAL}$= 18 pF, external capacitors are required: C_{LEXT} = 10 pF. Refer to the electrical specifications of the AT91SAM9XE series datasheet.
	XIN XOUT Main Oscillator in Bypass Mode	XIN: external clock source XOUT: can be left unconnected.	1.8V (VDDPLL) square wave signal Duty Cycle: 40 to 60% Refer to the electrical specifications of the AT91SAM9XE datasheet.
	XIN32 XOUT32 Slow Clock Oscillator	32.768 kHz Crystal Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent)	Crystal load capacitance to check ($C_{CRYSTAL32}$).  Example: for an 32.768 kHz crystal with a load capacitance of $C_{CRYSTAL32}$= 12.5 pF, external capacitors are required: C_{LEXT32}= 17 pF. Refer to the electrical specifications of the AT91SAM9XE datasheet.

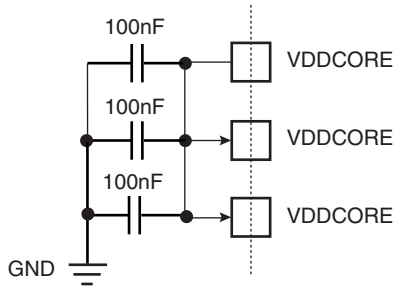
☑	Signal Name	Recommended Pin Connection	Description
	PLLRCA	Second-order filter Can be left unconnected if PLL not used.	See the Excel spreadsheet: “ATMEL_PLL_LFT_Filter_CALCULATOR_AT91_xxx.zip” (available in the software files on the Atmel Web site) allowing calculation of the best R-C1-C2 component values for the PLL Loop Back Filter.  R, C1 and C2 must be placed as close as possible to the pins.
	OSCSEL	Application dependent. Please refer to the I/O line considerations and errata section of the AT91SAM9XE datasheet.	Slow Clock Oscillator Selection. Must be tied to VDDBU to select the external 32,768 Hz crystal. Must be tied to GNDBU to select the on-chip RC oscillator.

☑	Signal Name	Recommended Pin Connection	Description
ICE and JTAG[5]			
	TCK	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TMS	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TDI	Pull-up (100 kOhm)[1]	No internal pull-up resistor.
	TD0	Floating	Output driven at up to V_{VDDIO1}
	JTAGSEL	**In harsh[6] environments, it is strongly recommended to tie this pin to GND if not used or to add an external low resistor value (such as 1 KOhm).**	Internal pull-down resistor (15 kOhm). Must be tied to V_{DDBU} to enter JTAG Boundary Scan.
	NTRST	Please refer to the I/O line considerations AT91SAM9XE datasheet.	Internal pull-up resistor to $V_{VDDIOP0}$ (15 kOhm)
Flash Memory			
	ERASE	Can be left unconnected for normal operations. **It is strongly recommended to tie this pin to GND in harsh[6] environments.** Must be tied to V_{VDDIO} to erase the General Purpose NVM bits (GPNVMx), the whole flash content and the security bit (SECURITY).	Internal pull-down resistor (15 kOhm). This pin is debounced by the RC oscillator to improve the glitch tolerance. Minimum debouncing time is 220 ms.
Reset/Test			
	NRST	Application dependant. Can be connected to a push button for hardware reset.	NRST is configured as an output at power up. NRST is controlled by the Reset Controller (RSTC). An internal pull-up resistor to $V_{VDDIOP0}$ (100 kOhm) is available for User Reset and External Reset control.
	TST	**In harsh[6] environments, it is strongly recommended to tie this pin to GND if not used or to add an external low resistor value (such as 1 KOhm).**	Internal pull-down resistor (15 kOhm).
Shutdown/Wakeup Logic			
	WKUP	0V to VDDBU	This pin is an input-only. WKUP behavior can be configured through the Shutdown Controller (SHDWC).
	SHDN	Application dependent. A typical application connects the pin SHDN to the shutdown input of the DC/DC Converter providing the main power supplies An external pull-up to VDDBU is needed and its value is to be higher than 1 MOhm. The resistor value is calculated according to the regulator enable implementation and the SHDN level.	The SHDN pin is a tri state output. No internal pull-up resistor. An external pull-up to VDDBU is needed. SHDN pin is driven low to GNDBU by the Shutdown Controller (SHDWC).

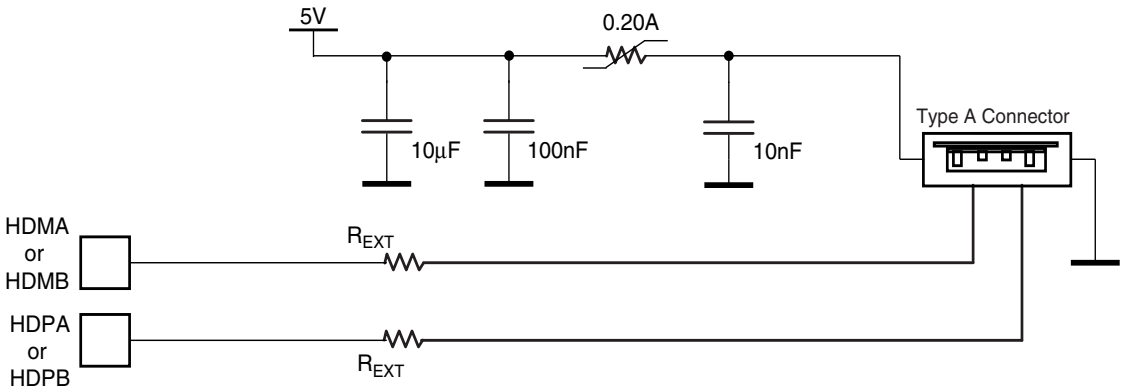
☑	Signal Name	Recommended Pin Connection	Description
		PIO	
	PAx PBx PCx	Application Dependant	All PIOs are pulled-up inputs at reset except those which are multiplexed with the Address Bus signals that require to be enabled as peripherals: PC4 (A23),PC5 (A24) and PC10 (A25). R pullup (typ) = 100 KOhm To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at '0' with internal pull-up disabled.
		EBI	
	D0-D15 (D16-D31)	Application dependent.	Data Bus (D0 to D31) Data bus lines D0 to D15 are pulled-up inputs to V_{VDDIOM} at reset. Note: Data bus lines D16 to D31 are multiplexed with the PIOC controller. Their I/O line reset state is input with pull-up enabled too.
	A0-A22 (A23-A25)	Application dependent.	Address Bus (A0 to A25) All address lines are driven to '0' at reset. Note: PC4 (A23),PC5 (A24) and PC10 (A25) are enabled by default at reset through the PIO controllers.
		SMC - SDRAM Controller - CompactFlash® Support - NAND Flash Support	
		See "External Bus Interface (EBI) Hardware Interface" on page 10.	
		USB Host (UHP)	
	HDPA HDPB	Application dependent[7]	To reduce power consumption, if USB Host is not used, connect HDPA/HDPB to GND.
	HDMA HDMB	Application dependent[7]	To reduce power consumption, if USB Host is not used, connect HDMA/HDMB to GND.
		USB Device (UDP) To reduce power consumption, USB Device Built-in Transceivers can be disabled (enabled by default).	
	DDP	Application dependent[8]	To reduce power consumption, if USB Device is not used, connect DHSDP to V_{VDDIOP}.
	DDM	Application dependent [8]	To reduce power consumption, if USB Device is not used, connect DHSDM to GND.

Notes: 1. These values are given only as a typical example.

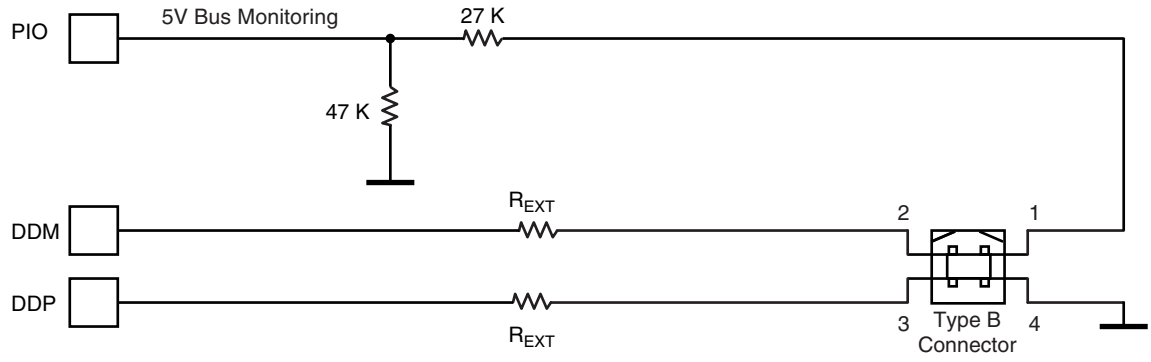
2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



3. The double power supplies VDDIOM, VDDIOP0 and VDDIOP1 power the device differently when interfacing with memories or with peripherals.
4. Some I/O lines of PIO Controller C are powered by VDDIOP0. See the section “Multiplexing on PIO Controller C” in the AT91SAM9XE datasheet**.** Some I/O lines of PIO Controller Bare powered by VDDIOP0 and VDDIOP1. See the section “Multiplexing on PIO Controller B” in the AT91SAM9XE datasheet**.**
5. It is recommended to establish accessibility to a JTAG connector for debug in any case.
6. In a well-shielded environment subject to low magnetic and electric field interference, the pin may be left unconnected. In noisy environments, a connection to ground is recommended.
7. Example of USB Host connection: A termination serial resistor (R_{EXT}) must be connected to HDPA/HDPB and HDMA/HDMB. A recommended resistor value is defined in the electrical specifications of the AT91SAM9XE datasheet**.**



8. Example of USB Device connection: As there is an embedded pull-up, no external circuitry is necessary to enable and disable the 1.5 kOhm pull-up. Internal pull-downs on DDP and DDM are embedded to prevent over consumption when the host is disconnected. A termination serial resistor (R_{EXT}) must be connected to DDP and DDM. A recommended resistor value is defined in the electrical specifications of the AT91SAM9XE datasheet.



4. External Bus Interface (EBI) Hardware Interface

Table 4-1 and Table 4-2 detail the connections to be applied between the EBI pins and the external devices for each Memory Controller:

Table 4-1. EBI Pins and External Static Devices Connections

Signals: EBI_	Pins of the Interfaced Device					
	8-bit Static Device	2 x 8-bit Static Devices	16-bit Static Device	4 x 8-bit Static Devices	2 x 16-bit Static Devices	32-bit Static Device
Controller	**SMC**					
D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7
D8 - D15	–	D8 - D15	D8 - D15	D8 - D15	D8 - 15	D8 - 15
D16 - D23	–	–	–	D16 - D23	D16 - D23	D16 - D23
D24 - D31	–	–	–	D24 - D31	D24 - D31	D24 - D31
A0/NBS0	A0	–	NLB	–	NLB(3)	BE0(5)
A1/NWR2/NBS2	A1	A0	A0	WE(2)	NLB(4)	BE2(5)
A2 - A22	A[2:22]	A[1:21]	A[1:21]	A[0:20]	A[0:20]	A[0:20]
A23 - A25	A[23:25]	A[22:24]	A[22:24]	A[21:23]	A[21:23]	A[21:23]
NCS0	CS	CS	CS	CS	CS	CS
NCS1/SDCS	CS	CS	CS	CS	CS	CS
NCS2	CS	CS	CS	CS	CS	CS
NCS2/NANDCS	CS	CS	CS	CS	CS	CS
NCS3/NANDCS	CS	CS	CS	CS	CS	CS
NCS4/CFCS0	CS	CS	CS	CS	CS	CS
NCS5/CFCS1	CS	CS	CS	CS	CS	CS
NRD/CFOE	OE	OE	OE	OE	OE	OE
NWR0/NWE	WE	WE(1)	WE	WE(2)	WE	WE
NWR1/NBS1	–	WE(1)	NUB	WE(2)	NUB(3)	BE1(5)
NWR3/NBS3	–	–	–	WE(2)	NUB(4)	BE3(5)

Notes:
1. NWR1 enables upper byte writes. NWR0 enables lower byte writes.
2. NWRx enables corresponding byte x writes. (x = 0,1,2 or 3)
3. NBS0 and NBS1 enable respectively lower and upper bytes of the lower 16-bit word.
4. NBS2 and NBS3 enable respectively lower and upper bytes of the upper 16-bit word.
5. BEx: Byte x Enable (x = 0,1,2 or 3).

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Table 4-2. EBI Pins and External Devices Connections

Signals: EBI0_, EBI1_	Pins of the Interfaced Device			
	SDRAM	CompactFlash (EBI0 only)	CompactFlash True IDE Mode (EBI0 only)	NAND Flash
Controller	**SDRAMC**	**SMC**		
D0 - D7	D0 - D7	D0 - D7	D0 - D7	I/O0-I/O7
D8 - D15	D8 - D15	D8 - 15	D8 - 15	I/O8-I/O15
D16 - D31	D16 - D31	–	–	–
A0/NBS0	DQM0	A0	A0	–
A1/NWR2/NBS2	DQM2	A1	A1	–
A2 - A10	A[0:8]	A[2:10]	A[2:10]	–
A11	A9	–	–	–
SDA10	A10	–	–	–
A12	–	–	–	–
A13 - A14	A[11:12]	–	–	–
A15	–	–	–	–
A16/BA0	BA0	–	–	–
A17/BA1	BA1	–	–	–
A18 - A20	–	–	–	–
A21/NANDALE	–	–	–	ALE
A22/NANDCLE	–	REG	REG	CLE
A23 - A24	–	–	–	–
A25	–	CFRNW(1)	CFRNW(1)	–
NCS0	–	–	–	–
NCS1/SDCS	CS	–	–	–
NCS2	–	–	–	–
NCS2/NANDCS	–	–	–	–
NCS3/NANDCS	–	–	–	CE
NCS4/CFCS0	–	CFCS0(1)	CFCS0(1)	–
NCS5/CFCS1	–	CFCS1(1)	CFCS1(1)	–
NANDOE	–	–	–	OE
NANDWE	–	–	–	WE
NRD/CFOE	–	OE	–	–
NWR0/NWE/CFWE	–	WE	WE	–
NWR1/NBS1/CFIOR	DQM1	IOR	IOR	–
NWR3/NBS3/CFIOW	DQM3	IOW	IOW	–
CFCE1	–	CE1	CS0	–
CFCE2	–	CE2	CS1	–

Table 4-2. EBI Pins and External Devices Connections (Continued)

Signals: EBI0_, EBI1_	**Pins of the Interfaced Device**			
	SDRAM	CompactFlash (EBI0 only)	CompactFlash True IDE Mode (EBI0 only)	NAND Flash
Controller	**SDRAMC**	**SMC**		
SDCK	CLK	–	–	–
SDCKE	CKE	–	–	–
RAS	RAS	–	–	–
CAS	CAS	–	–	–
SDWE	WE	–	–	–
NWAIT	–	WAIT	WAIT	–
Pxx[2]	–	CD1 or CD2	CD1 or CD2	–
Pxx[2]	–	–	–	CE
Pxx[2]	–	–	–	RDY

Notes: 1. Not directly connected to the CompactFlash slot. Permits the control of the bidirectional buffer between the EBI data bus and the CompactFlash slot.

2. Any PIO Line

5. AT91SAM Boot Program Hardware Constraints

See AT91SAM Boot Program section of the AT91SAM9XE datasheet for more details on the boot program.

5.1 AT91SAM Boot Program Supported Crystals (MHz)

5.1.1 On-chip RC Selected (OSCSEL=0)

If the Internal RC Oscillator is used (OSCSEL = 0) and the Main Oscillator is active:

Table 5-1. Supported Crystals (MHz)

	3.0	6.0	18.432	Other Crystal
Boot on DBGU	Yes	Yes	Yes	Yes
Boot on USB	Yes	Yes	Yes	No

Note: Any other crystal can be used but it prevents using the USB for SAM-BA® Boot.

If the Internal RC Oscillator is used (OSCSEL = 0) and the Main Oscillator is bypassed:

Table 5-2. Supported Input Frequencies (MHz)

	1.0	2.0	6.0	12.0	25.0	50.0	Other Frequency
Boot on DBGU	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Boot on USB	Yes	Yes	Yes	Yes	Yes	Yes	No

Note: Any other input frequency can be used but it prevents using the USB.

5.1.2 External 32,768 Hz Crystal Selected (OSCSEL=1)

If an external 32,768 Hz Oscillator is used (OSCSEL = 1) and the Main Oscillator is active or in bypass mode:

Table 5-3. Supported Crystals (MHz)

3.0	3.2768	3.6864	3.84	4.0
4.433619	4.9152	5.0	5.24288	6.0
6.144	6.4	6.5536	7.159090	7.3728
7.864320	8.0	9.8304	10.0	11.05920
12.0	12.288	13.56	14.31818	14.7456
16.0	17.734470	18.432	20.0	-

Note: Booting either on USB or on DBGU is possible with any of these input frequencies.

5.2 SAM-BA Boot

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

Table 5-4. Pins Driven during SAM-BA Boot Program Execution

Peripheral	Pin	PIO Line
DBGU	DRXD	PB14
DBGU	DTXD	PB15

Revision History

Doc. Rev	Comments	Change Request Ref.
6420C	(8) was edited on page 9.	6696
	In "USB Host (UHP)" on page 8, Recommended Pin Connection column was edited for HDPA-HDPB and HDMA-HDMB.	6697
6420B	XIN XOUT main oscillator, change capacitance of crystal in Section 3. "Schematic Check List"	rfo
	Change voltage to VDDIOP1 in Section 3. "Schematic Check List"	rfo
	VDDIOP to VDDBU change in Section 3. "Schematic Check List"	5857
	Add OSCSEL to table in Section 3. "Schematic Check List"	5863
	CAUTION message added before main table in Section 3. "Schematic Check List"	6124
	SHDN pin edit in Section 3. "Schematic Check List"	6029-6149
6420A	First issue	

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