PDA3

Photo Diode Array Detector System

User Manual

Warning

This equipment uses voltages which are dangerous to life. It should be serviced only by qualified personnel.

Lex van der Gracht , October 9, 2006
Electronics Group,
Faculty of Sciences
Vrije Universiteit *Amsterdam*, the Netherlands

Phone : +31-20-5987973
Fax : +31-20-5987899

Email : a.van.der.gracht@few.vu.nl
Web : http://www.few.vu.nl/~elec

Project ID : 20054007
Filename : Document1
Pages : 9
Last save : (October 13, 2006)

Table of contents

1 Precautions

Safety check has been done following the NEN-EN 50110-1 and NEN 3140.

Hazardous voltages exist in this apparatus. Besides the regular safety precautions the following should be observed when working with this unit:

1. When power is required, the unit should be plugged into an outlet with a properly grounded receptacle. The use of two prong plug adapters is not recommended.

2. The use of extension cords may compromise the safety of the operator and is not recommended.

3. Ensure that the fuses installed in the unit are of the correct rating.

4. A damaged power cord or plug may constitute a shock or fire hazard. Do not allow continued operation of the unit until the damaged cord or plug has been replaced.

5. Ensure that none of the ventilation openings in the apparatus are blocked. Excessive heat build up in the unit may cause failures.

6. Do not exceed maximum allowable mains input voltage.

7. The apparatus is designed for horizontal use only.

8. The apparatus should not be opened by the user; in case of a malfunction it will be serviced by the Electronics group.

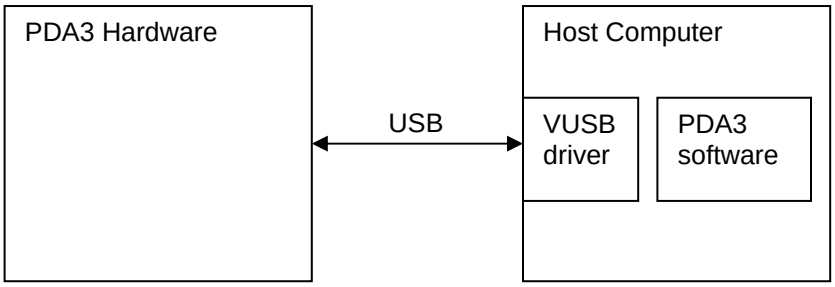
2 General Description

The PDA3 is a (dual) photodiode array detector system, designed to measure the double-beam output spectrum of a Spectrograph in a laser setup.
It's a redesign of the PDA2 system, using USB 2.0 for data transmission and control.

3 System Description

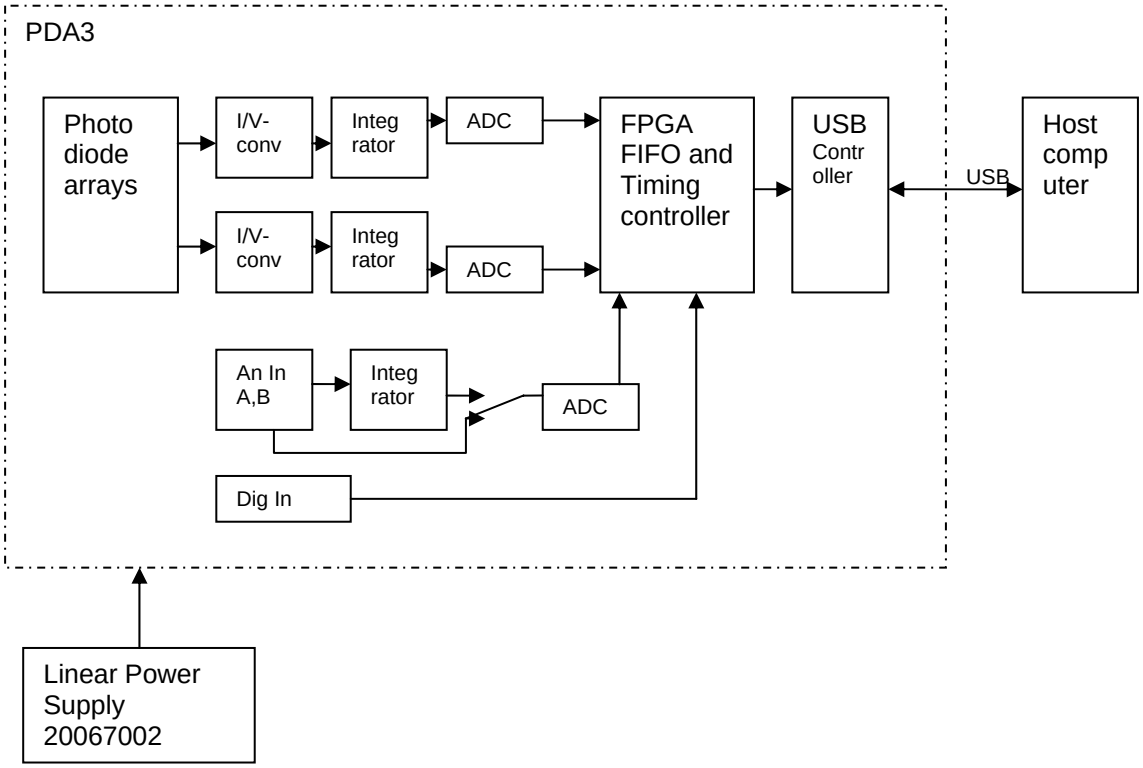
3.1.1 General

The PDA3 system is not a stand-alone instrument; it needs a host computer running the PDA3 software. This is a LabWindows/CVI program, written by members of the Biophysics department.



There is also a driver necessary for the communication between the PDA3 software and the hardware; the VUSB kernel driver. For Host Computer requirements and driver installation procedures, see the 'Installation Procedure' chapter.

3.1.2 Hardware Block Diagram



3.1.2.1 Block Diagram description

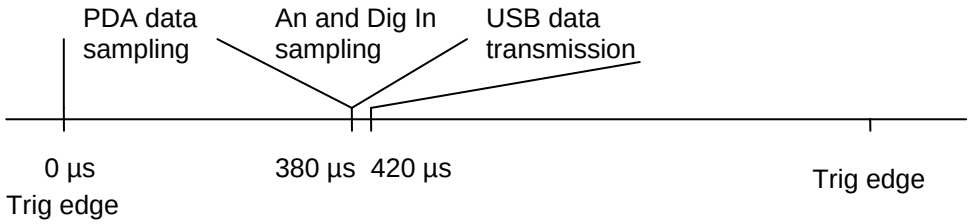
The photodiode arrays are an Upper-array and a Lower-array of 256 photodiodes, which signals are clocked out simultaneous by the FPGA. Output charges are first converted into a voltage, then integrated and sampled by a 16-bits AD converter. Inside the FPGA a data frame is build, and the sampled data goes into the FIFO (Lower data first). When all PDA data is collected, the An In ADC's are sampled and data is added to the FIFO. Finally the Dig In channels are converted into 16-bit values and added to the FIFO. When the Host computer requests data, the USB controller shifts data out of the FIFO, creating space for new data.

3.1.3 Power

The PDA3 uses a dedicated power supply; the Linear Power Supply 20067002.
This is a special power supply with a single multi-wired output cable to the PDA3 system. The power supply has a on/off switch at the rear, and a pushbutton 'Standby/On' at the front. When the power supply is switched on, it goes in standby. The PDA3 system can be switched on by pushing the 'Standby/On' button on the power supply or by using the pushbutton at the rear side of the PDA3 system. The status LED of the power supply should be green when the power is applied. If the status LED is red, a power error occurred. Turn off the device and bring it to the Electronics department for service.

3.1.4 Timing

After the rising edge of a trigger pulse, the PDA3 hardware collects data. Directly after the trigger pulse the PDA readout starts. PDA readout takes about 380 µs. When the PDA readout is finished, both rear Analog Inputs are sampled. Finally the rear Digital Inputs are sampled.
When all data is collected, the data transmission starts. The frame will be transmitted over USB within 40 µs, so the total frame handling takes less than 420 µs.



Both Upper and Lower Arrays of the PDA are clocked simultaneously. The output charge of each array element is converted into a voltage and integrated. The integrated signals are simultaneously sampled by the ADC's

3.1.5 Trigger Input

The trigger input signal should be a 1KHz TTL trigger pulse, generated by the laser system. The pulse width should have a minimum value of 250 ns. The maximum trigger rate is 2.2 KHz, now limited because data transfer is only allowed after the data collection. The driver uses a routine with a 6 sec timeout to read the data, so if the trigger rate is too slow the PDA3 system will give an error ('PDA3 Read failed').

3.1.6 Analog Inputs

These inputs are sampled after the PDA readout is finished. In normal mode the inputs are sampled and the digital values are added to the Frame contents. The analog inputs also have an integrated mode, but this mode still has to be implemented inside the FPGA.

4 Installation Procedure

The PDA3 sytem is a USB device. The PDA3 system needs a High-Speed USB connection to the host computer. If the system enumerates to a Full-Speed connection (12Mbits/sec) the PDA3 system error LED will be lit just after connecting.
The PDA3 system uses a dedicated driver, the VUSB kernel driver, to assure a constant data flow in a Windows environment. The hardware is using a small 8 kB FIFO memory. The host should be fast enough to read the data every 8 ms to prevent data loss.

Minimal host requirements are:

- Processor running 2.2 GHz or faster
- Windows 2000 or Windows XP
- USB 2.0 support

The VUSB kernel driver must be installed before the PDA3 hardware can be used. Download the latest software from the Electronics Web-page (see the front page of this manual). Installation notes can be found in the downloaded 'Read Me'-file.

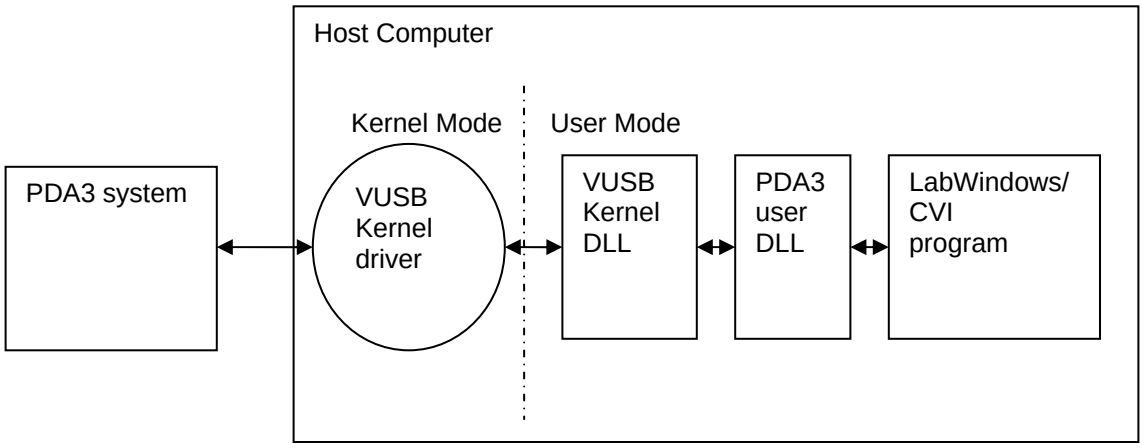
5 Data Frame contents

word	1	Identification Word (0xA5A5)
word	2	Frame Counter (starts at 0xFC00)
word	3	First pixel of lower PDA (16-bits data)
word	4	First pixel of upper PDA
word	5	Second pixel of lower PDA
word	6	Second pixel of upper PDA
word	7	Third pixel of lower PDA
word	8	Third pixel of upper PDA
word	511	255-th pixel of lower PDA
word	512	255-th pixel of upper PDA
word	513	256-th pixel of lower PDA
word	514	256-th pixel of upper PDA
word	515	Analog B input (from16-bits ADC)
word	516	Analog A input (from 16-bits ADC)
word	517	Digital GPIO0 input (0x0000 when LOW, 0xFFFF when HIGH)
word	518	Digital GPIO1 input (idem)
word	519	Digital GPIO2 input (idem)
word	520	Digital GPIO3 input (idem)
word	521	W521 (register values W521_H and W521_L)
word	522	W522 (register values W522_H and W522_L)

Frame size is kept identical to the PDA2 system, so the analyzing software could stay the same. The Identification word can be used to check for data alignment errors. The Frame counter word is a legacy item and is ignored in software. The last two frame words, W521 and W522 are 'spare' data words. In the current implementation they reflect internal FPGA register values. These values can be set through USB commands by software. The idea was to use these registers to add user info to the data, e.g. delay info.

6 VUSB User Information

The VUSB kernel driver is a driver for the PDA3 system.



Calls to this driver can only be made through a specific DLL, the 'VUSBkernel' DLL. This DLL uses a set of basic USB calls, independent of hardware or software. Another user space DLL called 'PDA3user' defines PDA3-specific calls and translates them into VUSBkernel calls.

6.1 USB Vendor Commands

USB Vendor commands	
User commands	
0xB0	Hardware reset
0xB1	Enable IN transfers (bulk transfer from PDA3 to host)
0xB2	Disable IN transfers
0xB3	Get hardware's USB status register
0xB4	Get PDA3 registers (in FPGA)
0xB5	Set PDA3 registers (in FPGA)
0xB6	Reset Hardware FIFO
Test commands	
0xC0	reset hardware's USB status register (only for testing!)
0xC1	read GPIFREADYSTAT register (for testing the GPIF)
0xC2	read ep6fifobuf (for testing the bulk buffer)
0xC3	fill ep6fifobuf (for testing the bulk buffer)

6.2 USB status register bits

read only

b7	b6	b5	b4	b3	b2	b1	b0
Res.	Res.	Res.	Res.	ExtFifoFullBit	EP6FifoFullBit	InEnableBit	EnumHighSpeedBit
				HIGH when External FIFO is FULL	HIGH when Endpoint6 FIFO is FULL	Bulk transfer enabled status	HIGH when device is High Speed Enumerated (Must be HIGH for PDA3)

7 PDA3 registers

Register	Regsel 2,1,0	b7	b6	b5	b4	b3	b2	b1	b0
GPIO	000	Res.	Res.	GPIO1_FPGA_HOSTn	GPIO0_FPGA_Hostn	GPIO3	GPIO2	GPIO1	GPIO0
				If GPIO1==Input (NOT NOW) GPIO1 output can be programmed from FPGA (HIGH) or controlled by Host program (LOW)	If GPIO0==Input (NOT NOW) GPIO0 output can be programmed from FPGA (HIGH) or controlled by Host program (LOW)	GPIO3 input status (Trigger Input on PDA3) (Read Only)	GPIO2 input status (Read Only)	GPIO1 input status (Read Only)	GPIO0 input status (Read Only)
CONTROL	001	UsbAct.	TestDATA	SLOWADCIntBn	SLOWADCIntAn	LED2	LED1	LED0	TrigEnable
		drives USB Activity LED	PDA3 generates dummy test data when HIGH	SLOW ADC_B INPUT is NORMAL when LOW, Integrated when HIGH	SLOW ADC_A INPUT is NORMAL when LOW, Integrated when HIGH	Drives the LED2 output	Drives the LED1 output	Drives the LED0 output	External triggers are Enabled when HIGH
W521_H	010	Internal W521_H register, High byte of 521-th word of frame contents							
W521_L	011	Internal W521_L register, Low byte of 521-th word of frame contents							
W522_H	100	Internal W522_H register, High byte of 522-th word of frame contents							
W522_L	101	Internal W522_L register, Low byte of 521-th word of frame contents							

The purpose of the last 4 registers is to provide the user a way to insert relevant information (scan info, timepoints etc.) into the raw data.

8 Specifications

Power

- Linear power supply: 230V~, 50W
- Fuse: 500mAT

Inputs and Outputs

- **PDA**
  Two 16-bits ADC's, generating 1Mb/sec data at 1kHz trigger rate.

- **Trig In**
  Trigger input: SMA connector, TTL in. (max +5 Volt), min pulse width 250 ns.
  Nominal frequency=1 kHz, max frequency 2.2 kHz.

- **CH0, CH1,CH2**
  Digital Chopper signal inputs on SMA connectors, TTL in (max +5V).
  CH0 -> Pump beam chopper
  CH1 -> Dump beam chopper
  CH2 -> Spare digital IO channel

- **AnInA,AnInB Analog Inputs**
  Analog input range: -10V until +10V.
  16-bits ADC.

- **AnOutU,AnOUtL Analog Outputs**
  (Analog Output range: -1V until +5V)
  Analog output of upper and lower photodiode array after integration.
  0V -> no light
  +2V -> saturation