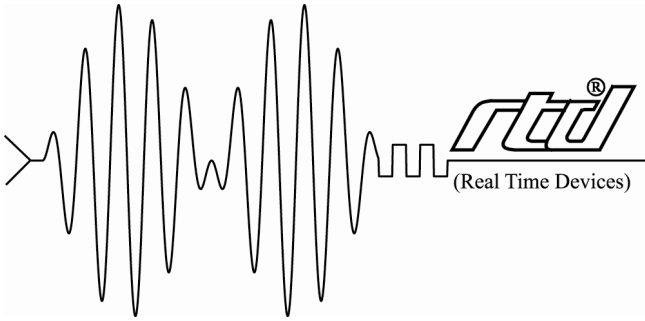
FPGA6800 User's Manual

Field Programmable Gate Array Board



RTD Embedded Technologies, Inc.
"Accessing the Analog World"®

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Rev B

FPGA6800 User's Manual

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Manual Revision History

Rev A	Initial Release
Rev B	Changed Signals SA0-SA23 to SA0-SA19 and LA17-LA23 in FPGA. Addition of switches noted. Added IDAN connector information and pin out.

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Introduction

Product Overview

The FPGA6800 is designed to provide platform to create any digital I/O that is required for your application. It interfaces with the ISA bus and features a Xilinx Spartan II 200,000 gate FPGA with a 50 MHz oscillator, a user installed oscillator, 20 user defined jumpers, an 82C54 counter/timer, and two 128K x 8 SRAMs. There are three connectors that provide a maximum of 33 I/O pins each for a total of 99 I/O.

Board Features

200,000 Gate Xilinx Spartan II FPGA

- Xilinx Spartan II System level features
  - SelectRAM+™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - 57,344 bits of configurable block RAM
    - Fast interfaces to external RAM
  - Low-power segmented routing architecture
  - Full readback ability for verification/observability
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
    - Multiply by 2 output (cascade 2 for multiply by 4)
    - 0, 90, 180, and 270 degree phase outputs
    - Divide by 1.5, 2, 2.5, 3, 4, 5, 8, or 16 output
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
  - 16 high-performance interface standards
  - Zero hold time simplifies system timing
- Fully supported by powerful Xilinx development system
  - ISE *WebPACK* (free download from http://www.xilinx.com/)
  - Foundation ISE Series: Fully integrated software
  - Alliance Series: For use with third-party tools
  - Fully automatic mapping, placement, and routing

Digital I/O Connectors

- 99 total ESD protected I/O lines (Human body model)
- 3 identical I/O connectors each with
  - 24 dedicated I/O
  - Two groups of 4 configurable as I/O or ground
  - One pin jumper selected as I/O or ground
  - 16 grounds
  - +5 volts @ 2 A max (fused)

SRAM Memory

Two fast 128K x 8 SRAMs (can be configured as 128K x 16 or 256K x 8) accessible through the FPGA.

Clock Options

- 50 MHz oscillator
- User oscillator installed in 8-pin DIO socket (3.3V or 5V)
- ISA System Clock (typically 8.33 MHz)
- ISA I/O Write (used for I/O register write cycles)

User jumpers

- 20 jumpers for user configuration
  - Two banks of 8 jumpers
  - One bank of 4 jumpers

82C54 Timer/Counters

- Three 16-bit Timer/Counter Channels
- Fully programmable
- 10 MHz maximum input frequency
- Input and outputs connected to FPGA

Physical Attributes

- Size: 3.6”L x 3.8”W x 0.6”H (90mm L x 96mm W x 15mm H)
- Weight: 0.22 lbs (0.10 Kg)
- Temperature
  - Operating: -40° C to +85° C
  - Storage: -55° C to +125° C
- Power Requirements:
  - Typical: 1.5 W @ +5 VDC

Available Options

The FPGA6800 is a general use FPGA module. You design your own FPGA or RTD’s team of experienced FPGA designers will do custom FPGA designs. Please contact RTD Embedded Technologies for more information on custom FPGA designs at +1-814-234-8087 or E-Mail sales@rtd.com.

Getting Technical Support

For help with this product, or any other product made by RTD, you can contact RTD Embedded Technologies via the following methods:

Phone: +1-814-234-8087

E-Mail: techsupport@rtd.com

Be sure to check the RTD web site (http://www.rtd.com) for product updates, including newer versions of the board manual and application software.

Hardware Description

Block Diagram

Below is a block diagram of the FPGA6800. Primary board components are in bold, while external I/O connections and jumpers are italicized.

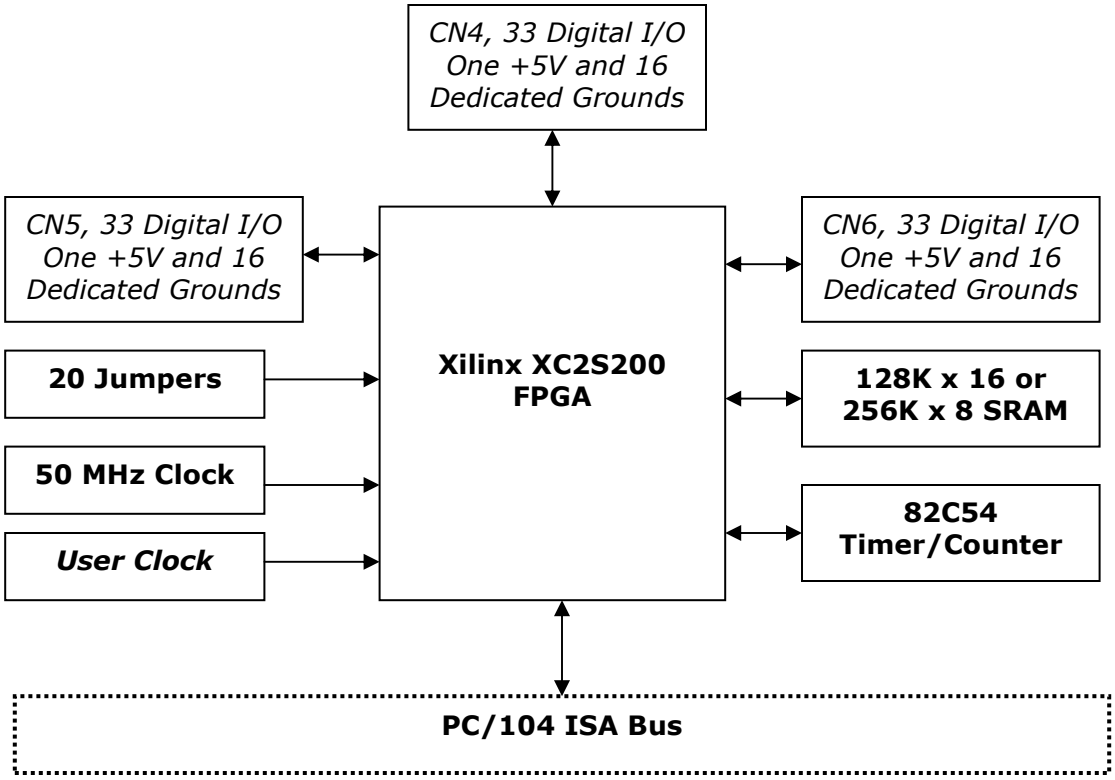

Figure 1: FPGA6800 Block Diagram

Connector and Jumper Locations

The following diagram shows the location of all connectors and jumpers on the FPGA6800. For a description of each jumper and connector, refer to the following sections.

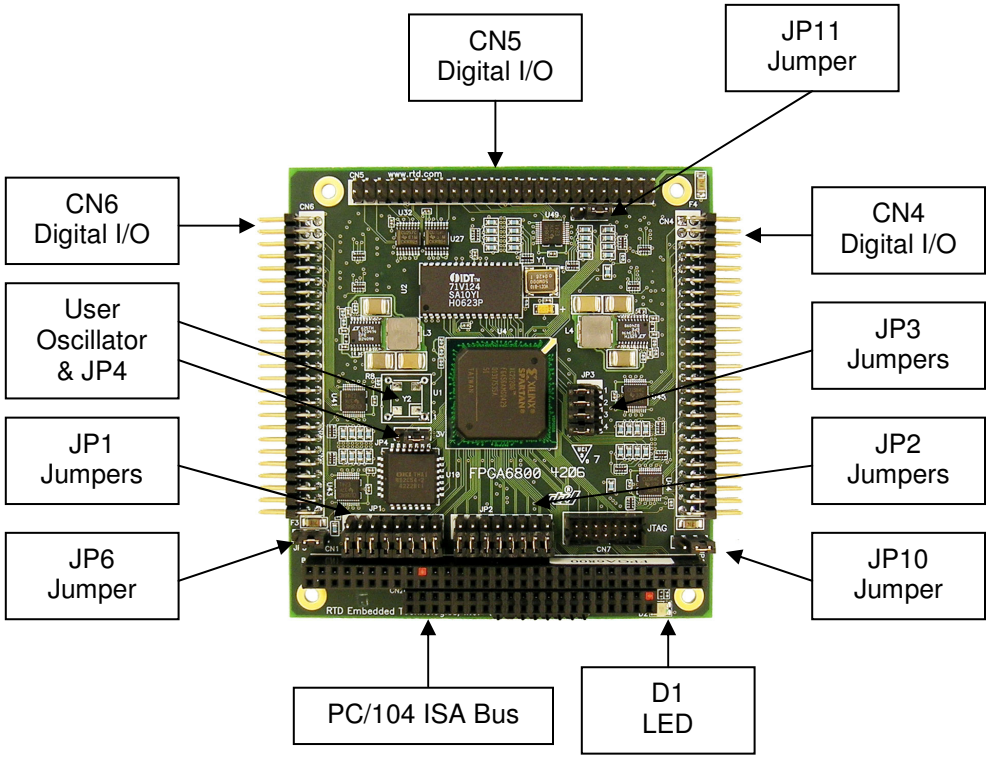

Figure 2: FPGA6800 Connector and Jumper Locations

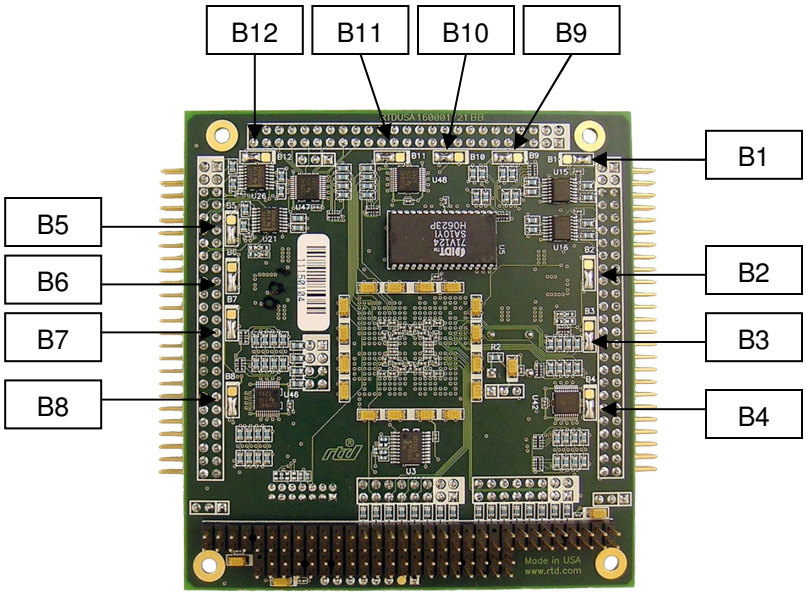

Figure 3: FPGA6800 Board Bottom Solder Blob Locations

External I/O Connections

The following sections describe the external I/O connections of the FPGA6800.

Connectors CN4, CN5, and CN6 – Digital Input / Output

Connectors CN4, CN5, and CN6 provide up to 33 digital input/output lines, along with a +5V pin and ground pins. All I/O pins go to the FPGA through pull up/down resistors and switches which are open during configuration. This allows the pull up/down resistors to control the level of the I/O pins until the FPGA is operational. The signal names reflect the signal names in the Xilinx UCF file with the device pin out. All three connector pin outs are identical.

Note: Pin 1 can be identified by a square solder pad. Pins 2 – 50 have round solder pads.

Table 1: CNx Pin Assignments (x = 4, 5, or 6)

Signal	Pin	Pin	Signal
CNx_pin_01	1	2	CNx_pin_02 or GND – Controlled by CNx_gnd_enable_1
CNx_pin_03	3	4	CNx_pin_04 or GND – Controlled by CNx_gnd_enable_1
CNx_pin_05	5	6	CNx_pin_06 or GND – Controlled by CNx_gnd_enable_1
CNx_pin_07	7	8	CNx_pin_08 or GND – Controlled by CNx_gnd_enable_1
CNx_pin_09	9	10	CNx_pin_10 or GND – Controlled by CNx_gnd_enable_2
CNx_pin_11	11	12	CNx_pin_12 or GND – Controlled by CNx_gnd_enable_2
CNx_pin_13	13	14	CNx_pin_14 or GND – Controlled by CNx_gnd_enable_2
CNx_pin_15	15	16	CNx_pin_16 or GND – Controlled by CNx_gnd_enable_2
CNx_pin_17	17	18	GND
CNx_pin_19	19	20	GND

Table 1: CNx Pin Assignments (x = 4, 5, or 6)

Signal	Pin	Pin	Signal
CNx_pin_21	21	22	GND
CNx_pin_23	23	24	GND
CNx_pin_25	25	26	GND
CNx_pin_27	27	28	GND
CNx_pin_29	29	30	GND
CNx_pin_31	31	32	GND
CNx_pin_33	33	34	GND
CNx_pin_35	35	36	GND
CNx_pin_37	37	38	GND
CNx_pin_39	39	40	GND
CNx_pin_41	41	42	GND
CNx_pin_43	43	44	GND
CNx_pin_45	45	46	GND
CNx_pin_47	47	48	GND
+5V, 2A max	49	50	CNx_pin_16/GND – Controlled by Jumper

Connectors CN4, CN5, and CN6 – Pull/pulldown Resistors

Connectors CN4, CN5, and CN6 provide 10K ohm pullup to +5V or pulldown to ground on all 33 digital input/output lines using solder blobs on the bottom of the board. The tables below indicate the blob to use for each pin.

Note: Each blob will pullup or pulldown multiple pins.

Table 2: CN4, CN5, and CN6 Solder Blob Assignments

CN6	CN5	CN4	Pin	Pin	CN4	CN5	CN6
B2	B10	B6	1	2	B5	B9	B1
			3	4			
			5	6			
			7	8			
			9	10			
			11	12			
			13	14			
			15	16			
B3	B11	B7	17	18	None		
			19	20	None		
			21	22	None		
			23	24	None		
			25	26	None		
			27	28	None		
			29	30	None		

Table 2: CN4, CN5, and CN6 Solder Blob Assignments

			31	32	None		
B4	B12	B8	33	34	None		
			35	36	None		
			37	38	None		
			39	40	None		
			41	42	None		
			43	44	None		
			45	46	None		
			47	48	None		
+5V, 2A max			49	50	B8	B12	B4

Connector CN7 – Xilinx JTAG Programming Adapter

Connector CN7 provides a connection to the Xilinx JTAG programming adapter. The pin assignments for CN7 are shown in Table 3.

Note: This connector is keyed to ensure proper connection with Xilinx's programming adapters.

Table 3: CN7 Pin Assignments

Signal	Pin	Pin	Signal
GND	1	2	3.3V VRef
GND	3	4	TMS
GND	5	6	TCK
GND	7	8	TDO
GND	9	10	TDI
GND	11	12	N/C
GND	13	14	N/C

Jumper JP1, JP2 and JP3 – User Jumpers

There are three jumper banks that can be defined by the user. JP1 and JP2 have eight positions numbered 1-8 and JP3 has four positions numbered 1-4. When the jumper is not installed the signal going to the FPGA is high. When the jumper is installed the signal going to the FPGA is low. The jumper assignments are as follows:

Table 4: JP1 Signal Assignments

JP1 Position	Xilinx UCF file Signal Name
1	JP1<1>
2	JP1<2>
3	JP1<3>
4	JP1<4>
5	JP1<5>
6	JP1<6>
7	JP1<7>

JP1 Position	Xilinx UCF file Signal Name
8	JP1<8>

Table 5: JP2 Signal Assignments

JP2 Position	Xilinx UCF file Signal Name
1	JP2<1>
2	JP2<2>
3	JP2<3>
4	JP2<4>
5	JP2<5>
6	JP2<6>
7	JP2<7>
8	JP2<8>

Table 6: JP3 Signal Assignments

JP3 Position	Xilinx UCF file Signal Name
1	JP3<1>
2	JP3<2>
3	JP3<3>
4	JP3<4>

LED D1

This tri-color LED is connected to the FPGA. Individual red, blue, and green LEDs can be enabled for a total of seven color options plus off. Driving the signal low will light the LED, tri-stating the LED to disable it.

Table 7: LED D1 Signal Assignments

LED Color	Xilinx UCF file Signal Name
Red	led_red
Green	led_green
Blue	led_blue

Board Installation

Installing the Hardware

The FPGA6800 can be installed into a PC/104 system. It can be located above or below the CPU.

Static Precautions

Keep your board in its antistatic bag until you are ready to install it into your system! When removing it from the bag, hold the board at the edges and do not touch the components or connectors. Handle the board in an antistatic environment and use a grounded workbench for testing and handling of your hardware.

Steps for Installing

1. Shut down the PC/104 system and unplug the power cord.
2. Ground yourself with an anti-static strap.
3. Set the Jumper and solder blobs as described in the previous chapter.
4. Line up the pins of the FPGA6800's PC/104 connectors with the corresponding bus connectors of the stack.
5. Apply pressure to both bus connectors and gently press the board onto the stack. The board should slide into the matching bus connectors. Do not attempt to force the board, as this can lead to bent/broken pins.
6. Attach any cables to the FPGA6800
7. If any boards are to be stacked above the FPGA6800, install them.
8. Attach any necessary cables to the PC/104 stack.
9. Re-connect the power cord and apply power to the stack.
10. Boot the system and verify that all of the hardware is working properly.

FPGA6800 Demo Functional Overview

FPGA6800 Demo VHDL

Delivered with your FPGA6800 is a demo VHDL application. It has the following features:

1. Each connector is configured as 16 inputs and 16 outputs that can be read or written through I/O instructions
    a. Pins 1 – 16 are configured as outputs
    b. Pins 17 – 47 odd are configured as inputs
2. The 50 MHz oscillator is divided by 8 in one of the CLKDLLs to get 6.25 MHz
3. The three 16-bit timers in the 82C54 are cascaded and set to mode 3 by the example software. Dividers are set to 500, 250, and 50 to provide a 1 Hz clock
4. The FPGA uses the 1 Hz clock to clock a 3-bit counter which steps the tri-color LED through all its colors
5. The SRAM is configured as 128K x 16 and is accessible through 16-bit I/O instructions
6. Jumper settings and power good status can be read using I/O instructions
7. Connector I/O ground switching for pins 2 – 16 even is controlled by an I/O register

Board Operation and Programming

ISA Interface

The FPGA attaches directly to the ISA bus and the FPGA6800 Demo is I/O mapped. The address is fixed at 300H – 31Fh. All registers are 8-bit except the SRAM registers which are 16-bit.

I/O Map Overview

Table 8 shows the I/O map of the FPGA6800 I/O registers.

Table 8: FPGA6800 I/O Map

Address (Hex)	Register Name	Register Function
Digital I/O CN4 (8-bit I/O)		
0x0300	Port_1_Out	Port 1 Output (pins 1 – 15 odd)
0x0301	Port_2_In	Port 2 Inputs (pins 17 – 31 odd)
0x0302	Port_3_In	Port 3 Inputs (pins 33 – 47 odd)
0x0303	Port_4_Out	Port 4 Outputs (pins 2 – 16 even)
Digital I/O CN5 (8-bit I/O)		
0x0304	Port_1_Out	Port 1 Output (pins 1 – 15 odd)
0x0305	Port_2_In	Port 2 Inputs (pins 17 – 31 odd)
0x0306	Port_3_In	Port 3 Inputs (pins 33 – 47 odd)
0x0307	Port_4_Out	Port 4 Outputs (pins 2 – 16 even)
Digital I/O CN6 (8-bit I/O)		
0x0308	Port_1_Out	Port 1 Output (pins 1 – 15 odd)
0x0309	Port_2_In	Port 2 Inputs (pins 17 – 31 odd)
0x030A	Port_3_In	Port 3 Inputs (pins 33 – 47 odd)
0x030B	Port_4_Out	Port 4 Outputs (pins 2 – 16 even)
82C54 Counter/Timer (8-bit I/O)		
0x030C	TC_COUNTER_0	Counter 0 Register
0x030D	TC_COUNTER_1	Counter 1 Register
0x030E	TC_COUNTER_2	Counter 2 Register
0x030F	TC_CON_WORD	Control Word Register
128K x 16 SRAM (16-bit I/O)		
0x0310	SRAM Address Low	SRAM Address A0 – A15
0x0312	SRAM Address High	SRAM Address A16
0x0314	SRAM Data	SRAM Data D0 – D15
0x0316	Reserved	Unused
Control (8-bit I/O)		
0x0318	JP1	Read JP1 setting
0x0319	JP2	Read JP2 setting
0x031A	JP3	Read JP3 setting
0x031B	DIO/Ground Control	Read/Write DIO/ground settings for CN4, CN5, and CN6
0x031C	Pin 50	Read Pin 50 for CN4, CN5, and CN6
0x031D	Power Good	Read 3.3V and 2.5V power good signals
0x031E	Reserved	Unused
0x031F	Reserved	Unused

Detailed Register Description

The following sections provide a detailed description of the individual registers. In the following register description sections, each register is described by a register table. The first row of the table lists the bits, i.e. D15 through D0. The second row lists the field name for each bit. The third row lists the properties of that bit; 'R' = bit can be read, 'W' = bit can be written to, and 'C' = bit can be cleared. The last row lists the value of the bit after reset. The register table is then

followed by a description of each of the fields where applicable. An "N/A" for the reset value indicates that the reset value is not applicable - read the field descriptions for more information.

Bits marked as "Reserved" in the field name are unused, and reads will always return their reset value. These bits should not be modified during writes for future compatibility.

Digital I/O CN4 (8-bit I/O)

Port_1_Out

This register holds the data being sent to CN4 pins 1 – 15 odd.

Table 9: CN4 Port 1 Output Register

7	6	5	4	3	2	1	0
Pin 15	Pin 13	Pin 11	Pin 9	Pin 7	Pin 5	Pin 3	Pin 1
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Port_2_In

This register reads the data from CN4 pins 17 – 31 odd.

Table 10: CN4 Port 2 Input

7	6	5	4	3	2	1	0
Pin 31	Pin 29	Pin 27	Pin 25	Pin 23	Pin 21	Pin 19	Pin 17
R	R	R	R	R	R	R	R

Port_3_In

This register reads the data from CN4 pins 33 – 47 odd.

Table 11: CN4 Port 3 Input

7	6	5	4	3	2	1	0
Pin 47	Pin 45	Pin 43	Pin 41	Pin 39	Pin 37	Pin 35	Pin 33
R	R	R	R	R	R	R	R

Port_4_Out

This register holds the data being sent to CN4 pins 2 – 16 even.

Table 12: CN4 Port 4 Output Register

7	6	5	4	3	2	1	0
Pin 15	Pin 13	Pin 11	Pin 9	Pin 7	Pin 5	Pin 3	Pin 1
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Digital I/O CN5 (8-bit I/O)

Port_1_Out

This register holds the data being sent to CN5 pins 1 – 15 odd.

Table 13: CN5 Port 1 Output Register

7	6	5	4	3	2	1	0
Pin 15	Pin 13	Pin 11	Pin 9	Pin 7	Pin 5	Pin 3	Pin 1
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Port_2_In

This register reads the data from CN5 pins 17 – 31 odd.

Table 14: CN5 Port 2 Input

7	6	5	4	3	2	1	0
Pin 31	Pin 29	Pin 27	Pin 25	Pin 23	Pin 21	Pin 19	Pin 17
R	R	R	R	R	R	R	R

Port_3_In

This register reads the data from CN5 pins 33 – 47 odd.

Table 15: CN5 Port 3 Input

7	6	5	4	3	2	1	0
Pin 47	Pin 45	Pin 43	Pin 41	Pin 39	Pin 37	Pin 35	Pin 33
R	R	R	R	R	R	R	R

Port_4_Out

This register holds the data being sent to CN5 pins 2 – 16 even.

Table 16: CN5 Port 4 Output Register

7	6	5	4	3	2	1	0
Pin 15	Pin 13	Pin 11	Pin 9	Pin 7	Pin 5	Pin 3	Pin 1
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Digital I/O CN6 (8-bit I/O)

Port_1_Out

This register holds the data being sent to CN6 pins 1 – 15 odd.

Table 17: CN6 Port 1 Output Register

7	6	5	4	3	2	1	0
Pin 15	Pin 13	Pin 11	Pin 9	Pin 7	Pin 5	Pin 3	Pin 1
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Port_2_In

This register reads the data from CN6 pins 17 – 31 odd.

Table 18: CN6 Port 2 Input

7	6	5	4	3	2	1	0
Pin 31	Pin 29	Pin 27	Pin 25	Pin 23	Pin 21	Pin 19	Pin 17
R	R	R	R	R	R	R	R

Port_3_In

This register reads the data from CN6 pins 33 – 47 odd.

Table 19: CN6 Port 3 Input

7	6	5	4	3	2	1	0
Pin 47	Pin 45	Pin 43	Pin 41	Pin 39	Pin 37	Pin 35	Pin 33
R	R	R	R	R	R	R	R

Port_4_Out

This register holds the data being sent to CN6 pins 2 – 16 even.

Table 20: CN6 Port 4 Output Register

7	6	5	4	3	2	1	0
Pin 15	Pin 13	Pin 11	Pin 9	Pin 7	Pin 5	Pin 3	Pin 1
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

82C54 Counter/Timer

The four 8-bit registers in the 82C54 counter/timer are directly accessible through I/O instructions. Please refer to the 82C54 Datasheet from Oki Semiconductor for information on programming the 82C54 timer counters. You can download the latest datasheet from www2.okisemi.com.

128K x 16 SRAM (16-bit I/O)

The two 128K x 8 SRAM parts are configured as one 128K x 16 in the demo application. They are assessable through three 16-bit I/O addresses.

SRAM Address Low

This is A0 – A15 address bits sent to the SRAM. This must be a 16-bit I/O instruction such as outpw() or inpw() in C.

Table 21: SRAM Address Low Register

15	14	13	12	11	10	9	8
A15	A14	A13	A12	A11	A10	A9	A8
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0
RW	RW	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

SRAM Address High

This is A16 address bit sent to the SRAM. This must be a 16-bit I/O instruction such as outpw() or inpw() in C.

Table 22: SRAM Address High Register

15	14	13	12	11	10	9	8
Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	A16
R	R	R	R	R	R	R	RW
0	0	0	0	0	0	0	0

SRAM Data

This is D0 – D15 data bits read from or written to the SRAM at the address stored in Address Low and Address High registers. This must be a 16-bit I/O instruction such as outpw() or inpw() in C.

Table 23: SRAM Data

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8
RW	RW	RW	RW	RW	RW	RW	RW

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
RW	RW	RW	RW	RW	RW	RW	RW

Control (8-bit I/O)

JP1

This register has the state of the jumpers in JP1. If a jumper is installed it will read low, if it is not installed it will read high.

Table 24: JP1 Status

7	6	5	4	3	2	1	0
JP1-8	JP1-7	JP1-6	JP1-5	JP1-4	JP1-3	JP1-2	JP1-1
R	R	R	R	R	R	R	R

JP2

This register has the state of the jumpers in JP2. If a jumper is installed it will read low, if it is not installed it will read high.

Table 25: JP2 Status

7	6	5	4	3	2	1	0
JP2-8	JP2-7	JP2-6	JP2-5	JP2-4	JP2-3	JP2-2	JP2-1
R	R	R	R	R	R	R	R

JP3

This register has the state of the jumpers in JP3. If a jumper is installed it will read low, if it is not installed it will read high.

Table 26: JP3 Status

7	6	5	4	3	2	1	0
0	0	0	0	JP3-4	JP3-3	JP3-2	JP3-1
R	R	R	R	R	R	R	R

DIO/Ground Control

This register determines if CNx pins 2 – 16 even will be digital I/O or grounds. A 0 will make the pins digital I/O and a 1 will make them grounds.

Table 27: DIO/Ground Control Register

7	6	5	4	3	2	1	0
0	0	CN6 10, 12, 14, 16	CN6 2, 4, 6, 8	CN5 10, 12, 14, 16	CN5 2, 4, 6, 8	CN4 10, 12, 14, 16	CN4 2, 4, 6, 8
R	R	RW	RW	RW	RW	RW	RW
0	0	0	0	0	0	0	0

Pin 50

This register has the state of Pin 50 of each connector.

Table 28: Pin 50 Status

7	6	5	4	3	2	1	0
0	0	0	0	0	CN6 Pin 50	CN5 Pin 50	CN4 Pin 50
R	R	R	R	R	R	R	R

Power Good

This register has the state of the 3.3 VDC and 2.5 VDC power good signals. These signals will read 1 if the power is good and 0 it the power is bad.

Table 29: Power Good Status

7	6	5	4	3	2	1	0
0	0	0	0	0	0	2.5 VDC	3.3 VDC
R	R	R	R	R	R	R	R

Additional Information

Xilinx Spartan II FPGA

For more information about the Xilinx XC2S200 FPGA, contact Xilinx, Inc. at:

www.xilinx.com

The ISE *WebPACK* FPGA design tool may be freely downloaded from the Xilinx web site.

82C54 Timer/Counter

For more information about programming and interfacing with the 82C54 Timer/Counter Chips, contact Oki Semiconductor at:

www2.okisemi.com

ISA Bus

For more information on the theory and operation of the ISA bus, refer to the following books:

ISA & EISA Theory and Operation
by Edward Solari
ISBN: 0-929392-15-9

ISA System Architecture
by Tom Shanley / Don Anderson
ISBN: 0-201-40996-8

Interrupts

For more information about interrupts and writing interrupt service routines, refer to the following book:

Interrupt-Driven PC System Design
by Joseph McGivern
ISBN: 0929392507

DC Characteristics

Absolute Maximum Ratings

	Min	Max	Units
DIO Vin[1]	-0.5	5.5	**V**
Operating Temp	-40	+85	**°C**

DC Input / Output Levels

Input Standard				Output Standard			
VIL		VIH		VOL	VOH	IOL	IOH
V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
-0.5	0.8	2.0	5.5	0.4	2.4	24	-24

1. DIO Vin DC overshoot must be limited to either 5.5V or 10mA and DC undershoot must be limited to either -0.5V or 10mA.
2. DIO pins may be driven to - 2.0V or + 7.0V provided these voltages last no longer than 11ns with a forcing current no greater than 100mA.
3. Inputs are terminated with 33Ω resistors and protection diodes.
4. DIO inputs should not be tied to voltages when the board is not powered.

IDAN External Connector Pin Out

Cables within the IDAN unit provide signal connections between the exterior of the IDAN frame and the headers on the FGPA6800 port P2, P3 and P4 connect to the FPGA6800 headers CN4, CN5, and CN6 respectively. The pin to pin mappings from IDAN port to FPGA6800 are shown in the following tables.

IDAN-FPGA6800 62 pin D connector

Figure 4: Dimensional Drawing of 62 pin D IDAN connector

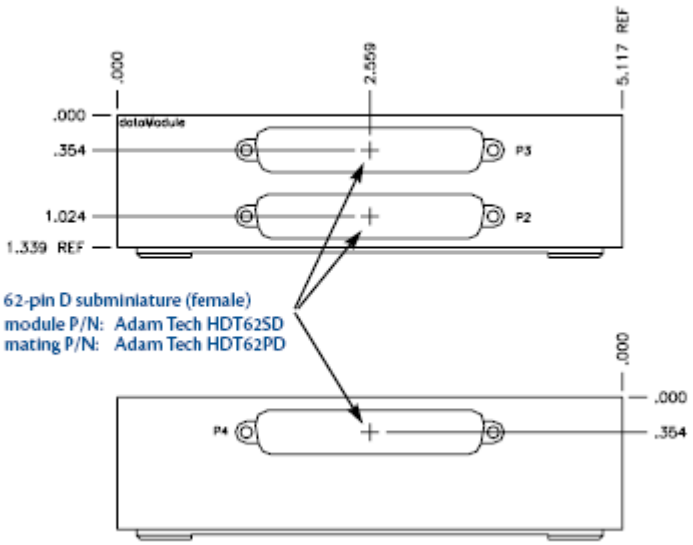

Figure 5: IDAN FPGA6800 Connector Pins

Table 30: IDAN 62D – 62 Pin Subminiature Connector (female)

IDAN 62D- 62 Pin Subminiature Connector (female)

IDAN P3 & P4 Pin #		P2,	Signal	FPGA 6800 CN4, CN5 & CN6
Row 1	Row 2	Row 3	(x=1,2,3)	
1	-	-	CNx Pin 1	1
-	22	-	CNx Pin 2/GND	2
-	-	43	CNx Pin 3	3
2	-	-	CNx Pin 4/GND	4
-	23	-	CNx Pin 5	5
-	-	44	CNx Pin 6/GND	6
3	-	-	CNx Pin 7+	7
-	24	-	CNx Pin 8/GND	8
-	-	45	CNx Pin 9	9
4	-	-	CNx Pin 10/GND	10
-	25	-	CNx Pin 11	11
-	-	46	CNx Pin 12/GND	12
5	-	-	CNx Pin 13	13
-	26	-	CNx Pin 14/GND	14
-	-	47	CNx Pin 15	15
6	-	-	CNx Pin 16/GND	16
-	27	-	CNx Pin 17	17
-	-	48	GND	18
7	-	-	CNx Pin 19	19
-	28	-	GND	20
-	-	49	CNx Pin 21	21
8	-	-	GND	22
-	29	-	CNx Pin 23	23
-	-	50	GND	24
9	-	-	CNx Pin 25	25
-	30	-	GND	26
-	-	51	CNx Pin 27	27
10	-	-	GND	28
-	31	-	CNx Pin 29	29
-	-	52	GND	30
11	-	-	CNx Pin 31	31
-	32	-	GND	32
-	-	53	CNx Pin 33	33
12	-	-	GND	34
-	33	-	CNx Pin 35	35
-	-	54	GND	36
13	-	-	CNx Pin 37	37
-	34	-	GND	38

-	**-**	**55**	CNx Pin 39	39
14	**-**	**-**	GND	40
-	**35**	**-**	CNx Pin 41	41
-	**-**	**56**	GND	42
15	**-**	**-**	CNx Pin 43	43
-	**36**	**-**	GND	44
-	**-**	**57**	CNx Pin 45	45
16	**-**	**-**	GND	46
-	**37**	**-**	CNx Pin 47	47
-	**-**	**58**	GND	48
17	**-**	**-**	5V, 2 A max	49
-	**38**	**-**	GND	50
-	**-**	**59**	NC	---
18	**-**	**-**	NC	---
-	**39**	**-**	NC	---
-	**-**	**60**	NC	---
19	**-**	**-**	NC	---
-	**40**	**-**	NC	---
-	**-**	**61**	NC	---
20	**-**	**-**	NC	---
-	**41**	**-**	NC	---
-	**-**	**62**	NC	---
21	**-**	**-**	NC	---
-	**42**	**-**	NC	---

IDAN-FPGA6800 68 pin D connector

Figure 6: Dimensional Drawing of 68 pin D IDAN connector

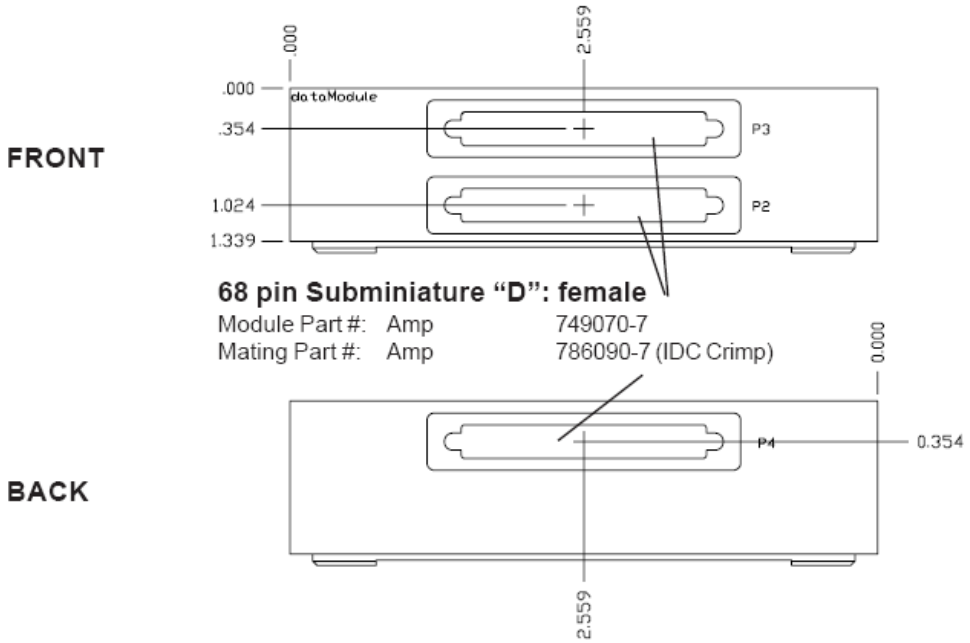

Figure 7: IDAN FPGA6800 68D Connector Pins

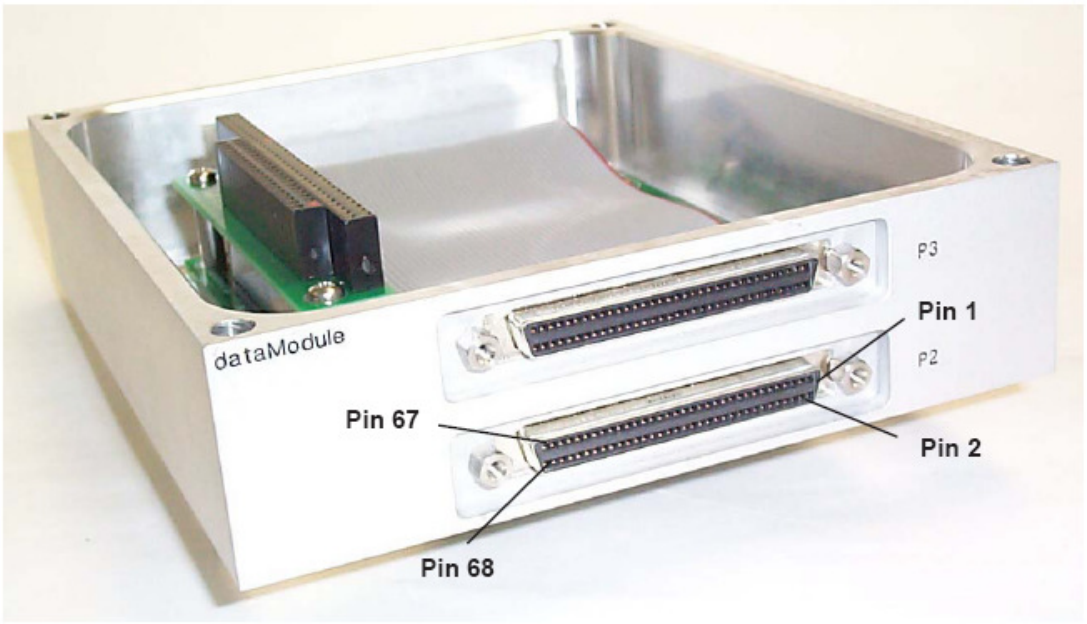

Table 31: IDAN 68D- 68 Pin High Density “D” Connector (female)

IDAN-FPGA6800HR-68D: 68 Pin High Density "D" Connector (Female)			
IDAN P2 Pin #		Signal	FPGA6800HR
Row 1	Row 2		CN4 Pin #
1		CN4_pin_01	1
	2	CN4_pin_02 or GND – Controlled by CN4_gnd_enable_1	2
3		CN4_pin_03	3
	4	CN4_pin_04 or GND – Controlled by CN4_gnd_enable_1	4
5		CN4_pin_05	5
	6	CN4_pin_06 or GND – Controlled by CN4_gnd_enable_1	6
7		CN4_pin_07	7
	8	CN4_pin_08 or GND – Controlled by CN4_gnd_enable_1	8
9		CN4_pin_09	9
	10	CN4_pin_10 or GND – Controlled by CN4_gnd_enable_2	10
11		CN4_pin_11	11
	12	CN4_pin_12 or GND – Controlled by CN4_gnd_enable_2	12
13		CN4_pin_13	13
	14	CN4_pin_14 or GND – Controlled by CN4_gnd_enable_2	14
15		CN4_pin_15	15
	16	CN4_pin_16 or GND – Controlled by CN4_gnd_enable_2	16
17		CN4_pin_17	17
	18	DIGITAL GND	18
19		CN4_pin_19	19
	20	DIGITAL GND	20
21		CN4_pin_21	21
	22	DIGITAL GND	22
23		CN4_pin_23	23
	24	DIGITAL GND	24
25		CN4_pin_25	25
	26	DIGITAL GND	26
27		CN4_pin_27	27
	28	DIGITAL GND	28
29		CN4_pin_29	29
	30	DIGITAL GND	30
31		CN4_pin_31	31
	32	DIGITAL GND	32
33		CN4_pin_33	33
	34	DIGITAL GND	34
35		CN4_pin_35	35

	36	DIGITAL GND	36
37		CN4_pin_37	37
	38	DIGITAL GND	38
39		CN4_pin_39	39
	40	DIGITAL GND	40
41		CN4_pin_41	41
	42	DIGITAL GND	42
43		CN4_pin_43	43
	44	DIGITAL GND	44
45		CN4_pin_45	45
	46	DIGITAL GND	46
47		CN4_pin_47	47
	48	DIGITAL GND	48
49		+5 VOLTS 2 Amp Max.	49
	50	CN4_pin_16/GND – Controlled by Jumper	50
51 - 68		RESERVED	-

Table 32: IDAN 68D- 68 Pin High Density "D" Connector (female)

IDAN-FPGA6800HR-68D: 68 Pin High Density "D" Connector (Female)			
IDAN P3 Pin #		**Signal**	**FPGA6800HR**
Row 1	**Row 2**		**CN5 Pin #**
1		CN5_pin_01	1
	2	CN5_pin_02 or GND – Controlled by CN5_gnd_enable_1	2
3		CN5_pin_03	3
	4	CN5_pin_04 or GND – Controlled by CN5_gnd_enable_1	4
5		CN5_pin_05	5
	6	CN5_pin_06 or GND – Controlled by CN5_gnd_enable_1	6
7		CN5_pin_07	7
	8	CN5_pin_08 or GND – Controlled by CN5_gnd_enable_1	8
9		CN5_pin_09	9
	10	CN5_pin_10 or GND – Controlled by CN5_gnd_enable_2	10
11		CN5_pin_11	11
	12	CN5_pin_12 or GND – Controlled by CN5_gnd_enable_2	12
13		CN5_pin_13	13
	14	CN5_pin_14 or GND – Controlled by CN5_gnd_enable_2	14
15		CN5_pin_15	15
	16	CN5_pin_16 or GND – Controlled by CN5_gnd_enable_2	16
17		CN5_pin_17	17
	18	DIGITAL GND	18

19		CN5_pin_19	19
	20	DIGITAL GND	20
21		CN5_pin_21	21
	22	DIGITAL GND	22
23		CN5_pin_23	23
	24	DIGITAL GND	24
25		CN5_pin_25	25
	26	DIGITAL GND	26
27		CN5_pin_27	27
	28	DIGITAL GND	28
29		CN5_pin_29	29
	30	DIGITAL GND	30
31		CN5_pin_31	31
	32	DIGITAL GND	32
33		CN5_pin_33	33
	34	DIGITAL GND	34
35		CN5_pin_35	35
	36	DIGITAL GND	36
37		CN5_pin_37	37
	38	DIGITAL GND	38
39		CN5_pin_39	39
	40	DIGITAL GND	40
41		CN5_pin_41	41
	42	DIGITAL GND	42
43		CN5_pin_43	43
	44	DIGITAL GND	44
45		CN5_pin_45	45
	46	DIGITAL GND	46
47		CN5_pin_47	47
	48	DIGITAL GND	48
49		+5 VOLTS 2 Amp Max.	49
	50	CN5_pin_16/GND – Controlled by Jumper	50
51 - 68		RESERVED	-

Table 33: IDAN 68D- 68 Pin High Density “D” Connector (female)

IDAN-FPGA6800HR-68D: 68 Pin High Density "D" Connector (Female)			
IDAN P4 Pin #		Signal	FPGA6800HR
Row 1	Row 2		CN6 Pin #
1		CN6_pin_01	1
	2	CN6_pin_02 or GND – Controlled by CN6_gnd_enable_1	2
3		CN6_pin_03	3
	4	CN6_pin_04 or GND – Controlled by CN6_gnd_enable_1	4
5		CN6_pin_05	5
	6	CN6_pin_06 or GND – Controlled by CN6_gnd_enable_1	6
7		CN6_pin_07	7
	8	CN6_pin_08 or GND – Controlled by CN6_gnd_enable_1	8
9		CN6_pin_09	9
	10	CN6_pin_10 or GND – Controlled by CN6_gnd_enable_2	10
11		CN6_pin_11	11
	12	CN6_pin_12 or GND – Controlled by CN6_gnd_enable_2	12
13		CN6_pin_13	13
	14	CN6_pin_14 or GND – Controlled by CN6_gnd_enable_2	14
15		CN6_pin_15	15
	16	CN6_pin_16 or GND – Controlled by CN6_gnd_enable_2	16
17		CN6_pin_17	17
	18	DIGITAL GND	18
19		CN6_pin_19	19
	20	DIGITAL GND	20
21		CN6_pin_21	21
	22	DIGITAL GND	22
23		CN6_pin_23	23
	24	DIGITAL GND	24
25		CN6_pin_25	25
	26	DIGITAL GND	26
27		CN6_pin_27	27
	28	DIGITAL GND	28
29		CN6_pin_29	29
	30	DIGITAL GND	30
31		CN6_pin_31	31
	32	DIGITAL GND	32
33		CN6_pin_33	33
	34	DIGITAL GND	34
35		CN6_pin_35	35

	36	DIGITAL GND	36
37		CN6_pin_37	37
	38	DIGITAL GND	38
39		CN6_pin_39	39
	40	DIGITAL GND	40
41		CN6_pin_41	41
	42	DIGITAL GND	42
43		CN6_pin_43	43
	44	DIGITAL GND	44
45		CN6_pin_45	45
	46	DIGITAL GND	46
47		CN6_pin_47	47
	48	DIGITAL GND	48
49		+5 VOLTS 2 Amp Max.	49
	50	CN6_pin_16/GND – Controlled by Jumper	50
51 - 68		RESERVED	-

Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD EMBEDDED TECHNOLOGIES, INC. This warranty is limited to the original purchaser of product and is not transferable.

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