TDA5150

SmartLEWIS™ TX

Programming the TDA5150

with hands-on examples and hints

Application Note

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Wireless Control

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Revision History: July 2012; V 1.1 (current revision)	
Previous Revision: V1.0; June 2010 edition	
Page	**Subjects (major changes since last revision)**
5	433 MHz band lower limit changed • from previous value of 425 MHz as defined per **TDA5150 Datasheet V1.0** (July 2009 edition) to • 433 MHz, in accordance with the limit listed in **TDA5150 Datasheet V1.1** (June 2012 edition) *Note: the change of the mentioned lower limit value does not affect the operability of devices intended for operation in compliance with the **ETSI EN300-220** or **FCC Part 15** standard. The 425.000 -432.999 MHz segment is beyond (below) the license-free (ISM) frequency band, defined by the respective standards. Thus devices intended for operation in the license-free 433 MHz ISM band are not affected by rise of the lower operating frequency limit from 425 MHz to 433 MHz. Above mentioned limit changed in **Chapter 1.1** and **Chapter 1.2** (both on Page 5).*
39	**Table 4** updated in accordance with Special Function Register definitions, as listed per **TDA5150 Datasheet V1.1** (June 2012 edition). *Note:* *1. according to **TDA5150 Datasheet V1.1** the following bits have been moved to **reserved** class: 0x0C.5; 0x10.5; 0x14.5; 0x18.5* *2. reassignment of above mentioned bits to **reserved** class does not affect chip functionality at all. The bits are set to 0 by Reset and Brownout Reset and shall be left unchanged.*
General	*Note: The chapter numbering and structure of **TDA5150 Datasheet V1.1** is identical with that of **TDA5150 Datasheet V1.0**. For better readability references to TDA5150 Datasheet chapter numbers in this material omit the datasheet version, as it is valid for both documents.*

Table of Contents

1 Introduction

This Application Note gives a systematic overview of the TDA5150 transmitter programming procedures and configuration. The approach stays close to the System Programmers viewpoint, explaining the particularities of the SPI protocol, the structure and functions associated with the Special Function Register bank (referred further as SFRs) and at last but not least best practice for programming the SFRs according to the required transmission parameters.

Further it explains the relations between modulation parameters and their influence on the RF-signal spectrum. This is an important aspect as long as the radiated signals must comply with one or more regulatory standards.

The final part of the material contains hints about system debugging (hardware and firmware) and some transmitter programming code examples.

1.1 TDA5150 overview

The TDA5150 is a low power ASK/FSK RF transmitter for the ISM frequency bands 300-320 MHz, 433-450 MHz, 863-870 MHz and 902-928 MHz.

Bi-phase modulation schemes like Manchester, bi-phase mark, bi-phase space, etc. are supported. The IC offers a high level of integration and needs only a few external components, like a crystal, a few blocking capacitors and the necessary matching elements on the RF-PA output. A fully integrated sigma-delta fractional-N PLL synthesizer covers all above mentioned frequency bands with a high frequency resolution, using only one VCO running around 1.8 GHz. The on-chip synthesizer comprises a VCO, several dividers, loop filter with programmable bandwidth and a highly accurate 3rd order sigma-delta modulator.

With a programmable data shaping filter, a very accurate GFSK modulation is achieved.

The output stage of the TDA5150 contains a C class power amplifier with a very good efficiency factor, several selectable power stages and user-selectable RF output power level.

An ASK-data input, with envelope shaping capability is also provided.

On chip antenna matching capacitor array is available (for tuning).

The main clock source is a single-pin crystal oscillator running at around 13.00 MHz. Datasheet specified frequency range of this reference clock is 12MHz..14MHz.

A programmable divided clock output is available. The device is configured by means of a 3-wire interface (SPI bus), programmable even during power down state.

1.2 TDA5150 features

The main features of the TDA5150 transmitter are

- Sigma-delta fractional-N PLL synthesizer with high frequency resolution (<7 Hz)
- Multiband / Multichannel operation (300-320 MHz, 433-450 MHz, 863-870 MHz, 902-928 MHz)
- Supply voltage range 1.9 V - 3.6 V
- Low battery detector with two threshold levels (2.1 V and 2.4 V)
- Small package size (TSSOP-10)
- Operating temperature range -40°C to +85°C
- Full qualification for automotive standard
- Modulation types ASK (OOK), FSK (CPFSK) and GFSK
- Supports all bi-phase encoding formats
- Low supply current (in Power Down mode less than 0.5 mA, RF transmission 9 mA @ +5 dBm)
- Programmable output power, with nominal levels of +5 dBm, +8 dBm, +10 dBm
- Software selectable on-chip tuning capacitors for antenna matching network
- Programmable divided clock output (for clocking external devices)
- Integrated 3-wire serial interface bus (SPI)

2 Things to keep in mind before starting code development

Before starting effective code development, study in advance carefully and thoroughly the ***TDA5150 Datasheet***. Notice and recheck each ambiguous point if you are at a guess.

Define your usecase (or cases) and scenarios and check if there are no contradictions between these and the required frame / message format.
Make a list of registers which must be programmed for the given usecase/ application (*Method 1*)

or use the register set, as generated by TESEUS for the given setup (*Method 2*).

For instance if only ASK modulation is used, the value of SFR GFDIV (Gaussian filter, 0x1D) may be left in the after-reset state, as its content is irrelevant if ASK mode is used.

Similarly, if only one PLL channel is used (say *Channel A*), the contents of Channel B; C; D are irrelevant and programming of those channels (the SFRs PLLINTB; PLLFRACB0; PLLFRACB1...up to PLLFRACD1) may be skipped (i.e. the associated SFRs left in after-reset state).

*Note: The SFR write operation may be followed by read of SPICHKSUM (0x00) register to make sure that the content have been transferred unaltered – like described by example in **Chapter 5**.*
*This procedure may be useful, but is not mandatory – especially by restricted µC resources or processing time allocation on the host side. See **Chapter 2.5.2** (SPICHKSUM) in **TDA5150 Datasheet** for details.*

Define the values for all the SFRs, which are required by your usecase /application. Before stepping to next project phase, check and verify if the transmission parameters (carrier/ channel frequency, datarate, modulation parameters, baudrate divider output frequency etc) are the same as the target specifications and no conflicts occur.

Adjust the parameters if there are significant deviations (resulting in error) versus nominal (target) values. For instance the frequency deviation (in FSK / GFSK mode) will change in small steps, and a slight error (in magnitude of less than 1%) may occur versus nominal frequency deviation, but this does not affect seriously either the spectrum of the generated signal, or the achieved Signal to Noise ratio (S/N) on the receiver side.

The SFRs required to set up of a particular transmission configuration may be programmed individually (SFR write) and the sequence (order) may be arbitrary (but all required SFRs must be set, of course),
or instead of individual SFR writes, the SFR burst write mode may be used.

In this last case the address of the first written byte is specified, and the following bytes are written to auto-incremented addresses. This procedure might shorten the dead time by SFR programming.

Clearly the consecutive SFR contents must be output in sequential order and not randomly during this procedure (see ***Timing Diagrams*** part in ***TDA5150 Datasheet***).

After programming all the required SFRs for the particular usecase, the transmission can be started. Clocking of data, output from µC into the transmitter may be:

- done by µC, in asynchronous mode, as described in ***Chapter 2.4.11.1*** of ***TDA5150 Datasheet***

or

- latched independently by TDA5150, in synchronous mode, as described in ***Chapter 2.4.11.2*** of the same document.

3 Modulation parameters and their influence on signal spectrum

It is not the system programmer's express mission to analyze and check the parameters describing RF performance, but knowledge about the main factors influencing signal quality and spectrum may help by system design and during firmware development.

If the transmitter will be part of an already given system (embedded), the modulation parameters are usually given and there is little room to change them. However, even if the modulation type (ASK; FSK or GFSK) is imposed (by system compatibility and specifications) certain parameters, which are programmable (by mean of SFRs) may have a major impact on modulated signal spectrum and occupied bandwidth.

3.1 Amplitude shift keying (ASK)

The amplitude shift keying (ASK) function is implemented in the following way: the RF signal, generated by VCO and under the control of the Sigma-Delta fractional-N PLL is fed to a group of class-C Power Amplifier stages, before being transmitted. The Power Amplifier (PA) includes an output power control, ASK sloping, switchable capacitors for antenna fine tuning and an auto switch -off mechanism, as part of the Fail-Safe system. If critical supply voltage or frequency error events occur, the Fail-Safe mechanism switches off the PA, thus preventing erroneous transmissions.

In FSK or GFSK mode, the PA is always ON during the transmission's duration. By ASK mode, the Sigma-Delta PLL delivers a continuous RF signal to the PA. The PA is switched ON and OFF, according the data signal to be transmitted. Additionally there is an ASK sloping mechanism, which switches the different power stages ON and OFF in a well determined sequence, correlated with the transitions on data signal line. This power ramping procedure minimizes out-of band transients and spectral splatter. The ASK modulator is described in detail in chapter ***2.4.8*** of ***TDA5150 Datasheet***.

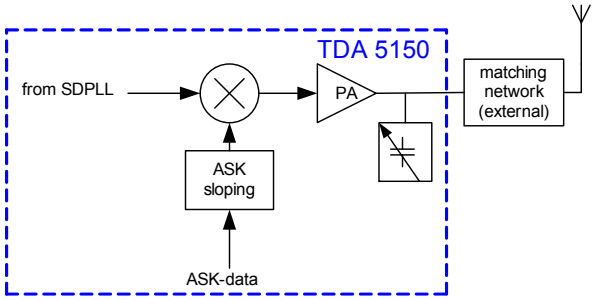

Figure 1 ASK modulator, block diagram

The PA comprises 11 elementary cells in parallel. Each one is a class-C amplifier. The cells are grouped in three PA blocks. PA Block 0 is composed of 9 stages, PA Block 1 and PA Block 2 are strong single stages.

Each PA Block can be individually enabled and disabled to optimize power consumption and efficiency in an output power subrange. The overall 11 PA stages allow control of the RF output power in 11 steps over a range of 20 dB. The PA can be switched OFF by disabling all the 11 stages.

The ASK or FSK modulation is selected by SFR TXCFG1 (0x05). There are two possible setups, designated ***ModulationSetting1***, and ***ModulationSetting2***.

The bit D of Transmit Command Byte selects the active setting. This allows fast switching between the two modulation setups, without any further register configuration.

An amplitude modulated signal can be described in time domain as:

(1)

$$f(t) = A_c \sin(\omega_c t + \varphi) \times \left(\sum_j A_{mj} \times \sin(\omega_m t + \theta_m) \right)$$

where *Ac* is the amplitude of the carrier signal and *Amj* the amplitude of the modulation signal components.

The modulated signal contains frequency components (denoted tones) which are grouped at multiples of the modulation frequency and centered around the carrier frequency as shown in **Figure 2**. If the RF carrier frequency is denoted *fc*, then the frequency of the tones, grouped around the carrier is $f_{tj} = (f_c \pm j*f_m)$ where f_m is the modulation frequency and j the order (harmonic) of the fundamental tone. These f_{tj} components are denoted also as sideband components, respectively upper- and lower sideband, relative to the carrier's frequency (upper sideband if $f_{tj} > f_c$ and lower sideband if $f_{tj} < f_c$).

If the modulating signal is a square-wave (as in case of the TDA5150) and the RF power amplifier is switched ON and OFF (i.e. ON/OFF keying, referred also as OOK is used) the spectrum of the modulated carrier contains the odd-order modulation tones, as dominants in the upper and lower sidebands, in other words the energy of the modulated RF-signal is expected to be grouped mainly around the $f_{tj} = [f_c \pm (2j+1)*f_m]$ spectral lines and significantly lower in the region of the even-order tones (of $f_{tj} = [f_c \pm 2j*f_m]$ frequency).

In practice this means that the occupied bandwidth (OBW) of an amplitude modulated signal, with modulation depth close to 100% (i.e. generated by switching the PA-stages of the transmitter on and off) will be always at least the double of the equivalent modulation frequency (OBW > 2 f_m) as both sidebands are contained.

If the occupied bandwidth is computed based on the criteria of including all the spectral components -20dB below the carrier power, the 3rd order sideband tones will fall also in this region and the expected value of the occupied bandwidth will be, for a given f_m equivalent modulation frequency:

(2)

$$OBW = 6 \times fm$$

In **Figure 2** the blue trace corresponds to a signal spectrum generated with square-wave modulating signal and modulation depth close to 100% (i.e. similar to the on-off keying method). The green plot corresponds to the same modulating signal, but modulation depth reduced to 30%. The plot have been recorded by measurement of a laboratory-quality signal generator with programmable AM modulation depth, instead of a TDA5150 transmitter, as this last uses on-off keying method and not an AM-modulator with programmable AM-depth.

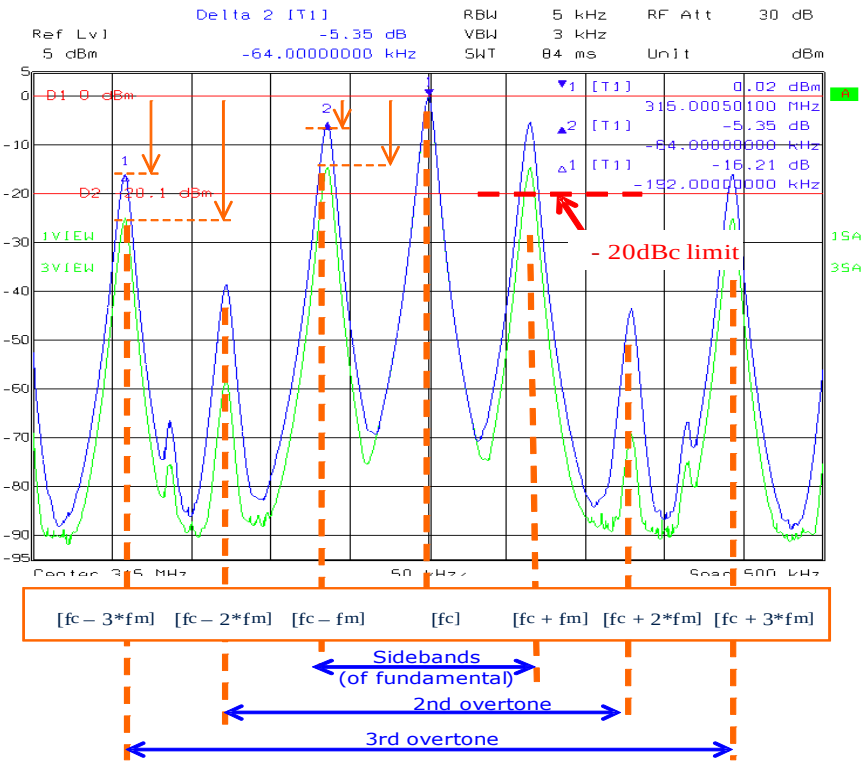

Figure 2 Sideband tones of an AM signal

Note: Judged only on occupied bandwidth criteria usage of a moderate modulation depth seems to have clear advantage versus on-off keying method, but it must be kept in mind that if the modulation depth is reduced, the RF-power amplifier will be never switched off during the transmission, thus reducing the DC power usage efficiency of the transmitter.

A means of reducing the occupied bandwidth and spectral splatter resulting due to the transients (mainly during off-on switching transitions) is the inherent on-chip ASK sloping capability provided within the TDA 5150.

This means that instead of switching all PA Stages at the same time, they are switched ON one after the other in a configurable time sequence. The power sloping is controlled by SFR SLOPDIV (0x19.7:0). The register content is equal with the number of reference oscillator cycles elapsed until the next PA stage is switched ON or OFF.

The power sloping mechanism is described in detail in ***Chapter 2.4.8.2*** of ***TDA5150 Datasheet***.

Figure 3 illustrates the difference in spectral energy distribution between two signals with same nominal power and datarate, both generated with ASK modulation. It is clearly visible that if power sloping option is used, the peak power radiated into adjacent channels is significantly lower for the sloped signal, onward the 5th order sidetone. In other words, the power sloped ASK signal will generate less interference at frequency offsets larger than [$f_c \pm 3*f_m$] as the unsloped signal.

It is recommended to implement power sloping in ASK applications, especially if higher data rates are used, and to verify the enhancement in terms of reduced spectral splatter.

Please keep in mind:

- a steep rise of the RF power may cause spectral splatter. This is not a chip issue, it is merely a consequence of physical laws. As steeper the transition (i.e. as shorter the rise time) as wider the expected bandwidth of the transient
- a controlled rise of the signal power (by AM modulation) does lead to a moderate increase of jitter by edge detection, but if edge detection and expected phase transition windows are handled properly (by Firmware) there will be no sensitivity loss (or just insignificant) on the receive side and, at the same time out-of-band signals (spectral splatter, due to transient) are efficiently minimized on the transmit side
- as rule of thumb activation of power sloping, with a moderate ratio (around 10%) is recommended. Very low ratios (in magnitude of 1..3%) may lead to crosstalk between carrier and sloping clock frequency, leading to sidetones close to carrier, therefore higher sloping ratios (>5%) are generally recommended.

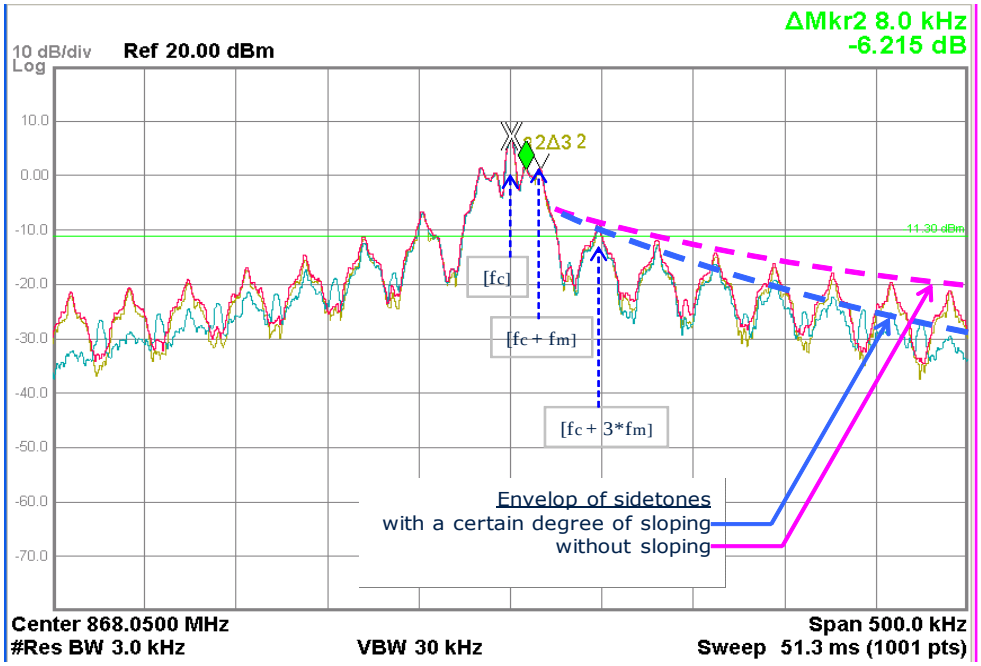

Figure 3 Level of sidebands, ASK signal with and without power ramping

The example shown in **Figure 4** depicts (from left to right) the time domain plot of an unsloped signal, generated by TDA5150 in ASK mode (left side plot), a signal sloped with 10% of bit duration (middle), and a signal sloped with 30%, which is the maxima of sloping setting on the right side.

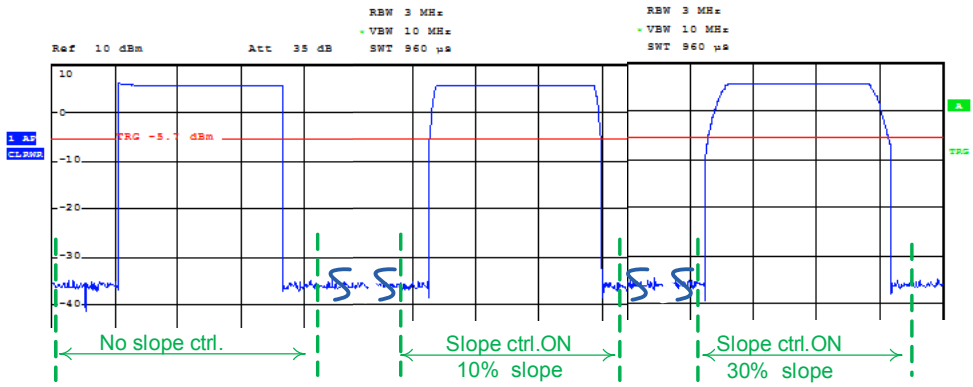

Figure 4 Effect of sloping on signal power (RF-power vs. time diagram)

A simple method for checking the effectiveness of RF-power sloping on the spectral splatter is the following:

- set a spectrum analyzer to center frequency equal to intended carrier frequency of the investigated transmitter
- set the frequency span to around 10..15MHz (or the *Start* and *Stop* frequencies, as their difference is the *Span*)
- set the resolution bandwidth (RBW) of the instrument to around 200..300 kHz
- set the video bandwidth to at least 3 times the RBW, to avoid distortion of the detected pulses
- set a reasonably long sweep time, peak detector mode and maximum hold for the respective trace (MaxHold)
- observe the “spikes” left and right from carrier, caused by the RF-power transient (mainly caused by the off-->on transient of the RF carrier). As long as the instrument is in MaxHold mode, from time to time a Clear & Record (Write) operation is necessary, to clear the recorded trace and achieve a new acquisition.

Recording more traces with the method described and at the same time varying the sloping ratio (SFR register value; SLOPDIV (0x19.7:0)) can give a fast (but coarse) indication about the effectiveness of a particular setting on the maxima of the expected transients. For accurate measurements the method described in the regulatory specification should be used, of course instead of the quick-check described above, and which is exemplified in **Figure 5**. In this example the transients in the signal with 10% slope ratio have visibly lower energy as in the signal generated with deactivated slope control.

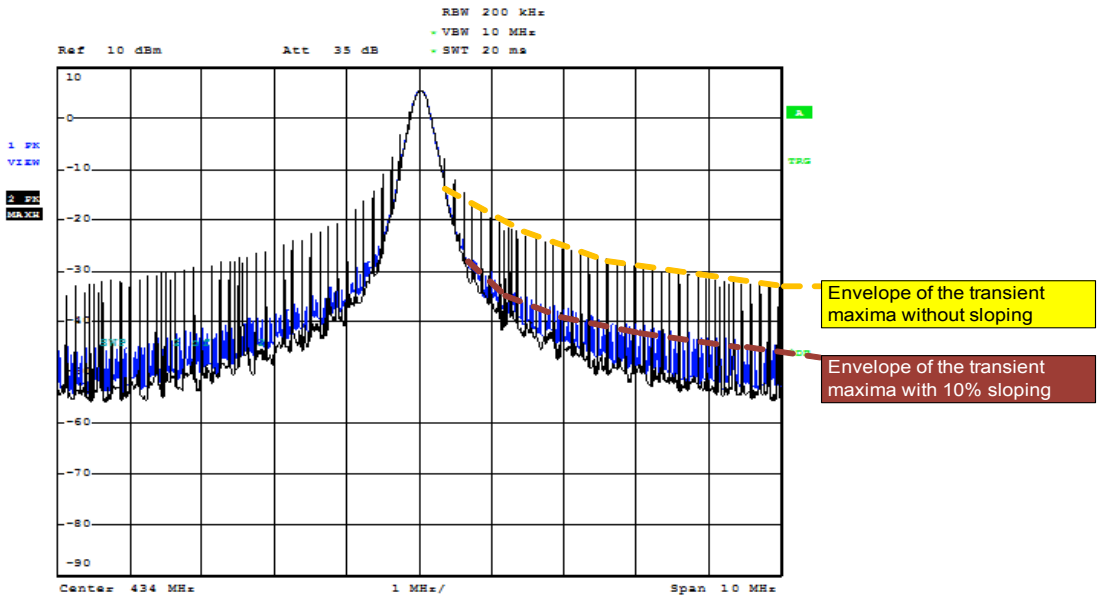

Figure 5 Effect of RF-power sloping on the transients

3.2 Frequency shift keying (FSK) and Gaussian shaped frequency shift keying (GFSK)

In FSK and GFSK modulation mode the two frequencies, corresponding to positive and negative frequency shift are directly associated with specific divider numbers (of the Sigma/Delta fractional PLL). The modulation is achieved by switching (or transiting) between these two divider numbers and it takes effect under the control of data signal state (and encoding scheme, if other then NRZ).

By this method, and assuming NRZ data encoding, a positive frequency deviation (relative to nominal carrier frequency) occurs for a logical "1" of the already encoded data, and a negative frequency deviation for a logical "0" if the data inversion bit INVERT in SFR TXCFG1 (0x05.3) is 0 (inversion OFF). If the inversion function is active (INVERT bit is set to 1), the frequency shift directions are inverted (i.e. negative frequency deviation for logical "1" of input data and positive deviation for “0”) for the same NRZ data stream.
With direct FSK modulation a well controlled frequency shift can be achieved and the pullability of the crystal in the reference frequency oscillator circuit is no issue anymore, like by the classical FSK, where usually a reactance does “pull” the crystal frequency.

If frequency modulation is used (FSK or GFSK) Carson's bandwidth rule can be applied to define the approximate bandwidth requirements.

This rule is valid for communications system components using frequency modulated carriers modulated by signals which can be regarded as continuous in time domain and having a broader spectrum of frequencies (in frequency domain) rather than a single frequency component. The rule delivers accurate results for occupied bandwidth calculation if the modulating components are sine waves with a well defined upper frequency limit, but has certain limitations in bandwidth prediction accuracy if the modulating signal has discontinuities (in time domain) such as a square wave or pulse (i.e. the equivalent Fourier series has a large number of components, or theoretically an infinite number).
However, due to the simplicity of the method Carson's bandwidth rule is worth to be used for a first, at least coarse approximation by estimation of occupied bandwidth. More elaborate models, taking in account the discontinuities in the signal shape deliver accurate results (i.e. the overtones are taken in account, the signal is decomposed in Fourier series for analysis) but the mathematical apparatus behind is more complex and usually requires a dedicated environment (software) for computations.

Carson's bandwidth rule is expressed by the relation **BWR = 2(Δf + fm)** where BWR is the bandwidth requirement, Δf is the peak frequency deviation, and fm is the highest frequency in the modulating signal.

For example, an FM signal with 50 kHz peak deviation, and a maximum modulating frequency of 4kHz, would require an approximate bandwidth of 2*(50 + 4) = 108 kHz.
The maximum modulating frequency has to be computed in accordance with the encoding scheme used.
For instance by NRZ encoding the fundamental frequency is half of the nominal datarate and by Manchester encoding it equals the datarate.

Note: A carrier modulated by a non-periodical signal will have theoretically speaking an infinite number of sidebands and hence an infinite bandwidth, but in practice all significant sideband energy (98% or more) is concentrated within the bandwidth defined by Carson's rule. It's a useful approximation, but setting the arbitrary definition of occupied bandwidth at 98% of the power still means that the power outside the band is only about 17 dB less than the carrier inside, therefore Carson's Rule is of little help by spectrum planning, as the limit (maxima) of power falling into adjacent channel(s), allowed by most regulatory standards is well below -17 dBc.

The TDA5150 transmitter has the capability of shaping the modulation signal in FM mode, according to transfer characteristics of a Gaussian filter. This option can further reduce the occupied RF bandwidth versus FSK modulation, as shown in **Figure 6**, where the blue trace is the spectral plot of an FSK signal and the green trace is the spectral plot of a GFSK signal, both having same frequency deviation, same datarate and are encoded according to the same scheme.

The Gaussian shaping is realized in the TDA5150’s modulator block as a number of fixed frequency steps (transitions) between the 2 FSK frequencies, corresponding to low and high, or 0 and 1 on the modulator input.

The data shaping is realized in digital domain, as Gaussian filtered FSK (GFSK) and can be enabled by setting the GFBYP bit of SFR GFXOSC (0x1E.3) to 0. The feature is described in detail in ***Chapter 2.4.7*** of ***TDA5150 Datasheet***.

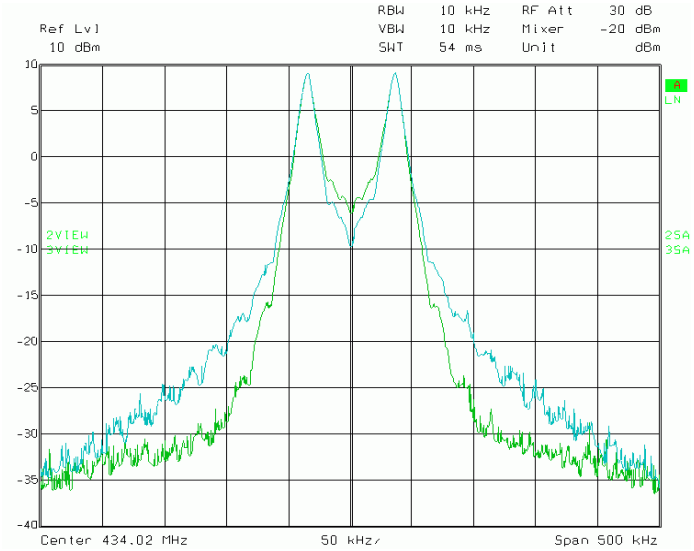

Figure 6 Occupied bandwidth of FSK and GFSK signals with same frequency deviation and datarate

It is recommended to program the GFDIV register in such way, that the GF divider's content, *NGF* is 16 times the chip-rate, which allows optimum Gaussian filtering. However this is a recommendation and not mandatory.
Figure 7 illustrates the difference between two Gaussian filter settings. Left side plot corresponds to 7 samples / chip setting (GFSK filter), right side plot stays for 20 samples / chip. All other parameters are identical.
It is obvious that the leaner left-side plot yields more margin versus the first "shoulder" of the spectrum mask (marked with dotted ellipse line) as the right -side plot, which was obtained by higher sampling rate / chip.

It must be kept in mind that the Gaussian filter setting on the transmit side (TX) does influence not only the spectrum of the radiated signal, but also the waveform on the receive side, or to be more concise the waveform on the receiver's FM-demodulator output. Therefore to achieve optimum performance the system designer has to focus on two aspects in terms of spectrum and signal quality:

- to "squeeze" the RF-spectrum of the signal generated by transmitter and radiated by antenna(s) within the prescribed spectrum mask (the mask is usually part of regulatory specifications) and
- to achieve best receiver sensitivity, the FM-modulated signal at the receiver's demodulator output must fulfill some performance criteria (noise, high- and low- threshold level, jitter, over- and undershoot etc).
  The visual check of the mentioned parameters is frequently referred as the "eye diagram" measurement. By fine-tuning the Gaussian filter settings of the TDA5150 in GFSK mode it is recommended to monitor at the same time the eye diagram pattern on the receiver's demodulator output, to make sure the simultaneous fulfillment of spectrum and signal quality criteria.

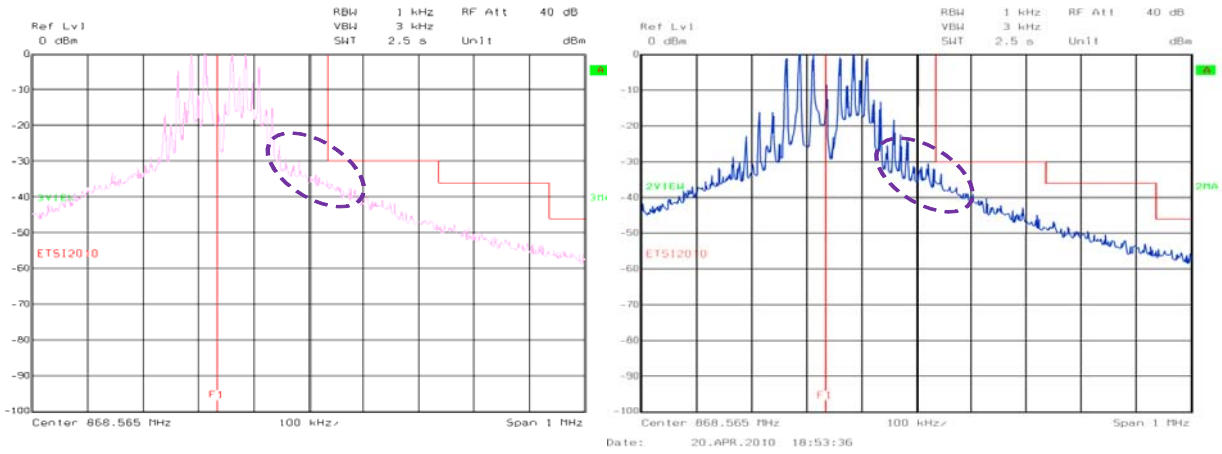

Figure 7 Gaussian filter's sampling rate influence on spectrum

3.3 Influence of PLL filter bandwidth on spectrum

In order to provide a high grade of flexibility by choice of modulation parameters, a PLL with programmable bandwidth have been implemented in the TDA5150. The PLL block is described in detail in ***Chapter 2.4.6*** of ***TDA5150 Datasheet***.

The PLL bandwidth is programmable by means of a 3 bit control field designated PLLBWTRIM in the SFR register PLLBW (0x25.6:4).

Aiming the minima of RF-energy leaking into the adjacent channel(s) and / or out of band transmissions, the PLL bandwidth should be set as narrow as possible, but not less than 1.5.. 2 times the chip rate, if FSK or GFSK modulation is used.

In order to maintain loop stability within the PLL and for optimum performance, the chargepump settings should be correlated with loop filter damping values, as described in ***Chapter 2.4.6.3*** of ***TDA5150 Datasheet***.

The PLL bandwidth setting has a noticeable influence on the phase noise of the RF-signal.
The dependencies of phase noise from PLL loop bandwidth are a complex topic in a fractional-N synthesizer system. **Figure 8** illustrates just the quantitative differences, visible on the slope of noise floor and which are obviously influenced by PLL loop bandwidth and damping factor settings.

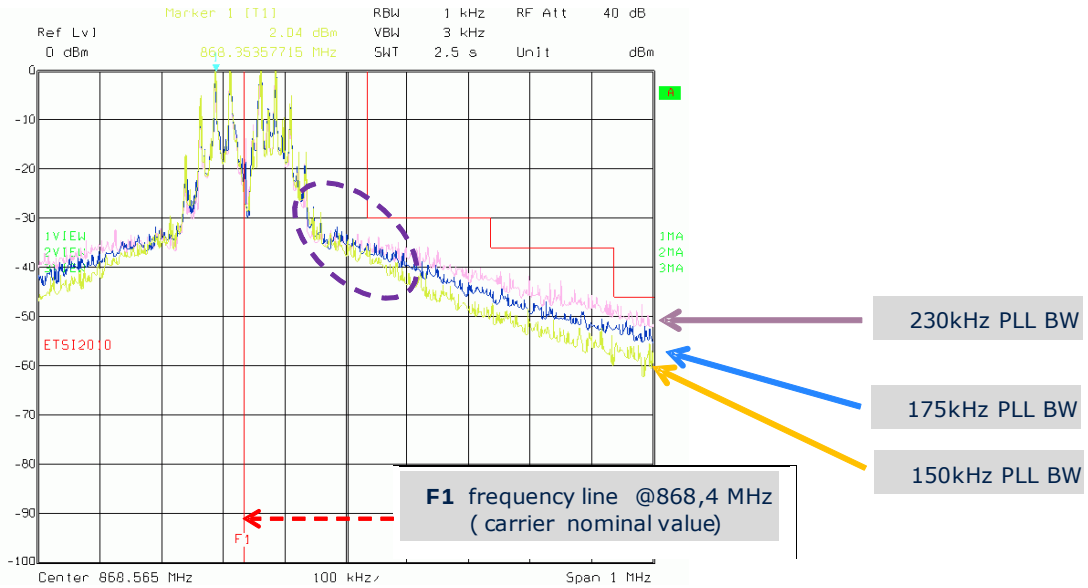

Figure 8 Influence of PLL BW on noise floor

Table 1contains a summary of the recommended PLL settings.

Table 1 Recommended PLL settings

Loop filter damping resistor selection			Chargepump settings and resulting current					Resulting nominal PLL bandwidth	Notes
PLLBW TRIM			CPTRIM				Current		
Bit2	Bit1	Bit0	Bit3	Bit2	Bit1	Bit0	[uA]	[kHz]	
0	0	0	*	*	*	*	*	*	not recommended
0	0	1	1	1	1	1	40	410	
0	1	0	1	1	0	0	32.5	375	
0	1	1	1	0	0	1	25	335	
1	0	0	0	1	1	0	17.5	270	
1	0	1	0	1	0	0	12.5	230	
1	1	0	0	0	1	0	7.5	175	
1	1	1	0	0	0	1	5	150	

4 Communication protocol on SPI bus and commands

4.1 The SPI protocol and timing diagrams

The control interface of TDA5150 is a 3-wire bus, compliant with Serial Peripheral Interface (SPI) definitions. It is used both for device control and data transmission. The function of pins assigned to the SPI-bus is the following:

- EN enable input with embedded pull-down resistor. High level on EN input enables the SPI transmission. The rising edge of the EN signal triggers the selection of the active SCK edge (for the consequent data transfer, until the EN line goes again low) thus transmission / sampling of data between the TDA5150 and the host (usually a µC) can start. For details refer to **Figure 9** and **Figure 10**.
- SDIO 3-state input/output. This bidirectional line is used for data transfer between the TDA 5150 and external host (usually a µC). On-chip pull-down resistor is connected to this pin.
- SCK clock input pin with embedded pull-down resistor. If SCK is at low level while EN goes high, the incoming SDIO data is sampled by falling edge of the SCK and the output SDIO data is set by the rising edge of SCK. Contrariwise, if SCK is at high level when EN goes high, the SDIO data is sampled at the rising edge of the SCK clock and output on SDIO by falling edge of the SCK clock. For details refer to **Figure 9**and **Figure 10**.

Note: The TDA5150 offers a clock output signal (CLKOUT), derived from the crystal frequency. It can be used as source for system clock or as synchronization source by bit (chip) rate generation. The output from different stages of the TDA5150's internal bit-rate divider can be routed to CLKOUT, as well as the output of the XTAL / 16 divider according to following rules:

1. *If SDIO is low when EN goes high, the selected output clock will be the XTAL/16 divider output (i.e. by default)*
2. *If SDIO is high when EN goes high, the source for output is selected as imposed by settings of the Clock pre- and afterscaler configurator Secial Function Register (CLKOUTCFG; 0x06).*

SPI commands are started by the rising edge of signals on the EN line and terminated by the falling edge (i.e. the SPI bus is responsive, until the EN line is held high).

A Burst Write mode is available as well and allows configuration of several SFRs within one block access, without cycling the EN line low - high - low to access the mentioned registers one by one.
By keeping the EN line at high level, subsequent bytes could be sent, and the byte address counter is always autoincremented (after completion of each byte transfer). Thus the total time required to transfer the content into a contiguous block several SFRs is shortend versus the sum of individual transfers involving the same total number of SFRs.

A self-explaining timing diagram, valid for the SPI bus is shown in **Figure 11**.

The active edge of SCK clock is programmable, and it is determined by the level on SCK line (high or low) at the moment of activation of the EN line (i.e. by the rising edge of pulse on EN line).

If the SCK line is low at that moment, the incoming SDIO data will be sampled by the falling edge of SCK pulse , and output by the rising edge (see **Figure 9** below).

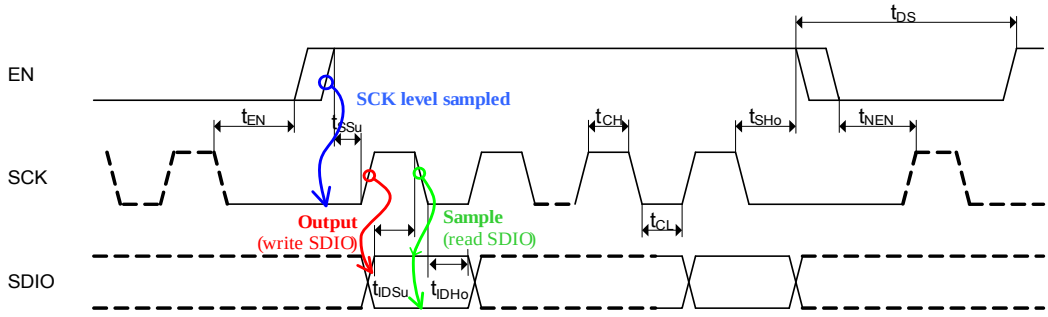

Figure 9 SPI Timing — scenario A: SCK low at rising edge of EN

If the SCK line is high during occurrence of rising edge on EN, the incoming SDIO data is sampled by the rising edge of the SCK signal, and output by the falling edge, as illustrated in **Figure 10**.

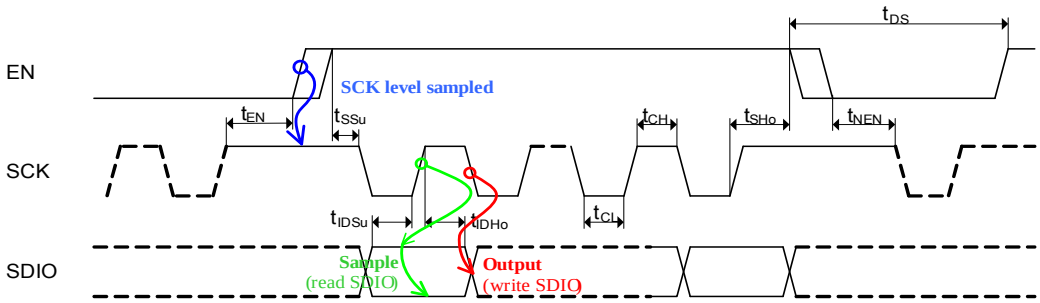

Figure 10 SPI Timing — scenario B: SCK high at rising edge of EN

In the following timing diagrams the four allowed SPI commands are shown - individual SFR write and read, respectively Burst Mode write and read.
The examples below are are plot assuming that SCK is held low during the leading edge of pulse on EN line, as shown by **Figure 9**. The incoming SDIO data will be sampled at the falling edge of SCK clock, and output on the SDIO line by the rising edge of pulse on SCK line.

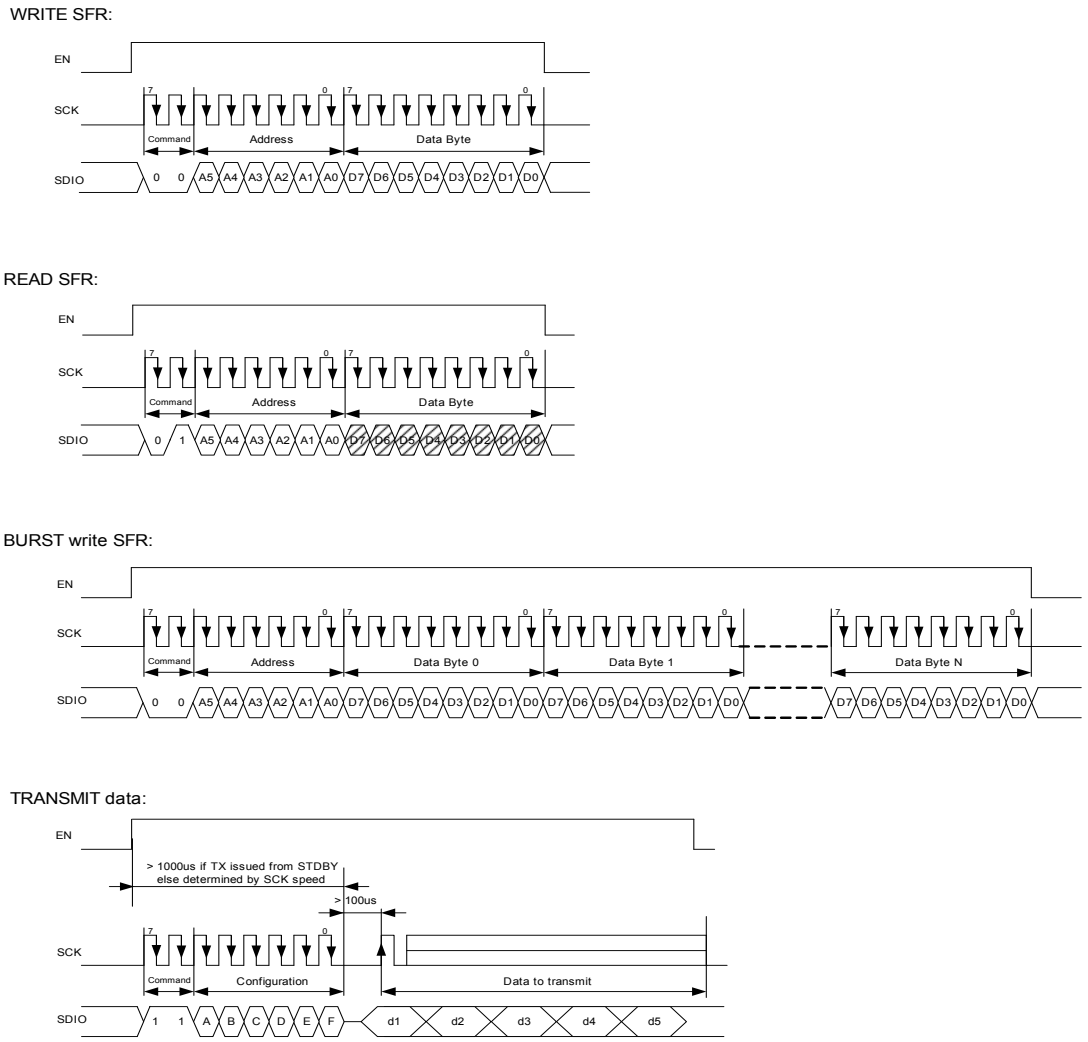

Figure 11 SPI bus timing diagrams

4.2 The XOR checksum

To enhance the reliability of communication over the SPI-bus in an environment which may be affected by EM noise and radio frequency radiations, the SPI block includes a checksum calculation mechanism, as an additional safety feature.

The checksum calculation is based on XOR operation between the address and the data during write operation of SFR registers. The checksum is in fact the XOR of the data 8-bit wise after every 8 bits of the SPI write command. The calculated checksum value is automatically written into SFR *SPICHKSUM* (0x00) and can be compared with the expected value. By executing a read operation of SFR *SPICHKSUM* (0x00) the register content is automatically cleared (after read). Read access to any of the other readable SFRs does not influence the SFR *SPICHKSUM.*

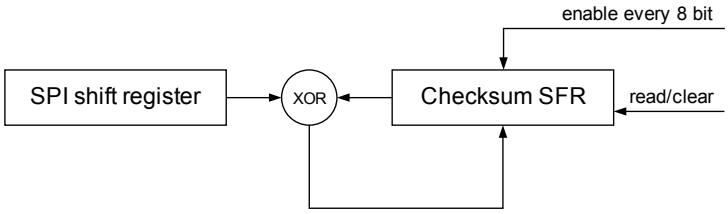

Figure 12 SPI checksum generator; block diagram

Example:

Write to SFR address 0x04, data 0x02, address 0x05, data 0x01

Table 2

Bytes transmitted via SPI	**Result in Checksum Register**
0000 0100	0000 0100
0000 0010	0000 0110
0000 0101	0000 0011
0000 0001	0000 0010

After writing into the registers, content of checksum SFR *SPICHKSUM* (0x00) will be 0x02.

Attention: If two consecutive read operations are executed on the SPICHKSUM (0x00) register, the first read operation delivers the correct result for checksum, and the second delivers 0x00, as the register was already cleared by the first read operation.

4.3 The SPI Command Byte

First byte of each SPI sequence is the **Command Byte**, containing a Function Code field and either an address field (by R/W operations) or Function Subfields (if the *Transmit Command* will be sent).

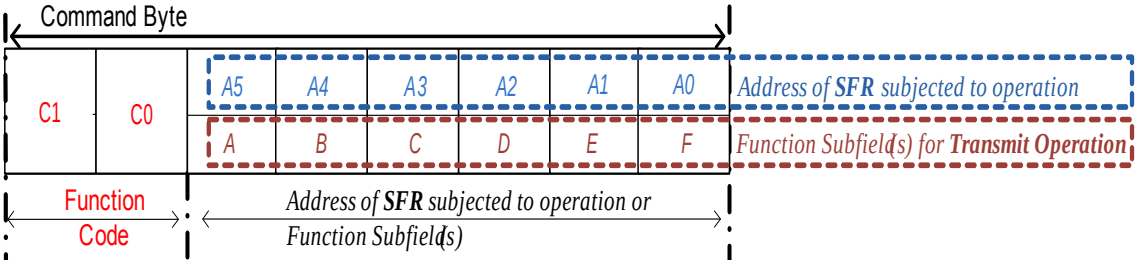

Figure 13 Command Byte structure

The first 2 bits **C1** and **C0** represent the Function Code field, which defines the command to be performed according to table below:

C1	C0	Function Code Configuration Bits
0	0	**Write** data into SFR register <A5:A0> field contains the SFR register's address There are 2 possible write modes (controlled by state of EN line): 1. write to a single address 2. burst mode write (with address auto increment)
0	1	**Read** data from SFR, <A5:A0> points to register address
1	0	**Reserved** (do not use)
1	1	**Transmit Command Byte** Bits <A5:A0>within this byte define the transmission parameters (see ***TDA5150 Datasheet*** for detailed description).

A special category of command is the *Transmit Command*, used for data transmission. It precedes the datagram to be transmitted. Its format is described below:

C1	C0	Transmit Command Configuration			
Function Code		**Bit**	Same bit position as *Address Bit n*	**Function**	**Value, description**
1	1	A	->*Addr5*	Data sync	0: off 1: on (at the same time Bit C - Encoding must be set also to 1 -->int. Encoding)
1	1	B	->*Addr4*	PA mode	0: PA off at the falling edge of EN (synchronized with bit-rate if bit A is high) 1: SDIO/DATA is latched at the falling edge of EN, PA stays on, TX data are kept constant. After the time-out of 65536 / f_{sys} which is ~5 ms for a 13 MHz crystal, PA and PLL are switched off.
1	1	C	->*Addr3*	Encoding	0: off 1: on (selects SFR register for encoding Bit A must be also set to1 -->Data sync)
1	1	D	->*Addr2*	Pwr. level/ ModSetting	0: selects PowerLevel/Modulation Setting1 1: selects Power Level/Modulation Setting2
1	1	<E,F>	->*Addr1..0*	Frequency selection	0 (A1 A0 ->00): selects frequency channel **A** 1 (A1 A0 ->01): selects frequency channel **B** 2 (A1 A0 ->10): selects frequency channel **C** 3 (A1 A0 ->11): selects frequency channel **D** (For detailed description of registers associated with frequency channels **A**..**D** see ***Chapter 2.4.11.3*** (Channel Hopping) in ***TDA5150 Datasheet***

Attention: ***1) Writing to address space beyond the valid SFR address range [0x04 - 0x27] may lead to system malfunction.***
2) After the last configuration bit for a new transmission was sent, a break of at least 100 µs must be provided (in order to achieve guaranteed PLL settling and lock). The only exceptions are hops with small frequency offset, as described in Chapter 2.4.11.3 of TDA5150 Datasheet.

An example of Write operation (having as target the SFR 0x04; TXCFG0) followed by a Read operation of the SPICHKSUM register (SFR 0x00) is shown in **Figure 14**.

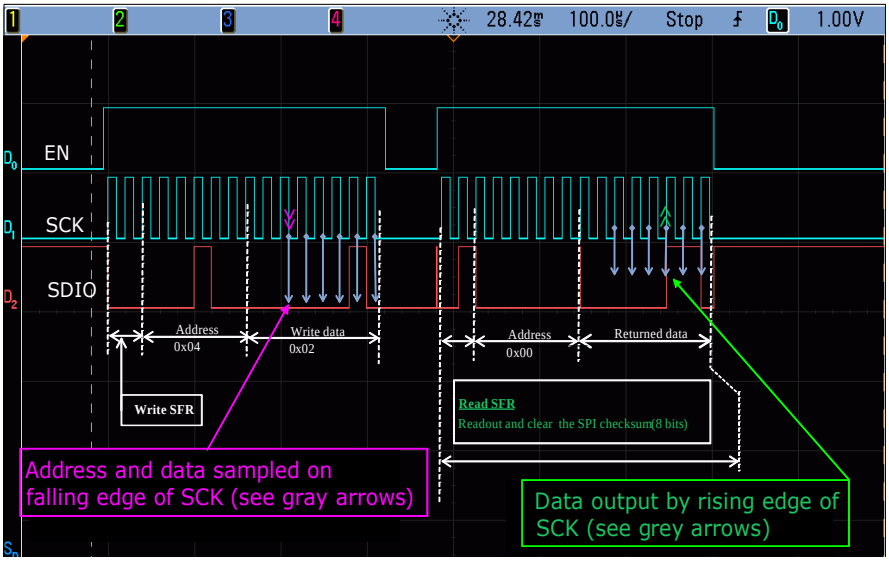

Figure 14 Example of register Write followed by Read operation

An example for Transmit Command is given in **Figure 15**.
It is worth to observe that the Transmit Command itself is clocked with significantly higher SPI clock frequency into the transmitter (transitions on SCK and SDIO lines) as the subsequent Data Clock frequency, used during the frame transmission (the data clock duration is 250 µsec in the given example, corresponding to 4kb/sec bitrate by data encoded according to Manchester coding scheme).

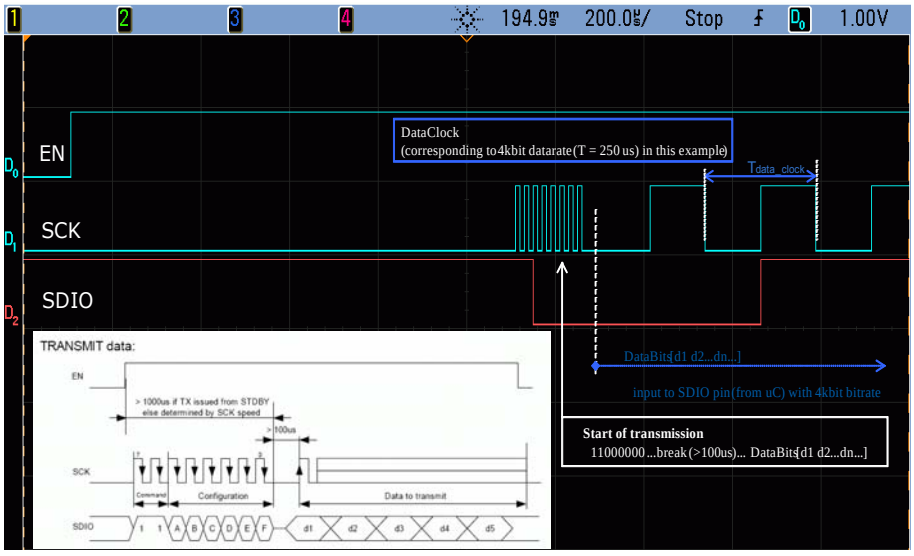

Figure 15 Transmit Command

An example for Transmit Command triggering a frame transmission is given in **Figure 16**.

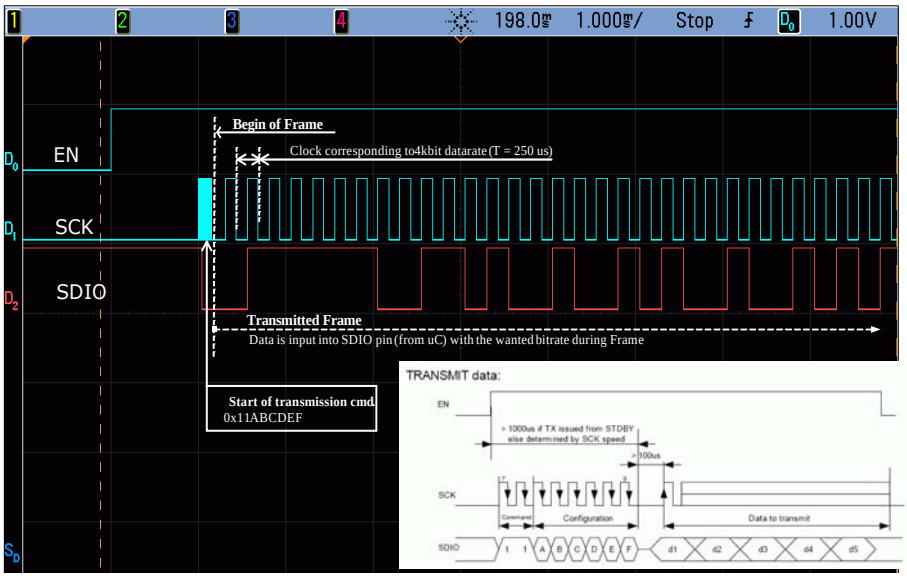

Figure 16 Front porch of a transmitted frame, including Transmit Command

5 TDA5150 programming example

As an example let us assume the following implementation: a transmitter operating in 315MHz band, on a single channel and using FSK modulation. In other words only one of the 4 available PLL channels of the TDA5150 transmitter will be used. The registers which are not used may be left in the post-reset state.

As mentioned in **Chapter 2** the first action is to define a list of registers which have to be programmed and their content. This can be easily achieved if the TESEUS tool is used, by simply exporting the register files of a given setup. However TESEUS exports always all the registers, thus the content is always correct for that setup, but the user must decide (analyze) which are the SFRs really required for a particular application. For details please consult the following documents: ***TDA5150_EvaluationKit_UserGuide*** and the ***TDA5150 Datasheet***.

As in above example just a limited set of registers will be used (see register map in **Figure 17**, required SFRs are marked blue, the others with gray) two possibilities may be considered:

- either individual write of the SFRs (in arbitrary sequence) or
- taking in account that there are two almost contiguous zones between the address spaces [0x04..0x0C] and [x019..0x27] burst write might be used, starting from the lowest addresses of the two zones. The advantage of burst write is that the address is transferred only once (during a write operation) for the register with lowest address and by the consecutive writes operations the SFR address is autoincremented.

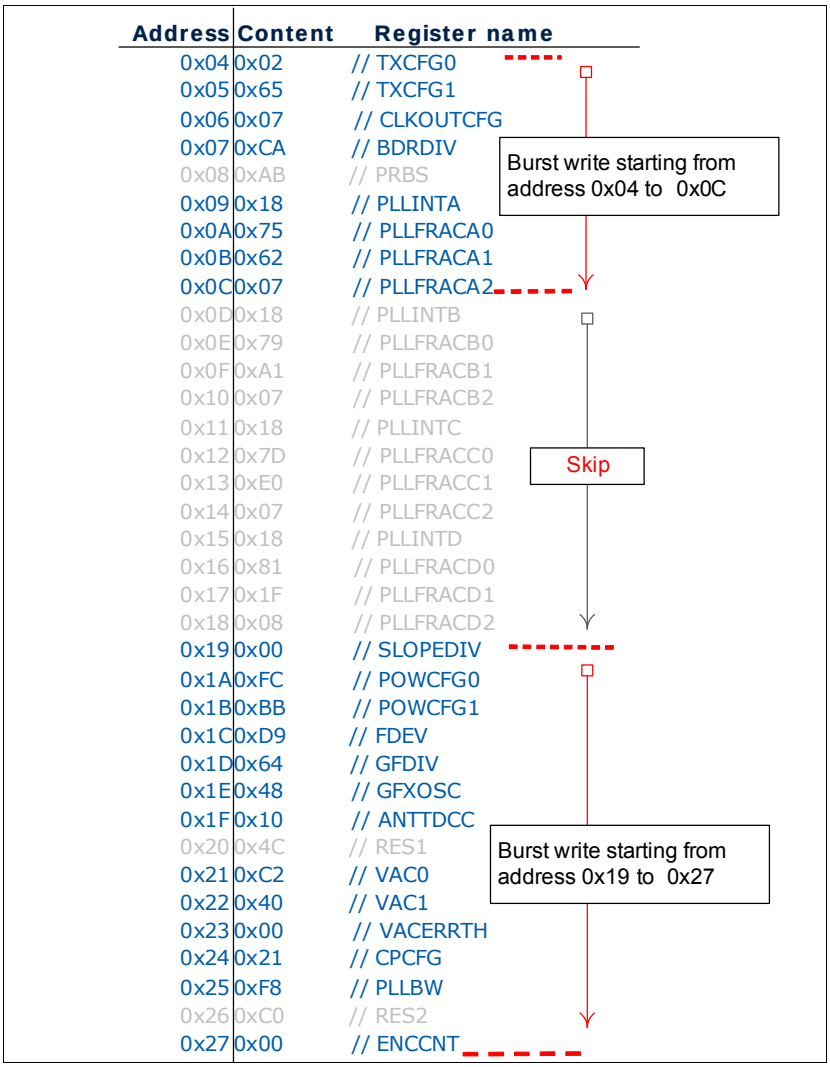

Figure 17 Map of registers used (example)

5.1 Individual SFR programming

Following description of individual register (SFR) programming is very close to the operation mode of TESEUS (the screenshots are taken during interaction of TESEUS tool with TDA5150). Some of the operations - like check of the SPI Checksum register are not mandatory and it is up to the system designer's decision if the checksum will be verified after each operation or not.

The first action is to read the Status Register (TXSTAT; SFR 0x01) to clear possible errors, which have been latched in this register. **Figure 18** is a screenshot of the read operation. As explained in **Chapter 4.1** the state of SCK line (high or low) during the leading edge of the SPI Enable signal (EN) determines which edge of the SCK clock will be used for Read and which for Write operation. For details see **Figure 9** and **Figure 10**.

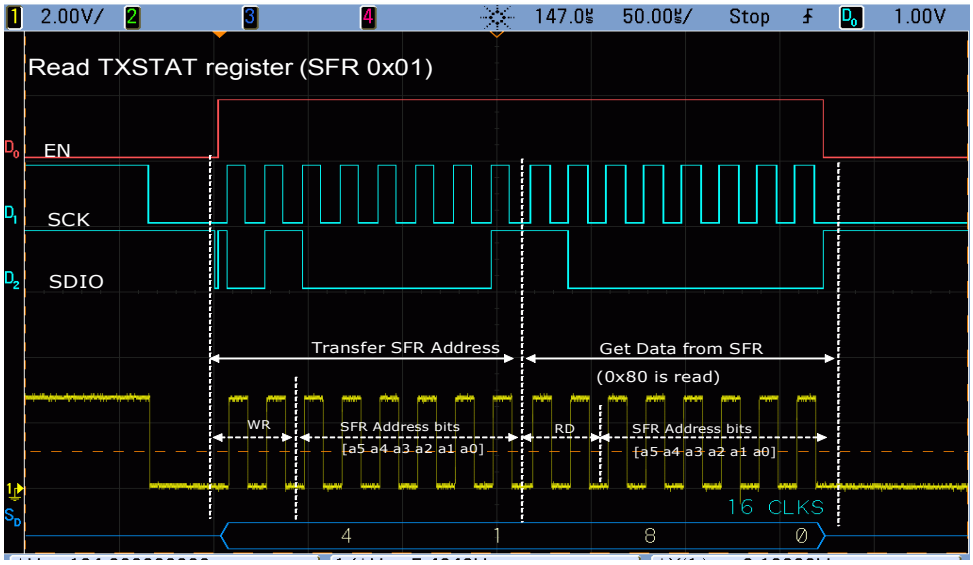

Figure 18 Read TXSTAT register

Having the content of Status Register (TXSTAT; SFR 0x01) acquired, the value can be analyzed and possible errors processed (by Host or µC). The next step in programming the TDA5150 transmitter is programming the SFRs, individually. In the screenshot below programming of the TXCFG0 register is shown, followed by read of the SPI checksum register.

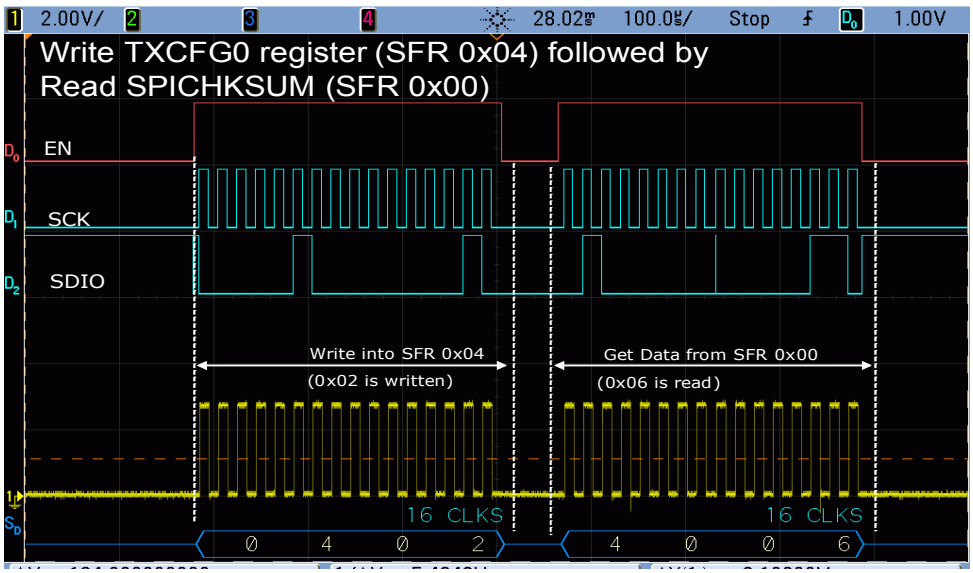

Figure 19 Write TXCFG0 register

The operation of writing one SFR after the other goes on until all the required SFRs are programmed. **Figure 20** is a screenshot of the write operation to TXCFG1 (SFR 0x05). Again the SPI checksum is verified after write operation.

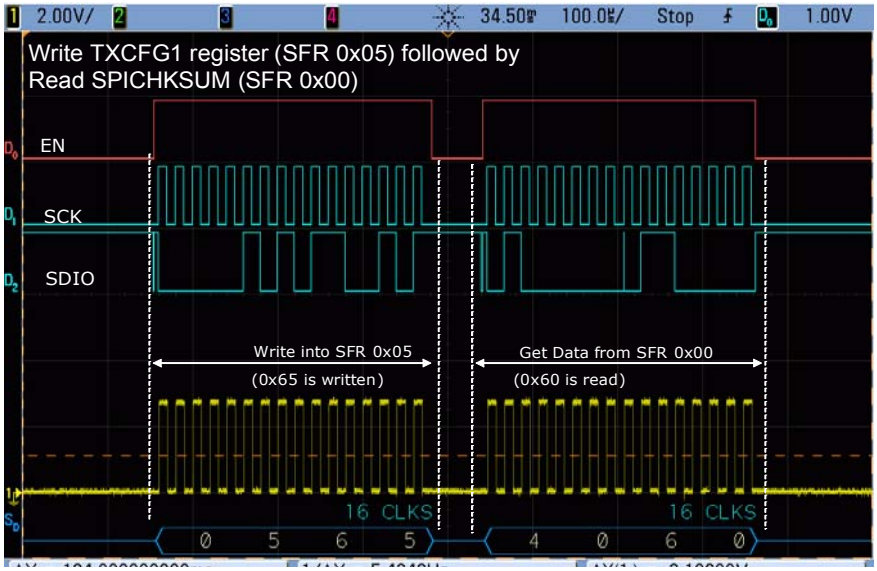

Figure 20 Write TXCFG1 register

After all the required SFRs have been programmed, the last step is to write the Transmit Data command and to output the data bits of the frame. The Transmit Data command is described in detail in **Chapter 4.3**.

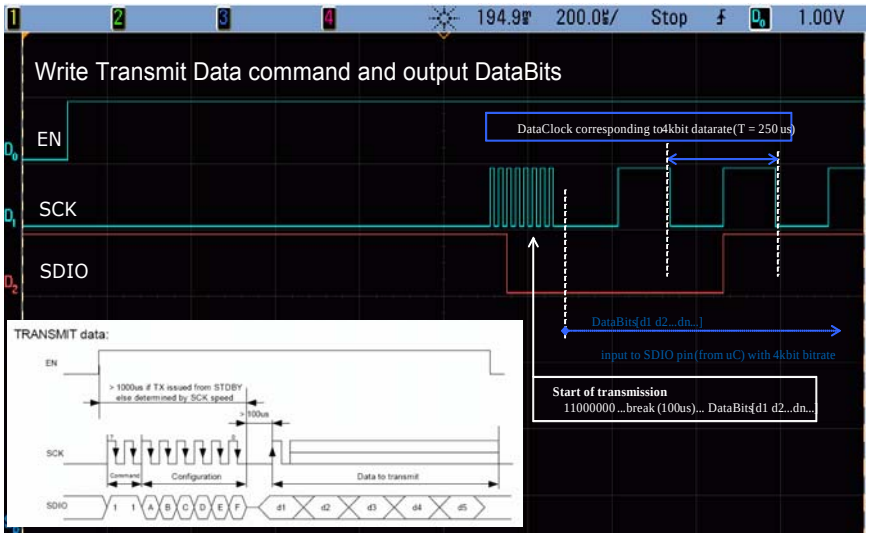

Figure 21 Write Transmit Data command and output the frame data

The transmission ends when:

- either an error condition occurs and the FailSafe mechanism forces the shutdown, or
- bit B of command byte was low and the Enable line (EN) is going low (a normal stop condition for SPI bus) or
- bit B of command byte is high, the transmitter continues to transmit according to latched SDIO state until the expiration of the time-out interval (2exp16 / f_{sys}) microseconds (if f_{sys} is given in MHz).

5.2 Burst Write mode

This mode is described in **Chapter 4.1** and the timing diagrams are shown by **Figure 11**. Advantage of BurstWrite mode is an increased transfer speed versus individual SFR write operations.

6 A valuable aid - the TESEUS software tool

TESEUS is part of the TDA5150 evaluation environment. The recent version can be downloaded free of charge from **www.infineon.com** . The package contains the firmware itself and a user manual.

In order to perform your evaluation task in conjunction with TESEUS, you will need:

- a TDA5150 SIB Board (version V1.2, acting as controller towards the TDA5150 transmitter)
- a USB cable for the interconnection between the SIB Board and the PC
- a TDA5150 Evaluation Board, assembled in accordance with the parameters listed in **Table 6** (frequency band and RF output power classes). This Evaluation Board can be plugged into the connector of a SIB board, but if the customer does wish so, it can be controlled by an external µC, via the SPI bus. In this case the proper supply voltage of 1,9..3,6V must be provided by an external power supply or from the µC-board (as the SIB-board is NOT plugged in, there is no supply voltage available from SIB-board in this case)
- a personal computer with at least one free USB port and one of the following operating systems (OS) installed: Windows 2000; Windows XP (32 bit or 64 bit); Windows Vista (32 or 64 bit); Windows 7 (32 or 64 bit)

The TDA5150 Evaluation Boards are deliverable in 5 different matching versions, each optimized in terms of output stage efficiency (RF-PA), for the ISM bands and nominal power classes listed below.

Additionally a ***SIB*** (System Interface Board) can be ordered, this last board is applicable for all ***Evaluation Boards***.

If a user requires Evaluation Boards for more ISM frequency bands - for instance for 315MHz and 915MHz, on cost saving reasons a single ***SIB*** may be ordered in conjunction with several ***Evaluation Boards***. However this solution (more Evaluation Boards and a single SIB) excludes the possibility of simultaneous work, with more Evaluation Boards at the same time.

Table 3 Deliverable Interface and Evaluation Board versions

ISM Band [MHz]	RF-Power [dBm]	ISAR Order Number
315	+5	SP000356305
434	+5	SP000356301
434	+10	SP000356304
868	+10	SP000356303
915	+10	SP000356302
SIB Board V1.2	x	SP000357842

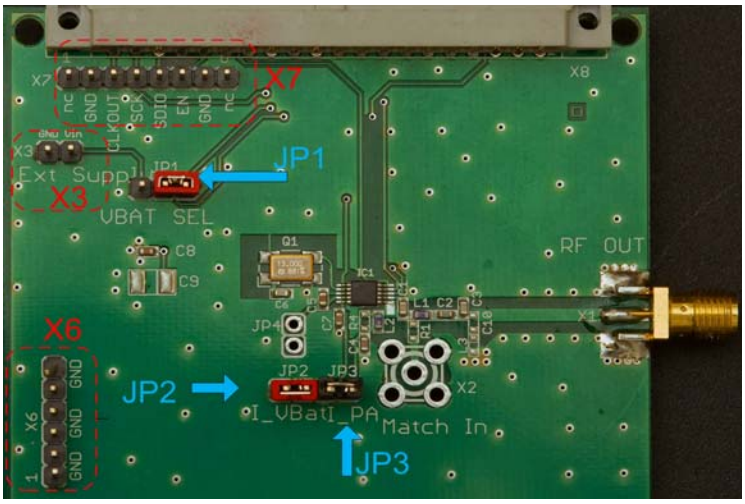

Figure 22 TDA5150 Evaluation Board (version V1.1; component side)

6.1 Hardware and Software Requirements

In order to work with TESEUS, the following hardware and software components are required

- PC with (at least) one of Microsoft's following OS installed:
  Windows 2000; Windows XP (32 bit or 64 bit); Windows Vista (32 or 64 bit) or Windows 7 (32 or 64 bit)
- One free USB port (for PC to SIB board connection)
- Recommended graphical screen resolution – 1024 by 768 pixels, or larger
- FTDI driver package for your installed Windows operating system.
  These drivers, required by SIB board (V1.2) are part of the TESEUS distribution package and are installed automatically during the installation of TESEUS tool

Attention: Please install TESEUS before plugging in the first time the SIB board to your PCs USB port (otherwise, after the Found New Hardware prompt you should be asked to localize the driver source files)

6.2 Working with TESEUS

Following part is a short description of user interface in TESEUS. For a complete description please refer to TDA5150_EvaluationKit_UserGuide_V1.0.pdf, a manual which is part of the downloadable TESEUS package.

6.2.1 GUI Description: Basic, Advanced and Firmware Mode configurations

TESEUS starts in a window which allows the user to choose from three possible Configuration GUIs

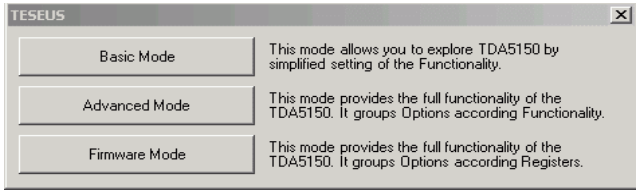

Figure 23 TESEUS startup GUI

These different GUIs visualize a choice of control tabs and settings, tailored to the user's needs. Namely these are:

- **Basic Configuration**: in this mode the user is asked to program just a minimum number of parameters. This configuration is recommended for getting aquintened with the device or for simple functional tests.
- **Advanced Configuration**: the user is offered a wider choice of programmable device registers (***SFR***s). Anyway TESEUS takes over the programming of some parameters in order to assist the user by setting the correct values and at the same time to reduce the probability of an erroneous configuration occurrence. This GUI is recommended for in-depth evaluation of the device.
- **Firmware Configuration**: within this GUI, the user is given access to all the parameters and SFRs, without any limitation imposed by the software. By providing a high degree of freedom, this GUI is recommended for users already familiarized with the device.

After one of the three ***Configuration GUI***s is selected, a new window opens, containing additional Tabs, like shown below.

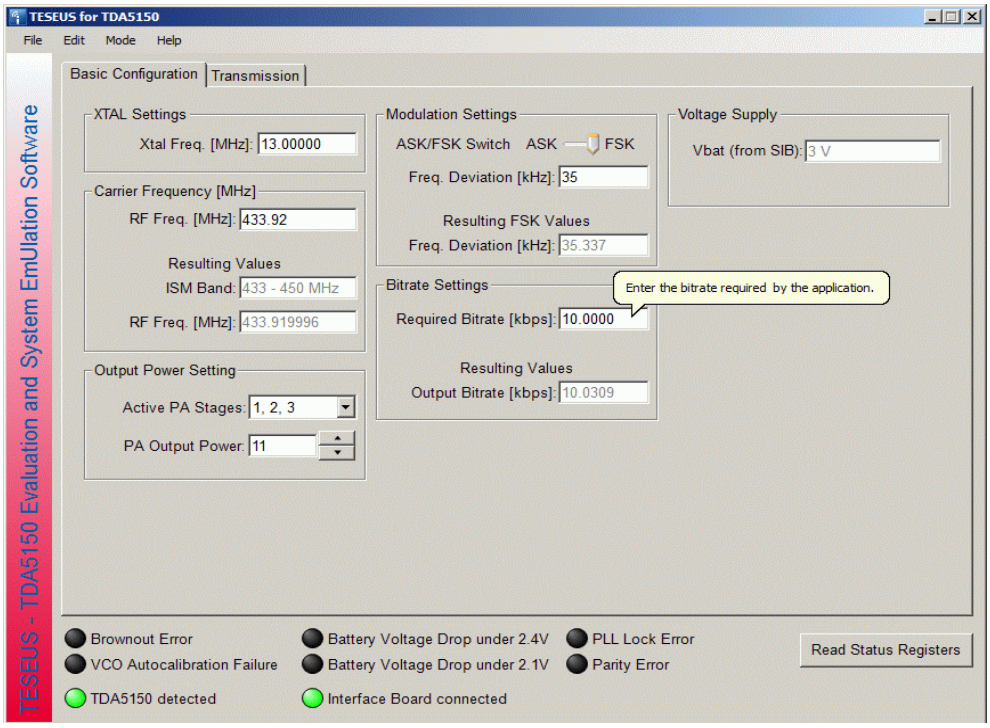

Figure 24 Basic Configuration GUI window

*Note: By un-checking the **Show Startup Selection Dialog** in the **Help** menu, the **Configuration GUI** window is disabled and TESEUS will start the next session with the last used GUI.*

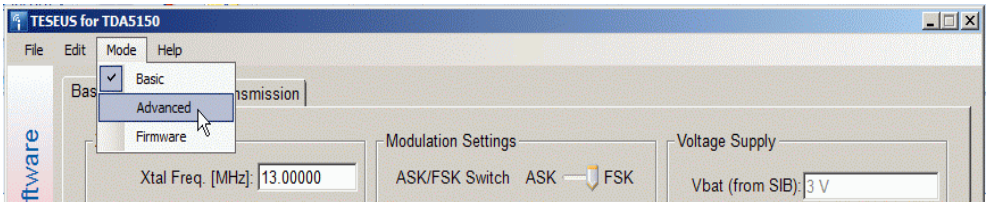

Figure 25 Switching between Configuration Modes

Each Configuration Mode allows the user to

- configure the registers
  (the number and function of user-accessible SFRs depends from the used Configuration Mode)
- configure the transmission mode (ASK; FSK; GFSK), RF-power and to transmit data but the degree of configuration flexibility and access to in-depth parameters is different

6.2.2 Configure the SFR registers

TESEUS assists the user by configuring the registers of the TDA5150 in an easy and comprehensive way. Each register is described by its tooltip descriptor which is visualized by passing the pointer of your mouse on the command. Please refer to the ***TDA5150 Datasheet*** for detailed explanation of the register functions and for the TDA5150 behavior. The mentioned registers are referenced as **SFR**s (**S**pecial **F**unction **R**egisters) in the ***TDA5150 Datasheet*** and ***Application Notes***.

By pressing <***F1***> when the pointer is hovering over special dialog boxes, an ***Explanation Note*** describing the particular function will pop up.

6.2.3 Transmission Modes

Using TESEUS can significantly shorten the design cycles by supporting the designer both in the evaluation process and the application development. This is achieved by the ability of transmitting both a continuous data stream for ***Device Evaluation*** purposes, or a signal modulated with a customer-specific datagram, as a normal application would do. This ability is referred within this document as ***System Emulation*** capability.

In this way, the Infineon TDA5150 Evaluation Kit comes closer to your final application.

Device Evaluation and ***System Emulation*** are options in the ***Transmission*** tabs of ***Basic Configuration***, ***Advanced Configuration*** and ***Firmware Configuration*** modes.

During programming the registers of the TDA5150 transmitter, via one of the three configuration modes (Basic; Advanced or Firmware), please check out the ***Transmission*** tab corresponding to the desired transmission mode (***Device Evaluation*** or ***System Emulation***)

*Note: In **Basic Mode** the appearance of the **Transmission** tab is slightly different from those in **Advanced Mode** and **Firmware Mode, as these offers a larger number of parameter choices and Data Frame configuration, some of these features are blanked out in Basic Mode.***

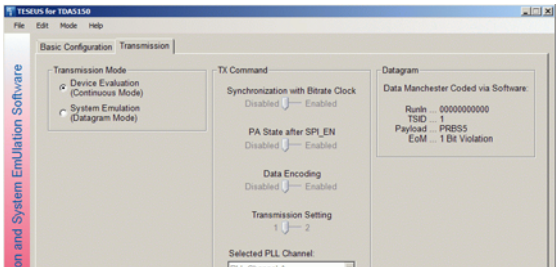

Figure 26 Device Evaluation and System Emulation options, as they appear in Basic Mode

6.2.3.1 Device Evaluation Mode

After selecting the ***Device Evaluation Mode***, a new transmission can be started by clicking the ***TX Start*** button. A continuous RF transmission is then generated according to the parameters downloaded into the ***SFR***s of the TDATDA5150. The modulated information is the datagram contained within *Transmission File* which has been selected in advance, iterated by an infinite loop. The transmission is interrupted (stopped) by clicking the ***TX Stop*** button or if editing any parameter in TESEUS is started. Thus inconsistencies (transmission of partially edited files) are avoided by forcing ***TX Stop*** during editing operations.

The effect of ***Device Emulation*** mode is the same for ***Basic***, ***Advanced*** and ***Firmware*** configuration GUIs. Contrary to ***Firmware*** and ***Advanced*** mode, in ***Basic*** mode a predefined datagram is used, and it is not possible to select a user-defined one.

6.2.3.2 System Emulation Mode

The ***System Evaluation*** mode allows you to program the device to transmit a datagram (i.e. a string of data) once or several times (by a programmable number of repetitions). According to the ***Basic Configuration*** vs. ***Advanced*** and ***Firmware*** configuration environments, a default message is sent instead of a fully definable one. The aim is to emulate via software the behavior of the TDA5150, as it would operate under the control of a generic microcontroller or an equivalent host.

The datagram is transmitted after clicking the ***TX Start*** button and ends when the datagram is completely transmitted or when the transmission is intentionally aborted by clicking the ***TX Stop*** button, whichever happens first.

6.2.4 Basic Mode

The ***Basic Mode*** GUI allows the programming of the device with a basic set of parameters. In this way the user can get accustomed with TESEUS and the TDA5150 architecture in a soft way, speeding-up the learning curve on the device. In this mode a significant part of the registers (***SFR***s) are blocked from editing as they are automatically programmed with default values.
Anyway some of the important ***SFR***s content is displayed -despite disabled editing, in order to make more comprehensive the behavior of the device in ***Basic Mode***. To use this mode, just start TESEUS and select ***Basic Mode*** from the ***Startup Selection Dialog*** window.

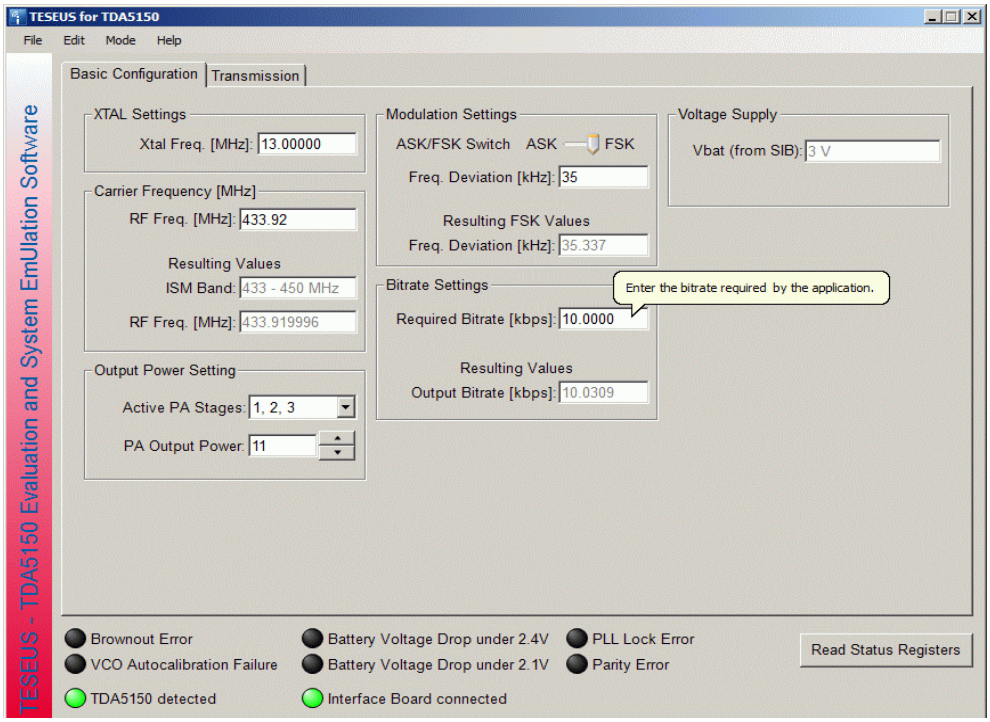

Figure 27 Basic Mode configuration

In the ***Basic Configuration*** tab, the editable parameters are grouped as

- ***XTAL Settings*** -this field contains the crystal frequency value, expressed in MHz. This must be in accordance with the crystal frequency on the used hardware (board). The TDA5150 EvalBoard provided by Infineon contains a crystal with nominal 13.00 MHz value. Anyway it is recommended to check the reference oscillator frequency and make fine adjustments (usually in magnitude below 1 kHz) if the unmodulated carrier (CW) frequency is offset from nominal RF channel value. This alignments can be done at best in ASK mode, as there is an equivocal carrier frequency, but also FSK (or GFSK) modulation may be used, with a symmetrical pattern (for instance 1010...10...) and then center the amplitude dip (i.e. the dip between the two FSK peaks, left and right from carrier on the frequency axis) on the nominal RF channel frequency by means of fine adjustments on the *XTAL Freq* value in the corresponding TESEUS tab. The alignments operation assumes access to a calibrated Frequency Counter or a Spectrum Analyzer, but with a slight trade off a frequency calibrated receiver may be used as well - then tune for best bit- or message error rate, by low RF signal levels. This assumes again an RF attenuator or a receiver placed almost to link range limit (far away from transmitter).
- ***Carrier Frequency*** - this field contains the RF frequency field value of the channel used. The ISM band field is automatically updated accordingly. It is recommended to select one or more channels within the ISM band for which your Evaluation Board is matched, otherwise a significant drop of the RF power might occur (as the RF-PA output would be severely mismatched). The ISM frequency band and nominal RF output power for which the board has been optimized are contained on a small sticker on the top side of the delivered Evaluation Boards.

- ***Output Power Settings*** - the RF output power of the device may be controlled by this parameter. Select the desired output power according to your Evaluation Board matching. To achieve the best PA efficiency and consequently low current consumption, make sure to configure the RF PA array for
  – 9 stages if + 5 dBm output power is required
  – 10 stages if +8 dBm output power is required
  – 11 stages if +10 dBm output power is required

Note: The output power is determined not only by the number of active PA stages of the TDA5150 but it is also influenced by the load impedance of the RF power amplifier. Thus it is recommended to set the PA parameters (number of active stages) in accordance with the impedance (and nominal power) of the evaluation board under test to yield a minima of current consumption and maxima of efficiency.

- ***Modulation Settings***: the possible modulation schemes are ASK and FSK. If FSK is chosen, the Frequency Deviation value has to be programmed as well (otherwise, with a default value of 0 Hz there should be no distinguishable RF carrier modulation)

6.2.4.1 Transmission in Basic Mode

In the ***Transmission*** Tab of the ***Basic Configuration***, both the ***Device Evaluation*** and ***System Emulation*** can be selected. With this GUI, the ***System Emulation Mode*** datagram is fixed and can not be redefined by user.

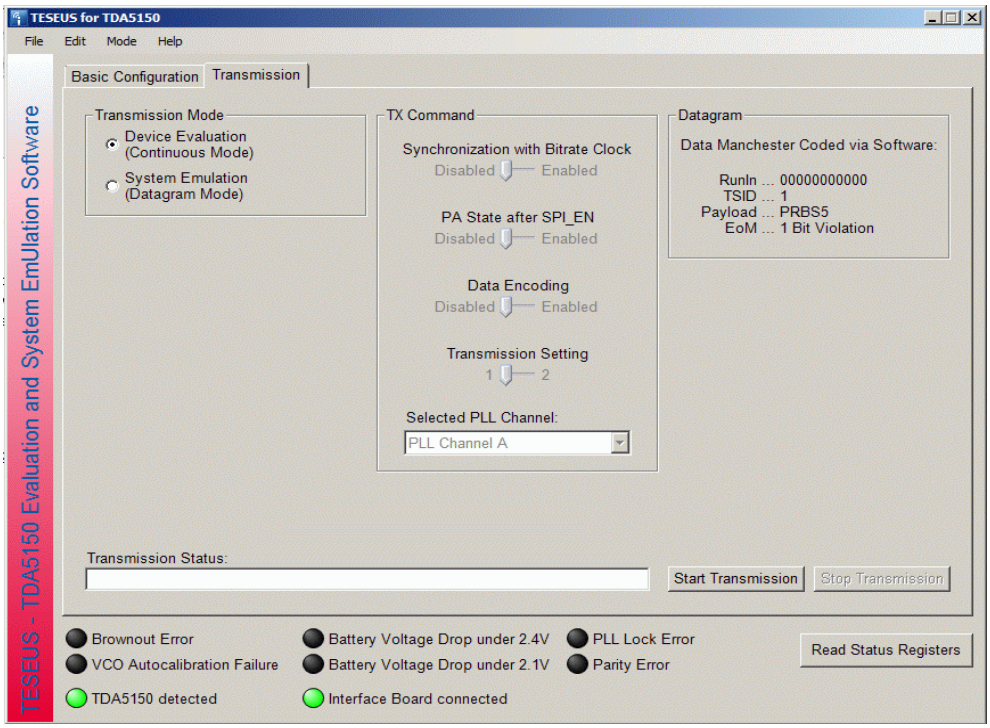

Figure 28 Transmission controls in Basic Mode

The default datagram is defined as following:

- Encoding: Manchester
- RunIn: 11 Bits of '0'
- TSID: 1 Bit of '1'
- PayLoad: PRBS5 (31 Bit)
- EoM: 1 Bit 'M', Manchester violation

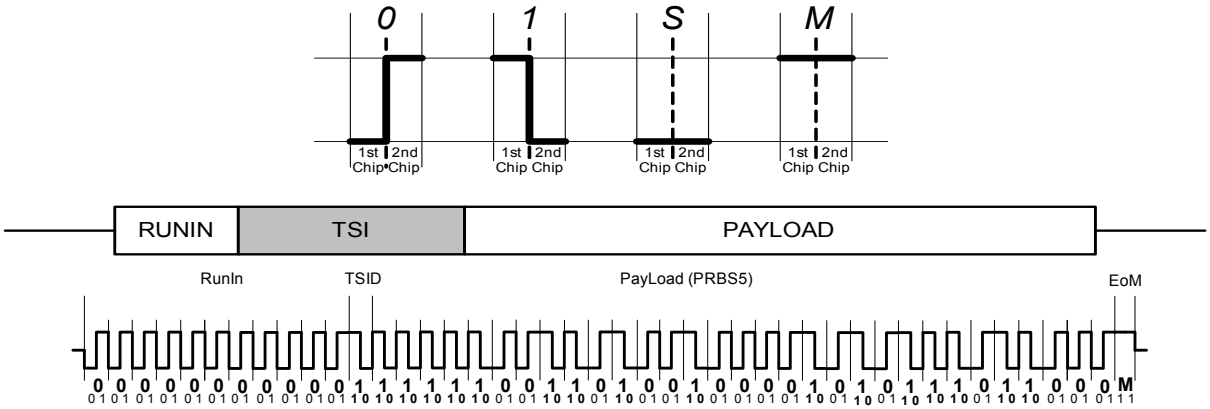

Figure 29 Default datagram structure, Basic Mode

The ***TX Command Byte*** is set by default according to the following description:

- Syncro with Bitrate disabled
- RF-PA off (disabled)
- Data Encoding disabled
- Transmission Setting 1
- Transmission Channel A

6.2.5 Advanced Mode

This GUI allows in this mode programming all the registers of the TDA5150. The user will be guided through the device´s setting. The registers are grouped in tabs according to functional building blocks and functions. Invalid data will be recognized by automatic controls and proof within the dialog boxes (for instance check of not allowed transmit frequencies).

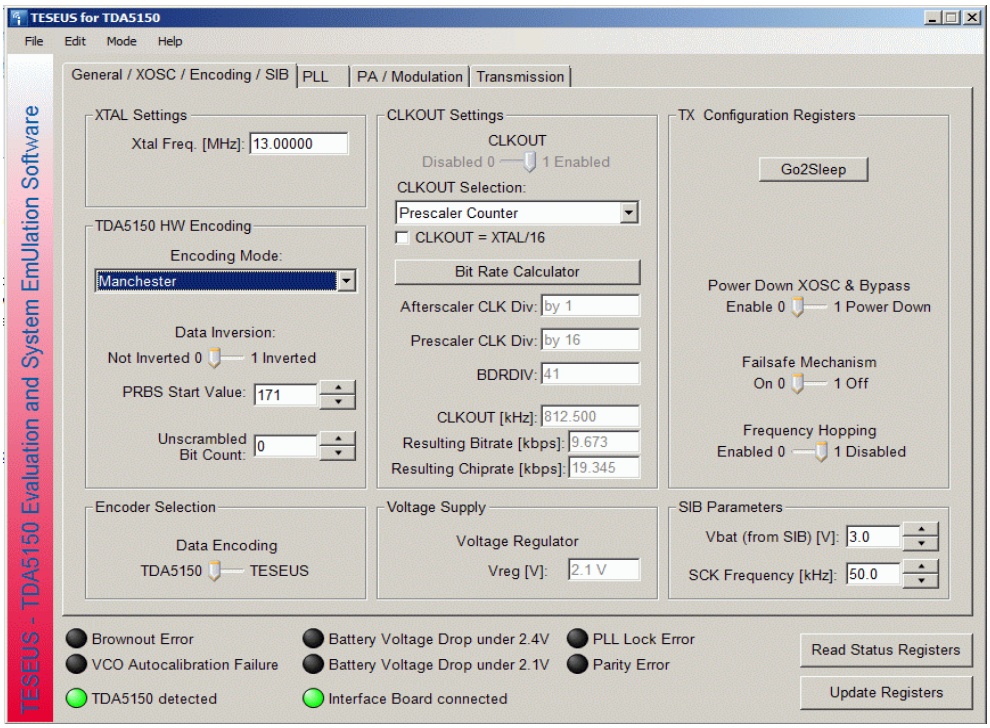

Figure 30 Advanced Mode: configuration tabs

For detailed description of registers and settings, please refer to the ***TDA5150 Datasheet*** and particularly to the ***SFR*** descriptions. The TESEUS Tooltips embeds and synthesizes this information within the software (refer to the ***Help menu***).

Note: The majority of the registers have a suggested (default) value. These values are set according to typical implementations and environmental usage, but may be edited and changed.

6.2.5.1 Advanced Mode configuration

One of the first inputs required to run the system is the nominal frequency of the crystal oscillator.

Remember that the TDA5150 Evaluation Board provided by Infineon Technologies contains a crystal resonating nominally at 13,00 MHz. It is possible to check the nominal frequency by reading the value on the case of the crystal (values are given usually in kHz by most of manufacturers, i.e. *13.000* is the reading of the crystals mounted on the Evaluation Boards).

Hint: Please follow these instructions, for easy measurement of actual crystal frequency

- Enter the nominal crystal frequency into the ***XTAL Settings*** field
- Program the device with the wanted nominal center frequency (***f_c***)
- Keep in mind that the nominal carrier frequency (***f_c***) is

$$fc = r \times fosc$$

where ***r*** is the fractional divider value programmed in the TDA5150 (***Divider*** window, as shown in **Figure 31**)

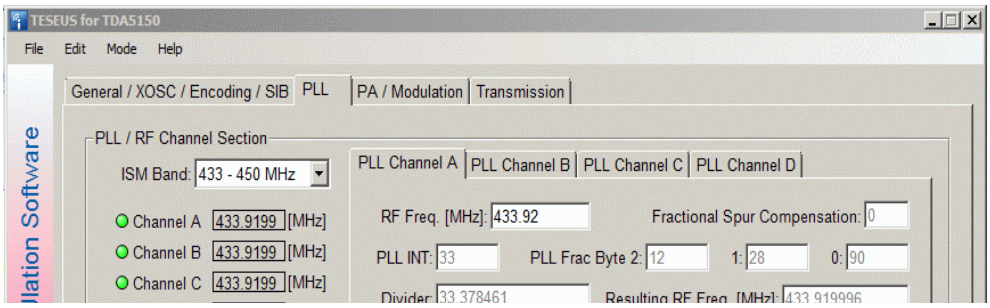

Figure 31 Channel frequency configuration in Advanced Mode

- Start a transmission in continuous mode (CW), choose FSK modulation with 0 Hz frequency deviation, and measure the actual carrier frequency with a spectrum analyzer or frequency counter. Using the value ***r*** it turns out that the actual crystal oscillator frequency is

$$\overline{fosc} = fc \div r$$

- Enter the new XTAL settings value in the corresponding TESEUS box and check again if the ***f_c*** carrier is centered exactly (or at least within the desired frequency accuracy window) relative to the nominal channel frequency.

In order to easily program the TDA5150, it is recommended to enable the ***Tooltip*** option.

Move the cursor and by pressing <***F1***> when the cursor is hovering over some specific fields, a related document will pop up. This explains in details the way the device or the particular function works, and delivers useful hints.

6.2.5.2 Transmission in Advanced Mode

In the ***Transmission Tab*** of the ***Advanced Configuration*** mode, both options ***Device Evaluation*** and ***System Emulation*** are available.

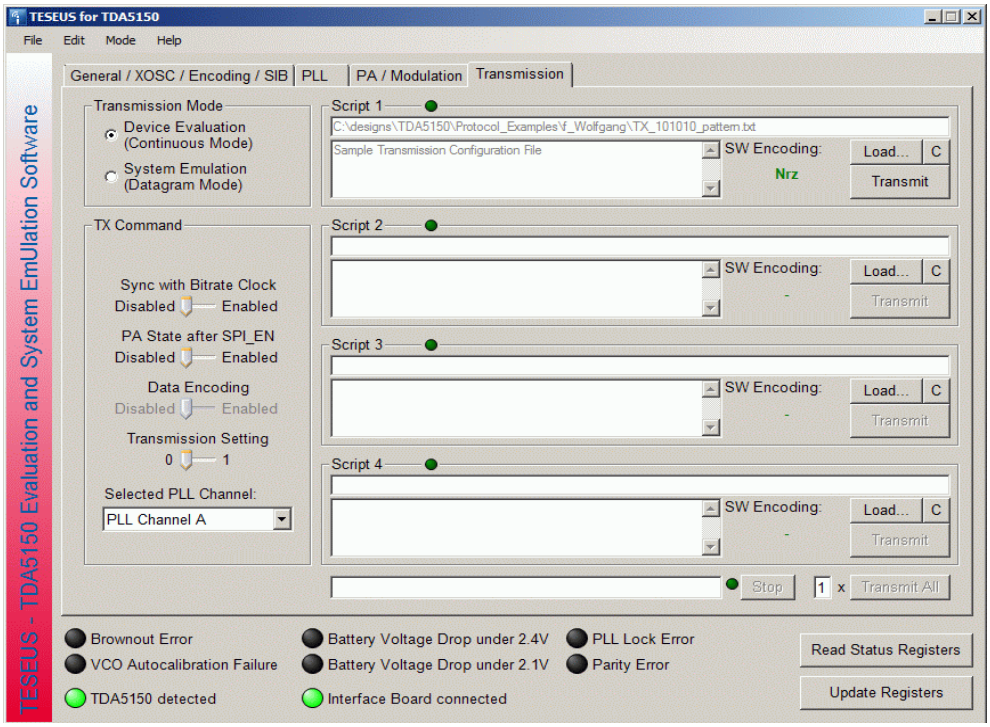

Figure 32 Advanced Mode - Transmission Tab and controls

Opposed to ***Basic Configuration*** Mode, the ***Transmission Command*** byte as well as the datagram must be defined by the user. The *TX File*, whose template can be found under the ***File*** menu, defines the structure and the content of the datagram.

- In ***Device Evaluation*** mode (Continuous Transmit Mode), the ***Transmission Command*** byte must be defined within the GUI. The transmitted data is extracted from the *TX File*
- In ***System Emulation*** mode both ***Transmission Command*** byte and *Datagram* must be defined within the Datagram file. TESEUS allows the usage of up to 4 datagram files at the same time, as shown **Figure 32**.

For explanations regarding the ***Transmission Command*** byte, please refer to the ***TDA5150 Datasheet***. To start a transmission, click on the ***Load*** button, which loads a *TX File*. A template can be found in the ***File*** menu. If the user does wish to clear the uploaded file, just press the button ***´C´***, followed by a click on the ***Transmit*** button.

To stop the transmission, click the ***Stop*** button, located at bottom right region.

In the same Tab up to 4 different TX Files can be processed within individual TX boxes (Datagram 1..4).

The datagram file can be created ad-hoc in order to meet the format required by your application. Open the file with a text editor (Notepad for instance). The TX File contains a self explicative description regarding its structure and organization.

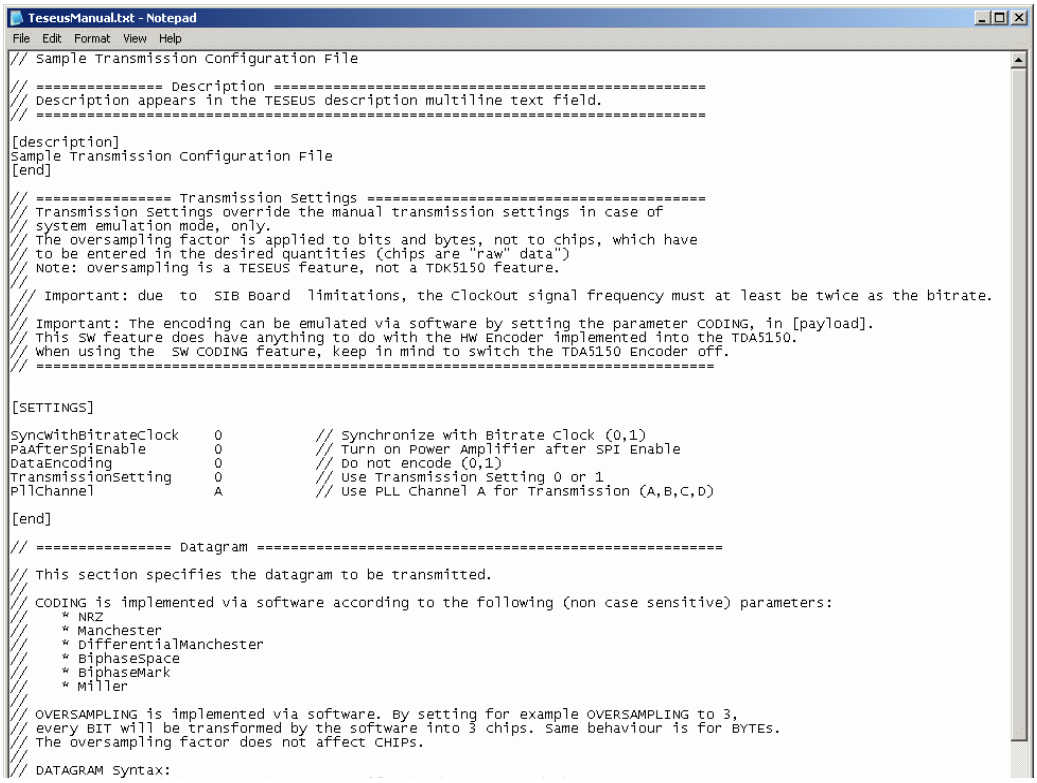

Figure 33 TX File structure

The transmission file is composed by three main fields

- description
- settings
- datagram

The **description** field contains the description you want to visualize within the datagram window in TESEUS. This feature can be used to easily visualize the description of the transmission and to distinguish it from other, alternative files.

The **settings** field defines the Transmission Command byte. Please refer to the ***TDA5150 Datasheet*** for detailed explanations.

The **datagram** field is composed of two commands OVERSAMPLING and CODING, followed by the datagram payload content, which should be transmitted.

OVERSAMPLING is used to oversample the data that is passed to the TDA5150.

By setting for example OVERSAMPLING to 5, every BIT will be transformed by the software into 5 chips. Same behavior is true for BYTEs.

For example, if the data rate is set to 1kbps and OVERSAMPLING is 5, the data passed to the TDA5150 will be 5 kchips per second.

That is, for every data-bit the device will receive and transmit 5 chips at a rate 5 times higher than the nominal data rate. This option can be useful for example during a ASK transmission for instance, if the protocol requires a moment of silence of 1.2 bits time length between two consecutive parts of the transmission, oversampling by 5 allows to transmit for the 0.2 chip long duration a space (break).

CODING is used to encode via SW the data which is then passed to the TDA5150.

The following parameters (non case sensitive) are implemented:

- NRZ
- Manchester

- Differential Manchester
- Biphase Space
- Biphase Mark
- Miller

Coding is accomplished by TESEUS and the datastream transferred to the SIB board afterwards. The data to be transmitted is specified by *Data Type* descriptors, as follows

- "BIT" ..... Bits, will be encoded. Data is contained in "01001" - like sequences. Spaces inserted in the string, for better overview and to structure the data are allowed.
- "CHIP" ..... Chips, usable for example for Manchester Code Violation patterns. Data is contained in "01001" - like sequences. Spaces in the string to structure the data are allowed.
- "BYTE" ..... Byte Data, will be converted to Bits (MSB transmitted first). Data is declared bytewise or string like, according to following styles
  - 0x0F ....Hexadecimal byte (C-style)
  - &H3A ..... Hexadecimal byte (VB.net style)
  - 127 ....Decimal Byte
  - 'B' ....Single ASCII Character
  - 'test' ....ASCII Character String

After defining the datagram, save the *TX File* into a work folder, load it according to previous instructions, and then click on the ***Transmit*** button.

6.2.6 Firmware Mode

This GUI, similar in functionality to the ***Advanced Configuration***, allows to accessing and programming all the registers (***SFR***s) of the TDA5150. The main difference versus the ***Advanced*** GUI is the graphical interface and a reduced set of restrictions by setting of the parameters. It is therefore recommended to use this GUI after all the device´s parameters and behavior is understood.

The sequence of the commands and programming parameters follows the actual order of the registers (hexadecimal addresses in incrementing order) rather than any other logical organization. The tabs are named in accordance with the TDA5150 ***SFR*** address regions and commands are grouped alike.

Some optional controls, like a PLL frequency calculator, a VAC calculator and a frequency deviation calculator are available for advanced users.

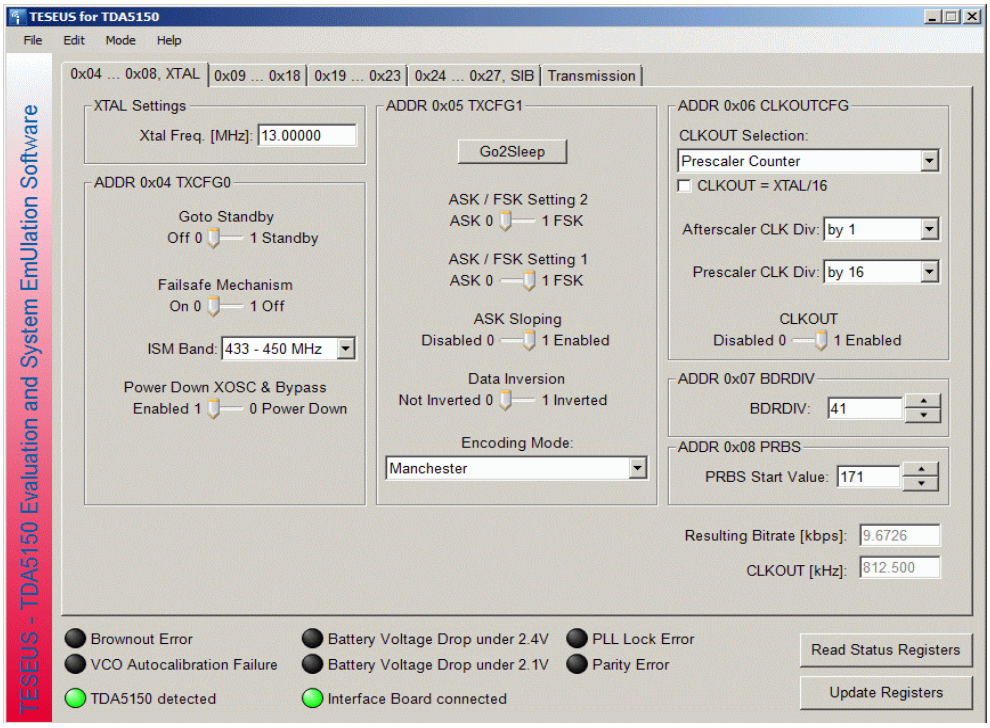

Figure 34 Firmware Mode - SFR tabs

The transmission tab reflects the same structure used in the ***Advanced Mode***.
Please refer to **"Transmission in Advanced Mode" on Page 32** for further details.

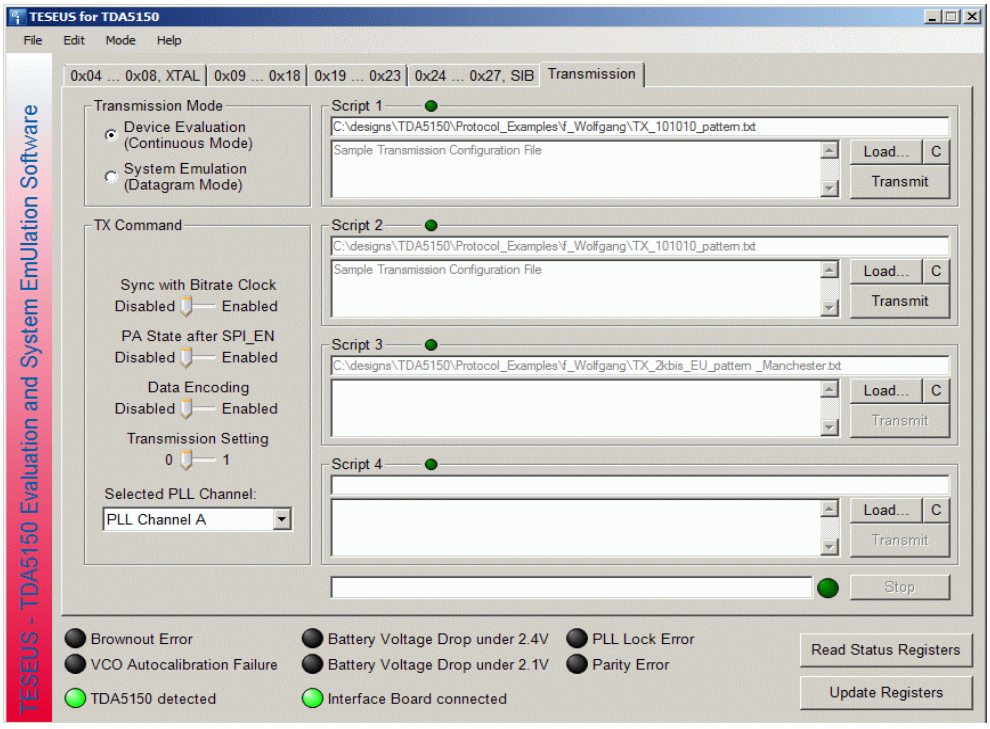

Figure 35 Firmware Mode - Transmission tab

7 Debugging

7.1 Some words about debug techniques

Below are listed some hints for debug action and efficient code debugging sequence. If the code (executed by µC) malfunctions or the transmitter does not work as expected, after it was programmed (by Host) at first try to identify and understand the root cause.

Frequent reasons are:

- inconsistent code
- lack (some “gaps”) in understanding and/ or interpretation of transmitter SFRs function

The µC code itself can be quickly debugged if established (and well-known) procedures are used. Debugging usually begins by setting breakpoint(s) and allocation of trace files to code segments (tracking of I/O pin state changes and register values). This is more efficient and less time consuming as “crash and relaunch” trials.

For a better understanding of the TDA5150 transmitter structure (at least at block diagrams level) and control functions, please refer to register (SFR) definition and usage, as described in recent ***TDA5150 Datasheet***.
The map of Special Function Registers is listed in **Appendix**, by **Table 4**.

If systematic code malfunction occurs, an efficient method, especially for those familiar with hardware debugging methods is to “watch” the SPI-bus and backtrace the transferred data.

This procedure is especially useful if there are doubts about data integrity, i.e. there are suspicions that glitches (usually due to crosstalk in the host system -but long enough to be interpreted as transitions by the SPI interface) have falsely triggered the system and by investigation of potential timing problems.

Figure 36 below is an example for glitch-free transfer, and **Figure 37** shows a trace with glitches due to Host activity, but the glitches do not interfere with the normal system functionality, as none of the SCK edges responsible for data transfer falls on critical points.

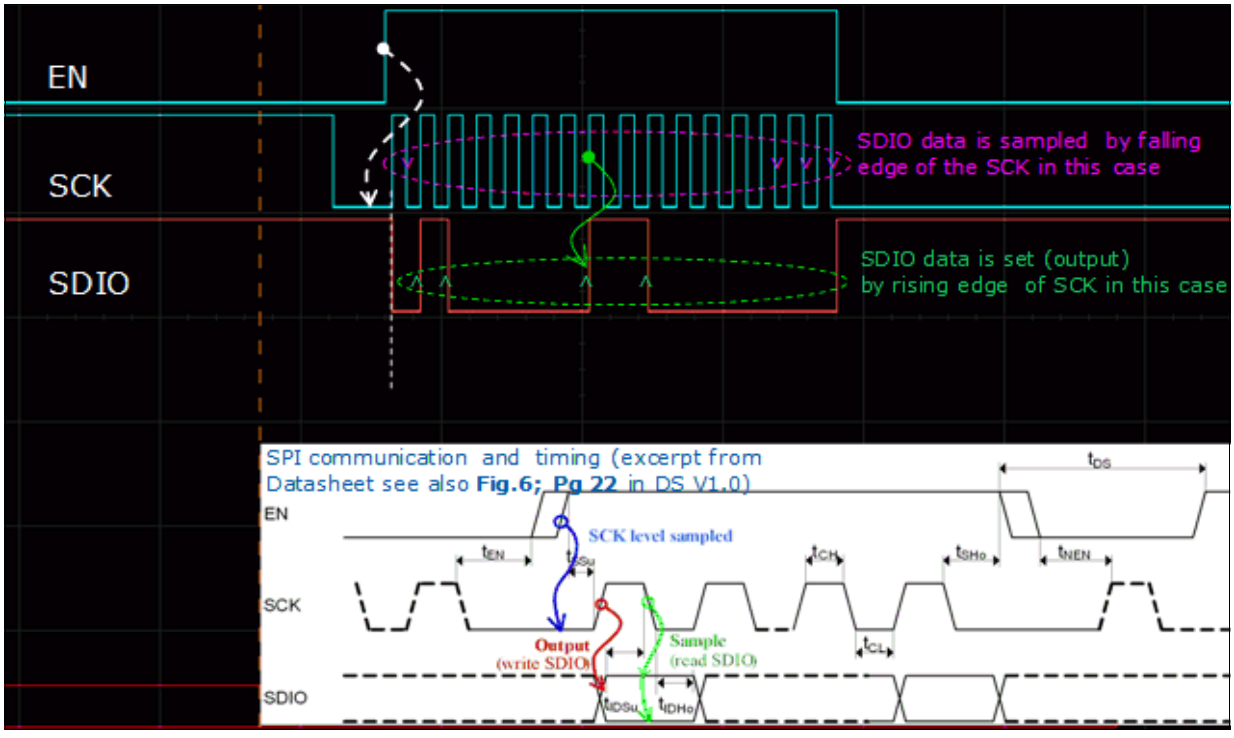

Figure 36 Example for the analysis of SPI communication protocol

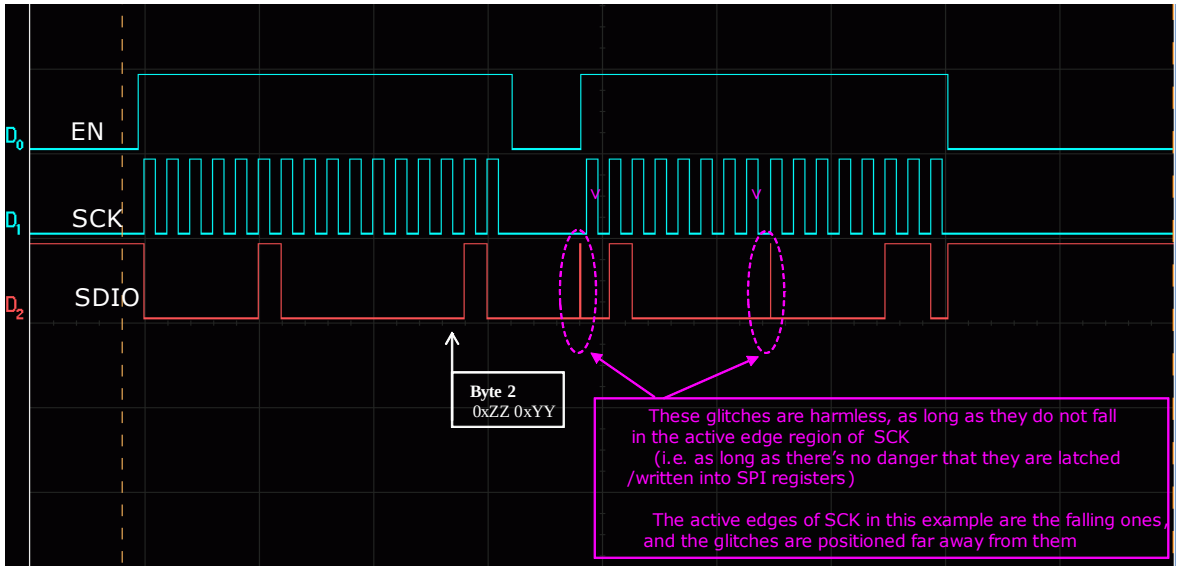

Figure 37 Glitches which cause no harm on SPI bus

An efficient tool - at least at the beginning of application development and of quick bugfixes for users having access to a TDA5150 Evaluation Kit (SIB Board V1.2 and TDA5150 Evaluation Board V1.2) is to split up the SPI control lines between Host and the TDA5150 transmitter on the module being debugged and hook up the SIB board. The SIB is acting as an ad-hoc controller. This might be not a perfect solution from signal integrity viewpoint (crosstalk and noise injection are potential risk factors) but for testing new setups and their effects works well and with low effort. The transmitter is entirely under control of the TESEUS application, thus a proven and reliable tool may be used for debugging and test. In **Figure 37** the docking points of the TDA5150 SIB Board V1.2 are shown (and accessed through the unpowered Evaluation Board) which allow access to the SPI bus and on-board, programmable supply voltage of the SIB board, acting as a Host controller.

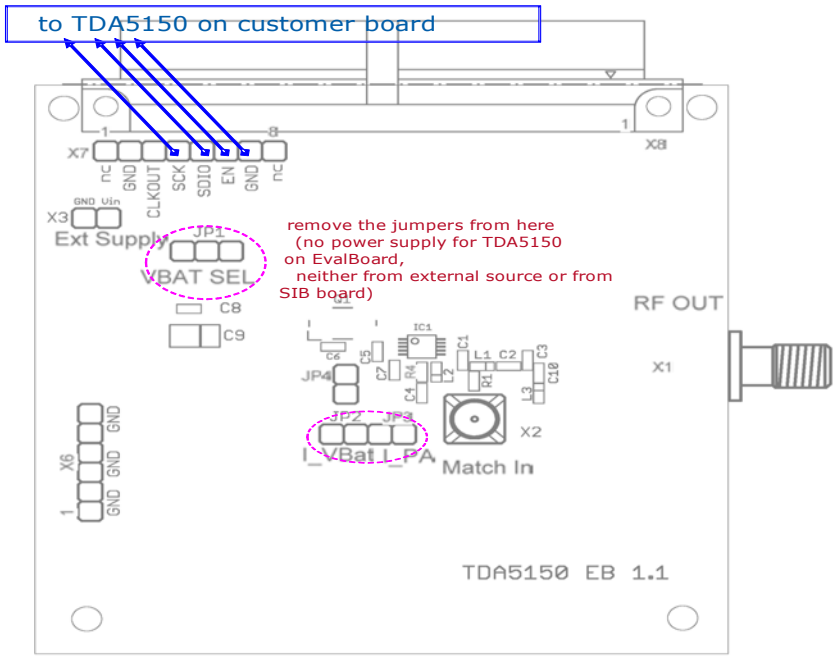

Figure 38 Docking points on TDA5150 Evaluation Board

7.2 A special case - the Brownout Reset

The brownout behavior is explained in detail in the ***TDA5150 Datasheet***, chapters ***1.5.6*** and ***2.4.10***.

The following part describes the behavior of the TDA5150 during reset and a special case of slowly rising supply voltage. Knowledge about brownout reset behavior is of importance, especially if external devices are clocked over the programmable clock output of the TDA5150 transmitter.

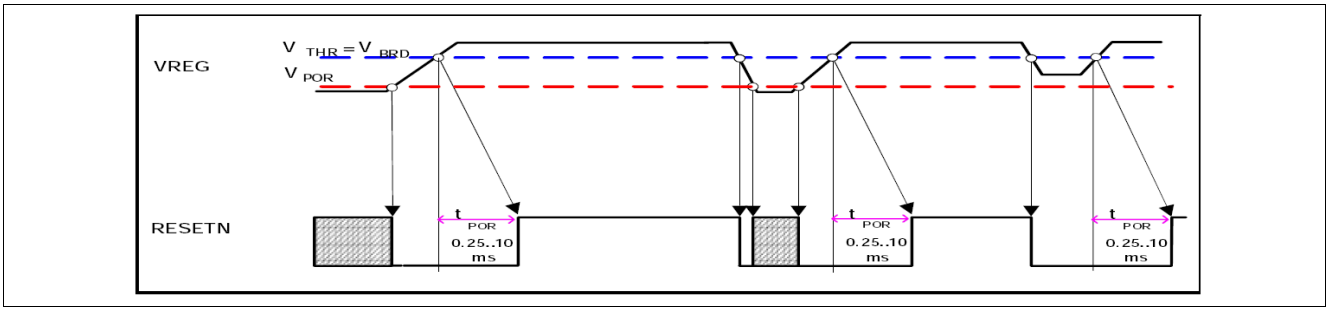

Figure 39 Brownout detector trigger points

A screenshot depicting the startup phase of the crystal oscillator and subdivided reference clock output is shown in **Figure 39**. A low supply voltage of around 0,5V, well below the guaranteed minima of operating voltage (1,9V) is applied and slowly increased.

- at point **A** (on time axis) the reference oscillator starts to swing and the CLKOUT pin delivers pulses but the chip is in a not guaranteed operating region (supply around 1,3V in point A, below 1,9V, the datasheet minima)
- at point **B** there is a “hop” in reference oscillator frequency, it locks on the crystal’s frequency of 13 MHz
- at point **C** the internal logic senses a “signal good” condition of the reference oscillator signal and at the same time forces an internal reset of 2exp12 reference oscillator periods. Notice that in point **B** the supply voltage reached the minimum guaranteed operating value (of 1,9V).
  After the reset countdown is elapsed (point **D**) the device enters normal operation mode. As the SDIO line was low when EN gone high in this example, the output clock chosen was XTAL/16 by default.
  If SDIO would have been low when EN gone high, the output clock would be selected as imposed by settings of SFR CLKOUTCFG (0x06). This is the configuration register for Clock pre- and afterscaler.
  Detailed description about configuration is given in ***Chapter 2.4.5.3*** of ***TDA5150 Datasheet***

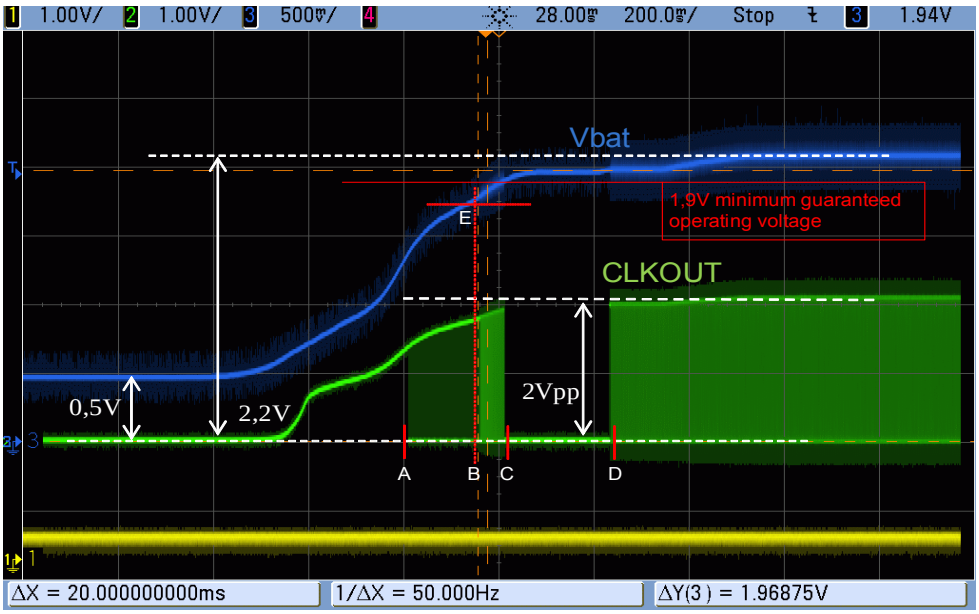

Figure 40 Clock output during a brownout reset

As an aid and to ease up the debug of timing problems **Figure 41** summarizes the bus operation timing and the direction of data flow. This is the same information as found in **Chapter 4.1** but in a condensed form.

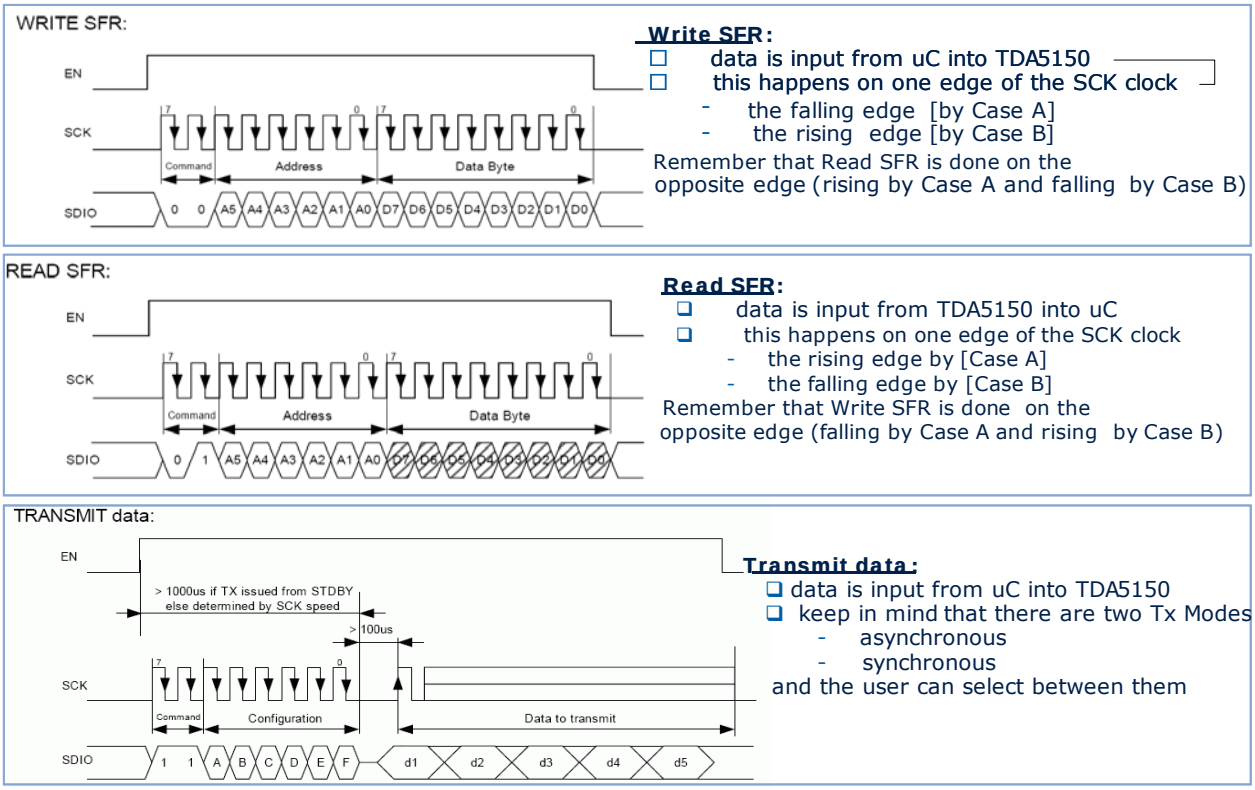

Figure 41 Overview timing diagrams, SPI bus

8 Appendix

Below is a short overview of the Special Function Register bank (SFRs) accessible to users in the TDA5150 transmitter. For a detailed functional description, settings, parameter calculation formulae and after reset state please refer to the ***TDA5150 Datasheet***.

Table 4 Special Function Registers overview

Register	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPICHKSM	0x00	SPICHKSM	SPICHKSM	SPICHKSM	SPICHKSM	SPICHKSM	SPICHKSM	SPICHKSM	SPICHKSM
TXSTAT	0x01	1	n.u.	LBD_2V1	LBD_2V4	VAC_FAIL	BROUTERR	PARERR	PLLLDERR
TXCFG0	0x04	GO2STDBY	reserved	reserved	FSOFF	ISMB	ISMB	reserved	reserved
TXCFG1	0x05	GO2SLEEP	ASKFSK2	ASKFSK1	ASKSLOPE	INVERT	ENCMODE	ENCMODE	ENCMODE
CLKOUTCG	0x06	CLKSRC	CLKSRC	AFTERSCLE	AFTERSCLE	PRESCALE	PRESCALE	PRESCALE	CLKOUTEA
BDRDIV	0x07	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV	BDRDIV
PRBS	0x08	PRBS	PRBS	PRBS	PRBS	PRBS	PRBS	PRBS	PRBS
PLLINTA	0x09	n.u.	PLLINTA	PLLINTA	PLLINTA	PLLINTA	PLLINTA	PLLINTA	PLLINTA
PLLFRACA0	0x0A	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0	PLLFRACA0
PLLFRACA1	0x0B	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1	PLLFRACA1
PLLFRACA2	0x0C	n.u.	n.u.	reserved	PLLFRACA2	PLLFRACA2	PLLFRACA2	PLLFRACA2	PLLFRACA2
PLLINTB	0x0D	n.u.	PLLINTB	PLLINTB	PLLINTB	PLLINTB	PLLINTB	PLLINTB	PLLINTB
PLLFRACB0	0x0E	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0	PLLFRACB0
PLLFRACB1	0x0F	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1	PLLFRACB1
PLLFRACB2	0x10	n.u.	n.u.	reserved	PLLFRACB2	PLLFRACB2	PLLFRACB2	PLLFRACB2	PLLFRACB2
PLLINTC	0x11	n.u.	PLLINTC	PLLINTC	PLLINTC	PLLINTC	PLLINTC	PLLINTC	PLLINTC
PLLFRACC0	0x12	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0	PLLFRACC0
PLLFRACC1	0x13	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1	PLLFRACC1
PLLFRACC2	0x14	n.u.	n.u.	reserved	PLLFRACC2	PLLFRACC2	PLLFRACC2	PLLFRACC2	PLLFRACC2
PLLINTD	0x15	n.u.	PLLINTD	PLLINTD	PLLINTD	PLLINTD	PLLINTD	PLLINTD	PLLINTD
PLLFRACD0	0x16	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0	PLLFRACD0
PLLFRACD1	0x17	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1	PLLFRACD1
PLLFRACD2	0x18	n.u.	n.u.	reserved	PLLFRACD2	PLLFRACD2	PLLFRACD2	PLLFRACD2	PLLFRACD2
SLOPEDIV	0x19	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV	SLOPEDIV
POWCFG0	0x1A	PA_PS2	PA_PS2	PA_PS2	PA_PS1	PA_PS1	PA_PS1	SLOPEDIV	SLOPEDIV
POWCFG1	0x1B	POUT2	POUT2	POUT2	POUT2	POUT1	POUT1	POUT1	POUT1
FDEV	0x1C	FDEVSCAE	FDEVSCAE	FDEVSCAE	FDEV	FDEV	FDEV	FDEV	FDEV
GFDIV	0x1D	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV	GFDIV
GFXOSC	0x1E	FHBLANK	reserved	reserved	reserved	GFBYP	GFDIV	GFDIV	GFDIV
ANTTDCC	0x1F	DCCVBYP	DCCDISALE	DCCCONF	DCCCONF	TUNETOP	TUNETOP	TUNETOP	TUNETOP
RES1	0x20	n.u.	reserved	reserved	reserved	reserved	reserved	reserved	reserved
VAC0	0x21	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR	VAC_CTR
VAC1	0x22	n.u.	VAC_NXOC	VAC_NXOC	VAC_NXOC	VAC_NXOC	VAC_NXOC	VAC_NXOC	VAC_CTR
RES2	0x23	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
CPCFG	0x24	n.u.	reserved	reserved	reserved	CPTRIM	CPTRIM	CPTRIM	CPTRIM
PLLBW	0x25	reserved	PLLBWTRM	PLLBWTRM	PLLBWTRM	reserved	reserved	reserved	reserved
RES3	0x26	reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved
ENCCNT	0x27	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT	ENCCNT

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