USER'S MANUAL

An Open Platform based on Texas Instruments' OMAP L138 processor

Revision 0.1
Preliminary

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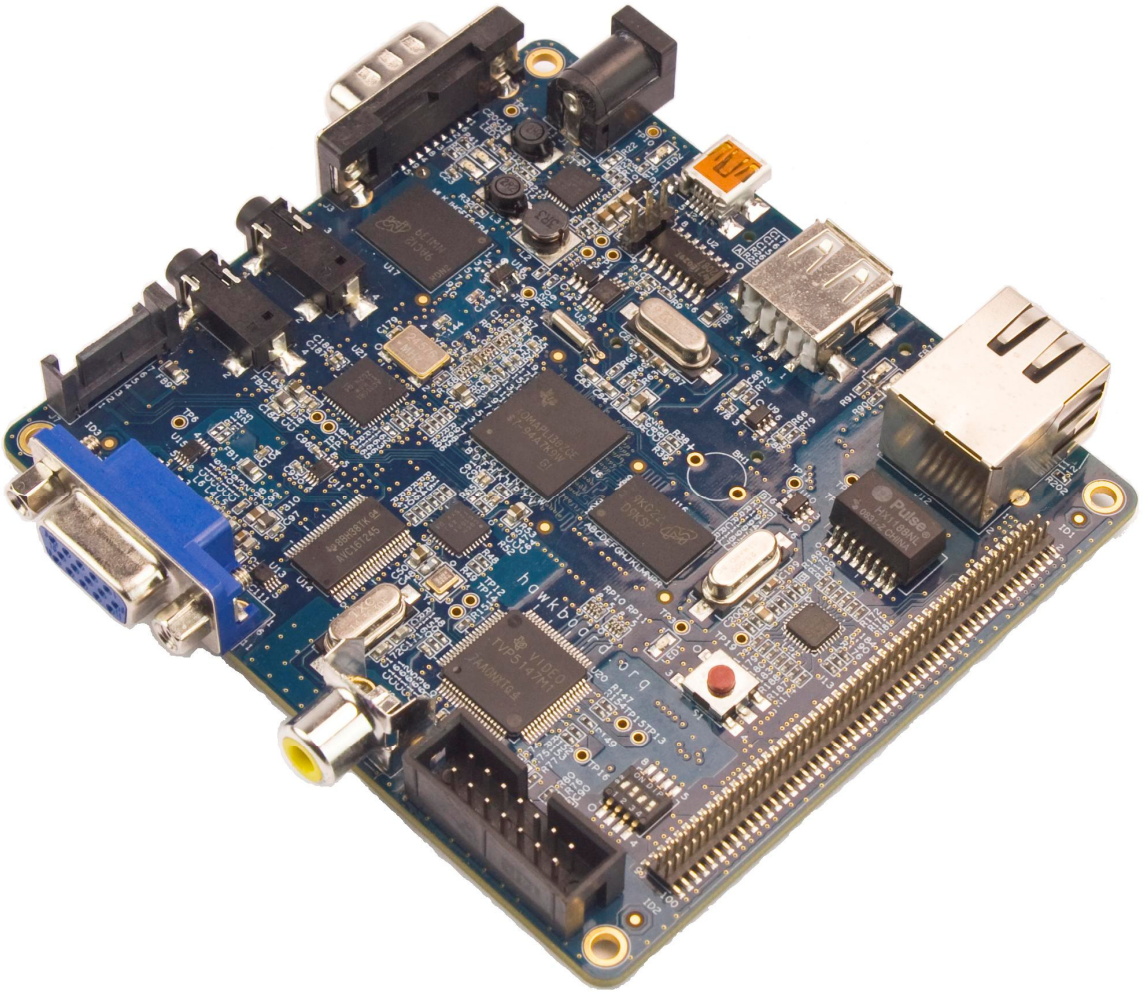
Hawkboard Photograph



1. Introduction

Hawkboard is an open community board mainly designed to provide to the community a feature rich & economical solution based on Ti's OMAP L138 processor. With a wide range of peripheral support, this board is an ultimate tool for digital media & storage applications

The OMAP L138 offers an integrated ARM9 and a Ti DSP. Its low power consumption level opens this system to a large range of Embedded & industrial applications.

Internal Memory controller offers support for wide range of memories including DDR2/MDDR/SDRAM/NOR & NAND FLASH.

Inbuilt SATA controller supporting SATA I & SATA II interfaces are available for extending the storage capacity of this platform.

Inbuilt MMC/SD controller provides an instant add on storage for personal collections.

UPP provides a high speed parallel interface to FPGAs & other data converters.

Two USB ports provide wide variety of peripheral connectivity. The USB OTG port also provides an option to power the Hawkboard when connected to a PC/LAPTOP.

1.1 Features

Processor

- Ti OMAP-L138 Low Power Application Processor
- 300-MHz ARM926EJ-STM RISC CPU
- 300-MHz C674x VLIW DSP
- On-Chip RTC

Memory

- 128 MByte DDR2 SDRAM running at 150MHz
- 128 MByte NAND FLASH
- 1 SD/MMC Slot

Interfaces

- One RS232 Serial Port
- One Fast Ethernet Port (10/100 Mbps)
- One USB Host port (USB 1.1)
- One USB OTG port (USB 2.0)
- One SATA Port (3Gbps)
- One VGA Port (15 pin D-SUB)
- Two AUDIO Ports (1 LINE IN & 1 LINE OUT)
- One Composite IN (RCA Jack)

Expansion Interface

- VPIF
- UPP
- PRU
- LCDC
- UART(x2)
- SPI (x2)
- I2C (x1)
- eCAP
- eHRPWM
- GPIO

Software Support

- U-Boot
- Linux BSP

1.2 Hawkboard diagram

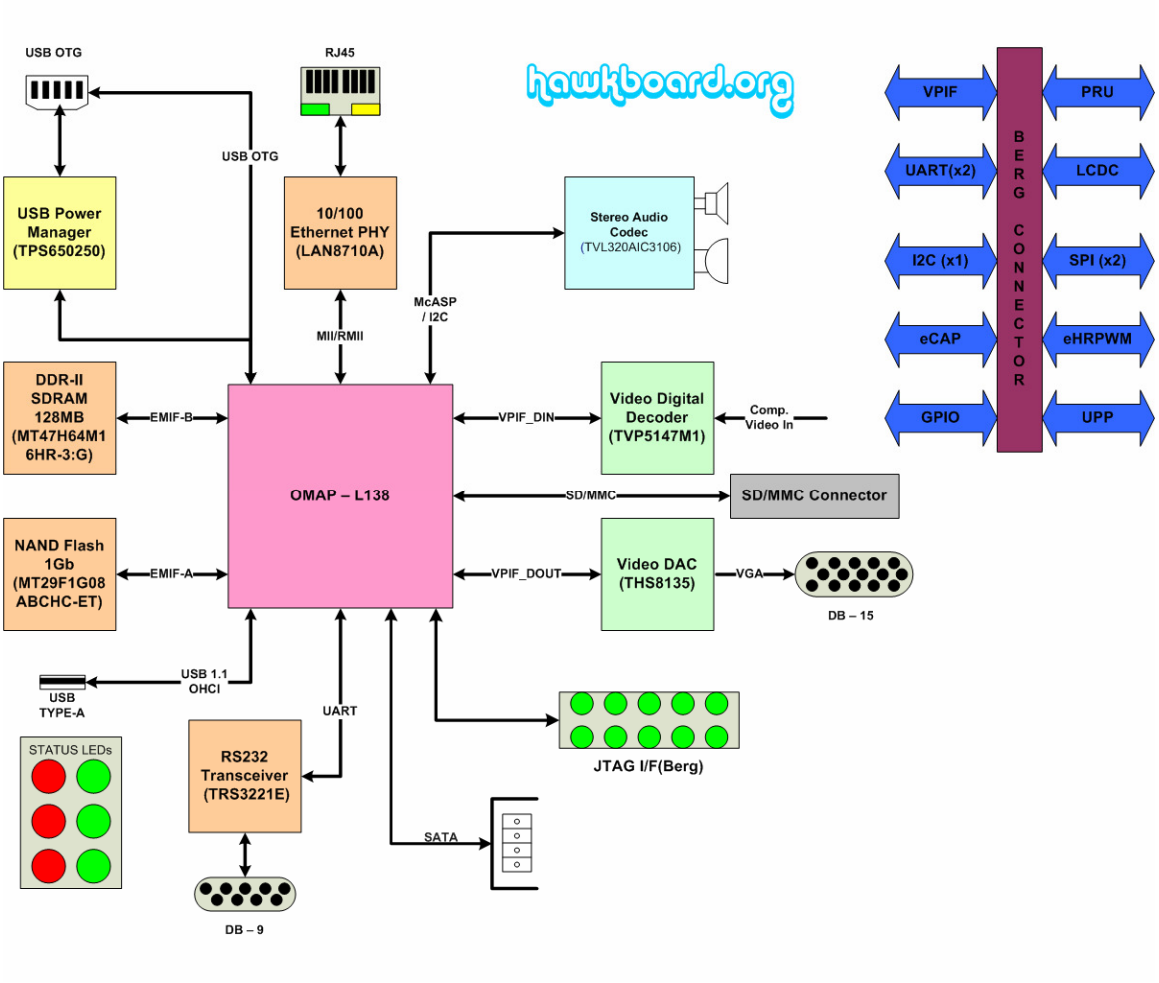


Figure 1. Hawkboard diagram

1.3 Hawkboard component location

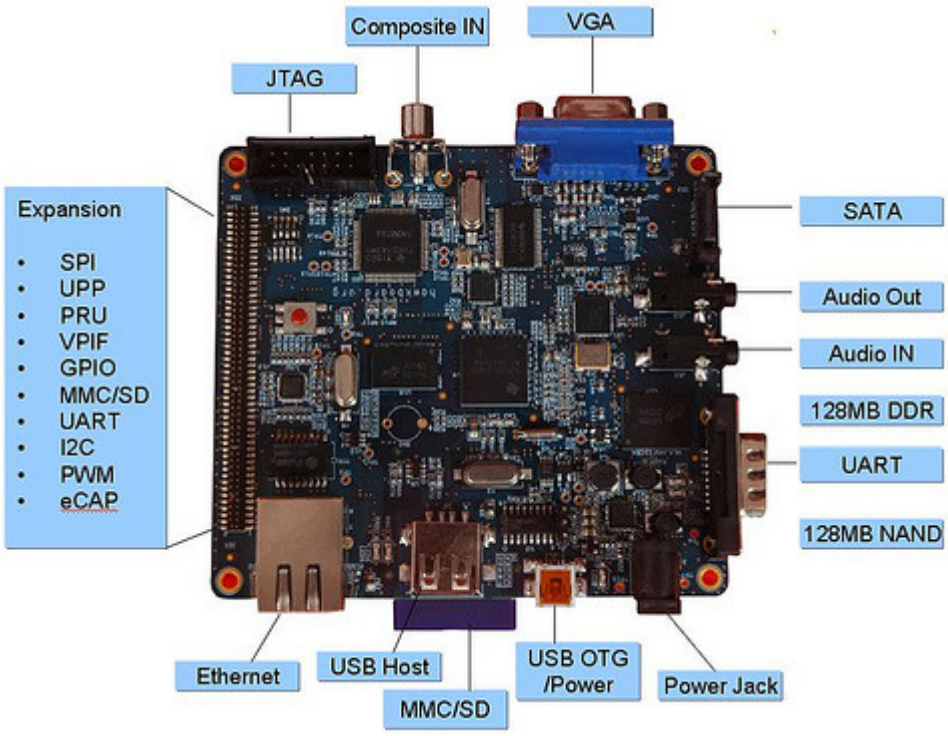


Figure 2. Hawkboard location

2. Hawkboard setup

2.1 Unpacking Instructions

Unpack the equipment from the shipping carton. Carefully check the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.

Avoid touching areas of integrated circuitry; static discharge can damage circuits.

2.2 Board Configuration

The Hawkboard is factory tested & comes with a pre-built Linux image. The user should require a 5V, 1.5A DC Adapter & a Serial Null modem cable (female to female) in order to verify the working of Hawkboard.

Make sure the Switch SW1 is set to the following

- Pin1 = ON
- Pin2 = OFF
- Pin3 = OFF
- Pin4 = OFF

2.3 Powering hawkboard

Connect the adapter to the 5V DC socket (J1) & connect the serial cable between the serial port (J3) of Hawkboard & the PC.

Open a terminal emulator such as HyperTerminal / TeraTerm on the PC. The terminal equipment need to have the following setting: Baud Rate = 115200, data = 8-bit/char, stop bit = 1, parity=none, flow control=none.

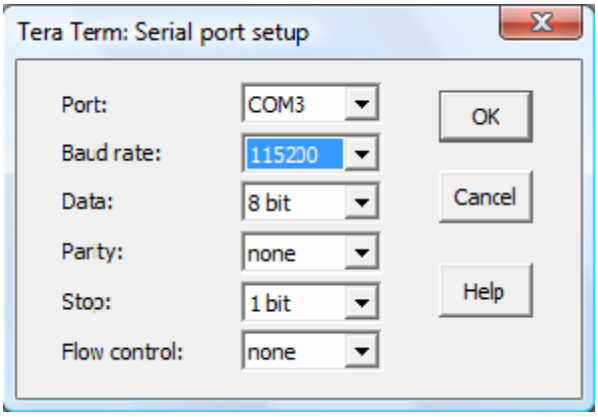


Figure 3. Terminal Emulator setup

Power On Hawkboard & you could see U-Boot booting with appropriate messages being displayed on the terminal emulator as shown in the picture below.

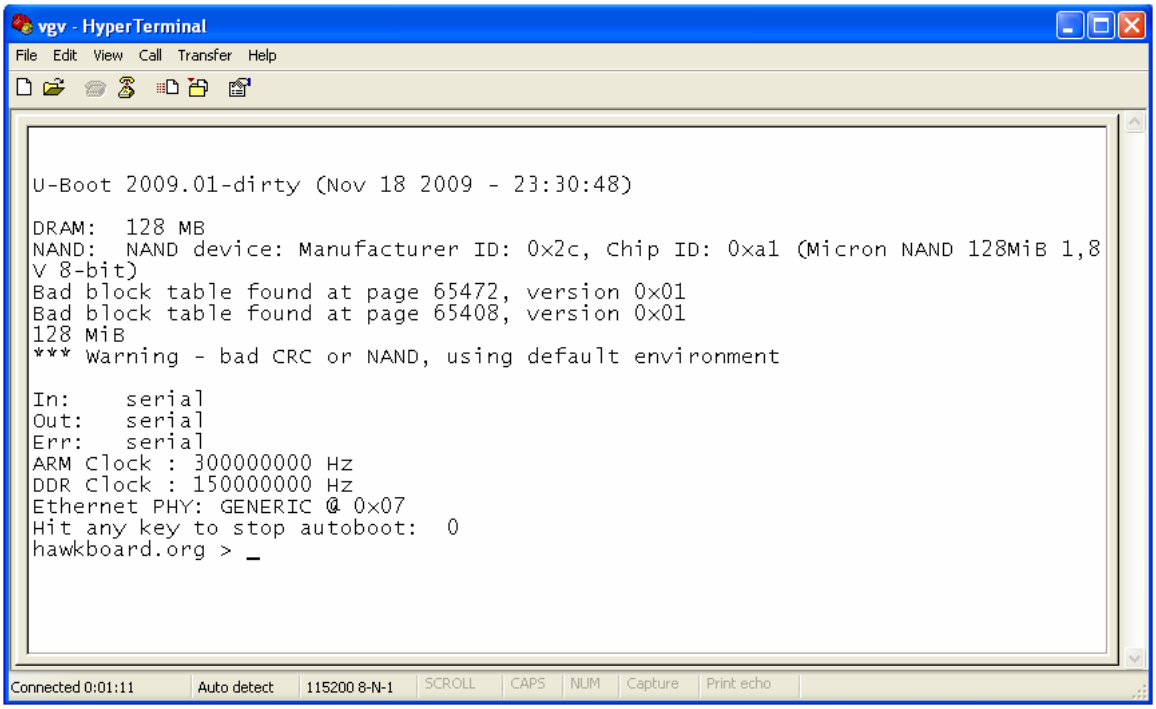


Figure 4. Running U-Boot

3. Functional Description

3.1 OMAP L130 Low Power Application processor

The Hawkboard is based on Texas Instruments OMAP-L138 processor, which is specifically designed to address low power embedded applications. The Processor architecture offers a very attractive design density by combining on-chip rich peripheral controllers enabling OEMs and ODMs to quickly bring to market devices featuring robust operating systems support, rich user interfaces, and high processing performance life through the maximum flexibility of a fully integrated mixed processor solution.

The dual-core architecture of the device provides benefits of both DSP and Reduced Instruction Set Computer (RISC) technologies, incorporating a high-performance TMS320C674x DSP core and an ARM926EJ-S core.

The device DSP core uses a two-level cache-based architecture. The Level 1 program cache (L1P) is a 32KB direct mapped cache and the Level 1 data cache (L1D) is a 32KB 2-way set-associative cache. The Level 2 program cache (L2P) consists of a 256KB memory space that is shared between program and data space. L2 also has a 1024KB Boot ROM. L2 memory can be configured as mapped memory, cache, or combinations of the two. Although the DSP L2 is accessible by ARM and other hosts in the system, an additional 128KB RAM shared memory is available for use by other hosts without affecting DSP performance.

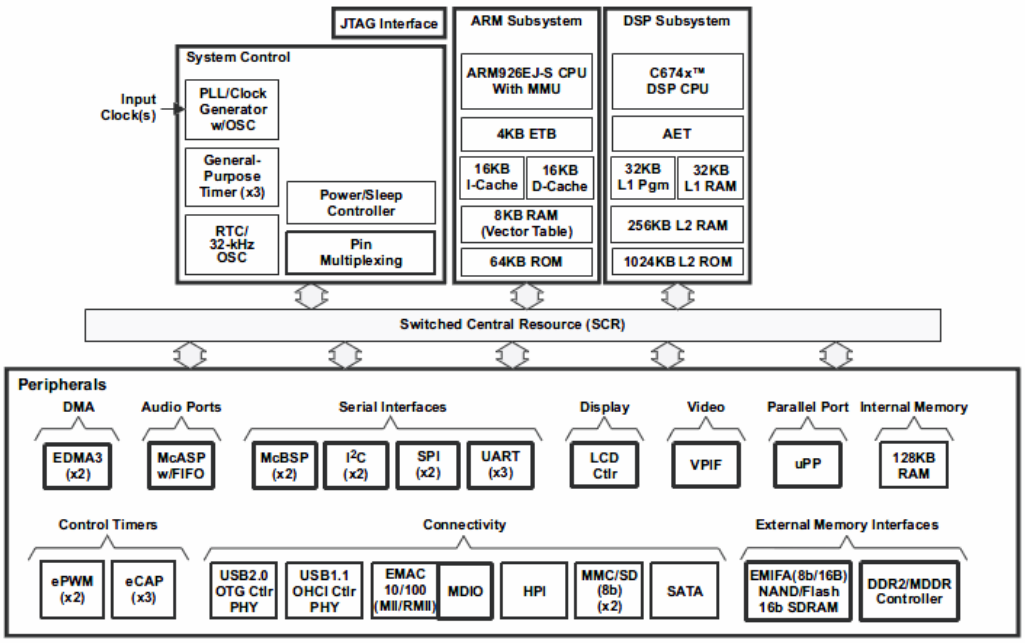


Figure 5. OMAP L138 Block Diagram

3.2 External Memory Interface Controller (EMIFA)

EMIFA is one of two external memory interfaces supported on the device. It is primarily intended to support asynchronous memory types, such as NAND and NOR flash and Asynchronous SRAM. However on this device, EMIFA also provides a secondary interface to SDRAM.

The EMIFA data bus width is up to 16-bits.The device supports up to 24 address lines and two external wait/interrupt inputs. Up to four asynchronous chip selects are supported by EMIFA (EMA_CS[5:2]). At present a 128 MB NAND flash is connected to this interface.

3.3 DDR2/mDDR Interface

The OMAP-L138 integrates fully programmable DDR2/mDDR memory controller that operates at 150 MHz. It supports JESD79D-2A standard compliant DDR2 SDRAM devices and compliant Mobile DDR SDRAM devices.

The DDR2 SDRAM present on board is connected to this interface

3.4 MMC/SD Interface

The OMAP-L138 integrates two MMCSD controllers which are compliant with MMC V3.31, Secure Digital Part 1 Physical Layer Specification V1.1 and Secure Digital Input Output (SDIO) V2.0 specifications.

The Hawkboard is equipped with one MMC/SD slot

3.5 SATA Interface

One SATA interface is provided, which interfaces directly to the on-chip SATA controller. The Serial ATA Controller (SATA) provides a single HBA port operating in AHCI mode and is used to interface to data storage devices at both 1.5 Gbits/second and 3.0 Gbits/second line speeds.

3.6 USB Interface

The OMAP-L137 incorporates two on chip USB controllers. The USB 2.0 interface is brought out to a micro A/B connector.

A jumper is provided to make a flexible host, peripheral, and USB on the go interface. The second USB 1.1 interface is brought out to an A type host interface connector.

3.7 Ethernet Interface

The OMAP-L138 has one on-chip Ethernet Controller. The Ethernet Media Access Controller (EMAC) provides an efficient interface between device and the network. The EMAC supports both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode, with hardware flow control and quality of service (QOS) support.

The Ethernet controller is connected to the External PHY using the MII interface. The PHY device is configured by a set of MII registers accessed trough the serial management interface.

3.8 UART Interface

The internal UART2 on the OMAP-L138 device is driven to connector J3. The UART's interface is routed to the RS-232 line drivers prior to being brought out to a DB-9 connector, J3.

3.9 AUDIO Interface

The Hawkboard incorporates a Texas Instruments TLV320AIC3106 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I2C bus is used as the AIC3106's control channel. The control channel is generally only used when configuring the codec; it is typically idle when audio data is being transmitted,

McASP is used as the bi-directional data channel. All audio data flows through the data channel.

The codec is clocked via a 24.576 MHz oscillator. The internal sample rate generator subdivides the default system clock to generate common audio frequencies. The sample rate is set by a codec register.

3.10 Composite Video In

The hawkboard incorporates the TVP5147M1 device, which is a high-quality, single-chip digital video decoder that digitizes and decodes all popular baseband analog video formats into digital component video.

The TVP5147M1 decoder supports the analog-to-digital (A/D) conversion of component YPbPr signals, as well as the A/D conversion and decoding of NTSC, PAL, and SECAM composite and S-video into component YCbCr.

The TVP5147M1 is interfaced to the processor using the Video port interface, which is capable of capturing digital video streams (SD & HD format), for further processing of the video streams.

A 14.318-MHz clock is required to drive the PLL, which generates the system and pixel clocks.
Communication with the TVP5147M1 decoder is via an I2C host interface.

3.11 VGA Interface

Texas Instruments THS8135 Video DAC is used to provide a VGA interface to the hawkboard. The THS8135 is a general-purpose triple high-speed D/A converter optimized for use in video/graphics applications.

Input for the THS8135 is provided by the 16 bit LCDC interface of the processor. Binary RGB signals are fed to the input of the Video DAC & an analog RGB o/p is obtained, which is used by a Display unit. The Sync signals, HSYNC & VSYNC, are directly fed to the VGA connector from the processor.

Hawkboard also provides EDID interface, which enables the user to derive the display device configuration parameters using I2C commands.

3.12 I^2C0 Interface

The I^2C0 bus on the OMAP-L138 is ideal for interfacing to the control registers of many devices. On the hawkboard the I^2C0 bus is used to configure the Audio Codec, Composite Video In & the EDID Interface.

The I^2C interface supports the following standard and enhanced features:

- up to 400-kHz operation
- 8-bit data transfers
- 7-bit addressing
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters

4. Hawkboard Resources

4.1 Peripheral Chip Select

The OMAP L138 processor provides several chip selects for specific peripheral devices. The table below list the chip selects that has been used.

Chip Select	Peripheral
DDR_CS	DDR2 SDRAM
EMA_CS[3]	NAND FLASH

Table 1. Peripheral Chip Select

4.2 Memory Map

The Hawkboard is equipped with 128MB DDR RAM & 128MB Nand Flash. Following table indicates the memory regions used by these two devices.

Peripheral	Memory Map
DDR	0xC0000000 – 0xC7F00000
NAND	0x00000000 – 0x07F00000

Table 2. Memory Map

4.3 Clock Signals

Hawkboard uses numerous clocks on board for the processor & other peripheral devices. The OMAP L138 uses 24MHz crystal as its main clock. This clock is internally multiplied to produce various frequencies to support multiple on chip peripherals. Apart from this, there are different clocks that are required by various on board peripherals

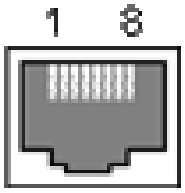
CLOCK(MHz)	Device
24.000	OMAP L138
25.000	SATA
32.768KHz	RTC
14.31818	Video Decoder
24.576	Audio
25.000	Ethernet Phy

Table 3. Hawkboard Clock Sources

5. Hardware Description

5.1 Fast Ethernet port

The OMAP-L138 Processor supports one 10/100 Fast Ethernet port. The RJ45 connector pin assignment is shown below.



Pin #	Signal Description	Pin #	Signal Description
1	TXD+	7	NC/GND
2	TXD-	8	NC/GND
3	RXD+	9	LED1+
4	NC/GND	10	LED1-
5	NC/GND	11	LED2+
6	RXD-	12	LED2-

Table 4. Ethernet Port Pin description

5.2 USB Host 1.1

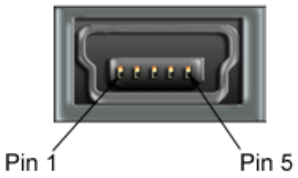
A standard USB A type connector is provided on this interface. This connector is connected directly to the OMAP L138 processor.

Pin #	Signal Description
1	5V
2	D-
3	D+
4	GND

Table 5. USB Host Port Pin Description

5.3 USB OTG 2.0

The connector provided is MINI A/B type of connector. Hawkboard can also be powered through this connector. When used as a host, the board supplies up to 500 ma of current to the USB_VBUS via a TPS2087. This is enabled via the OMAP-L138's DRV_VBUS pin.



Pin #	Signal Description
1	5V
2	D-
3	D+
4	ID
5	GND

Table 6. USB OTG Port Pin Description

5.4 Power Connector

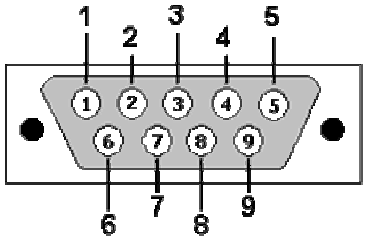
The input power connector brings in +5 volts to the hawkboard. This is a 2.5mm jack. The inside of the jack is tied to through a fuse to VCC_5VD_IN.The other side is tied to ground. The figure below shows this connector as viewed from the card edge.

Pin #	Signal Description
1	5V
2	GND
3	GND

Table 7. Power Connector Pin Description

5.5 UART Connector

The UART connector is a 9 pin male D-connector which provides a UART interface to the Hawkboard. This connector interfaces to the TRS3221 RS-232 line driver and is located on the top side of the board. A view of the connector from the card edge is shown in the figure below.
The signals present on this connector are defined in the following table.

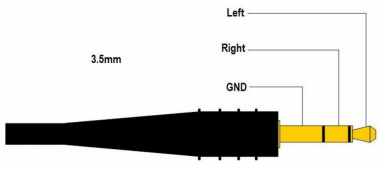


Pin #	Signal Description
1	NC
2	RX
3	TX
4	NC
5	GND
6,7,8,9	NC

Table 8. RS232 Connector Pin Description

5.6 Audio IN

The connector is a stereo audio line input. The input connector is a 3.5 mm stereo jack.
The signals on the mating plug are shown in the figure below.



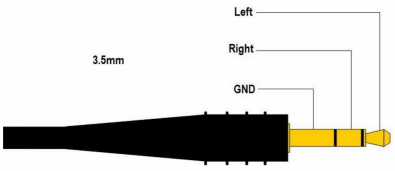
Pin #	Signal Description
1	GND
2	LEFT_LI+
3	RIGHT_LI+
4	GND

Table 9. Line IN Connector Pin Description

5.7 Audio OUT

The audio line out connector is a stereo output. The output connector is a 3.5 mm stereo jack.

The signals on the mating plug are shown in the figure below.

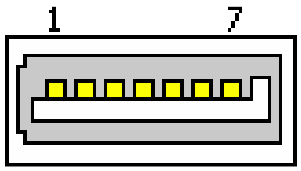


Pin #	Signal Description
1	GND
2	LEFT_LO+
3	RIGHT_LO+
4	GND

Table 10. Line OUT Connector Pin Description

5.8 SATA Connector

The SATA connector connects directly to the SATA controller on the OMAP-L138 processor. The signals present on this connector are defined in the following table.

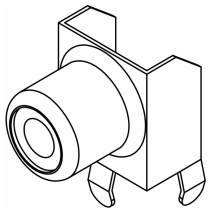


Pin #	Signal Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

Table 11. SATA Connector Pin Description

5.9 Composite IN

A yellow colour RCA Jack is provided to interface any analog video input to the TVP5147M1 video decoder. The signals present on this connector are defined in the following table.

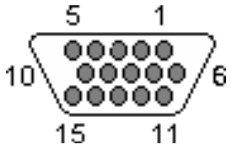


Pin #	Signal Description
1	GND
2	VIDEO_IN
3,4	GND

Table 12. Composite IN Connector Pin Description

5.10 VGA Connector

This connector is a half size VGA connector (DB-15). The Analog video signal & the EDID signals terminate on this connector. The signals present on this connector are defined in the following table.



Pin #	Signal Description	Pin #	Signal Description
1	RED	9	NC
2	GREEN	10	GND
3	BLUE	11	NC
4	NC	12	DATA
5	GND	13	HSYNC
6	GND	14	VSYNC
7	GND	15	CLK
8	GND		

Table 13. VGA Connector Pin Description

5.11 SD/MMC Connector

The SD/MMC connector is located on the bottom side of the board and is used to provide an interface to the following interfaces: SD and MMC.
The pin out for this connector is shown in the table below.

Pin #	Signal Description	Pin #	Signal Description
1	DATA3	8	DATA1
2	CMD	9	DATA2
3	GND	10	CARD DETECT
4	3.3V	11	WRITE PROTECT
5	CLK	12	GND
6	GND	13	GND
7	DATA0	14	GND

Table 14. SD/MMC Connector Pin Description

5.12 Jumper JP1

One 3 pin male berg header is provided for the jumper JP1. This Jumper is used to pull up/pull down the ID signal that is connected to the USB OTG connector.
The pin out for this jumper is provided below.

Pin #	Signal Description
1	5V
2	ID
3	GND

Table 15. Jumper Pin Description

5.13 JTAG Connector

The JTAG Connector is a 2 x 7 double row male header. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs.

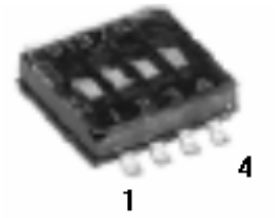
The pin out for the connector is shown in the figure below.

Pin #	Signal Description	Pin #	Signal Description
1	TMS	2	TRST
3	TDI	4	GND
5	3.3V	6	GND
7	TDO	8	GND
9	RTCK	10	GND
11	TCK	12	GND
13	EMU0	14	EMU1

Table 16. JTAG Connector Pin Description

5.14 Boot Mode Selection Switch

The switch is a 4 position Dip Switch. The four positions can be used select multiple boot options. Currently hawk board supports two boot selection methods, which are defined below.



Pin #	UART Boot	NAND Boot
1	OFF	ON
2	ON	OFF
3	OFF	OFF
4	ON	OFF

Table 17. Boot Switch Pin Description

5.15 LEDs

Four LEDs are provided on board for status indication & two LEDs are provided for general purpose usage. The table below shows the description of the LEDs.

LED #	Description
LED1	RESET
LED2	POWER
LED3	UART2 TX
LED4	UART2 RX
LED5	GPIO6[12]
LED6	GPIO6[13]

Table 18. LED Function Description

5.16 Expansion Connector

The Expansion connector is 50 x 2 double row male header. It consists of spare signals that are routed onto the Expansion connectors. Many of these signals have multiple functionalities.

The signals present on this connector are defined in the following table.

Pin #	EXPANSION SIGNALS	PRU SIGNALS
1	SPI0_CLK / EPWM0A / GP1[8] / MII_RXCLK	
2	SPI0_ENA / EPWM0B / MII_RXDV	PRU0_R30[6]
3	SPI0_SIMO / EPWMSYNCO / GP8[5] / MII_CRS	
4	SPI0_SOMI / EPWMSYNCI / GP8[6] / MII_RXER	
5	SPI0_SCS[0] / TM64P1_OUT12 / GP1[6] / MDIO_D / TM64P1_IN12	
6	SPI0_SCS[1] / TM64P0_OUT12 / GP1[7] / MDIO_CLK /TM64P0_IN12	
7	SPI0_SCS[2] / UART0_RTS / GP8[1] / MII_RXD[0] /SATA_CP_DET	
8	SPI0_SCS[3] / UART0_CTS / GP8[2] / MII_RXD[1] /SATA_MP_SWITCH	
9	SPI0_SCS[4] / UART0_TXD / GP8[3] / MII_RXD[2]	
10	SPI0_SCS[5] / UART0_RXD / GP8[4] / MII_RXD[3]	
11	SPI1_CLK / GP2[13]	
12	SPI1_ENA / GP2[12]	
13	SPI1_SIMO / GP2[10]	
14	SPI1_SOMI / GP2[11]	
15	SPI1_SCS[0] / EPWM1B / GP2[14] / TM64P3_IN12	PRU0_R30[8]
16	SPI1_SCS[1] / EPWM1A / GP2[15] / TM64P2_IN12	PRU0_R30[7]
17	SPI1_SCS[4] / UART2_TXD /I2C1_SDA /GP1[2]	
18	SPI1_SCS[5] / UART2_RXD /I2C1_SCL /GP1[3]	
19	AXR15 / EPWM0TZ[0] / ECAP2_APWM2 / GP0[7]	
20	AXR7 / EPWM1TZ[0] / GP1[15]	PRU0_R30[17]
21	AXR0 / ECAP0_APWM0 / GP8[7] / MII_TXD[0] / CLKS0	
22	AXR8 / CLKS1 / ECAP1_APWM1 / GP0[0]	PRU0_R31[8]
23	VP_CLKIN0 / UHPI_HCS1 / GP6[7] / UPP_2xTXCLK	PRU1_R30[10]
24	VP_CLKIN1 / UHPI_HDS1 / GP6[6]	PRU1_R30[9]
25	VP_CLKIN2 / MMCSD1_DAT[3] / GP6[4]	PRU1_R30[3]
26	VP_CLKOUT2 / MMCSD1_D2 / GP6[3]	PRU1_R30[2]
27	VP_CLKIN3 / MMCSD1_DAT[1] / GP6[2]	PRU1_R30[1]
28	VP_CLKOUT3 / GP6[1]	PRU1_R30[0]
29	MMCSD1_DAT[0] / UPP_CH0_CLK / GP8[15]	PRU0_R30[25]

30	MMCSD1_CLK / UPP_CH0_START / GP8[14]	PRU0_R30[24]
31	MMCSD1_CMD / UPP_CH0_ENABLE / GP8[13]	PRU0_R30[23]
32	UPP_CH0_WAIT / GP8[12] G3 I/O CP[30]	PRU1_R30[8]
33	UHPI_CNTL0 / UPP_CH1_CLK / GP6[11]	PRU0_R30[29]
34	UHPI_HCNTL1 / UPP_CH1_START / GP6[10]	PRU0_R30[28]
35	UHPI_HHWIL / UPP_CH1_ENABLE / GP6[9]	PRU0_R30[27]
36	UHPI_HRW / UPP_CH1_WAIT / GP6[8]	PRU1_R31[17]
37	VP_DOUT[7] / LCD_D[7] /UPP_XD[15] / GP7[15]	PRU1_R31[15]
38	VP_DOUT[6] / LCD_D[6] /UPP_XD[14] / GP7[14]	PRU1_R31[14]
39	VP_DOUT[5] / LCD_D[5] /UPP_XD[13] / GP7[13]	PRU1_R31[13]
40	VP_DOUT[4] / LCD_D[4] /UPP_XD[12] / GP7[12]	PRU1_R31[12]
41	VP_DOUT[3] / LCD_D[3] /UPP_XD[11] / GP7[11]	PRU1_R31[11]
42	VP_DOUT[2] / LCD_D[2] /UPP_XD[10] / GP7[10]	PRU1_R31[10]
43	VP_DOUT[1] / LCD_D[1] /UPP_XD[9] / GP7[9]	PRU1_R31[9]
44	VP_DOUT[0] / LCD_D[0] /UPP_XD[8] / GP7[8]	PRU1_R31[8]
45	VP_DOUT[15] / LCD_D[15] /UPP_XD[7] / GP7[7] / BOOT[7]	
46	VP_DOUT[14] / LCD_D[14] /UPP_XD[6] / GP7[6] / BOOT[6]	
47	VP_DOUT[13] / LCD_D[13] /UPP_XD[5] / GP7[5] / BOOT[5]	
48	VP_DOUT[12] / LCD_D[12] /UPP_XD[4] / GP7[4] / BOOT[4]	
49	VP_DOUT[11] / LCD_D[11] /UPP_XD[3] / GP7[3] / BOOT[3]	
50	VP_DOUT[10] / LCD_D[10] /UPP_XD[2] / GP7[2] / BOOT[2]	
51	VP_DOUT[9] / LCD_D[9] /UPP_XD[1] / GP7[1] / BOOT[1]	
52	VP_DOUT[8] / LCD_D[8] /UPP_XD[0] / GP7[0] / BOOT[0]	
53	VP_DIN[7] / UHPI_HD[15] / UPP_D[15] / RMII_TXD[1]	PRU0_R31[29]
54	VP_DIN[6] / UHPI_HD[14] / UPP_D[14] / RMII_TXD[0]	PRU0_R31[28]
55	VP_DIN[5] / UHPI_HD[13] / UPP_D[13] / RMII_TXEN	PRU0_R31[27]
56	VP_DIN[4] / UHPI_HD[12] / UPP_D[12] / RMII_RXD[1]	PRU0_R31[26]
57	VP_DIN[3] / UHPI_HD[11] / UPP_D[11] / RMII_RXD[0]	PRU0_R31[25]
58	VP_DIN[2] / UHPI_HD[10] / UPP_D[10] / RMII_RXER	PRU0_R31[24]
59	VP_DIN[1] / UHPI_HD[9] / UPP_D[9] / RMII_MHZ_50_CLK	PRU0_R31[23]
60	VP_DIN[0] / UHPI_HD[8] / UPP_D[8] / RMII_CRS_DV	PRU1_R31[29]
61	VP_DIN[15]_VSYNC / UHPI_HD[7] / UPP_D[7]	PRU0_R31[15]
62	VP_DIN[14]_HSYNC / UHPI_HD[6] / UPP_D[6]	PRU0_R31[14]
63	VP_DIN[13]_FIELD / UHPI_HD[5] / UPP_D[5]	PRU0_R31[13]
64	VP_DIN[12] / UHPI_HD[4] / UPP_D[4]	PRU0_R31[12]
65	VP_DIN[11] / UHPI_HD[3] / UPP_D[3]	PRU0_R31[11]
66	VP_DIN[10] / UHPI_HD[2] / UPP_D[2]	PRU0_R31[10]
67	VP_DIN[9] / UHPI_HD[1] / UPP_D[1]	PRU0_R31[9]
68	VP_DIN[8] / UHPI_HD[0] / UPP_D[0] / GP6[5]	PRU1_R31[0]
69	MMCSD1_DAT[7] / LCD_PCLK / GP8[11]	PRU1_R30[7]
70	MMCSD1_DAT[5] / LCD_HSYNC / GP8[9]	PRU1_R30[5]
71	MMCSD1_DAT[4] / LCD_VSYNC / GP8[8]	PRU1_R30[4]
72	LCD_AC_ENB_CS / GP6[0]	PRU1_R31[28]
73	MMCSD1_DAT[6] / LCD_MCLK / GP8[10]	PRU1_R30[6]

74	EMA_A[13] / GP5[13]	PRU0_R30[21]
75	EMA_A[12] / GP5[12]	PRU1_R30[20]
76	EMA_A[11] / GP5[11]	PRU1_R30[19]
77	EMA_A[10] / GP5[10]	PRU1_R30[18]
78	EMA_A[9] / GP5[9]	PRU1_R30[17]
79	EMA_A[8] / GP5[8]	PRU1_R30[16]
80	EMA_A[7] / GP5[7]	PRU1_R30[15]
81	EMA_A[6] / GP5[6]	
82	EMA_A[5] / GP5[5]	
83	EMA_A[4] / GP5[4]	
84	PHP_RSTn	
85	5V	
86	5V	
87	5V	
88	5V	
89	GND	
90	GND	
91	GND	
92	GND	
93	GND	
94	GND	
95	GND	
96	GND	
97	3.3V	
98	3.3V	
99	3.3V	
100	3.3V	

Table 19. Expansion Connector Pin Description

6. Electrical Information

The Hawkboard operates from a single +5V external power supply connected to the main power input (J1), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into core voltage, +1.8V and +3.3V using Texas Instruments TPS650250 Power Management Unit.

The +3.3V and +1.8V supply are used for the Processors I/O buffers and other chips on the board.

Hawkboard can also be powered through the USB OTG connector. In this scenario, the current available is only up to 500mA (MAX). The complete operation of Hawkboard is not guaranteed in this case.

The Input to the Hawkboard should not exceed 5V in any case, failing which the board might get damaged.

7. Mechanical Information

Parameter	Max
Board Height	Approx. 90cm
Board Breadth	Approx. 100cm
Board Weight	TBW

Table 20. Mechanical Information