# ADVance MS Quick Reference Guide

## Mentor Graphics web site:

www.mentor.com

## Mentor Graphics Support:

**North America**
**Phone: 1-800-547-4303**
**www.mentor/supportnet**
**Worldwide**
**www.mentor.com/supportnet/support_offices.html**

## Installation / Environment / Licensing

### Documentation

Getting Started with ADVance MS: *adms_gs.pdf*
ADVance MS User's Manual: *adms_ur.pdf*
VHDL-AMS Quick Reference: *vhdlams_qr.pdf*

### Environment Variables

| | | |
|---|---|---|
| LM_LICENSE_FILE | **Required** | Pathname of *anacad.license* |
| ADMSIM | Optional | Pathname of *adms.ini* file |

### PATH Environment Variable

Add /<install_dir>/$anacad/bin to $PATH

### Starting the License Server

Copy *anacad.license* to /<install_dir>/$anacad/mgls/
Run /<install_dir>/$anacad/com/setup_mgls

### Invoking ADVance MS

Run /<install_dir>/$anacad/bin/vasim

## Key Simulation Control Commands (.cmd file)

| Command Syntax | Description |
|---|---|
| **.tran** *tprint tstop [tstart]* | Activates transient analysis with print step and duration of analysis |
| **.option** NOASCII | Simulation does not generate ASCII output (.chi) |
| **.plot** dc/ac/tran V(*node*) I(*node*) | Plot simulation results for voltage/current at node |
| **.plot** FOUR ... | Plot Fast Fourier Transform results |
| **.probe** VTOP | Gives output showing all top level node voltages |
| **.extract** ... | Extract waveform characteristics |
| **.ac** dec\|oct\|lin *n fstart fstop* | AC analysis; start and stop frequencies can be set |
| **.dc** ... | DC analysis |
| **.defmac** *mac_name*(*arg*{, *arg*}) | Macro definition with written arguments |
| **.defwave** | Waveform definition |
| **.end** | End Eldo netlist |
| **.four** label=*lname wname* | FFT select waveform |
| **.ic** v(*nn*)=*val* {v(*nn*)=*val*} | Initial transient analysis conditions |
| **.include** *fname* | Include a filename in an input netlist |
| **.nodeset** | DC analysis conditions |
| **.noise** *outv insrc nums* (X*subckt*) | Noise Analysis |
| **.noisetran** ... | Transient Noise Analysis |
| **.op** ... | DC Operating Point calculation |
| **.option** ... | Simulator configuration |
| **.param** *par=val* \| *par={expr}* \| *par="name"* | Global parameter declarations |
| **.plotbus** *bname* | Plotting of bus signals |
| **.print** ... | Printing of results |
| **.setbus** *bname pn* | Creates a bus *bname* with number of bits *pn* |
| **.sigbus** ... | Sets signal on a bus |
| **.temp** *ts* | Set circuit temperature |
| **.use** ... | Use previously simulated results |

## Key ADVance MS Commands (see User's Manual for more)

| Command | Where Used<br>**(Sh)ell**<br>**(ADMS)** | Description<br>For details on these commands refer to the ADVance MS User's Manual |
|---|---|---|
| **vacom** | Sh, ADMS | VHDL-AMS compiler |
| **vadel** | Sh, ADMS | Deletes a unit from a selected library |
| **vadir** | Sh, ADMS | Selectively lists the contents of a design library |
| **valib** | Sh, ADMS | Creates a design library |
| **vasetlib** | Sh | Sets the default working library |
| **vaunlock** | Sh | Restores the unlocked library **lib_name** |
| **vasim** | Sh, ADMS | VHDL-AMS and/or Verilog simulator |
| **vamap** | Sh, ADMS | Defines or displays library mappings |
| **valog** | Sh, ADMS | Verilog and Verilog-A compiler |
| **import_adms** | Sh, ADMS | Used to import from ADVance MS to ModelSim |
| **import_ms** | Sh, ADMS | Used to import digital portions from ModelSim to ADVance MS |
| **add log** | ADMS | Creates log files (*dou* and *cou*) for analysis with the "Wave" window |
| **add log -delta** | ADMS | **The si**mulator only has to solve analog data when it has sufficiently changed more than the given delta value |
| **add wave** | ADMS | Adds signals, quantities or terminals to the "Wave" window |
| **add wave -delta** | ADMS | **The si**mulator only has to solve analog data when it has sufficiently changed more than the given delta value |
| **add list** | ADMS | Will give signal output as an ASCII window |
| **write list** | ADMS | This will record the contents of the List window in an output file |
| **batch_mode** | ADMS | Typically used as a condition in an if statement. Returns 1 if ADVance MS is in batch mode and 0 if not |
| **cd** | Sh, ADMS | Changes directory |
| **change** | ADMS | Modifies the value of a VHDL-AMS variable or constant |
| **examine** | ADMS | Examines one or more VHDL-AMS item and displays its value in the "Transcripts" window |
| **exit** | ADMS | Exits the simulator and the ADVance MS application |
| **find** | ADMS | Displays full pathnames of matching VHDL-AMS items |
| **force** | ADMS | Forces interactive stimulus on VHDL-AMS nets |
| **history** | ADMS | Lists previous commands |
| **ms** | ADMS | Used with a simulation that uses ADVance MS and ModelSim together requires alternate sequential commands |
| **noforce** | ADMS | Removes the effect of any active **force** commands on selected VHDL-AMS items |
| **probe** | ADMS | Updates the mask on a net when running an AC analysis or running a *.do* file |
| **pwd** | Sh, ADMS | Displays current path |
| **quit** | ADMS | Exits the simulator and the ADVance MS application |
| **restart** | ADMS | Restarts the simulator |
| **run** | ADMS | Advances the simulation time |
| **view** | ADMS | Opens an ADVance MS window and brings it to the front |

## vasim

### Key Arguments (use -help for full list)

| | |
|---|---|
| [-help] | Display vasim syntax help |
| [-c] | Command line mode |
| [-lib <physical_lib_name>] | Specifies the work library to be used during simulation |
| [-cmd <CMD-file>] | If top is VHDL-AMS the simulation command file is specified<br>If top is Eldo/SPICE the Eldo netlist file is specified |
| [-do <startup_file_name>] | Execute the command(s) specified by the startup file named by <startup_file_name> |
| [-nature <whole_nature_name>] | Used only with mixed Eldo and VHDL-AMS descriptions |
| [<design_unit>] | Top of the design to simulate in case of a VHDL-AMS on top |
| [-ms {<ms_options>}] | Specifies that ms_options are for the ModelSim engine |
| [-mach] | Enables the use of Mach |
| [-dcal] | Performs auto-calibration |

### Examples

```
vasim
vasim -cmd file.cir
vasim -cmd file.cmd MY_ENTITY MY_ARCHITECTURE
```

## vaunlock

### Key Arguments (use -help for full list)

| | |
|---|---|
| <lib_name> | Specifies physical name of the unlocked library to restore |

## Files

| | |
|---|---|
| adms.ini | System initialization file or project file; stores information such as locations of libraries |
| transcript | Default file name that ADVance MS transcript window activity is saved to |
| .vams_setup | Preference file, if saved in the working or home directory, then preferences will be loaded on next startup of ADVance MS. Delete this file to return to default settings |
| pref.tcl | Preference file |
| modelsim.tcl | Model*Sim* preference file; Window sizes, positions, colors, etc.; user Tcl/Tk code<br>Model*Sim* Initialization;<br>Stores library locations, simulator resolution, paths, etc. |
| .cmd | Key Simulation Control Commands (.cmd file) |

## vacom

### Key Arguments (use -help for full list)

| | |
|---|---|
| [-help] | Display vacom syntax help |
| [-work <physical lib name>] | Specify working library |
| [-nocheck] | Disables run time checking |
| [-nodebug] | Compile without generating debug info |
| [-noexplim] | Compile without truncating exponential |
| [-constants] | Compile without optimizing constants |
| [-gccopt] | Max optimization performed by gcc |
| [-force] | No warning about overwriting |
| [-ams] | Compile in ADVance MS and import into ModelSim |
| [-link] | Compile ignoring empty architectures |
| [-spice] | Import SPICE subcircuit |
| [-ms <ms_options>] | Import ModelSim VHDL model |

### Examples

```
vacom example.vhd
vacom -nodebug example.vhd
vacom example1.vhd example2.vhd -ms -nocheck
vacom -link "myentity(arch)"
```

## vasetlib

### Key Arguments (use -help for full list)

| | |
|---|---|
| <lib_name> | Specifies physical name of default library |

## vamap

### Key Arguments (use -help for full list)

| | |
|---|---|
| <logical_name> | Specifies the logical name of the library to be mapped |

## valib

### Key Arguments (use -help for full list)

| | |
|---|---|
| [-help] | Display valib syntax help |
| [-link] <ms_lib> | Mirrors Model*Sim* library into ADVance MS library |
| <directory_name> | Pathname of library to be created |
| [-copy <ms_lib>] | Mirrors the ModelSim library into the ADVance MS library |

### Example

```
valib -link <MS_lib_pathname> <ADMS_lib_pathname>
```

## More Information

### Online (see documentation sub-directory)

| | |
|---|---|
| Getting Started | *adms_gs.pdf* |
| User's Manual | *adms_ur.pdf* |

### Internet

www.mentor.com/ams

## valog

### Key Arguments (use -help for full list)

| | |
|---|---|
| [-help] | Display valog syntax help |
| [-work] <physical lib name> | Specify working library |
| [-link] | Compile ignoring empty architectures |
| [-ms [<ms_options>]] or [-ms_bit [<ms_options>]] | Import Verilog ModelSim Model |
| [<Verilog-A_options>] | Options for Verilog-A usage |

### Examples

```
valog -work TOOLS -link my_invertor
valog -work TOOLS -link my_invertor -ms_bit
valog -work TOOLS invertor.v -ms
```

## vadel

### Key Arguments (use -help for full list)

| | |
|---|---|
| [-help] | Display vadel syntax help |
| <logical_name> | Specifies the logical name of the library to be mapped |
| [-del] | Deletes the mapping specified by <logical_name> from current project file |
| <path> | Specifies the pathname of directory to which the library is to be mapped |
| [-ms <ms_options>] | Invokes compilation of ModelSim |

### Examples

```
vadel xor behavior
vadel -lib TOOLS base
vadel xor -ms
```

## import_ms

### Key Arguments (use -help for full list)

| | |
|---|---|
| [-help] | Display import_ms syntax help |
| [-lib <path>] | Specifies the pathname of the ADVance MS library |
| [-vhdl <design_unit>] | Specifies the VHDL design unit to be transferred to AIMS |
| [-vlog [-b <ms_options>] <module> ...] | Gives the Verilog module list to be transferred into ADMS |
| [-c] | Enter command line batch mode |

## pref.tcl

### Loading Order

Always loads *$anacad/adms/$admsver/gui/pref.tcl*

Loads the first found from:

1. a file called *.vams_setup* in the working directory (the directory where the **vasim** command has been run)
2. a file called *.vams_setup* in the home directory (in the login directory)
3. The file called *$anacad/adms/$admsver/gui/pref.tcl*

## ADVance MS Main window language (Tcl/Tk)

### Language Syntax

```
command arg1 arg2 arg3 ...
```

### Language Syntax: Commands

```
set <var><value>
expr <math expression>
exec <ShellCommand>
info <option><procedure name>
```

### Language Syntax: Procedures

```
proc name {arglist}{body}
```

### Language Syntax: Conditionals

```
if {boolean}{bodytrue} else {bodyfalse}
```

### Language Syntax: Loops

```
while {boolean}{body}
foreach loopVar {valuelist}{cmndBody}
for {initial}{test}{final}{body}
```

### Getting Information in ADVance MS Tcl

| | |
|---|---|
| info | Get information on a Tcl construct |
| info xx | Find out args to info |

### Examples

#### #Print the string length of "Hello, World"

```
set len [string length "Hello World"]
echo "Hello, World is $len characters long"
```

#### #Print the result of a mathematical expression

```
set a 25
set b 11
set c 3
echo "the result is [expr ($a + $b)/$c]"
```

#### #Set the date to always be put into datime at the beginning of the simulation

```
proc set_date {} {
global env
set do_the_echo [set env(DO_ECHO)]
set s [exec date]
force -deposit datime $s
if {do_the_echo} {
echo "New time is [examine -value datime]"
}
}
```

## adms.ini

### Loading Order

1. $ADMSIM environment variable
2. In the current directory if $ADMSIM is not set
3. In *$anacad/adms/$admsver/libs*

### For detailed information see:

ADVance MS User's Manual:
"System Initialization/Project File"

## Standards Supported

### VHDL

IEEE 1076-1993
IEEE 1076.1-1999 (VHDL-AMS)
VITAL 2.2b
VITAL'95 - IEEE 1076.4-1995

### Timing

SDF 1.0 to 3.0

### Verilog

IEEE Std 1364-1995
Verilog-A