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*          HYTEC VME - VSMC 2256          *
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*        FOUR CHANNEL STEPPER MOTOR       *
*                                         *
*               CONTROLLER                *
*                                         *
*             TECHNICAL MANUAL            *
*                                         *
*         AND CIRCUIT DESCRIPTION         *
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CONTENTS

Circuit Diagrams:-

1. Introduction

This single width 6U high VME module contains four independent Stepper Motor control channels which generate step and direction signals for, and receive limit, fault and opto-encoder signals from, an external drive system and motor assembly. The unit offers 24 bit plus sign step magnitude, with programmable speed, ramp rate and slow-down count, independently programmable for each channel.
Read-back of each step counter "on the fly" is allowed, as well as "soft stop". Full Interrupt masking and handling is provided.

2. Stepper Control Channel - Register Set Overview

Each of the four independent channels is equipped with its own complete set of VME registers in A16 (short addressing) space, in line with Hytec's standard scheme which is modelled on the VXI Configuration Register set, see Figure 1.

This register set comprises the following:-

a) An ID register, indicating manufacturer and type.
b) A vector register, for programming interrupt acknowledge data.
c) A Model Code register, showing 2256 decimal, the unit's type no.
d) A Control and Status Register through which the channel is controlled and its status observed.
e) A Mask register, which selects certain bits in the CSR as possible interrupt sources.
f) A Request register, showing unmasked status bits and the vector loaded.
g) A 24-bit step counter register, formed as 16 + 8
h) A Profile Register, for speed control, ramp rate selection, multiplier (speed X1, X10, X100), direction and encoder control.
i) A Slow Down Count register for detecting the ramp down point

3. Setting Up - Switches and Jumpers

Before installing the module, there are some switches and jumpers to configure as follows:-

8-way DIL switch: This sets the board's VME Base address, and therefore the addresses of the registers in all four channels.

Switches 1 to 6 select '1' or '0' for each of 6 address lines, switches 7 and 8 do nothing. Switch 1 corresponds to address line A13, switch 6 to A08. Switch 'OPEN' means that address line must be a '1', switch 'CLOSED' means the address line must be '0'. Address lines A15 and A14 must both be '1' to start at HEX C000 in line with Hytec's standard 'VXI' scheme.

For example: To select D700 as the start address:

A15	A14	A13	A12	A11	A10	A09	A08	
1	1	0	1	0	1	1	1	Where 'C'= 'closed'
fixed	fixed	C	O	C	O	O	O	& 'O' means 'open'.

Channel 1 start address will then be D700, Channel 2 will start at D740, Channel 3 at D780 and Channel 4 at D7C0. Total address space used - 256 bytes, from D700 to D7FF.

Jumpers: There are 5 jumpers on the unit; jumpers 1 to 4 select step output pulse widths for channels 1 to 4 respectively, that is JP1 selects pulse width for channel 1: Jumper installed = 20 microsecond pulse, jumper out = 1 microsecond pulse; jumper 5 connects the unit's Interrupt output signal to the VMEbus IRQ4 line (see section 6 on Interrupts).

4.   VME Interface - Full Register Set Description

All registers in this module may be accessed in 16-bit or 8-bit mode, that is they are all D16 D08(EO) compatible, as required by the VMEbus Specification. For some, the 'top half' has no meaning, but accesses to these will have no effect .

Running through our 'Overview' list (sect. 2), the following is a full description of the format and function of each register (see Fig. 1).

Item   Name Offset from Channel Base Address (HEX)

a)/b) ID/Vector   + 00

The ID register and Vector register are at the same address. You read the ID and write the vector.

Reading the ID gives HEX FF7F, where 'F7F' on bits 0-11 is Hytec's unique VXI identifier, and 'F' on bits 12-15 means that this unit is A16 only, register based.

Writing an 8-bit number to this location (D0-D7) stores a vector with which it will respond during interrupt acknowledge cycles.

c)   Model Code + 02

This simply shows the unit's Hytec catalogue number, which is 2256 decimal.

d)   Control and Status Register + 04

This is a 16-bit register (CSR for short) through which the channel is controlled and its status observed.

It implements first a channel booking scheme, so that not only the module, but also one channel, may be a multi-master device. A READY/BUSY flagging system is used to show whether or not the channel is in use. In addition to this, there are several 'fixed' bits, which derive from the VXI spec. and then the following:-

i) Interrupt Enable - one bit to enable the output of this channel's logic as an interrupt source.

ii) Status bits for each limit and Drive System fault.

iii) A 'GO' bit for starting the channel.

iv) A 'RUN' bit for seeing if the channel is running.

For more details on the CSR bit assignments and function, see sect. 5.

e)   Mask register   + 0A

This is an 8-bit register residing in the 'top half' of this location, which selects certain bits in the CSR as possible interrupt sources. It must be understood that this register is not 'writeable', it is 'TOGGLEABLE', that is you can switch or toggle chosen bits in it in a similar way to that used in CAMAC. If you write to this register with a '1' in a certain position, that means 'change this bit'. You must therefore read it first to see if its current state matches the desired state, then act accordingly.

The function of the Mask Register is discussed in more detail in section 6 - Interrupts.

f)   Request register + 0C

This register is the logical AND of Status bits and Mask bits in its 'top half' and the Interrupt vector loaded via location 00 in its 'bottom half'. The data in this register is exactly that which is output when an Interrupt Acknowledge cycle takes place to this channel (see section 6).

g)   Step Counter Register + 0E and + 10

This 24-bit register is the actual step counter for the channel, and is formed as 16 bits at base + 0E and 8 bits at base +10.

You may read the counter at any time but you should only write to it when the channel is stopped, for obvious reasons. The counter is loaded with the required number of steps to be taken or the number of shaft encoder output pulses expected and proceeds to count down to zero, whereupon the channel stops. Since this register is in two halves, care needs to be taken to ensure that reading it and 'reconstructing' the result does not give rise to errors due to intervening counts. It is recommended that you read the lower 16 bits first, then the top 8, then the lower 16 again. Then, if there has not been a major transition in the lower 16, the result of the 'reconstruction' will be good.

Writing to the counter should only be done when the channel is stopped, as mentioned above. You should be certain that the ramp-down is complete, since there is logic which allows the channel to 'RUN-ON' after the GO bit is reset during 'soft stop', and if this is still taking place, loading a non-zero value into the step counter will
start the channel running and counting again. Observing the state of 'RUN' in the CSR is recommended.

Having established that the channel has definitely stopped, you should load the step count in the following recommended sequence: top 8 bits first, then the bottom 16, otherwise loading may not be achieved correctly.

h) Profile Register + 12

This 16-bit register handles speed control, ramp rate selection, multiplier (speed X1, X10, X100), direction and encoder control and also permits drive system 'Boosting' and step counter disabling.

```
  15    14    13    12  11   10   09   08   07  - - - - - - - - 00
| DIS | DIR | ENC | B | M2 | M1 | R2 | R1 |  ------ SPEED  ----- |
```

The lower 8 bits of this register control the normal running speed or 'high' speed of the channel. The start/stop speed is one tenth of this speed. With a multiplier of X1, 255 decimal gives a high speed of 5000 steps per second. This 8-bit number controls a current which in turn generates a frequency. In order to reduce noise influences, it is recommended that a higher speed number be preferred, with a lower multiplier; e.g. 129 X10 is better than 13 X100. Furthermore, since there is a degree of overlap between the ranges, more granularity is available (fine speed control) when higher numbers are used.

The other bits of the register act as follows:-

R2, R1 control the ramp time as follows:-

R2	R1	Ramp Time
0	0	4 seconds
0	1	2 seconds
1	0	1 second
1	1	0.5 seconds

M2, M1 control the speed multiplier as follows:-

M2	M1	Multiplier
0	0	X1
0	1	X10
1	1	X100

B - '1' = Boost - Controls boost output to drive system to increase drive current, typically by 25%, during acceleration.

ENC - '1' = Encoder - Use quadrature encoder outputs for generating counting pulses and direction signal; '0' means count step pulses.

DIR - Direction - '1' = 'Clockwise' or towards Full Travel Limit.

DIS - '1' = Disable Counter - unconditionally disables the step counter - useful in encoder applications for fine positioning.

The function of the Profile Register is shown pictorially in Figure 2.

i) Slow Down Count Register + 14

This 16-bit register is continuously compared with the top 16 bits of the step count (bits 8-23). The comparison is sequential for all channels, and is interrupted by addressing the module. Please note that addressing the module more often than every 20 microseconds may cause this scanning system to miss an event. The host computer must calculate the number of steps taken during slow-down and write this register accordingly:- e.g.

High speed = 1000 steps/sec., (so start/stop = 100 s/s), ramp time = 1 second. Number of steps during ramp down = (High + start/stop) x time / 2.

This equates to the average speed during ramp down multiplied by the ramp time, which in our example, will be 550 x 1 = 550. Now divide that by 256 and subtract 1 to arrive at the number to be loaded = 1.

(We subtract 1 because the comparator is examining the top 16 count bits, and the bottom 8 will all be '1' when equality occurs)

5. Control and Status Register Format

The format of this register is as follows:-

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	MAN	RUN	GO	FLT	FULL	HOME	INTEN	0	0	RDY	1	1	0	BUSY

BUSY and RDY are complementary, and form the channel booking scheme. After power-up, RDY is '1' and BUSY is '0'. When the CSR is first read, these are seen as such, i.e. the channel is available, and the trailing edge of that read command sets the BUSY flag to ensure that all further reads show BUSY as '1' and RDY as '0'. These two bits stay in that state until a 'reset' is given, which involves writing a '1' to bit 0 - this means 'finished using channel'.

Bits 1, 2, 3, 5, 6, 14 and 15 are 'fixed' by the VXI specification and are always read as shown. Writing them has no effect.

Bit 7 is INTEN or Interrupt Enable, specific to this channel. If this bit is a '1', then the appearance of any CSR bit which has a corresponding mask bit set to '1' will cause this channel to assert its interrupt request. This may give rise to VME IRQ4 as we see later.

Bit 8 is the state of the Home Limit switch (provided the outer or Dead Stop Limit is open) - '1' = 'open' or 'hit limit' - read only.

Bit 9 is the same but for the Full Travel Limit - read only.

Bit 10 reflects the state of the drive system's Fault output, which is usually continuously energised to indicate 'OK'; - read only.

Bit 11 is the GO bit, written as '1' to start a movement, written to '0' to 'soft-stop' or ramp down to start/stop speed and stop. This bit is cleared when the step count reaches zero, or a limit is hit, or reset is given.

Bit 12 is RUN, which reflects the state of GO, except that it remains true during ramp down after a soft-stop command.

Bit 13 is MAN or Manual, which indicates that the manual controller has been plugged in. This disables the channel's own step and direction signals, so the host must not attempt to move the channel when this bit is set. While the manual controller is in use, the step counter follows any movements to allow the host to observe any positioning which may be done.

6. Interrupts

The interrupt output of a channel is the logical OR of the AND product of the relevant CSR and Mask Register bits. (see Fig. 3)

The Limit and Fault bits work in the 'true' sense, i.e. when they are both '1', the AND will be true. The RUN bit works in the opposite sense, so that when it goes to '0' i.e. "movement finished", the AND will be true.

The interrupt outputs of all four channels are fed to a prioritiser, which has one output which indicates one or more interrupt sources present, and two more which output a code, indicating the highest numerical source present.

The 'one present' output will cause the VME IRQ4 line to be asserted provided JP5 is fitted and the Global Interrupt Enable (GIE) command has been given. This GIE command is an address only access on any channel at base address plus 1E HEX, and allows us to implement ROA (Release-on-Acknowledge) protocol without having to clear any source or mask bits. A valid Interrupt Acknowledge cancels this GIE, so it will need reissuing after each interrupt service.

When the module receives an IACK cycle with code 100 on address bits A03 to A01 (i.e. a level 4 acknowledge), if no channel has its interrupt output set, then the acknowledge is passed on, as are acknowledge cycles on other levels.

If one or more channels are requesting service, then the two-bit code from the prioritiser is latched and that address used to select the channel which is then instructed to output its Request Register data on D00-D15.

7. Detailed Operating Sequence

Having loaded the Step Register, Profile register and Slow-down Count, the channel is operated as follows (see Figure 4):

The setting of the GO bit in the CSR causes the RUN signal and the High/low speed signal to be set to '1'. The Run signal causes step pulses to be generated and the High/low signal selects Start/stop speed or High speed.

The High/low signal being set to a high level causes the output of a ramp generator to start increasing from 10% of final value towards VCC, which represents High speed.

The output of the ramp generator feeds a voltage to frequency converter consisting of a programmable current source charging a capacitor. A comparator senses when the capacitor voltage reaches 0V and then discharges it, generating a pulse which lasts about 200 nanoseconds. The time the capacitor takes to charge is governed by the voltage from the ramp generator, which is presented to a DAC as a reference. The digital value used by the DAC, which is an 8-bit device, is the lower 8 bits of the profile register. A voltage of 5V from the ramp generator gives about 450,000 steps per second (slightly less than 500,000 because of the discharge time).

The pulse output of the comparator goes to a divide by 10, divide by 100 circuit and also to the counter chip. Inside the counter chip is logic which prevents a counting edge while a read of the count is in progress. Further logic selects which signal is used as the step output: the original comparator output pulse, or one of the two divided signals, depending on the multiplier selected. The selected signal is used to clock the step counter and also a monostable which produces the output step pulse, either 1 or 20 microseconds long.

While the channel is running, the scanning logic is periodically sampling the state of each counter by enabling its outputs onto the data bus and comparing them with a number from the slow-down count memory. This memory contains values loaded by the host appropriate to the speed and ramp rate chosen, and when the top 16 bits of the counter are the same as the slow-down count a clear pulse is sent to the High/low speed flip-flop for the relevant channel and a ramp down to start/stop speed is started.

The number should be calculated so that given the high speed and the ramp rate, the speed will have dropped to start/stop speed by the time the ramp down is complete. When the counter reaches all '0's this will knock down the GO signal.

7.1 Soft Stop, Limits and Fault

Soft Stop

If the GO bit is reset by VME command, the High/low flip-flop is cleared and Ramp Down starts. A comparator associated with the ramp generator then looks for an output voltage just above 'low' voltage, which denotes "bottom of ramp". Until this point is reached, the comparator generates a signal called RUN-ON which allows step pulses to continue up to 'bottom of ramp'.

Limits (see Figure 5)

When a limit switch opens, when travelling in the appropriate direction, a slow-down signal is generated and a ramp down starts. Nothing happens then until the Dead Stop limit opens, which knocks down GO. If the Dead Stop limit is left open, the channel will then stop immediately, without ramping down. Limit and Dead Stop will set the appropriate bit in the Control and Status Register.

Fault

If the Fault input is de-energised, the GO signal is immediately reset and the corresponding Status Register bit set.

NOTE: Encountering a Limit or Fault at high speed obviously means not only that the position of the motor is now unknown, due to the time taken to stop, but also that the Ramp Generator will at that moment be in the wrong state for another move, i.e. it has not returned to the start/stop level. Under these circumstances a wait of 2 seconds should be allowed so that the ramp has a chance to decay.

7.2 Power-on-Reset, Abort etc.

Special consideration should be given to the following:-

Power-on-reset ensures that all logic powers up in the "non-active" state. However, when power is first applied to the module, the integrating capacitors in the ramp generators will all be fully discharged. 4 seconds should be allowed for them all to settle to the correct voltage.

Reset/Abort

A RESET Command, initiated by writing a '1' to bit 0 in the CSR clears all GO flip-flops and resets all LAM Mask bits. It also clears the step counter, to force an immediate "Hard Abort" for the channel. After issuing this command, you should wait at least 2 seconds to allow the ramp generators to settle.

Hard Stop

This is not designed in as a command, but can be useful as a quicker alternative to Soft Stop. Simply write a small number into the step counter, so that in no time - it stops! Zero might work, but the possibility exists that the logic might just be about to take a step and the counter would overflow and start again without 'noticing' the "all '0's" state, so try a value of 5.

8. Programming Information

The following sequence shows how to go about running a stepper motor channel in the VSMC 2256:-

1) Write the number of steps required into the counter, in the recommended sequence.

2) Assemble the Profile Register data and write this.

3) Calculate the slow-down count for the profile, work out the slow-down number to be written and write it.

4) Read the Control and Status Register to check that Fault is not present and also that with your selected direction, you do not have a limit condition.

5) If you have zero in bits 8, 9 and 10, set up the Mask with bits corresponding to Limits and Fault, so that any one of them causing "Stop" will generate Interrupt.

6) Set the GO bit by writing bit 11 to the CSR.

7) Now, if you wish, you can set the Mask bit corresponding to the Absence of RUN, selecting that as an interrupt source.

8) Set the Interrupt Enable bit in the CSR and issue the Global Interrupt Enable command.

9) Either wait for Interrupt or continuously poll the Status Register, looking for absence of RUN or other Fault/Limit status bits.

Clearly if you are not working on interrupts, you do not need to do anything to the Mask register or interrupt enable functions.

Having set the channel in motion, a movement can be curtailed in one of four ways, three of which initiate a controlled or "soft stop"; that is, ramp down to low speed and stop. These three sources are:-

a) Clockwise limit when going clockwise.
b) Counter-clockwise limit when going counter-clockwise.
c) Dataway Soft-Stop by resetting GO bit in CSR.

If either limit is encountered, when travelling in the appropriate direction, the HIGH/LOW speed flip-flop is reset for that channel, and a ramp down to slow speed occurs. This movement at start/stop speed continues until the DEAD STOP limit is encountered. DEAD STOP is normally two outer limit switches wired in series. If DEAD STOP is left open then the motor will stop immediately on encountering a LIMIT.

If the GO bit in the CSR is reset, a ramp down starts, and when almost complete, the motor is stopped. RUN then goes 'false'.

The fourth source of "stop" is External Fault, the de-energising of the Fault input, which causes an immediate Stop without ramp down.

Limits and External Fault all give rise to module Interrupt through the setting of bits in the Status Register, if the corresponding Mask bits are set.

9. Input/Output Interface

All connections to the external drive system are via four 15 way Cannon socket connectors mounted on the front panel.

Step, Direction and Boost outputs are opto isolated, as is the Fault input. Limit inputs are directly coupled through RC networks and Schmitt Trigger logic gates. Encoder inputs are terminated RS422 pairs.

9.1 Connector Pinout

Pin No	Function
1	External Ground (Step, Direction, Fault common)
2	Step pulse output
3	Direction output
4	External VCC (Drive system +5V to energise optos)
5	Dead Stop limit input
6	Home Limit input (CCW)
7	Full Travel limit input (CW)
8	Boost output
9	Incremental Encoder phase A +ve
10	Incremental Encoder phase A -ve
11	Incremental Encoder phase B +ve
12	Incremental Encoder phase B -ve
13	Limits common (module ground - 0V)
14	Module VCC to power encoder (may be linked back to external VCC)
15	External Fault input

9.2 Output Interface - Step, Direction and Boost

+5V

4
o
EX. VCC

560R

2, 3, 8
o
STEP/DIR/BOOST

OPTO-COUPLER
CTR > 50%

o
1
EXT. GND

9.3 Input Interface - Fault

+5V

10K

1K0

4
o
EXT. VCC

0V

CTR > 50%

15
o
EXT. FAULT
SIGNAL

9.4 Input Interface - Limits

+5V

10K

5,6,7
o
LIMIT

100nF

0V

13
o
LIMITS COMMON (GND)

9.5 Interface Signal Levels

Outputs

ON STATE	VSAT < 0.5V at Iout = 2mA	
OFF STATE	VMAX = 15V	Io < 100uA

Inputs

Limits:	Wetting current: 0.5mA	
	Total permitted external resistance: 1K ohm	
Fault:	'On' State	I on > 3.0 mA
	'Off' State	I off < 100 uA

The output interface for step pulse and direction signals is designed to be compatible with Hytec's Stepper Motor Drive System, type SMDS4 and will also be compatible with most other types of translator cards, in particular the PKS Digiplan range CD10, 20 etc., and will produce step pulses as required by them, i.e. 20uS width. Operation of this unit with translators at up to 40 metres distance would be quite satisfactory, bearing in mind the opto isolated "current loop" mode of connection.

9.6 Manual Controller Connector

The pinout of this 16-way IDC connector, mounted just behind the front panel in the centre of the module is as follows:-

Pin	Function
1	Module Ground
2	No connection
3	Step - Channel 1
4	Direction - Channel 1
5	Stop output - Channel 1
6	Step - Channel 2
7	Direction - Channel 2
8	Stop output - Channel 2
9	Step - Channel 3
10	Direction - Channel 3
11	Stop output - Channel 3
12	Step - Channel 4
13	Direction - Channel 4
14	Stop output - Channel 4
15	VCC output
16	/MANUAL input (connect to ground)

9.7 Special Modification - Remote/Manual Changeover

(Customer Request only)

This modification involves the connection of the Boost output of channel 1 to the /MANUAL signal on pin 16 of the Manual connector. Thus through this output of channel 1, the user can control whether the step and direction signals for any channel come from the module's electronics or from the manual controller connector. As mentioned above, switching over involves the disabling of each channel's step and direction outputs.

Ch. 1 Boost = '1': Manual Controller inputs active
Ch. 1 Boost = '0': Channel electronics active.