Broaddown4 User Manual

Issue – 2.00 draft

Kit Contents

You should receive the following items with you Broaddown4 development kit:

1 - Broaddown4 Board
2 - Programming Cable Prog2

Figure 1 - Broaddown4 Board

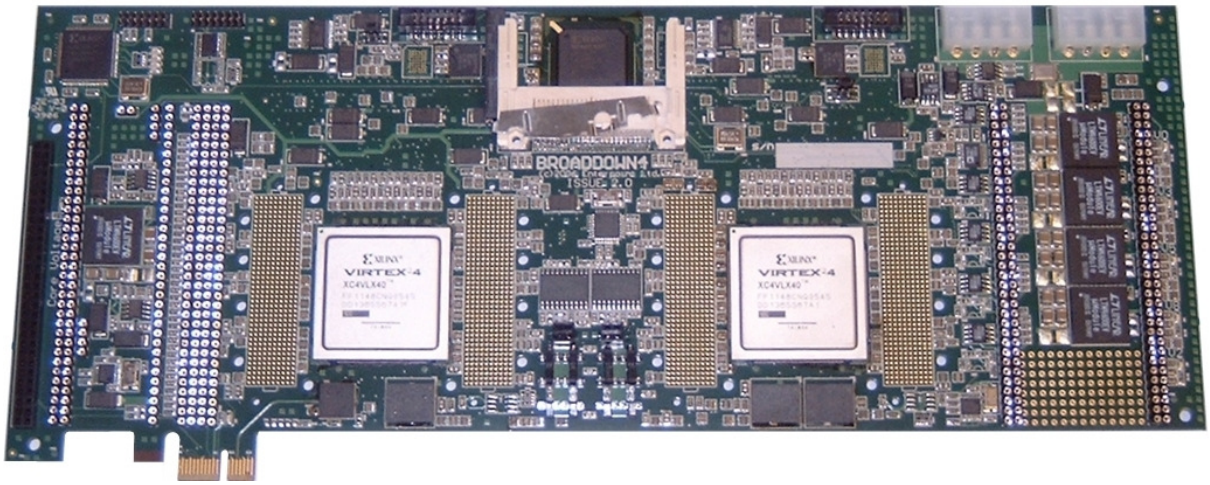
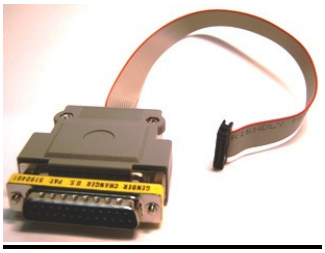


Figure 2 - Prog2 Programming Cable



Foreword

PLEASE READ ALL OF THIS MANUAL BEFORE PLUGGING IN OR POWERING UP YOUR BROADDOWN4. PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN THE MANUAL.

Trademarks

Introduction

Welcome to your Broaddown4 the "Ultimate Virtex-4 Development Board". Broaddown4 is a member of Enterpoint's Moel-Bryn product range and offers a highly flexible approach to prototyping FPGA and System designs.

The aim of this manual is to assist in using the main features of Broaddown4. There are features such as regulator shutdown control and advanced programming features that are beyond the scope of this edition of the manual. Should you have a need to use these features then please contact the support email support@enterpoint.co.uk for detailed instructions to use these advanced features.

Broaddown4 has 2 positions for Virtex-4 devices and the capability to take 2 more FPGAs with Swinyard1, Swinyard2 or future modules fitted to the Moel-Bryn expansion sockets. Each Virtex-4 position can support a choice of 6 device sizes, in 3 speed grades, and in industrial and commercial temperature speed grades giving a massive range of device combinations.

An on-board Spartan-3 FPGA is also available to handle programming structures, power management functions, and CFCARD/SDCARD access.

A wide range of modules are available for Broaddown4 including:

Swinyard1 - Single Virtex-4 LX40-160 or SX55 with DDR2 DRAM,
Swinyard2 - Single Virtex-5 LX55-110 (coming soon),
Ethernet 10/100 Module,
Ethernet 10/100/1000 Module (coming soon),
A/D Converter Module,
Dot Matrix LED Display,
RS232 Module,
RS485 Module,
PS2 Module,
USB I/F Module,
SODIMM Expansion Header - SODIMM used as I/O

We can also offer custom variants of Broaddown4 or modules should you require a function not covered by our current product range. Contact board sales on boardsales@enterpoint.co.uk for your exact requirements.

Block Diagram

The following block diagram shows the main interconnects available on Broaddown4. Individual interfaces are described in more detail elsewhere in this manual.

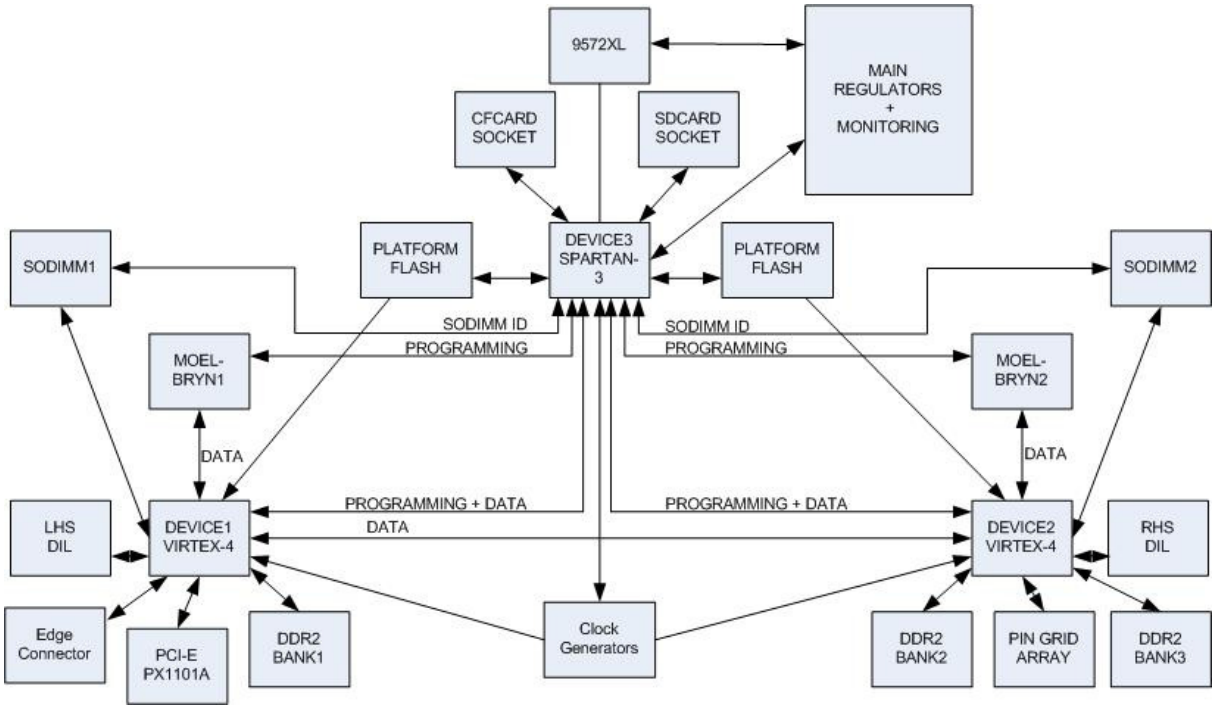


Figure 1 - Simplified Broaddown4 Block Diagram

Feature Finder - Finding Your Way Around

Figure 2 - Front Side of Broaddown4

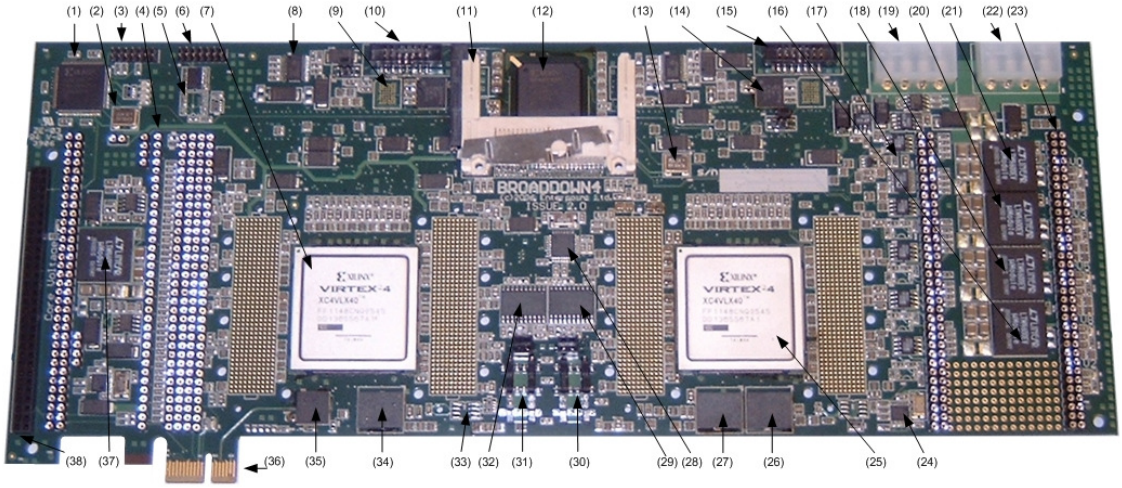
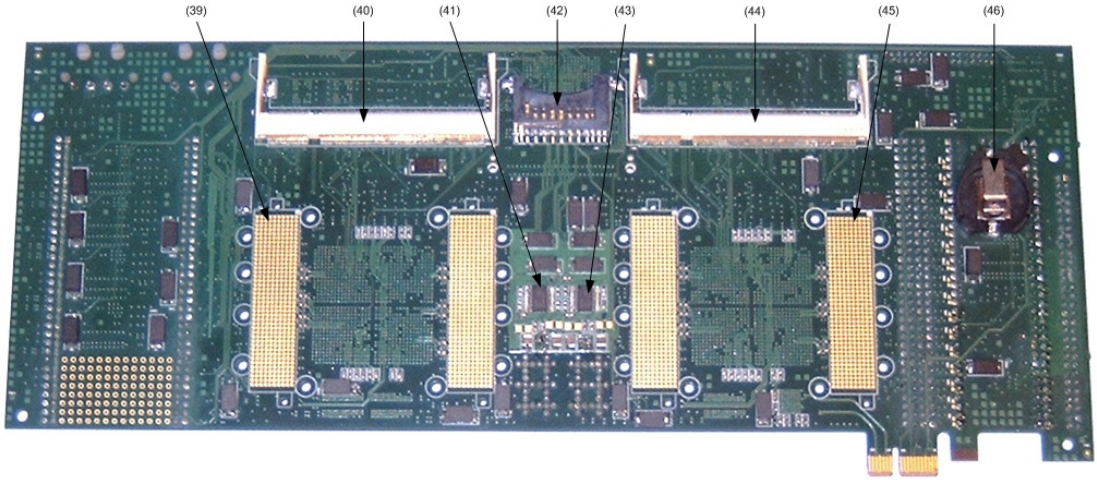


Figure 3 - Back Side of Broaddown4



Features

(1) XC9572XL CPLD
(2) OSCILLATOR
(3) JTAG HEADER
(4) LHS DIL HEADER
(5) PLATFORM FLASH (SPARTAN-3)
(6) JTAG HEADER

(7) VIRTEX-4 FPGA (DEVICE1)
(8) TPS70402 REGULATOR (CPLD + SPARTAN-3)
(9) PLATFORM FLASH (VIRTEX-4 – DEVICE1)
(10) JTAG HEADER
(11) CFCARD SOCKET
(12) SPARTAN-3 FPGA (SERVICES FPGA)
(13) OSCILLATOR
(14) PLATFORM FLASH (DEVICE2)
(15) JTAG HEADER
(16) LT4600 10A REGULATOR (1.2V)
(17) POWER MONITORING
(18) LT4600 10A REGULATOR (1.8V)
(19) POWER INPUT SOCKET1 (5V, 12V)
(20) LT4600 10A REGULATOR (2.5V)
(21) LT4600 10A REGULATOR (3.3V)
(22) POWER INPUT SOCKET2 (5V, 12V)
(23) RHS DIL HEADER
(24) OSCILLATOR
(25) VIRTEX-4 FPGA (DEVICE2)
(26) DDR2 SDRAM BANKx DEVICE2
(27) DDR2 SDRAM BANKx DEVICE2
(28) ICS8442 100-700MHZ CLOCK GENERATOR
(29) CLOCK BUFFER
(30) DEVICE2 I/O BANK VOLTAGE SELECTOR
(31) DEVICE1 I/O BANK VOLTAGE SELECTOR
(32) CLOCK BUFFER
(33) LM86 THERMAL DIODE MEASUREMENT I.C.
(34) DDR2 SDRAM BANKx DEVICE1
(35) NXP PA1101A PCI-E PHY
(36) X1 PCI-E CONNECTOR
(37) LM4600 10A REGULATOR (1.2V or 1.0V to MOEL-BRYN)
(38) EDGE CONNECTOR
(39) MOEL-BRYN SOCKET2
(40) DDR2 SODIMM SOCKET DEVICE2
(41) MOEL-BRYN SOCKET USER REGULATOR1
(42) SDCARD/MMC CARD SOCKET
(43) MOEL-BRYN SOCKET USER REGULATOR2
(44) DDR2 SODIMM SOCKET DEVICE1
(45) MOEL-BRYN SOCKET1
(46) ENCRYPTION KEY BATTERY HOLDER

Getting Started

(1) Please read the whole of this manual before starting with your board.

(2) Connect the Broaddown4 to a computer power supply (un-powered) using the disk drive type power cables that are in most personal computers. The Broaddown4 can be operated either in X1 PCI-E slot, or stand alone on the bench, but does need both a 5V and 12V to be connected for full operation. The PCI-E connector will not supply sufficient power for Broaddown4 to operate and the disk drive power input must always be used even when fitted with a PC.

(3) Switch on your power source.

Device1 Virtex-4 FPGA

Device1 has the following clock connections,

CLOCK CONNECTION	DEVICE1 PIN (p)	DEVICE1 PIN (n)
Cypress CLKA	AG17	~
Cypress CLKB	AH17	~
Cypress CLKC	AH18	~
Cypress CLKX	AG18	~
Cypress PECAL	AF16	AG16
PLL	E16	F16
PLL feedback in	F18	G18
PLL feedback out	K19	J19

FPGA Device1 (7) is one of Xilinx Virtex-4 FPGAs LX40, LX60, LX80, LX100, LX160 or SX55. These devices are available in speed grades -10, -11, -12 and in both commercial and industrial temperature grades. Enterpoint's flexible manufacturing system allows a build to order options such that you can specify size, speed grade and temperatures options of the device that we fit in this socket.

FPGA Device1 has interfaces to PCI-E (35/36), SODIMM1 (44), LHS DIL Header (4), EDGE Connector (38), Moel-Bryn Socket1 (45), Device2 (25), Device3 (12) and DDR2 Bank1 (34). It is supported by clock circuits (28/32) capable of being programmed to deliver clocks up to 700 MHz .

I/O banks 8, 9, 10, 11, 12 and 14 of Device1 can individually be jumper selected to voltages of 1.2V, 1.8V, 2.5V or 3.3V using the bank voltage selector (31).

DCI impedance matching features are available on Banks 1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 13 and 14 of Device1. Each VRN and VRP signal of these banks has 100R resistors wired appropriately.

The PCI-E interface is based on a NXP(Philips) Semiconductors PXA1101A Phy (35) and delivers a X1 PCI-E interface. At the normal clocking rate of 2.5GHz this interface can transfer at up to 2 GBits/s of data which is a significant increase over conventional PCI interfaces. The PCI-E interface, unlike conventional PCI, does not share the bus to/from the PCI-E slot and the loss of bandwidth typically seen in conventional PCI is less prevalent. Structures of the PCI-E implemented in the host personnel computer may restrict the bandwidth of the PCI-E. Discussion of these restrictions is beyond the topic of this manual. The PCI-E logic IP is not included with Broaddown4. A number of providers exist for this IP.

SODIMM1 (44) supports a DDR2 module of up to 2 Gbyte's in a X64 data configuration. This memory socket is capable of running up to TBA MHz and can deliver a memory bandwidth up to TBA GByte/s. If not used for a memory function our optional SODIMM I/O Expansion Module allows the use of the Device1 connections to this socket as general I/O. Enterpoint can also provide custom modules including microprocessors or other functions in the SODIMM format.

The LHS DIL Header (4) provides a simplistic expansion capability. Enterpoint provides a range of modules for this socket including RS232, RS485, ADV7202, IDE, ADC, CODEC, and Displays. Up to 102 I/O are available on this header for use with modules. The header also provides power at 3.3V, 2.5V and optionally 1.8V or 1.2V.

The EDGE Connector (38) provides 48 3V3 capable IO's there is also GND, 3V3 and 2V5 power pick up points with the POWER at the top pin1 and GND spread throughout the connector.

When Device2 (25) is fitted 76 connections to/from Device1 can support up to 38 GBit/s of data transfer between the 2 FPGAs. The interface supports source synchronous interfaces including compensative clock looping on the interface to correct for board level delays. The clocking structure of Broaddown4 also support matched clocking structures to both Device1 and Device2 allowing a simpler hook up between the devices albeit at lower data rates.

CAUTION PLEASE MAKE SURE THE BANK VCCIO's
ARE MATCHED BEFORE POWERING UP BROADDOWN4

Device3 (12) interface offers access to CFCARD, SDCARD facilities. It also can support the programming of Device 2, The Platform Flash, and both Moel-Bryn sockets. To support these facilities suitable designs must be implemented within Device1 and Device3 to support these advanced features. Access to voltage and current monitoring capabilities is also possible through this interface.

DDR2 Bank1 (34) – A single X16 DDR2 device is supported on this interface. This interface is capable of running at TBA MHz offering up to TBA GByte/s data transfer.

Programming of Device1 can be from Platform Flash devices U12 and U13 or by JTAG cable socket J13. The JTAG socket takes a Xilinx standard 14 pin, 2mm, ribbon cable connection.

Alternatively programming can be handled by Device3 which can be loaded with designs to support programming data routed through Device1 – either from PCI-E interface, a source on Moel-Bryn Socket1, a source on the LHS DIL Headers or from some algorithmic function contained in Device1. Device3 can also support programming of data from either CFCARD or SDCARD sockets either from memory cards inserted or via Ethernet, serial or other special network connections host via these sockets.

Please note that reprogramming Device1 may disrupt the function of the PCI-E interface unless special measures are taken to either store the PCI-E configuration data and to restore after re-configuration or to cause a host system reboot.

Enterpoint does not supply IP for the enhanced Device3 programming features with the Broaddown4 but suitable designs can be supplied to your specification at a charge. Contact board sales boardsales@enterpoint.co.uk for a quote and timescale for your specific needs.

Device2

Device2 has the following clock connections,

CLOCK CONNECTION	DEVICE2 PIN (p)	DEVICE2 PIN (n)
Cypress CLKA	AJ17	~
Cypress CLKB	AH17	~
Cypress CLKC	AF18	~
Cypress CLKX	AG18	~
Cypress PECAL	AK18	AK17
PLL	E18	E17
PLL feedback in	G17	G16
PLL feedback out	F18	G18

The Device2 position of Broaddown4 supports one of Xilinx Virtex-4 FPGAs LX40, LX60, LX80, LX100, LX160 or SX55. These devices are available in speed grades -10, -11, -12 and in both commercial and industrial temperature grades. Enterpoint's flexible manufacturing system allows a build to order options such that you can specify size, speed grade and temperatures options of the device that we fit in this socket.

Device2 has interfaces to SODIMM2, RHS DIL Header, Moel-Bryn Socket2, Device1, Device3, DDR2 Bank2, and DDR2 Bank3. It is supported by clock circuits capable of being programmed to deliver clocks up to 700 MHz .

I/O banks 8, 9, 10, 11, 12 and 14 of Device1 can individually be jumper selected to voltages of 1.2V, 1.8V, 2.5V or 3.3V.

DCI impedance matching features are available on Banks 1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 13 and 14 of Device1. Each VRN and VRP signal, of these banks, has 100R resistors wired appropriately.

SODIMM2 supports a DDR2 module of up to 2 GByte in a X64 data configuration. This memory socket is capable of running up to TBA MHz and can deliver a memory bandwidth up to TBA GByte/s. If not used for a memory function our optional SODIMM I/O Expansion Module allows the use of the Device1 connections to this socket as general I/O. Enterpoint can also provide custom modules including microprocessors or other functions in the SODIMM format.

The RHS DIL Header provides a simplistic expansion capability. Enterpoint provides a range of modules for this socket including RS232, RS485, ADV7202, IDE, ADC, CODEC, and Displays. Up to 68 I/O are available on this header for use with modules. The header also provides power at 3.3V. Extra I/Os are available in this header when larger devices are fitted in the Device2 position.

The PIN Grid array allows a greater expansion of the RHS DIL header providing an extra 78 IO's but also extra power support by providing extra GND pins but also 2V5, 1V8 and 1V2, it is Enterpoint's intention that this slot can support another FPGA or microprocessor module for more dedicated purposes.

76 connections to/from Device1 can support up to 38 GBit/s of data transfer between the 2 FPGAs. The interface supports source synchronous interfaces including compensative clock looping on the interface to correct for board level delays. The clocking structure of Broaddown4 also support

matched clocking structures to both Device1 and Device2 allowing a simpler hook up between the devices albeit at lower data rates.

The Device3 interface offers access to CFCARD, SDCARD facilities. It also can support the programming of Device 1, The Platform Flash, and both Moel-Bryn sockets. To support these facilities suitable designs must be implemented within Device2 and Device3 to support these advanced features. Access to voltage and current monitoring capabilities is also possible through this interface.

DDR2 Bank2 – A single X16 DDR2 device is supported on this interface. This interface is capable of running at TBA MHz offering up to TBA GByte/s data transfer.

DDR2 Bank3 – A single X16 DDR2 device is supported on this interface. This interface is capable of running at TBA MHz offering up to TBA GByte/s data transfer.

Programming of Device2 can be from Platform Flash devices U23 and U24 or by JTAG cable socket J20. The JTAG socket takes a Xilinx standard 14 pin, 2mm, ribbon cable connection.

Alternatively programming can be handled by Device3 which can be loaded with designs to support programming data routed through Device1 – either from PCI-E interface, a source on Moel-Bryn Socket1, a source on the LHS DIL Headers or from some algorithmic function contained in Device1. Device3 can also support programming of data from either CFCARD or SDCARD sockets either from memory cards inserted or via Ethernet, serial or other special network connections host via these sockets.

Enterpoint does not supply IP for the enhanced Device3 programming features with the Broaddown4 but suitable designs can be supplied to your specification at a charge. Contact board sales boardsales@enterpoint.co.uk for a quote and timescale for your specific needs.

Device3

Device3 has a dedicated clock which is routed to the device this is notionally 50MHz.

CLOCK SOURCE	SPARTAN PIN
S3_CLOCK	AB12

Device3 (12) is a Xilinx Spartan-3 XC3S1000/1500 FPGA. This device provides a wide range of services to Device1 and Device2. Including CFCARD and SDCARD access, current and voltage measurement of main power rails, and programming of Device1, Device2, Moel-Bryn Socket1 and Moel-Bryn Socket2. To use these services a suitable design for Device3 must be loaded into the Platform Flash (5) supporting these features.

SPARTAN JTAG SIGNALS	DEVICE 1	DEVICE 2
TCK	E2	E21
TMS	D1	D22
TDI	G2	G21
TDO	G6	G22
TDO CONNECTOR	P1	J22
TDO PROM 2	D2	E20
INT_B	C1	C21
PROG_B	D3	E19
BUSY	F4	K21
DONE	E1	G19
CCLK	F3	C22
HSWAP_ENABLE	L5	L22
READ_WRITE	L6	L20
CS_B	K2	L21
ENEXTSEL	G1	F21
REV_SEL0	H5	F19
REV_SEL1	F5	F20
M0	K3	L18
M1	K4	L17
M2	K1	L19
D0	F2	K22
D1	E3	E22
D2	G5	D21
D3	D4	D20
D4	C4	F18
D5	C3	D19
D6	C2	C20
D7	E4	E18
MOEL BRYN SIGNALS		
TCK	M3	Y22
TMS	M1	Y20
TDI	M2	Y21
TDO	N4	W22
INT_B	V2	N19

PROG_B	W3	M21
BUSY	M5	W19
DONE	M6	Y19
CCLK	V1	M22
RESET_N	M4	V19
READ_WRITE	W2	M20
CS_B	Y3	M17
SP1	N3	W21
SP2	N2	V22
DOUT	N1	W20
M0	U5	U20
M1	W1	M19
M2	T4	U21
M3	Y1	M18
DIN	T6	V21
D1	T5	V20
D2	U4	T22
D3	T1	N21
D4	U3	T21
D5	U2	N22
D6	T2	U19
D7	V3	N20
CARD ID1	L4	K20
CARD ID2	L1	K19
CARD ID3	V5	G17
CARD ID4	W4	G18
CARD ID5	Y2	R18
CARD ID6	V4	T18
CARD ID7	L2	U18
CARD ID8	L3	T17

CFCARD and SDCARD sockets can be used to host memory cards or other interfaces such as Ethernet, USB, RS232, RS485 to name a few possibilities. The data delivered can be used for programming of any of Device1, Device2, Moel-Bryn socket1 and Moel-Bryn Socket2 or can be used as general data to support embedded microprocessors or other functions needing substantial data.

The Device3 pins supporting the CFCARD are as follows:

FLASH MEMORY PIN	SPARTAN PIN
A0	AA8
A1	W9
A2	AA10
A3	Y10
A4	U7
A5	V8
A6	V10
A7	U13
A8	V13

A9	AB13
A10	V14
D0	U6
D1	W6
D2	AA6
D3	W18
D4	Y17
D5	V16
D6	Y16
D7	U16
D8	Y6
D9	W5
D10	AA5
D11	Y18
D12	AA17
D13	W16
D14	U17
D15	AA15
CD1	V18
CD2	AA4
WP	Y5
WE	U14
OE	Y13
CE1	W17
CE2	V17
BVD1	V6
BVD2	V7
REG	V9
INPACT	AA9
RESET	AA11
WAIT	AB10
VS1	W14
VS2	W8
CSEL	U10
REDY	U12
IORD	AA13
IOWR	W13

The Device3 pins supporting the MMC/SDCARD are as follows:

MULTI-MEDIA CARD PIN	SPARTAN PIN
PIN1	AB18
PIN2	AB15
PIN3	AB14
PIN4	AB11
PIN5	AB9
PIN6	AB8
PIN7	AB5

PIN8	AB4
PIN9	AA18
WRITE PROTECT1	Y4
WRITE PROTECT2	AA3
CARD DETECT1	AB20
CARD DETECT2	AA20

Device3 also hosts the serial SPI interface controlling the ADC AD7927 which measures voltage drops over a 5mΩ on the main 3.3V, 2,5V, 1.8V and 1.2V power rails of the board**.** It is possible to build a current profile for operation of the board and store the data on a memory card or using the sockets as a network connection remotely on a hard drive etc.

ADC CHIP	SPARTAN PIN
CS	A5
SCLK	A9
DOUT	A11
DIN	A8

Device3 hosts the serial interface to control the 3 clock generators on board, the two dedicated cypress CY22394 parts that provide 4 clocks to each individual Virtex4. The third clock generator ICS8442 is capable of delivering 2x700MHz LVDS clock signals, these signals are fed into two ICS8745 PLL's, which are controlled by Device3, and should allow synchronisation of both Virtex4 devices up to TBA MHz.

ICS8442 PIN	SPARTAN PIN
N0	F9
N1	E9
M0	C11
M1	D11
M2	D10
M3	E11
M4	F11
M5	D9
M6	C10
M7	F10
M8	E10
PLOAD	F12
SDATA	F13
SLOAD	E13
TCLK	E15
XSEL	D14
MR	D12
VCOSEL	E12
SCLOCK	C12

ICS8745 PIN	S3 PIN FOR DEVICE1	S3 PIN FOR DEVICE2
PLL_SEL	B12	E16
SEL0	C13	E17

SEL1	D13	F17
SEL2	D5	A14
SEL3	F6	E14
MR	B13	F16

CY22394 PIN	S3 PIN FOR DEVICE1	S3 PIN FOR DEVICE2
SHUTDOWN	E7	C18
SUSPEND	D7	D17
SCLK	E6	D18
SDAT	D6	C19

Device3 also has control of the temperature diode sensor IC, monitoring each Virtex4's temperature diode embedded in each device with the alert signals routed to Device3 and the Alarm signal routed to the CPLD.

LM86 PIN	S3 PIN FOR DEVICE1	S3 PIN FOR DEVICE2
CLK	C5	B17
DATA	F7	C17
ALERT	B8	D15
ALARM	CPLD 87	CPLD 89

Device3 also has support busses that can be programmed to do any function the user wishes, there is a 20bit bus between the CPLD and Device3 the intention is that this bus would be used to route regulator control and PCIE jtag pins through to Device3, a 10bit bus between Device1 and Device2 has also been routed the intention of this bus is as a way for Device1 to control the clock generation and higher functions supported by Device3.

SPARTAN VIRTEX BUS	SPARTAN PIN	VITREX PIN
SB5	G3	V27
SB6	G4	W27
SB7	J4	U31
SB8	H4	U30
SB9	N6	U27
SB10	N5	U26
SB25	R5	U23
SB26	P6	T23
SB27	H1	V32
SB28	H2	W32

SPARTAN TO CPLD BUS	SPARTAN PIN	CPLD PIN
1	A4	16
2	B6	13
3	B18	18
4	A15	20
5	C6	14
6	B5	15
7	B14	25

8	B4	17
9	A12	28
10	B15	23
11	B20	33
12	A19	36
13	A13	27
14	B11	29
15	B19	39
16	A10	30
17	A18	40
18	B9	3
19	B10	99
20	C7	4

Other functions that are supported by Device3 include regulator control for the TPS70402 regulator's onboard the enable and reset function of these devices are routed to Device3.

TPS70402 USER RAIL	SPARTAN PIN
REG1 EN1	V12
REG1 EN2	Y12
REG2 EN1	W10
REG2 EN2	W11

Broaddown4 Features

Picture - power structure.

Power Inputs

Broaddown4 takes current from the Disk Drive Connectors (19/22) at the top right of the card. Depending on your card configuration and designs loaded into Devices1/2/3 you may need either a single feed in or a dual feed in. Each connector is each capable of carrying 5 amps of 5V input. The power supplies on the PCI-E edge connector are not used as they are inadequate to operate Broaddown4.

The principal input to Broaddown4 is the 5V input. The 12V input is only used to provide a voltage for N-Channel MOSFET gate enhancement that are used in the power protection and monitoring circuits and the Moel-bryn connectors 12v rail.

Main Power Regulators

Broaddown4 uses 4 Linear Technology LTM4600 switching regulators to deliver current to the main 3.3V, 2.5V, 1.8V and 1.2V rails. Each of these rails is capable of supporting 10 amps in the basic configuration of Broaddown4. Further current capability may be possible by special build of Broaddown4. A further LTM4600 supports the core voltages used on the Moel-Bryn sockets and can support Swinyard1 (Virtex-4) and Swinyard2 (Virtex-5) core voltages of 1.2V and 1V respectively to a further 10 amps capability by a resistor fit change.

Secondary Voltage Regulators

Two TPS70402 regulators U8 and U19 provide power for the Spartan-3 FPGA, XC9572XL, power management and programming circuits.

User Voltage Regulators

TPS70402 regulators U46 and U47 provide 4 user settable rails that are available to use on the Moel-Bryn expansion modules. Two of these rails have 1 amp capability. The remaining two rails can support 2 amps each.

Negative Voltage Regulators

Regulators U26 and U39 provide -5V and -12V supplies of 100mA capability to the Moel-Bryn sockets. These supplies are not highly regulated and a linear regulator should post-regulate if high accuracy is required when these rails are used.

PUSH-PULL Voltage Regulators

Regulators U3 and U5 provide 1.25V and 0.9V supplies to the Moel-Bryn sockets, Sodimm sockets, Virtex4 devices as bank references and PX1101A PCIe Phillips phy. These supplies are essential in the operation of the DDR memory and Phillips phy interfaces and as such should not be tampered with to change voltage output levels.

Power Pickups

Broaddown4 has power pickup points that can be picked up from the LHS DIL Header, RHS DIL Header, Bank Voltage Selector J17 and Bank Voltage Selector J18. Please see the relevant sections for more details on these features.

Also available on Broaddown4 is two 4 pin headers that provide complete core voltage power rails enabling the possibility of Virtex5 modules to be fitted to the LHS DIL headers also available is the encryption key battery voltage please see figure 5.

The voltages that are available on power pickup points on broaddown4 are as in the following table.

Voltage	Header	Note
12V	Moel-bryn	
5V	Moel-bryn	
3.3V	Moel-bryn, PIN grid array, LHS DIL header by selection and VCCIO headers J17/J18.	On board Virtex4 IO voltage's 10A max
2.5V	Moel-bryn, PIN grid array, LHS DIL header by selection and VCCIO headers J17/J18.	On board Virtex4 IO and VCCAUX voltage's 10A max
1.8V	Moel-bryn, PIN grid array, LHS DIL header by selection and VCCIO headers J17/J18.	On board Virtex4 IO and DDR voltage's 10A max
1.2V	Moel-bryn, PIN grid array, LHS DIL header by selection and VCCIO headers J17/J18.	On board Virtex4 core voltage's 10A max
CORE	Moel-bryn and 4 pin headers.	10A max for Virtex4/5 support in the Moel-bryn expansion slots.
User1 Rail	Moel-bryn.	1A max
User2 Rail	Moel-bryn.	2A max
User3 Rail	Moel-bryn.	1A max
User4 Rail	Moel-bryn.	2Amax

Please note secondary voltage rails on Device3's power circuit are not available at any power pick up points.

Selecting FPGA Bank (Vcciox)

Broaddown4 divides the variable voltage I/O pins of the fitted Virtex4's into 6 banks for Device1 and 5 banks for Device2. The FPGA does natively support 14 banks however on Broaddown4 banks 1+5+6 on both Devices share their Vccio's set to 1.8V for Sodimm operation. Bank 7 on Device1 and Banks 7+8 also share there Vccio's set to 1.8V for dedicated DDR2 IC operation. Bank 13 on Device1 and Bank 14 on Device2 share there Vccio's set to 2.5V for LVDS communication between each device. Also the Two clock banks per device are fixed to 3.3V and 2.5V. The key to voltage selection and hence supported I/O standards is headers J17 and J18. From these headers the variable IO bank voltages can individually be selected from 3.3V, 2.5V, 1.8V and 1.2V. Please note that the headers are **pinned out the same way** for each output power rail. The pin-out chosen makes it unlikely that input power rails can be shorted together using a single jumper. The header layouts are shown bellow.

DEVICE 1 VCCIO SELECTION

	VD1V8			VD1V8	
VD1V2	BANK11	VD3V3	VD3V3	BANK12	VD1V2
	VD2V5			VD2V5	
	VD2V5			VD2V5	
VD1V2	BANK10	VD3V3	VD3V3	BANK9	VD1V2
	VD1V8			VD1V8	
	VD1V8			VD1V8	
VD1V2	BANK14	VD3V3	VD3V3	BANK8	VD1V2
	VD2V5			VD2V5	

DEVICE 2 VCCIO SELECTION

	VD1V8			VD1V8	
VD1V2	n.c.	VD3V3	VD3V3	BANK12	VD1V2
	VD2V5			VD2V5	
	VD2V5			VD2V5	
VD1V2	BANK10	VD3V3	VD3V3	BANK9	VD1V2
	VD1V8			VD1V8	
	VD1V8			VD1V8	
VD1V2	BANK11	VD3V3	VD3V3	BANK13	VD1V2
	VD2V5			VD2V5	

CAUTION: BANKS 11, 9 of Device1 and BANKS 12, 10 of Device2 are connected together and need to be set to the same voltage.

Also Note that BANK13 of Device1 and BANK14 of Device2 are connected to 2.5volts and connect to each other for devices other than LX40, LX60 and SX55 devices.

Programming Broaddown4

Figure 4 - JTAG Connector Positions

The programming of the FPGA, CPLD and Platform Flash parts on Broaddown4 is achieved using JTAG chains. Principally it is anticipated that a JTAG cable will be used in conjunction with Xilinx ISE software although other alternatives do exist including self re-programming.

There are 4 JTAG chains on Broaddown4. The first chain allows the programming of the CPLD. Normally users will not need to reprogram this device. However to use special power sequencing and/or advanced programming features reprogramming of these devices may be needed. If you are considering using these features you should study the Broaddown4 circuits and understand the full functionality before modifying the CPLD programming.

The second JTAG chain allows the programming of the Spartan-3 and Platform Flash devices for the Spartan device.

The Third and Forth JTAG chain allows programming of the Virtex4, Platform Flash and Moel-bryn connectors also controllability can be taken over by the Spartan3 fitted onboard. However to use the advanced programming features reprogramming of the Spartan3 may be needed. If you are considering using these features you should study the Broaddown4 circuits and understand the full functionality before modifying the Spartan3 programming.

Each JTAG connector has a layout is as follows:

3.3V	TMS	TCK	TDO	TDI	n.c.	n.c.
GND	GND	GND	GND	GND	GND	GND

The CPLD chain looks like this:

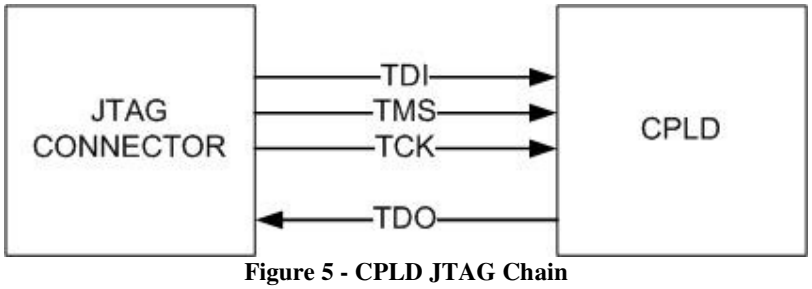


Figure 5 - CPLD JTAG Chain

The Spartan3 FPGA JTAG chain looks like this:

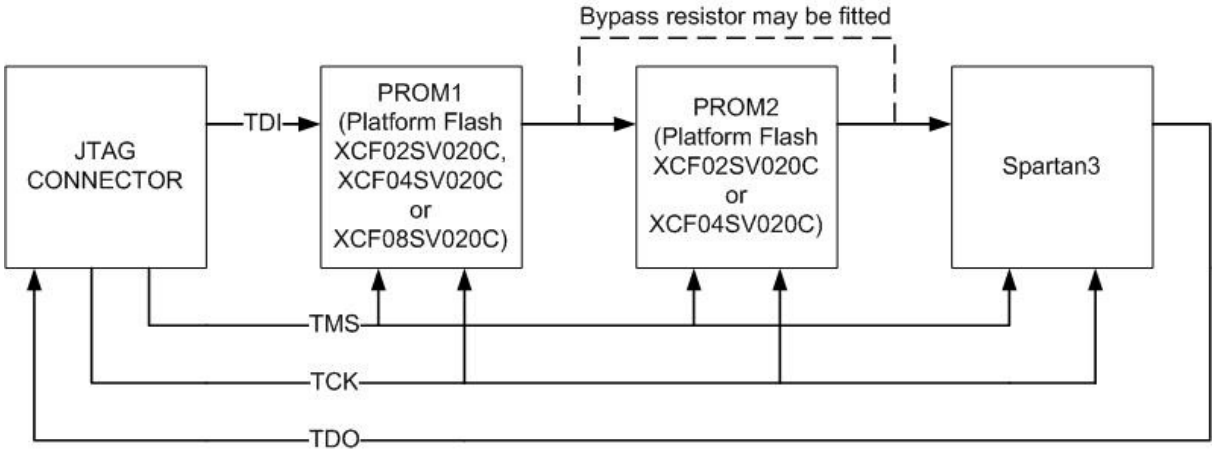


Figure 6 - SPARTAN FPGA JTAG Chain

The Virtex4 FPGA JTAG chain looks like this in its simplest form:

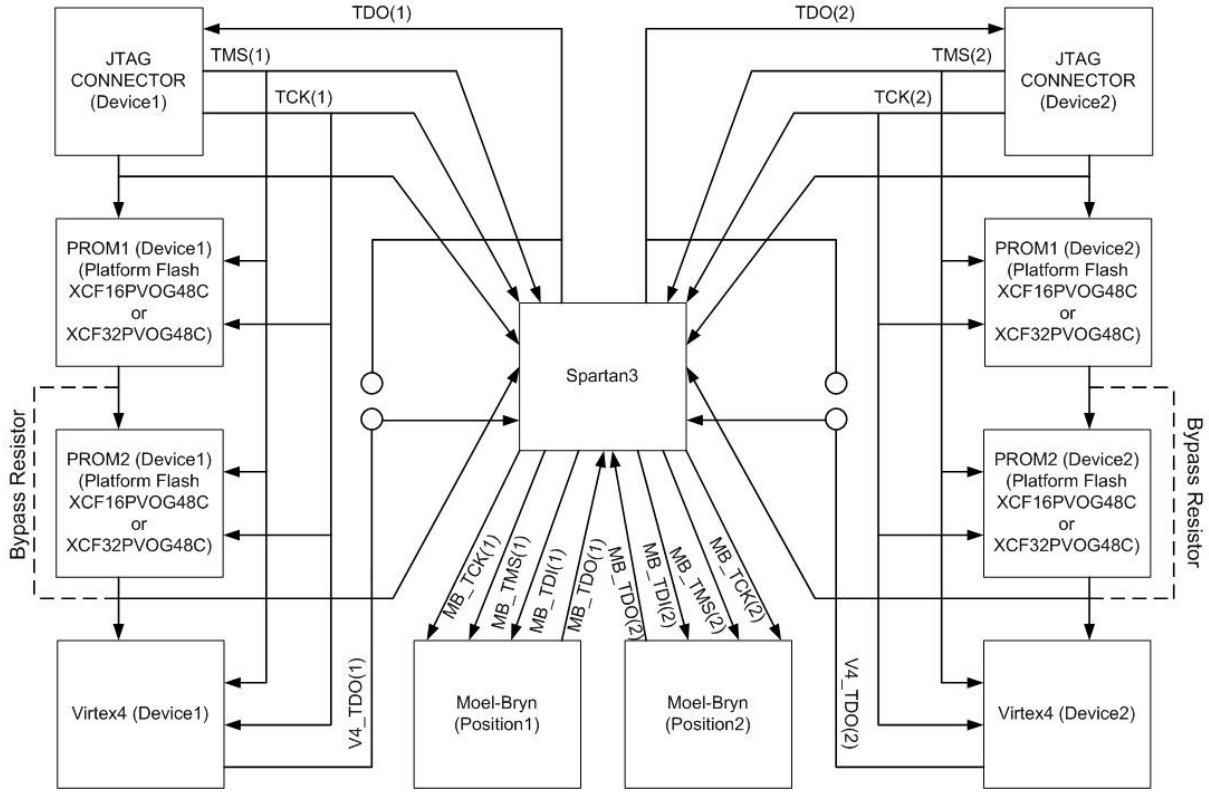


Figure 9 – VIRTEX FPGA JTAG Chain

If a Moel-Bryn module supporting a JTAG programmable device is fitted then the jumpers J16 and J22 can be removed.

Programming of the Spartan3 FPGA and Virtex4 FPGA can be achieved by direct JTAG programming or from the Platform Flash memory/s. By default the Virtex4 devices are programmed

from the Platform Flash memories at power up. However the default configuration mode can be altered by reprogramming the Spartan3 on Broaddown4. Direct JTAG programming is volatile and the FPGA will lose its configuration every time the board power is cycled. From sustained use of FPGA design programming the design into the Platform Flash memory is recommended. Generation of suitable Platform Flash content files and control of the JTAG chain can be achieved using the XILINX ISE tool IMPACT.

Primary Voltage Regulators

Figure10 - Primary Power Regulator Features

Broaddown4 has a power backbone based on four LM4600 integrated switching regulators. These regulators are capable of delivering 10 amps. The structure of these four regulators is a non-chain so that effectively all the current taken out of the system passes through the 5.0V rail and. Therefore the absolute maximum current that can be delivered into Broaddown4 is limited by the amount supplied to the board.

The output voltages of the regulators are 3.3V, 2.5V, 1.8V and 1.2V. Practically the current delivered by the board is unlimited with the only limitation being that a max of 10 amps per rail can be delivered.

On each rail a 5mΩ power resistor is in line with the supply to the board with an Op-amp circuit over it this allows measurement of individual currents on each rail including the input 5 volts via an ADC controlled by the Spartan3. This features primary objective is to act as a fault condition and power monitoring circuit enabling controlled and emergency shutdown features, by the CPLD on board each rails over and under voltage condition are monitored to allow decision making on short circuit or over current sourcing is occurring.

The secondary use of this feature is as current and power profiling of designs this information can be directly passed through the PCI_E interface or stored through to the CF or SD card for reading later on in a PC.

Secondary Power Regulators

Figure 11 - Secondary Power Regulators

Broaddown4 has four secondary regulators. These regulators are derived from twin regulator devices TPS70402. These regulators will deliver 1 or 2 amps depending on which section of the TPS70402 is being used. The following voltage rails are derived using these regulators.

VOLTAGE	DEVICE	CURRENT RATING	O/P SERIES RESISTOR
Vccaux (SPARTAN3)	U19	2 AMP	YES
Vccint (SPARTAN3)	U8	1 AMP	YES
3.3V (SPARTAN3 IO)	U19	2 AMP	YES
1.8V (NOT USED)	U8	1 AMP	YES

Current measurement can be achieved by replacing a zero resistor with a low ohm sense resistor where the above table indicates a suitable resistor position.

As these regulators are variable regulators rail voltages can be modified to suit particular voltage applications if necessary. The minimum that the TPS70402 will regulate to is 1.22V.

Negative Rail Generation

Broaddown4 has 2 inverting LT1054 charge pump regulators fitted. Each regulator will deliver about 100 mA. The regulators are operated in simple inverting mode and do not offer much in regulation in this mode. If you need tight regulation, or low noise, you should fit a post regulator to improve these parameters.

The LT1054 regulators will deliver the approximate inverse of their input voltages. The inputs to these regulators are the 5.0V and 12.0V supplied from the disk drive connector and are fed directly to the Moel-Bryn connectors.

Figure 12 - Negative Voltage Regulators Input Selection (J31 / J32)

SODIMM Socket

Figure 73 - SODIMM Features

WARNING – DO NOT INSERT A DDR1 SODIMM INTO THE DDR2 SODIMM SOCKET. IT WILL SHORT OUT THE POWER SUPPLIES.

THE SODIMM SOCKETS ON BROADDOWN4 ARE PINNED OUT TO XILINX MIG1.5 SPECIFICATION. THE DETAILS IN THIS SECTION ARE FOR YOUR INFORMATION ONLY.

Broaddown4 has two DDR2 SODIMM socket allowing the fitting of I/O expansion modules to utilise the IO if memory is not inserted.

Figure 84 - SODIMM I/O Module

The SODIMM I/O Module can also be used to support loopback testing of the SODIMM Socket when used in conjunction with a suitable test build loaded into the Virtex4 FPGA.

The pin-out of the sodimm sockets are as follows,

SODIMM1/2	FPGA DEVICE 1 PIN	FPGA DEVICE 2 PIN
DQ0	B23	B23
DQ1	A23	A23
DQ2	A26	A26
DQ3	B26	B26
DQ4	A24	A24
DQ5	A25	A25
DQ6	G25	G25
DQ7	C23	C23
DQ8	F25	F25
DQ9	F26	F26
DQ10	D24	D24
DQ11	D25	D25
DQ12	D26	D26
DQ13	E2	E2
DQ14	F24	F24
DQ15	E24	E24
DQ16	G23	G23
DQ17	H24	H24
DQ18	A28	A28

DQ19	A29	A29
DQ20	B25	B25
DQ21	C25	C25
DQ22	J25	J25
DQ23	K26	K26
DQ24	B22	B22
DQ25	A30	A30
DQ26	B30	B30
DQ27	K24	K24
DQ28	J24	J24
DQ29	C29	C29
DQ30	B21	B21
DQ31	A21	A21
DQ32	J20	J20
DQ33	L19	L19
DQ34	H15	H15
DQ35	G21	G21
DQ36	H20	H20
DQ37	G15	G15
DQ38	F14	F14
DQ39	F21	F21
DQ40	A15	A15
DQ41	B15	B15
DQ42	N19	N19
DQ43	N18	N18
DQ44	L15	L15
DQ45	L14	L14
DQ46	E21	E21
DQ47	D21	D21
DQ48	D12	D12
DQ49	C12	C12
DQ50	B10	B10
DQ51	C10	C10
DQ52	A11	A11
DQ53	B11	B11
DQ54	C9	C9
DQ55	G12	G12
DQ56	F10	F10
DQ57	G10	G10
DQ58	D11	D11
DQ59	D10	D10
DQ60	A8	A8
DQ61	B8	B8
DQ62	E11	E11
DQ63	F11	F11
DQS0	B27	B27
DQS_N0	C27	C27
DQS1	F23	F23

DQS_N1	E23	E23
DQS2	A31	A31
DQS_N2	B31	B31
DQS3	B28	B28
DQS_N3	C28	C28
DQS4	B20	B20
DQS_N4	A20	A20
DQS5	F13	F13
DQS_N5	G13	G13
DQS6	H10	H10
DQS_N6	H9	H9
DQS7	B13	B13
DQS_N7	B12	B12
DM0	C24	C24
DM1	D27	D27
DM2	C22	C22
DM3	E28	E28
DM4	F20	F20
DM5	J14	J14
DM6	G11	G11
DM7	A6	A6
CKE0	A14	A14
CKE1	A13	A13
CK0	D30	D30
CK_N0	D31	D31
CK1	G27	G27
CK_N1	G28	G28
A0	H22	H22
A1	H13	H13
A2	H14	H14
A3	M20	M20
A4	N20	N20
A5	F31	F31
A6	E31	E31
A7	B33	B33
A8	B32	B32
A9	L26	L26
A10	L25	L25
A11	F29	F29
A12	F28	F28
A13	E12	E12
A14	C18	C18
A15	C19	C19
BA0	H12	H12
BA1	J21	J21
BA2	B5	B5
RAS_N	J11	J11
CAS_N	B7	B7

WE_N	C7	C7
ODT0	F8	F8
ODT1	G8	G8
CS0_N	A10	A10
CS1_N	A9	A9
SDA	SPARTAN B7	SPARTAN C16
SCL	SPARTAN A7	SPARTAN D16
SA0	SPARTAN E8	SPARTAN A16
SA1	SPARTAN D8	SPARTAN B16

The SODIMM Socket is keyed and will only support DDR2 style SODIMM modules. DDR2 SODIMM module pin-out is incompatible with DDR1 SODIMM pin-out. Do not remove the mechanical key to allow DDR1 modules to fit. Notionally these connectors only support 1.8V and as such all-relevant bank Vccio's are wired to 1.8V.

Additionally when not used as a memory interface do not exceed the Virtex4 maximum I/O voltage for 1.8V IO signalling i.e. 2.5V as this violates the catching diode specification and damage to the FPGA will ensue.

When used for a DDR2 memory function the following signal features are available:

(1) 64 bit data
(2) A0 TO A13 address
(3) BA0 to BA2 bank address
(4) DM0 to DM3
(5) CK0, CK1
(6) CKE0, CKE1
(7) RAS
(8) CAS
(9) CS0, CS1

Peak data rates of 200 MHz (100 MHz clock) are to be expected.

SODIMM configuration prom reading is supported indirectly via the Spartan3 and can be accessed by the virtex4 FPGA via the Spartan3 Expansion Bus. This feature is not automatically enabled when Broaddown4 is delivered and you should contact support support@enterpoint.co.uk if this feature is needed or relevant programming is required.

The LP2996 regulator will provide a +/- 1.5 amp termination voltage at half the 1.8V main voltage input, this is used by the Virtex4 for termination.

PCI-E Interface

Figure 9 - Broaddown4 PCI Interface Features

An LED Just above the PCI-E interface has been added to show indication when plugged into a PCI-E slot correctly.

For this interface to work as a PCI-E interface you will need to buy, or design, a suitable FPGA PCI-E logic circuit or IP core**. Broaddown4 will not be supplied with any PCI-E IP core to use**. A 30 day trial version of Xilinx PIPEX core can be downloaded for the Xilinx Internet website.

PCI EXPRESS SIGNAL	DEVICE1 PIN
TX DATA K	AL18
TX DATA 0	AM20
TX DATA 1	AL20
TX DATA 2	AD21
TX DATA 3	AB16
TX DATA 4	AJ21
TX DATA 5	AB17
TX DATA 6	AG20
TX DATA 7	AH20
RX DATA K	AK16
RX DATA 0	AM17
RX DATA 1	AM16
RX DATA 2	AL16
RX DATA 3	AM15
RX DATA 4	AF15
RX DATA 5	AG15
RX DATA 6	AL14
RX DATA 7	AL15
TX CLK	AL19
RX CLK	AP20
RX STATUS 0	AG22
RX STATUS 1	AH22
RX STATUS 2	AJ22
RX IDLE	AH14
RX VALID	AN20
RX DET LOOPB	AB15
RX POL	AD16
PHY STATUS	AJ20
POWER DOWN 0	AC15
POWER DOWN 1	AM18
RESET_N	AB18
TX COMP	AD17
TX IDLE	AJ15

Broaddown4 supports a X1 implementation of PCI-E.

If you don't want to use the PCI-E Edge Connector for PCI-E and run Broaddown4 standalone you can, as the Disk Drive Power Connector is the main power supply to the board.

All the other Signals such as the JTAG, and SMB bus are routed to the CPLD and can be pushed onto the Spartan3 with an appropriate build programmed into the CPLD.

PCI EXPRESS SIGNAL	CPLD PIN
SMCLK	94
SMDATA	95
WAKE	97
POWERGOOD	6
TRST#	8
TCK	9
TDO	11
TDI	10
TMS	12

Right Hand Side DIL Header

The RHS DIL Header provides a simple mechanical and electrical interface for add-on modules. The connectors on this header are on a 0.1 inch, 2.54 mm, pitch and allow either custom modules, stripboard or even dil style components (3.3V only) to be fitted. The RHS DIL Header supports modules and components with horizontal lead pitches of 1.6 inch pitches.

The header has a permanent positive power row on the left of the right column. It also has a Gnd (0V) row to the right of left column of the header.

The RHS DIL Power Rail is fixed to 3.3V, 2.5V,1.2V or 1.8V can be picked up from the pin grid array. It is advised that voltages outside 0 to 3.3V are not used unless special precautions are taken to protect Virtex4 I/Os. The Virtex4 has an absolute input voltage rating of 4.05V. The pin-out of the selection header is as follows:

The Virtex4 pin-out connections are shown in the following table as is LVDS pair support.

D2 PIN	VOLTAGE		VOLTAGE	D2 PIN	PIN #
C34	GND		VD3V3	D32	1
C33	GND		VD3V3	C32	2
E34	GND		VD3V3	E33	3
D34	GND		VD3V3	E32	4
G33	GND		VD3V3	G31	5
G32	GND		VD3V3	G30	6
H30	GND		VD3V3	F34	7
H29	GND		VD3V3	F33	8
J30	GND		VD3V3	H34	9
J29	GND		VD3V3	H33	10
K33	GND		VD3V3	J32	11
K32	GND		VD3V3	H32	12
L31	GND		VD3V3	K34	13
L30	GND		VD3V3	J34	14
M33	GND		VD3V3	K29	15
M32	GND		VD3V3	K28	16
N30	GND		VD3V3	AC27	17
N29	GND		VD3V3	AD27	18
N12	GND		VD3V3	AD32	19
AD30	GND		VD3V3	AE32	20
AE34	GND		VD3V3	AE31	21
AE33	GND		VD3V3	AF31	22
AF34	GND		VD3V3	AF30	23
AF33	GND		VD3V3	AF29	24
AH33	GND		VD3V3	AG31	25
AH32	GND		VD3V3	AG30	26
AH30	GND		VD3V3	AH34	27
AJ30	GND		VD3V3	AJ34	28
AK32	GND		VD3V3	AJ32	29
AK31	GND		VD3V3	AJ31	30
AL34	GND		VD3V3	AK34	31

AL33	GND		VD3V3	AK33	32
AM33	GND		VD3V3	AL31	33
AM32	GND		VD3V3	AM31	34

The signals marked as LVDS_P and LVDS_N are routed such that the trace lengths approximately match and skew is minimised within pair. Adjacent LVDS_P and LVDS_N form the matched pair at the RHS DIL Header and the Virtex4 FPGA. For example V11 and W11 form one pair.

LVDS pairs have no termination onboard and termination should be designed into any module plugged into the RHS DIL header for correct LVDS communication.

When not used as LVDS signals can be used as general I/O subject to Bank Voltage Vccio's setting and standards mixture.

LHS DIL Header + EDGE Connector

The LHS DIL Header provides a simple mechanical and electrical interface for add-on modules. The connectors on this header are on a 0.1 inch, 2.54 mm, pitch and allow either custom modules, stripboard or even dil style components (3.3V only) to be fitted. The LHS DIL Header supports modules and components with horizontal lead pitches of 0.6 and 1.6 inch pitches.

The header has a permanent positive 3.3V power row to the left of the right column followed by a permanent 2.5V and resistor selectable 1.8v or 1.2V. It also has Gnd (0V) to the right of left column of the header. It is also possible to connect any other from pin 4 down ion the 0.6 column to the Gnd (0V) Rail by means of solder bridges on the back of the Broaddown4. If any of the solder bridges are made then the user should ensure that the Virtex4 FPGA does not attempt to drive the relevant pin. Failure to do so may damage the Broaddown4.

The forth Power Rail (row just bellow J10 silk screen indicator) can be selected by resistor to 1.8V or 1.2V. Alternatively other supplies can be connected to the selector by flying wire. It is advised that the native resistor R21 connecting the 1.2V is removed before attempting anything, as a short will be made.

The LHS DIL Header Virtex4 pin-out connections are shown in the following table, as is LVDS pair support.

D1 PIN	VOLTAGE		D1 PIN		VOLTAGE	VOLTAGE	VOLTAGE	D1 PIN	PIN #
C3	GND		D2		VD1V2/VD1V8	VD2V5	VD3V3	E4	1
C4	GND		C2		VD1V2/VD1V8	VD2V5	VD3V3	D4	2
E2	GND		F3		VD1V2/VD1V8	VD2V5	VD3V3	G2	3
E3	GND		F4		VD1V2/VD1V8	VD2V5	VD3V3	G3	4
E1	GND		J5		VD1V2/VD1V8	VD2V5	VD3V3	H2	5
D1	GND		J6		VD1V2/VD1V8	VD2V5	VD3V3	H3	6
G5	GND		H4		VD1V2/VD1V8	VD2V5	VD3V3	K4	7
F5	GND		H5		VD1V2/VD1V8	VD2V5	VD3V3	J4	8
L6	GND		L4		VD1V2/VD1V8	VD2V5	VD3V3	N7	9
K6	GND		L5		VD1V2/VD1V8	VD2V5	VD3V3	M7	10
M1	GND		K1		VD1V2/VD1V8	VD2V5	VD3V3	G1	11
L1	GND		K2		VD1V2/VD1V8	VD2V5	VD3V3	F1	12
N12	GND		M8		VD1V2/VD1V8	VD2V5	VD3V3	L9	13
N13	GND		L8		VD1V2/VD1V8	VD2V5	VD3V3	M10	14
L3	GND		P5		VD1V2/VD1V8	VD2V5	VD3V3	P9	15
K3	GND		N5		VD1V2/VD1V8	VD2V5	VD3V3	P10	16
AD5	GND		M2		VD1V2/VD1V8	VD2V5	VD3V3	M5	17
AD6	GND		M3		VD1V2/VD1V8	VD2V5	VD3V3	M6	18
AE1	GND		AC2		VD1V2/VD1V8	VD2V5	VD3V3	AB12	19
AF1	GND		AC3		VD1V2/VD1V8	VD2V5	VD3V3	AB13	20
AE8	GND		AB8		VD1V2/VD1V8	VD2V5	VD3V3	AA11	21
AF8	GND		AC7		VD1V2/VD1V8	VD2V5	VD3V3	Y11	22
AG1	GND		AD1		VD1V2/VD1V8	VD2V5	VD3V3	AC4	23
AG2	GND		AD2		VD1V2/VD1V8	VD2V5	VD3V3	AC5	24
AE6	GND		AD7		VD1V2/VD1V8	VD2V5	VD3V3	AC8	25
AF6	GND		AE7		VD1V2/VD1V8	VD2V5	VD3V3	AC9	26

AK1	GND		AG7		VD1V2/VD1V8	VD2V5	VD3V3	AF4	27
AL1	GND		AG8		VD1V2/VD1V8	VD2V5	VD3V3	AF5	28
AD4	GND		AE2		VD1V2/VD1V8	VD2V5	VD3V3	AF3	29
AE4	GND		AE3		VD1V2/VD1V8	VD2V5	VD3V3	AG3	30
AJ1	GND		AH4		VD1V2/VD1V8	VD2V5	VD3V3	AH2	31
AJ2	GND		AH5		VD1V2/VD1V8	VD2V5	VD3V3	AH3	32
AK2	GND		AM1		VD1V2/VD1V8	VD2V5	VD3V3	AL3	33
AK3	GND		AM2		VD1V2/VD1V8	VD2V5	VD3V3	AM3	34

The Edge Connector has dedicated signal connections to Virtex4 and the signalling levels applyed at this connector are selectable. Signalling outside the 0V to 3.3V should not be used on this connector as it could damage the Virtex4, which is connected to these signals. The pinout of the Card Edge Connector is as follows.

EDGE PIN	DEVICE1 PIN	DEVICE1 PIN	EDGE PIN
1	VD3V3	VD3V3	60
2	VD2V5	VD2V5	59
3	GND	GND	58
4	AP6	AP7	57
5	AH7	AH8	56
6	AN9	AP9	55
7	AP10	AP11	54
8	AP12	AN12	53
9	AN13	AM13	52
10	GND	GND	51
11	AN4	AP4	50
12	AJ5	AJ6	49
13	AJ7	AK7	48
14	AK8	AL8	47
15	AJ9	AJ10	46
16	AL13	AK13	45
17	GND	GND	44
18	AL4	AL5	43
19	AM5	AM6	42
20	AM7	AN7	41
21	AK9	AL9	40
22	AL10	AL11	39
23	AM11	AM12	38
24	GND	GND	37
25	AN8	AN3	36
26	AJ4	AK4	35
27	AN5	AP5	34
28	AK6	AL6	33
29	AM8	AN8	32
30	AM10	AN10	31

FPGAs

Figure 10 - Broaddown4 FPGA

Broaddown4 supports a Spartan-3 device in the FG456 package and Virtex4 devices in the 1148 package. Broaddown4 is normally available with both industrial and commercial grade silicon and all speed grades fitted in two sizes for the Spartan3 device XC3S1000, and XC3S1500 and six devices for the Virtex4 LX40, LX60, LX80, LX100, LX160 and SX55.

Broaddown4 has two Platform Flash sites supporting XCF02, XCF04 and XCF08 devices in a daisy chain configuration for the Spartan3 device. These sites allow a programming capacity of between 2 and 16 Mbits. The size and number of devices fitted will depend which variant of Broaddown4 is ordered. Broaddown4 also has two Platform Flash sites supporting XCF08, XCF16 and XCF32 devices in a daisy chain configuration for the Virtex4 devices allowing serial or parallel programming of the FPAG. These sites allow a programming capacity of between 8 and 64 Mbits. The size and number of devices fitted will depend which variant of Broaddown4 is ordered.

Broaddown4 supports the DCI feature of Virtex4 devices. DCI can be used to match signal impedances to improve signal integrity. Broaddown4 supports independent DCI functions for each bank of the Virtex4. By default a 100 ohm resistor is connected between VRN, VRP FPGA terminals and the appropriate power rails on the reverse of Broaddown4.

Moel-Bryn Expansion Position

Figure 11 - Moel Bryn Expansion

Moel-Bryn expansion uses solder-less connector's to connect modules to the Broaddown4. Enterpoint will be releasing a series of modules shortly for this advanced expansion capability.

The details of this interface will only be released under license and may be subject to license or royalty fee.

The associate YFS connectors allow I/O expansion over the normal Broaddown4 capabilities when a Moel-Bryn Expansion Module is fitted.

CPLDS

Figure 12 - Broaddown4 CPLDs

The CPLD has its notional own 50Mhz dedicated clock source,

CLOCK SOURCE	CPLD PIN
CPLD_CLOCK_SOURCE	22

There is a single 9572Xl CPLD in the TQ100 package fitted to Broaddown4. This CPLD supports indirect access for the Spartan-3 FPGA PCI-E SMB bus and JTAG. This device controls the switching regulators. Using these features either groups or individual regulators can be turned off or on enabling sections of Broaddown4 please see the customer schematics for more detail.

VOLTAGE CONTROL	CPLD PIN
5V0	32
3V3	56
2V5	55
1V8	54
1V2	53
CORE VOLTAGE	92
1V25 PUSH PULL	91
0V9 PUSH PULL	93

PCI EXPRESS SIGNAL	CPLD PIN
SMCLK	94
SMDATA	95
WAKE	97
POWERGOOD	6
TRST#	8
TCK	9
TDO	11
TDI	10
TMS	12

To access these features the Spartan3 FPGA is connected to the CPLD by a 20 way bus. This bus may be used as the user wishes. However Enterpoint has developed a build that enables all power and voltage monitoring signals and sequencing to start Broaddown4 correctly.

SPARTAN TO CPLD BUS	SPARTAN PIN	CPLD PIN
1	A4	16
2	B6	13
3	B18	18
4	A15	20
5	C6	14
6	B5	15
7	B14	25

8	B4	17
9	A12	28
10	B15	23
11	B20	33
12	A19	36
13	A13	27
14	B11	29
15	B19	39
16	A10	30
17	A18	40
18	B9	3
19	B10	99
20	C7	4

Routed from the CPLD are 4 LED's that can be used to indicate the status of the board or higher level functions the user can program into the CPLD.

LED'S	CPLD PIN
1	42
2	41
3	37
4	35

As an extra feature onboard there is voltage monitoring that indicates when the voltage supplies go outside 2% of the notional 3.3v, 2.5v, 1.8v and 1.2v range, the indications of over and under voltage conditions are logic based and are routed to the CPLD.

VOLTAGE SENSOR PIN	CPLD PIN
OVER 3V3	85
UNDER 3V3	86
OVER 2V5	81
UNDER 2V5	82
OVER 1V8	78
UNDER 1V8	79
OVER 1V2	76
UNDER 1V2	77

The CPLD power supply is in the shape of the 3.3V from a TPS70402 twin regulator package shared with the Spartan3 device. By having regulators independent of the Main Regulators modelling of wake-up power systems is possible.

Medical and Safety Critical Use

Broaddown4 is not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd will accept no liability for any failure or defect of the Broaddown4, or its design, when it is used in any medical or safety critical application.

Warranty

Broaddown4 comes with a 90 return to base warranty. There are a number of places that Broaddown4 can be soldered by a user. We have sited these on the back of the board to avoid damage to other components when solder bridges are made. However do not attempt to solder connections if you are not competent to do so. Enterpoint reserves the right to not honour a warranty if the failure is due to poor soldering technique or other maltreatment of the Broaddown4.

Outside warranty Enterpoint offers a fixed price repair or replacement service. We reserve the right not to offer this service where a Broaddown4 has been maltreated or otherwise deliberately damaged. Please contact support if need to use this service.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on boardsales@enterpoint.co.uk if you are interested in these types of warranty,

Support

Enterpoint offers support during normal United Kingdom working hours 9.00am to 5.00pm. Please examine our Broaddown4 FAQ web page and the contents of this manual before raising a support query. We can be contacted as follows:

Telephone - +44 (0) 1684 585262
Email - support@enterpoint.co.uk