AN11695

NXQ1TXA5 one-chip 5 V Qi wireless transmitter

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Document information

Info	Content
Keywords	NXQ1TXA5, wireless charger, A11 Qi coils, low power
Abstract	This application note describes the NXQ1TXA5 wireless charger solution designed for A11 Qi coils. It is based on the NXP Semiconductors NXQ1TXA5 fully integrated wireless power transmitter product for Qi compliant 5 volt low-power transmitters.

Revision history

Rev	Date	Description
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1. Introduction

This application note describes the NXQ1TXA5 wireless charger solution designed for A11 Qi coils. It is based on the NXP Semiconductors NXQ1TXA5 fully integrated wireless power transmitter product for Qi compliant 5 V low-power transmitters.

The NXQ1TXA5 comes in a 5 mm × 5 mm HVQFN32 package. It implements all the logic and power electronics required to realize a compact ultra-low component count 5 W Qi power transmitter application. To complete the whole application, only a handful of small passive components and a charging coil are required. The application operates from a 5 V power supply (e.g. a USB adapter).

In this application note guidelines are given for the implementation of a fully operating wireless power transmitter. Electrical, thermal and compliance aspects are covered. Recommendations for tuning and potential customizations are explained.

1.1 Features

- Single-chip WPC1.1.2 Qi-compliant device for A5/A11/A12/A16 5 V single-coil low-power transmitters
- Operates from a 5 V supply
- Integrated high-efficiency full-bridge power stage with low EMI radiation, meeting EN55022 radiated and conducted emission limits
- Very few external components required, minimizing cost, complexity, and board space
- Extremely low-power receiver detection circuitry; standby power 10 mW (typical)
- Power stage fully protected against overcurrent and overtemperature
- Fully integrated accurate coil current measurement
- Demodulates and decodes communication packages from Qi-compliant receivers
- PID regulation for closed-loop power drive and control
- Internal 1.8 V digital supply generation for the logic electronics
- LED (2x) and buzzer outputs
- NTC input for external temperature check and protection
- On-chip thermal protection
- Small HVQFN32 package (5 mm × 5 mm) with 0.5 mm pitch
- Foreign Object Detection (FOD) with automatic switching between V 1.1 and V 1.0 for legacy receiver support
- FOD levels can be adjusted using external resistors to compensate for application differences and meet Qi certification requirements
- Smart Power Limiting (SPL) function to adapt to power-limited 5 V supplies
- Static Power Reduction (SPR) function for multiple NXQ1TXA5 on a single USB supply
- Supports Near Field Communication (NFC) TAG applications with delayed start-up

2. Schematic, bill of materials, and layout

Figure 1 shows a full basic circuit diagram for a NXQ1TXA5 wireless power transmitter application. The circuit diagram includes the status LED indicators and a connection for a buzzer. They may be omitted if not required, but their connections are shown for the sake of completeness. The same is true for the temperature sensors. One or more sensors can be implemented in a specific application. However, it is also possible to omit the sensors and in this way ignore specific temperature information. In this case, only the NXQ1TXA5 internal temperature protection remains intact.

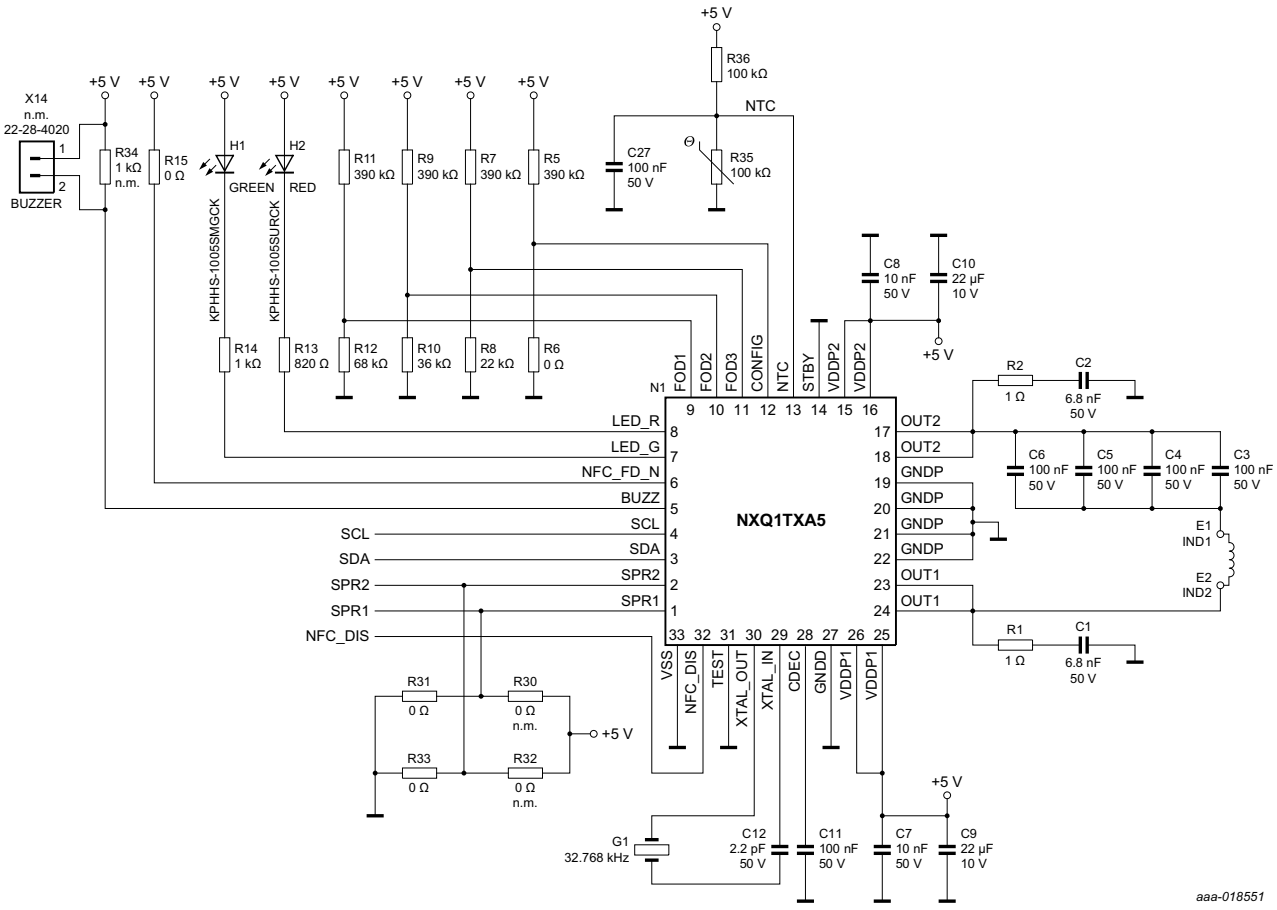
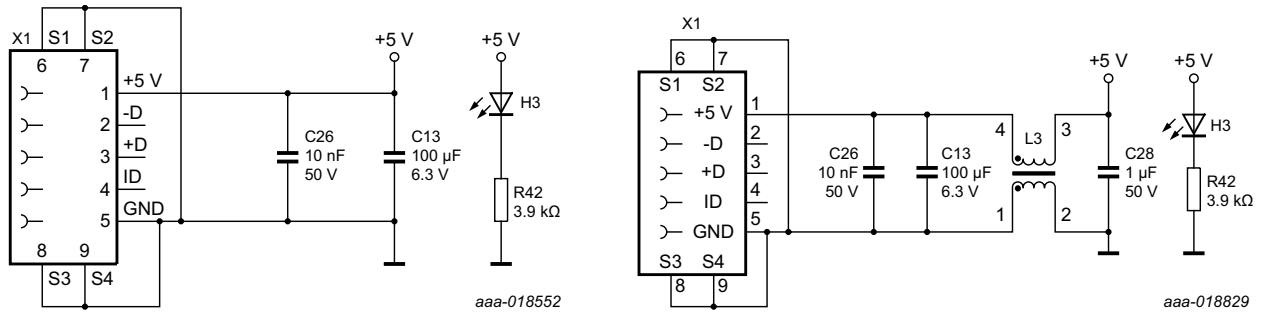


Fig 1. NXQ1TXA5 wireless power transmitter circuit diagram

A USB powered wireless power transmitter is a standard application for the circuit shown in Figure 1. Figure 2a and Figure 2b show two potential implementations of the power interface circuit. Figure 2a is only a buffer. However, with a proper layout the result is an already very good EMI performance.

The circuit of Figure 2b contains an additional common mode choke (L3). This interface actively contributes to maximizing EMI reduction. An additional LED (H3) shows that the application is powered.

The power drawn by the H3 LED must be low because the current flowing in the LED has a negative impact on the standby current of the application. So a relatively high-ohmic current limiting resistor (R42) is chosen (3.9 kΩ).



a. 5 V USB power input circuit

b. 5 V USB input power circuit with EMI filter

Fig 2. 5 V USB input power interface options

2.1 Circuit description

2.1.1 Power transfer

The power transfer section is on the left-hand side in the circuit diagram. The NXQ1TXA5 IC contains a full (4-MOSFET) power bridge that drives the series-resonant network consisting of capacitance C_p (realized by connecting capacitors C3, C4, C5, and C6 in parallel) in series with the transmitter coil L_p (connected to terminals IND1 and IND2). The NXQ1TXA5 regulates the amount of power that the coil transmits by varying the switching frequency of the bridge. At high frequency (e.g. 205 kHz), power transfer is low and at low frequency (e.g. 110 kHz), power transfer is high.

If at 205 kHz switching frequency the power transfer is still higher than required by the load, the NXQ1TXA5 IC reduces the operation duty cycle to arrive at the required power transfer level. During the on-period of the duty cycle, the switching frequency is 205 kHz.

To limit ElectroMagnetic Interference (EMI), snubber networks are connected from the two bridge-output nodes to ground (resistor R1/capacitor C1 and resistor R2/capacitor C2). Supply decoupling of the power stage is implemented using capacitors C7, C8, C9, and C10.

2.1.1.1 Optimizing the LC resonant tank

According to Wireless Power Consortium (WPC) Qi specification (Ref. 1), values have been specified for both the inductance (L_p) and the capacitance (C_p) in the resonant tank.

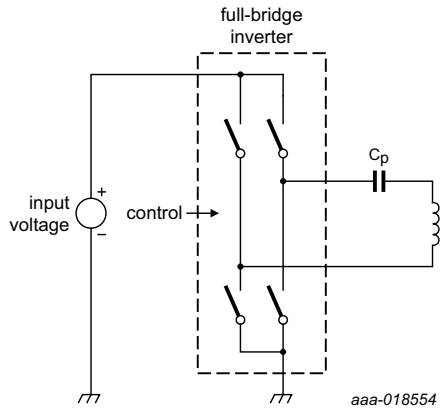


Fig 3. Qi power transmitter principle - inverter plus resonant tank

The assembly of the inductor coil and the shielding and accessories must have an inductance (L_p) of 6.3 μH (±10 %). The capacitance (C_p) of the series capacitor must be 0.4 μF (±5 %). The input voltage to the full-bridge inverter must be 5 V (±5 %). The combination of L_p and C_p is intended to give the tank a target resonant frequency of:

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_p \cdot C_p}} \approx 100.26\ kHz\ (\pm 8\ \%) \quad (1)$$

Under various conditions, tuning the resonant tank to perform optimally can be an option. For example, when the inductance of a specific transmitter coil assembly is high, a lower value for the capacitance can be chosen to shift the resonant frequency towards the target resonant frequency. The result of failing to do so can be that the inverter/resonant tank combination is not able to transfer the required amount of power at the lowest operating frequency (110 kHz). Tune the C_p capacitance value through a small series of practical experiments. When C_p consists of a number of capacitors in parallel, make sure that the individual capacitances have approximately the same value (preferably not more than 20 % difference). This way of tuning leads to the best performance when a specific transmitter coil is chosen.

Realizing maximum power transfer can be easier when the resonant frequency of the resonant tank is shifted slightly upwards (e.g. 105 kHz). When transferring power to a critical receiver, a slightly upward frequency shift is beneficial. However, the resonant frequency must never be so close to 110 kHz that the spread in component values causes it to be higher than 110 kHz.

2.1.2 Crystal oscillator

The NXQ1TXA5 uses an external low-cost 32.768 kHz crystal with a 1 % accuracy. The crystal must support a load capacitance of approximately 12 pF (the load capacitance is embedded in the NXQ1TXA5). It is connected to the oscillator input pin (XTAL_IN) via a 2.2 pF series capacitor. To prevent oscillations or overtones, the length of the crystal connections must be approximately 1 cm. Do not connect the crystal to the NXQ1TXA5 using vias. Connect it directly on the top layer of the PCB. If possible, shield the crystal by connecting the casing to ground.

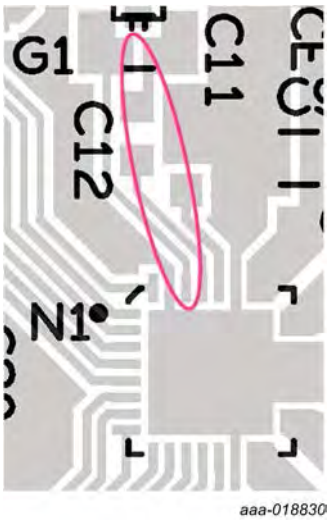


Fig 4. Crystal to NXQ1TXA5 IC typical connection layout

2.1.3 NXQ1TXA5 configuration

The NXQ1TXA5 contains 4 configuration inputs: FOD1, FOD2, FOD3, and CONFIG. Each time the NXQ1TXA5 enters the digital ping mode, the input levels are sampled. The results are used to configure the NXQ1TXA5. The input voltage levels to the respective pins are set with resistor combinations R5/R6, R7/R8, R9/R10, and R11/R12.

2.1.3.1 FOD1, FOD2, and FOD3

The NXQ1TXA5 features FOD functionality according to the Qi 1.1.2 standard. It switches to FOD (Foreign Object Detection) mode if the received power level reported by the Qi receiver ($P_{received}$) is not in line with the transmitted power level provided by the NXQ1TXA5 application ($P_{transmitted}$). In this way, the heating up of a foreign object (e.g. a coin) when it happens to be in the wireless power transfer path, is prevented. Similarly, when misalignment between the transmitter and the receiver coils is too large and losses in the wireless power transfer path are beyond a configurable threshold level, wireless power transfer halts.

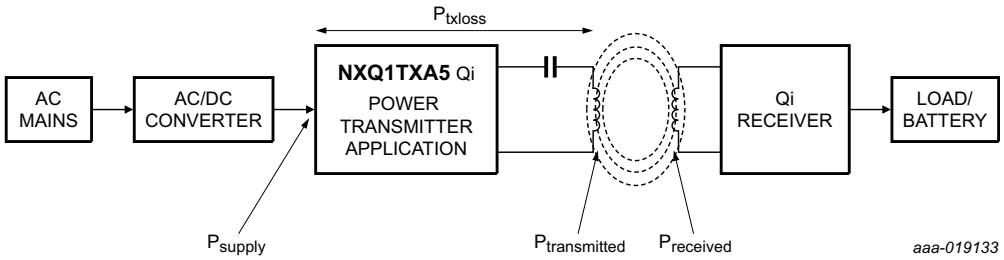


Fig 5. Wireless power transmission chain

FOD1

In practical situations, there is always a mismatch between the power transmitted by the NXQ1TXA5 application ($P_{transmitted}$) and the power received by the Qi receiver ($P_{received}$).

$$P_{diff} = P_{transmitted} - P_{received} \quad (2)$$

The difference between the two values (P_{diff}) can be used to trigger FOD mode in the NXQ1TXA5 IC. The threshold level above which FOD mode must be entered can be set with the voltage level on the FOD1 pin of the IC. On the low end, when 0.25 V is applied to pin FOD1, a maximum P_{diff} level of 0.167 W is tolerated. On the high end, when 1.29 V is applied, a 0.86 W difference is tolerated. Any threshold level between 0.167 W and 0.86 W can be set, as well as a default level of 0.5 W and a mode where FOD is being ignored altogether (see Table 1).

Table 1. FOD threshold difference

Input voltage on pin FOD1	FOD threshold level
$V_{FOD1} < 0.04$ V	no FOD
$0.25 \text{ V} < V_{FOD1} \leq 1.29$ V	V_{FOD1} (V) / 1.5 W[1]
$1.335 \text{ V} < V_{FOD1} \leq V_{DDP}$ (V_{DDP} is maximum input level)	0.5 W (default value)

[1] This equation assumes V_{DDP} = 5 V. To compensate for changes in the supply voltage level, the results are automatically adjusted.

The NXQ1TXA5 FOD calculation tool (available from NXP, see FOD calibration section) can be used to calculate the appropriate value for resistor R12. This resistor, in combination with pull-up resistor R11, sets the voltage on pin FOD1.

FOD2 and FOD3

The transmitted power level (the power that the NXQ1TXA5 application delivers to the magnetic field) can be calculated by subtracting the power loss in the application from the input power supplied to the application:

$$P_{transmitted} = P_{supply} - P_{txloss} \quad (3)$$

The NXQ1TXA5 IC calculates P_{supply} by multiplying the supply voltage (V_{DDP}) with the current flowing into the IC. However, the NXQ1TXA5 IC cannot measure P_{txloss} because it cannot 'see' losses that occur in peripheral components (e.g. transmitter coil, resonant capacitors) and PCB tracks. So, the NXQ1TXA5 IC must estimate a value for P_{txloss}. How the NXQ1TXA5 estimates P_{txloss} values is explained in the FOD calibration section.

FOD calibration

In a calibration situation, we can acquire measured values for P_{txloss}. If a calibrated Qi receiver (with attached variable load resistor; Ref. 4) is optimally aligned with the transmitter coil, it reports the amount of power that is available in the magnetic field ($P_{transmitted}$). In that specific situation $P_{received}$ equals $P_{transmitted}$.

Using a Qi sniffer (Ref. 5), the $P_{received}$ values reported by the calibrated Qi receiver are captured. So we know the $P_{transmitted}$ value in relation to the P_{supply} value. Hence, it is possible to calculate P_{txloss} by subtracting $P_{transmitted}$ from P_{supply} (see Equation 3).

Fig 6. Calibrated Qi receiver simulator with attached variable load (resistor)

Fig 7. Qi sniffer tool

By measuring a series of $P_{supply}/P_{received}$ pairs, it is possible to make a graph of the P_{supply} versus P_{txloss} relationship. The measurements must be executed with a calibrated Qi receiver and the transmitter and the receiver are optimally aligned. Table 2 shows an example of the results of a calibration session. Figure 8 shows the graph.

V_{supply} and I_{supply} are read from calibrated voltage and current meters. $P_{received}$ is read from the Qi sniffer. P_{supply} and P_{txloss} are calculated.

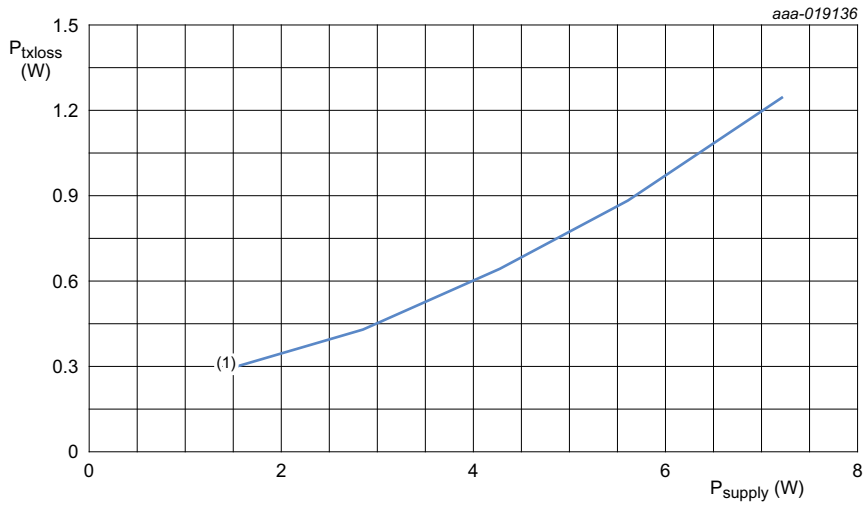
$$P_{supply} = V_{supply} \times I_{supply} \quad (4)$$

$$P_{txloss} = P_{supply} - P_{transmitted} \quad (5)$$

Table 2. Calibration session recording - example

Load point # [-]	V_supply [V]	I_supply [A]	P_supply [W]	P_received [W]	P_txloss [W]
1	5.023	0.300	1.507	1.210	0.297
2	5.001	0.570	2.851	2.421	0.430
3	5.000	0.855	4.275	3.632	0.643
4	5.008	1.120	5.609	4.726	0.883
5	5.016	1.440	7.223	5.976	1.247

Fixed values
Input values
Calculated values



(1) P_{txloss} (measured)

Fig 8. Graphical representation of measured P_{txloss} versus P_{supply}

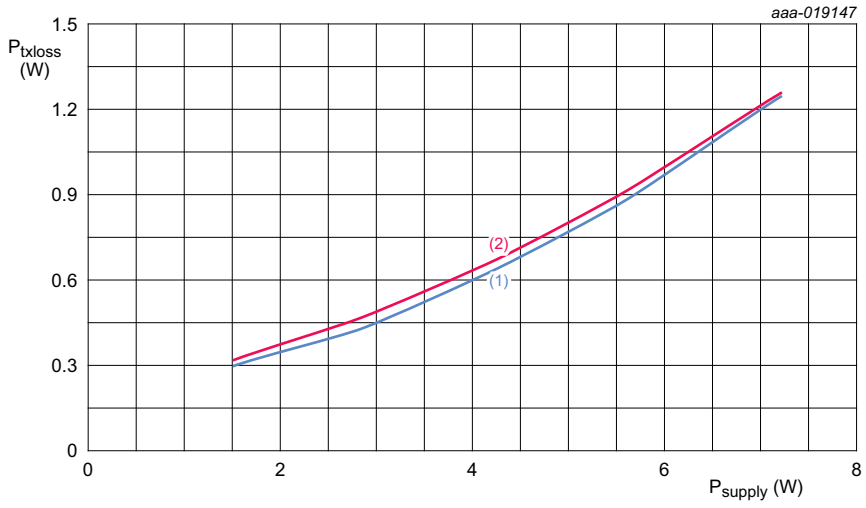
Based on the measured data in Table 2 (graphically represented in Figure 8), a second-order polynomial that closely approximates the measured P_{supply} versus P_{txloss} curve can be constructed:

$$P_{txloss(estimated)} = A + BP_{supply} + CP_{supply}^{2} \quad (6)$$

Where:

- A = 0.2 W (fixed)
- B is the linear proportionality factor; the voltage level on the FOD2 pin determines the value (see Table 4)
- C is the second-order proportionality factor; the value is configured via the voltage level applied to pin FOD3 (see Table 5)

With A fixed to 0.2 W, the target is to select values for B and C in such a way that the curve shown in Figure 8 is approximated with minimal (weighted) overall error. It can be done in various ways, but the most convenient way is to use the NXQ1TXA5 FOD calculation tool which is available from NXP (Ref. 6). In the tool, measurement values are entered like in Table 2. As a result, the tool gives suggested values for B and C and how to set these values using resistors R10 (FOD2) and R8 (FOD3). These resistor values also depend on the pull-up resistor value (390 kΩ default). Figure 9 shows the result of the curve-fitting exercise.



(1) P_{txloss} (measured)

(2) P_{txloss} (estimated)

Fig 9. Measured and estimated P_{txloss} versus P_{supply} - fitted by the NXQ1TXA5 FOD calculation tool

Table 3. NXQ1TXA5 FOD calculation tool

Fixed values							
Input values							
Calculated values							
Load point # [-]	**V_supply [V]**	**I_supply [A]**	**P_supply [W]**	**P_received [W]**	**P_txloss [W]**	**P_txloss(est) [W]**	**error [W]**
1	5.023	0.300	1.507	1.210	0.297	0.318	0.021
2	5.001	0.570	2.851	2.421	0.430	0.469	0.039
3	5.000	0.885	4.275	3.632	0.643	0.676	0.033
4	5.008	1.120	5.609	4.726	0.883	0.914	0.031
5	5.016	1.440	7.223	5.976	1.247	1.259	0.012

A [W]	**B [-]**	**C [1/W]**
0.2	0.11	0.012

FOD threshold level	
0.5	[W]

Pull-up resistors R11/R9/R7		**FOD1 resistor R12**		**FOD2 resistor R10**		**FOD3 resistor R8**	
390	[kΩ]	68.1	[kΩ]	12.1	[kΩ]	OPEN	[kΩ]

Table 4. B-coefficient value set via FOD2

Input voltage on pin FOD2	FOD parameter B
V_{FOD2} < 0.04 V	default value for parameters B and C: B = 0.11 and C = 0.012
0.085 V < V_{FOD2} ≤ 1.29 V	0.067 × V_{FOD2} (V) + 0.05[1]
1.335 V < V_{FOD2} ≤ V_{DDP} (V_{DDP} is maximum input level)	reserved

[1] This equation assumes V_{DDP} = 5 V. To compensate for changes in the supply voltage level, the results are automatically adjusted.

Table 5. C-coefficient value set via FOD3

Input voltage on pin FOD3	FOD parameter C
0.210 V < V_{FOD3} < 0.290 V[1]	0.006
0.585 V < V_{FOD3} < 0.665 V[1]	0.008
0.960 V < V_{FOD3} < 1.040 V[1]	0.010
V_{FOD3} > 1.335 V (V_{DDP} is maximum input level)[1]	0.012
other voltage levels	reserved

[1] This condition assumes V_{DDP} = 5 V. To compensate for changes in the supply voltage level, the conditions are automatically adjusted.

The B and C coefficients are properly calculated when the above procedure is followed. However, the values of the B and C coefficients may be set differently to allow more freedom of placement of a Qi receiver and to correct for product and application spread.

By setting B and/or C to a higher value than calculated, more freedom of placement is realized. The consequence is that the FOD mechanism only triggers when a higher amount of power is dissipated in a foreign object.

An acceptable compromise must be found for most practical situations. For that reason, examine a small series (e.g. 10) assembled NXQ1TXA5-based Qi wireless power transmitter applications regarding the aspects mentioned above. Based on that examination, proper B and C coefficient settings must be chosen.

2.1.3.2 CONFIG

The voltage level applied to the CONFIG pin determines the behavior of the LEDs and the buzzer connected to the NXQ1TXA5 IC. Table 6 clarifies what mode is selected for a certain voltage level (V_{CONFIG}).

Table 6. Mode selection

Input voltage on pin CONFIG	Mode name
V_{CONFIG} < 40 mV	two LED 1
85 mV < V_{CONFIG} < 165 mV	two LED 2
210 mV < V_{CONFIG} < 290 mV	two LED 3
335 mV < V_{CONFIG} < 415 mV	two LED 4
460 mV < V_{CONFIG} < 540 mV	two LED 5
585 mV < V_{CONFIG} < 665 mV	two LED 6
710 mV < V_{CONFIG} < 790 mV	two LED 7
835 mV < V_{CONFIG} < 915 mV	two LED 8
960 mV < V_{CONFIG} < 1040 mV	one LED 1 & 2
1085 mV < V_{CONFIG} < 1165 mV	one LED 3 & 4
1210 mV < V_{CONFIG} < 1290 mV	one LED 5 & 6
V_{CONFIG} > 1335 mV	debug LED

Table 7 describes the behavior of the LEDs for each of the modes. Table 8 describes the behavior of the buzzer.

Table 7. LED modes

LED Mode	Digital_Ping - LED_G		Charging - LED_G (Power_Transfer mode)	Receiver charged[1]	Fault detected[2]	
					LED_R	LED_G
Two LED 1	blink for 100 ms every 4 seconds blink for 100 ms every 400 ms when object detected		on: full power blink at 0.5 Hz: limited power (SPL, SPR or average current exceeds 2 A)	off	blink at 1 Hz	off
Two LED 2	off			off		
Two LED 3	blink for 100 ms every 4 seconds blink for 100 ms every 400 ms when device detected			off	blink at 0.5 Hz	
Two LED 4	off			off		
Two LED 5	blink for 100 ms every 4 seconds blink for 100 ms every 400 ms when device detected			off	blink at 1 Hz	blink at 1 Hz
Two LED 6	off			off		
Two LED 7	off			off	blink at 2 Hz	blink at 2 Hz
Two LED 8	reserved					
One LED 1 & 2[3]	LED_G:	blink for 100 ms every 4 seconds blink for 100 ms every 400 ms when device detected	on: full power blink at 0.5 Hz: limited power (SPL, SPR or average current exceeds 2 A)	off	x	blink at 2 Hz for TX/RX error; no blink on FOD
	LED_R	blink for 100 ms every 4 seconds blink for 100 ms every 400 ms when device detected		off	off	x
One LED 3 & 4[3]	LED_G:	off		off	x	blink at 2 Hz for TX/RX error; no blink on FOD
	LED_R	off		off	off	x
One LED 5 & 6[3]	LED_G:	blink for 100 ms every 4 seconds blink for 100 ms every 400 ms when device detected	blink at 0.5 Hz	on	x	blink at 2 Hz for TX/RX error; no blink on FOD
	LED_R	off		on	off	x
Debug LED	reserved					

[1] ‘charge complete’ or ‘charge status 100 %’ message received via RX (NXQ1TXA5 remains in Power_Transfer mode while ‘charge status 100 %’ is reported; it switches to Charged mode when a ‘charge complete’ message is received).

[2] Receiver reports ‘internal fault’, ‘overtemperature’, ‘battery failure’, or ‘no response’. Transmitter reports OTP or FOD. If the receiver reports ‘overcurrent’, ‘overvoltage’, or ‘unknown’, the device restarts and goes back to ping state.

[3] User can connect LED to either LED_R or LED_G; so the voltage on CONFIG could be used to enable two separate One LED modes.

Table 8. Buzzer modes

LED mode	Buzzer mode		
	Start charging	**Receiver fully charged**	**Error (FOD, OTP, RX); ASK time-out not an error**
Two LED 1	two short beeps on entering state	off	one short beep every 4 S while in state
Two LED 2	two short beeps on entering state	off	one short beep every 4 S while in state
Two LED 3	two short beeps on entering state	4 short beeps on entering state	one short beep every 4 S while in state
Two LED 4	two short beeps on entering state	4 short beeps on entering state	one short beep every 4 S while in state
Two LED 5	two short beeps on entering state	off	one short beep every 4 S while in state
Two LED 6	two short beeps on entering state	off	one short beep every 4 S while in state
Two LED 7	two short beeps on entering state	4 short beeps on entering state	one short beep every 4 S while in state
Two LED 8	two short beeps on entering state	4 short beeps on entering state	one short beep every 4 S while in state
One LED 1&2	two short beeps on entering state	off	one short beep every 4 S while in state
One LED 3&4	two short beeps on entering state	4 short beeps on entering state	one short beep every 4 S while in state
One LED 5&6	two short beeps on entering state	off	one short beep every 4 S while in state
Debug LED	two short beeps on entering state	4 short beeps on entering state	one short beep every 4 S while in state

2.1.4 Smart Power Limiting (SPL) and Static Power Reduction (SPR)

When the 5 V supply (V_{DDP}) drops to below 4.2 V (the SPL threshold), SPL limits the supply current. SPL continues to limit the output power until the supply voltage recovers (even if the receiver requests more power). SPL can be disabled using the SPR1 and SPR2 pins (see Table 6).

This way a proprietary application can be realized that e.g. operates from a 3.6 V battery source (e.g. low-power application for wearables). However, to protect the power supply, SPL is mandatory for a Qi certified application.

SPR limits the supply current independently of the supply voltage. This feature can be used, for example, when the supply is taken from a limited USB source. The SPR level is selected using the SPR1 and SPR2 pins (see Table 6). If the SPR function is not required, the SPR1 and SPR2 pins must be connected to ground or to V_{DDP}. The pins cannot be left floating.

Table 9. SPL status and SPR level

SPR1	SPR2	SPL status and SPR level
0 (ground)	0 (ground)	SPL on; no SPR limiting
0 (ground)	1 (V_{DDP})	SPL on; 500 mA
1 (V_{DDP})	0 (ground)	SPL on; 1000 mA
1 (V_{DDP})	1 (V_{DDP})	SPL off; no SPR limiting

2.1.5 LEDs and buzzer

The LEDs (H1 and H2) and the optional buzzer implement an elementary visual and audial user interface. Implementing either the LEDs or the buzzer in the application is not required. However, end users may appreciate some form of feedback regarding the operation and status of the application. The user interface behavior is set using the CONFIG pin (see Section 2.1.3) and the *One-chip 5 V Qi wireless transmitter* data sheet (Ref. 2). LED and buzzer output pins are open-drain and may be connected to GND if necessary.

2.1.6 Thermal protections

One or more thermal tripping points can be implemented in an NXQ1TXA5 application. When the voltage supplied to the NXQ1TXA5 NTC pin (pin 13) drops to below 0.8 V, the NXQ1TXA5 stops delivering power. When the voltage level exceeds 1.1 V, the power transfer recommences.

Figure 1 shows the implementation of a single temperature measurement point. NTC resistor R35 can be placed in the coil center, so the legacy devices with Qi 1.0 receivers can be supported and protected. The combination of R35 and R36 determines at what temperature the thermal protection trips and at what temperature normal operation resumes.

For example, a 100 kΩ resistor (R36) in series with a 100 kΩ NTC (R35, 1 % thermistor with nominal β-parameter of 4500 K) causes the triggering of the thermal protection at 62 °C. The application resumes operation when the temperature has dropped to 52 °C. This combination creates a hysteresis of 10 °C.

Capacitor C27 is used to suppress noise. Basically, a low-pass filter is created.

When an application requires monitoring the temperature of more than one location, an option to combine the temperature 'data' from more than one NTC sensor is available. An OR-ing circuit consisting of diodes connects the sensor circuits. In Figure 10, D4A and D4B are the OR-ing diodes. D4C compensates for the voltage drop across D4A and D4B. The signal on the left-hand side must be connected to the NXQ1TXA5 NTC pin.

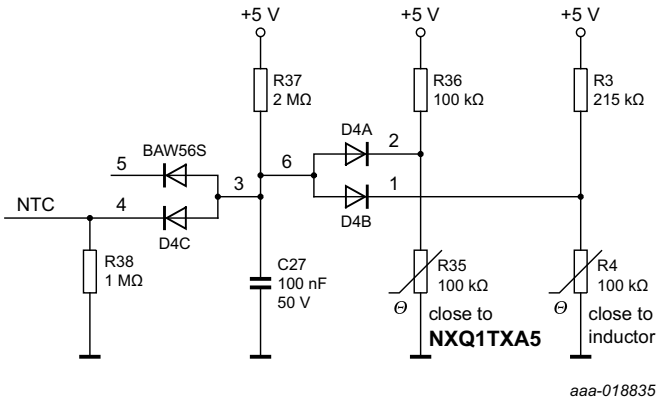


Fig 10. Multi-temperature protection using an OR-ing circuit

In a similar configuration, more than two temperatures can be monitored and used for tripping/resuming.

The tripping temperature and the resume temperature of an NTC measuring branch can easily be calculated. Input required:

- The value of the pull-up resistor (R_{PU})
- The nominal resistance value of the NTC thermistor R_{NTC} (normally specified in a data sheet at 25 °C; 298.15 K)
- The NTC temperature dependency β-parameter

The tripping temperature T_{trip} (in K) can now be calculated with Equation 7. The resume temperature T_{res} (in K) can be calculated with Equation 8.

$$T_{trip} = \frac{1}{\frac{1}{298.15} + \frac{1}{\beta} \cdot \left(ln\left(\frac{4}{21}\right) + ln\left(\frac{R_{PU}}{R_{NTC}}\right)\right)} \quad (7)$$

$$T_{res} = \frac{1}{\frac{1}{298.15} + \frac{1}{\beta} \cdot \left(ln\left(\frac{11}{39}\right) + ln\left(\frac{R_{PU}}{R_{NTC}}\right)\right)} \quad (8)$$

The NXQ1TXA5 calculation tool contains a module that supports calculations.

2.1.7 NFC (optional)

The NXQ1TXA5 can be used with an NFC enabled device. When the NFC_FD_N pin (pin 6) is LOW, a start-up delay of about 2 seconds is added when an NFC enabled receiver is placed on the charger. The 2 seconds delay allows the NFC device to finalize communication with an NFC TAG before power transfer begins. The NXQ1TXA5 starts after the delay. When it has detected a WPC-compliant Qi receiver, it starts to transfer power to this device. The NXQ1TXA5 disables the NFC reader by pulling low the NFC_DIS pin (pin 32).

If the NFC start-up delay function is not required, the NFC_FD_N pin must be connected to V_{DDP} (5 V).

When the NXQ1TXA5 is in power transfer mode, the NFC_DIS output is active-LOW (open-drain). If NFC_DIS is not used, the pin can be connected to GND.

2.1.8 I^2C interface (optional)

An I^2C interface is provided with the SDA and SCL pins (pin 3 and pin 4). Communication with the NXQ1TXA5 processor core can take place through these pins.

To use the SDA and SCL I^2C lines, they must have a pull-up resistor to a 3.3 V (maximum 3.6 V) voltage level.

When I^2C communication is not required, the pins can be left floating or they can be grounded.

The detailed use of the I^2C interface is outside the scope of this application note. Contact NXP application support for assistance.

2.2 Bill Of Materials (BOM)

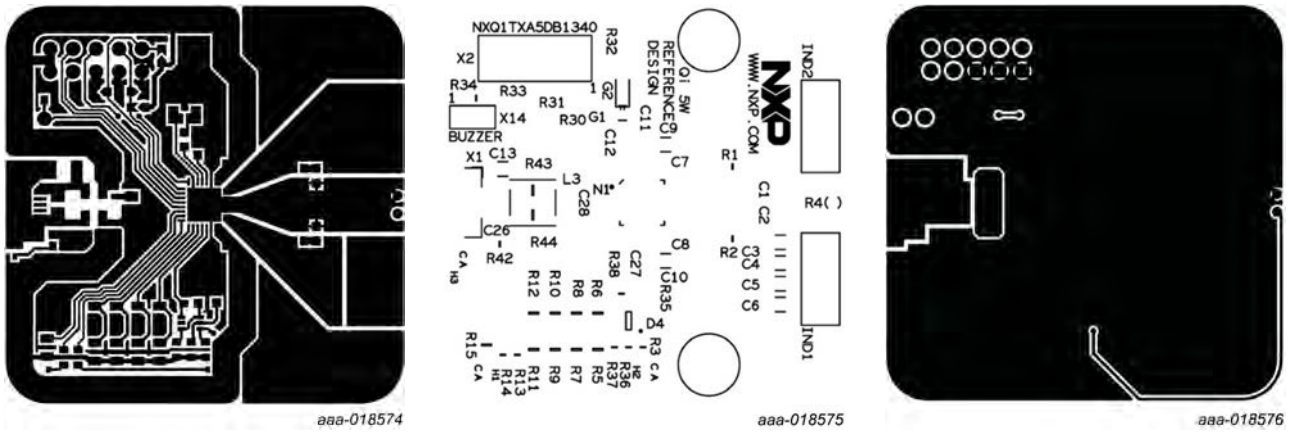
Table 10 contains the component list for a basic stand-alone NXQ1TXA5 application. The bill of materials more or less corresponds with the NXQ1TXA5 reference application as described in the user manual *NXQ1TXA5DB1340 one-chip 5 V Qi wireless transmitter demo board* user manual (Ref. 3).

Table 10. NXQ1TXA5 bill of materials

Reference	Description and values	Part number	Manufacturer
C1; C2	capacitor; 6.8 nF; 50 V; 0603	-	-
C3; C4; C5; C6	capacitor; 100 nF; 50 V; NP0; 1206 (see Section 2.1.1.1)	-	-
C7; C8	capacitor; 10 nF; 50 V; NP0; 0603	-	-
C9; C10	capacitor; 22 μF; 10 V; X7R; 1206	-	-
C11	capacitor; 100 nF; 50 V; X7R; 0603	-	-
C12	capacitor; 2.2 pF; 50 V; 0603	-	-
C13	capacitor; 100 μF; 6.3 V; X5R; 1206	-	-
C26	capacitor; 10 nF; 50 V; X7R; 0805	-	-
C27	capacitor; 100 nF; 25 V; X7R; 0603	-	-
C28	capacitor; 1 μF; 25 V; X7R; 0805	-	-
G1	XTAL; 32.768 kHz	-	-
H1	LED (green)	-	-
H2	LED (red)	-	-
H3	LED (blue)	-	-
L3	inductor; common-mode choke (optional)	DLW5BTM251SQ2L	Murata
N1	IC	NXQ1TXA5	NXP Semiconductors
R1; R2	resistor; 1 Ω; 0603	-	-
R5; R7; R9; R11	resistor; 390 kΩ; 1 %; 0603	-	-
R6; R15	resistor; 0 Ω; 0603	-	-
R8	resistor; 22 kΩ; 1 %; 0603	-	-
R10	resistor; 36 kΩ; 1 %; 0603	-	-
R12	resistor; 68 kΩ; 1 %; 0603	-	-
R13	resistor; 820 Ω; 0603	-	-
R14	resistor; 1 kΩ; 0603	-	-
R30; R32	resistor; not mounted; 0 Ω	-	-
R31; R33	resistor; 0 Ω; solder closed	-	-
R34	resistor; not mounted; 1 kΩ	-	-
R35	thermistor; 100 kΩ NTC; beta = 4500 K	-	-
R36	resistor; 100 kΩ; 0603	-	-
R42	resistor; 3.9 kΩ; 0603	-	-
X1	micro-USB PCB socket	-	FCI

2.3 Layout

The layout of an NXQ1TXA5 wireless power transmitter application is critical from an electrical and a thermal point of view. Both aspects are covered. A two-sided layout is presented as an example. This layout is also used for the *NXQ1TXA5DB1340 one-chip 5 V Qi wireless transmitter demo board* user manual.



a. Top copper b. Component silk screen c. Bottom copper

Fig 11. NXQ1TXA5 layout

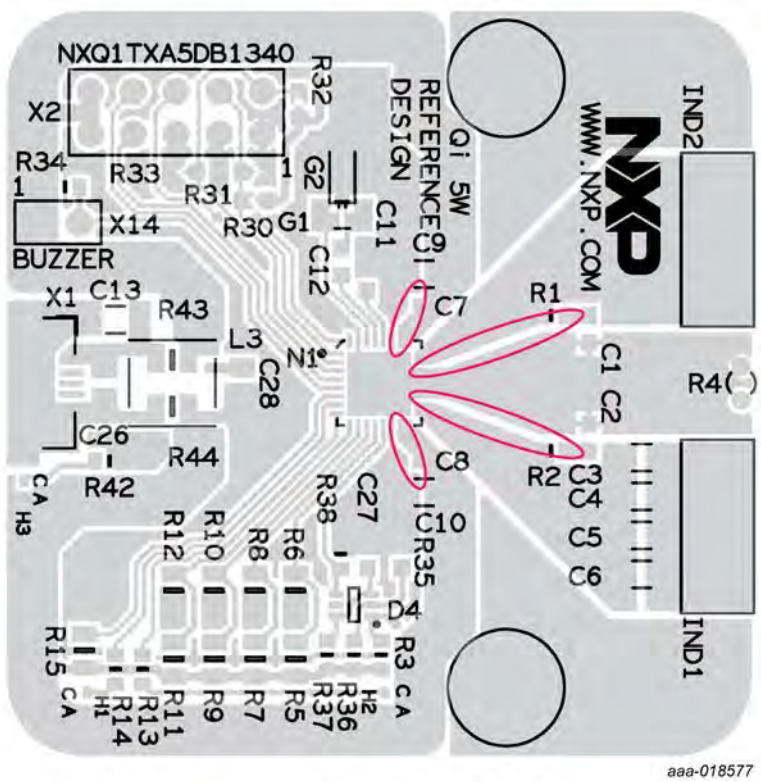


Fig 12. Top side with silk screen

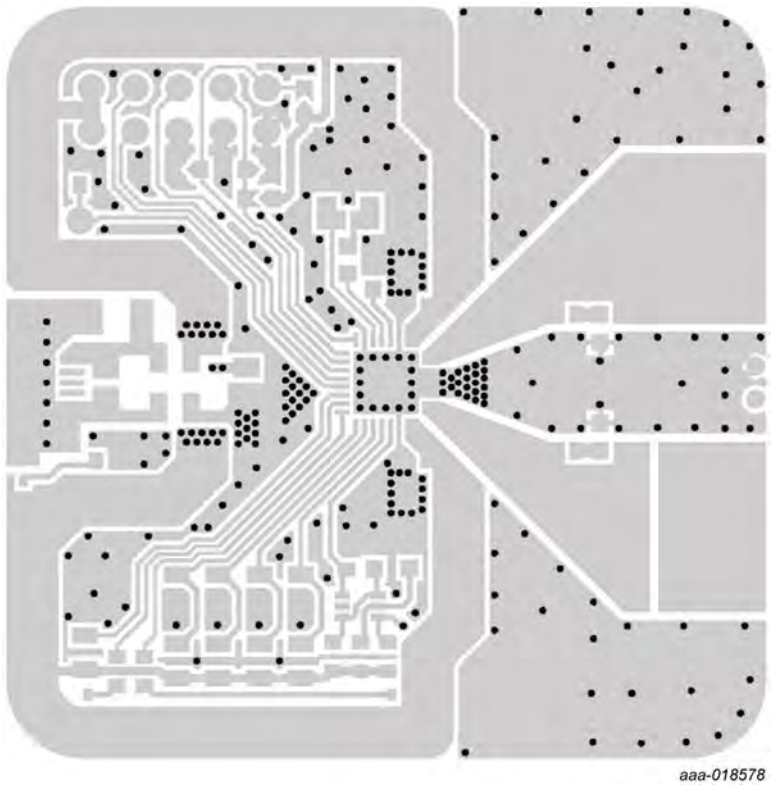


Fig 13. Top side with via pattern

2.3.1 Electrical layout aspects

From the electrical perspective, the following points require special attention:

- A shielding GND plane (in this case on the bottom layer) must be maximally uninterrupted.
- To prevent power loss because of the high current (in the order of 2 A), V_{DD} power traces to pins 15 and 16 and pins 25 and 26 must be low-impedance/low-loss (wide traces).
- Decoupling capacitors C10 and C8 must be mounted close to pins 15 and 16. They must have a low-impedance connection to power GND. Capacitor C8 (10 nF) must be closest to pins 15 and 16.
- Decoupling capacitors C9 and C7 must be mounted close to pins 25 and 26. They must have a low-impedance connection to power GND. Capacitor C7 (10 nF) must be closest to pins 25 and 26.
- Traces from the output pins 17 and 18 and pins 23 and 24 must be very low-impedance/low-loss (wide traces).
- Decoupling capacitor C11 must be mounted close to pin 28. It must have a low-impedance connection to GND.
- To prevent overtones, traces leading to the G1 crystal in series with the C12 capacitor must be approximately 1 cm.

- To prevent adverse effects in power transmission coil characteristics, solder the coil terminals directly to the PCB. Do not use extension wires.
- A thick copper layer (70 μm) conducts twice as good as a thin (35 μm) copper layer. Consider using a 70 μm top copper layer.
- Snubber circuit capacitor C1 and resistor R1 and capacitor C2 and resistor R2 must be mounted close to the output pins (pins 17 and 18; pins 23 and 24). The GND connection of the snubber circuits must be close to pins 19, 20, 21, and 22.
- Shielding (non-current conducting) GND planes in the top copper layer must be stitched to the non-current conducting GND areas of the bottom layer GND plane. The stitching must be done with vias on the edges of the planes. The intended stitching can easily be recognized on the right-hand side of the picture in Figure 13.

2.3.2 Thermal layout aspects

The NXQ1TXA5 IC is the main dissipating component on the NXQ1TXA5 PCB.

All thermal measures taken on an NXQ1TXA5 PCB must have one objective: Keep the NXQ1TXA5 IC as cool as possible.

From the thermal perspective, the following points require special attention:

- Attach as much copper as possible to the grounded pins of the IC; good thermal conduction from pins 33, 19, 20, 21, and 22 is especially important.
- Attach sufficient copper to the output pins 17, 18, 23, and 24. It is not only good for electrical conduction, but also results in thermal conduction benefits.
- Attach sufficient copper to the supply pins 15,16, 25 and 26. The concept layout in Figure 14 gives an idea of a power-wise optimal layout.
- Place the NXQ1TXA5 IC more or less in the center of the PCB. In that way, the IC benefits most from its cooling circle.

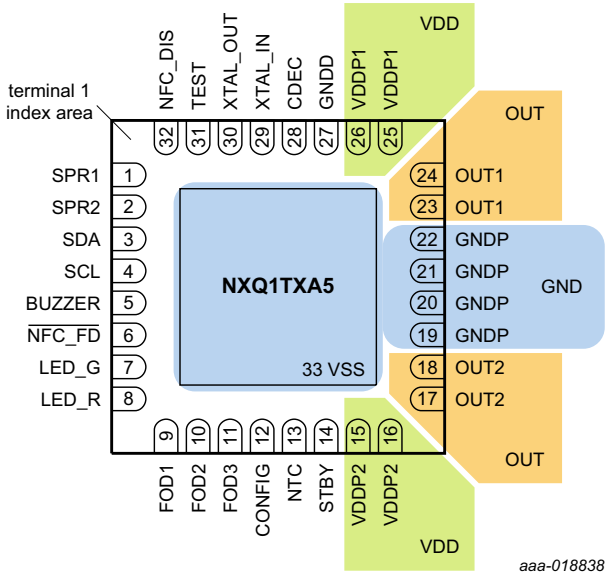


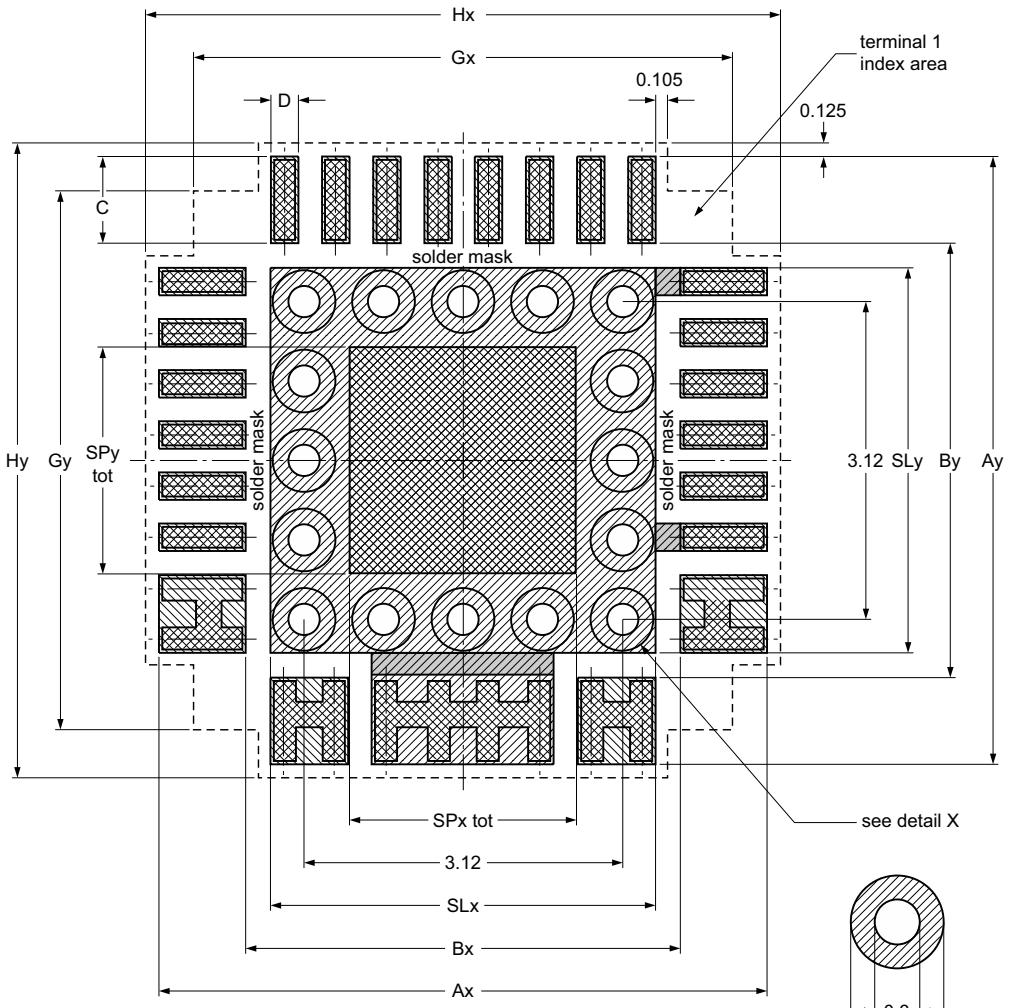
Fig 14. Concept of a power-wise optimal layout for the NXQ1TXA5 IC

- Underneath the NXQ1TXA5 IC, a pattern of 16 thermal vias must conduct heat from the top side to the bottom side of the PCB. These vias are preferably copper filled vias, but ceramic filled vias are a good second choice. A larger number of open vias is fine as well. However, there is a risk that, during the assembly process, much solder paste that must connect pin 33 (the exposed lead frame pad) to the PCB is sucked into these vias. The sucking of solder paste in to the vias can have a negative influence on the quality of the thermal connection from pin 33 to the PCB.

  Figure 15 shows the recommended footprint (for reflow soldering) for the NXQ1TXA5 IC. The recommendation includes the 16 thermal vias.

  This footprint info was taken from the *One-chip 5 V Qi wireless transmitter* data sheet (Ref. 2).

Footprint information for reflow soldering of HVQFN32 package **NXQ1TXA5**



Recommended stencil thickness: 0.1 mm

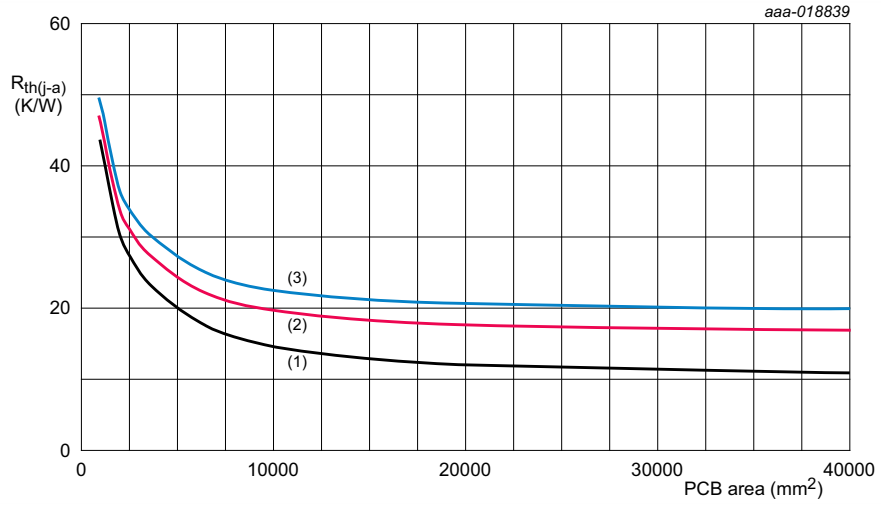
Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	nSPx	nSPy	Gx	Gy	Hx	Hy
0.5	5.95	5.95	4.25	4.25	0.85	0.27	3.75	3.75	2.2	2.2	-	-	-	-	5.25	5.25	6.2	6.2

Issue date ~~15-06-24~~ 15-06-30 *nxq1txa5_fr*

Fig 15. Application-specific reflow soldering footprint

- More thermal vias that surround the IC from the top GND layer to the bottom GND layer can improve the thermal connection from top to bottom.
- Thermal vias in remote areas (that is: relatively far from the dissipating element) do not really contribute to thermal performance. The thermal gradient from top to bottom layer is already minimal in remote areas. So, connecting them with a low thermal impedance path does not bring much improvement. All remote vias shown in Figure 13 have an electrical (non-thermal) purpose.
- The bottom layer (or other inner layer if there is a multi-layer PCB) must be a (nearly) fully filled copper layer. This layer spreads the heat over the PCB and, if the layer is the bottom layer, radiates the heat to the ambient.
- The outer layers (top and bottom layers) of the PCB must be covered with a high-emissivity coating. In most circumstances, normal solder resist is good enough because it has an emissivity of 0.9 to 0.95. Do not leave the copper blank or coat it with a reflective (e.g. gold) finish.
- Making the PCB larger enhances thermal performance of the application significantly and making the PCB too small brings the application into thermal trouble. Thermal radiation is an important factor to move heat out of the NXQ1TXA5 component and the PCB. Board surface area is more or less proportional to the capability of the board capability to lose heat through radiation. Figure 16 shows a graph that gives an impression of how $R_{th(j-a)}$ (thermal resistance from the NXQ1TXA5 IC silicon to the ambient) varies with PCB area. Trend lines for 2-layer/70 μm copper, 4-layer/35 μm copper and 4-layer/70 μm copper are given.



(1) 4-layer; 70 μm
(2) 4-layer; 35 μm
(3) 2-layer; 70 μm

Fig 16. Typical trend lines for the $R_{th(j-a)}$ versus the PCB area

The NXQ1TXA5 demo board that was used as illustration in this application note has a PCB area of approximately 2000 mm^2, giving the board an R_{th} value of approximately 30 K/W. Figure 16 shows that a smaller board can rapidly cause thermal issues for the assembly. It also shows that increasing the PCB area beyond a certain point (for this application say beyond 10000 mm^2) only ensures minimal thermal improvement. In all cases, the dissipating IC was right in the center of the PCB. The other recommendations listed above were also implemented.

Figure 17 and Figure 18 show the preferred 2-layer and 4-layer PCB constructions.

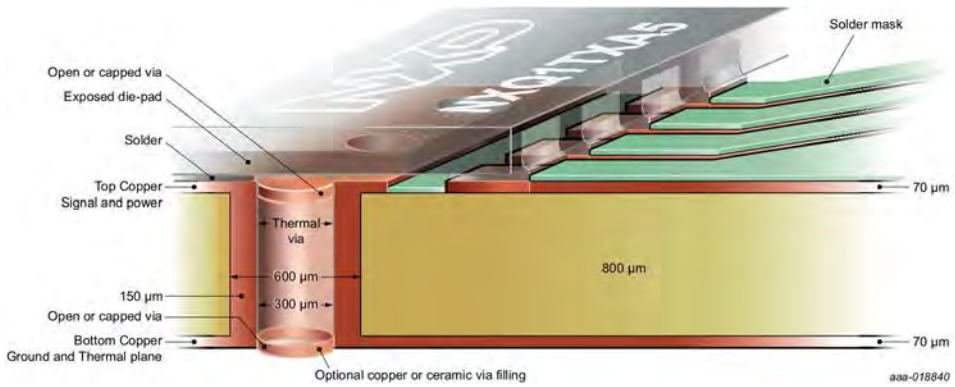


Fig 17. Preferred 2-layer PCB construction

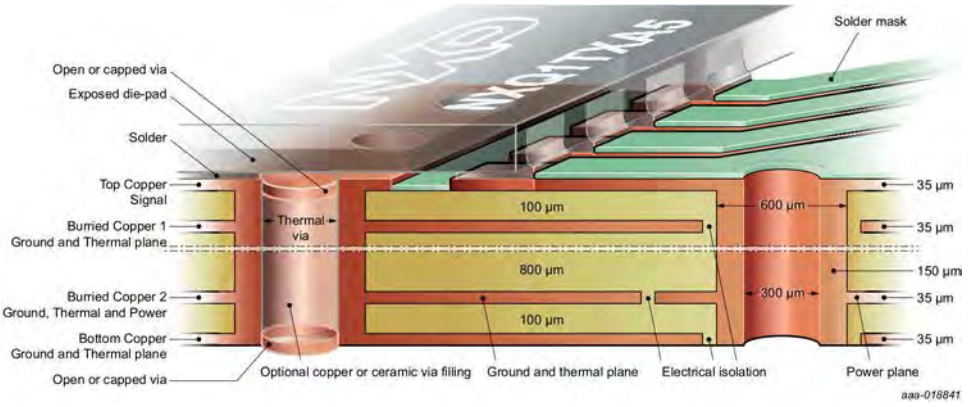


Fig 18. Preferred 4-layer PCB construction

3. Abbreviations

Table 11. Abbreviations

Acronym	Description
EMI	ElectroMagnetic Interference
FOD	Foreign Object Detection
LED	Light-Emitting Diode
NFC	Near Field Communication
NTC	Negative Temperature Coefficient
SPL	Smart Power Limiting
SPR	Static Power Reduction
WPC	Wireless Power Consortium

4. References

[1] **Qi System Description Wireless Power Transfer —** Volume I: Low Power, Part 1: Interface Definition, Version 1.1.2, June 2013

[2] **One-chip 5 V Qi wireless transmitter —** Data sheet, NXP Semiconductors, 2015

[3] **NXQ1TXA5DB1340 one-chip 5 V Qi wireless transmitter demo board —** User manual, UM10917, NXP Semiconductors, 2015

[4] **Qi Receiver Simulator Quick Start Guide —** AVID Technologies Inc, Twinsburg, Ohio USA (www.avid-tech.com)

[5] **AVID Qi Sniffer Quick Start v1.2 —** AVID Technologies Inc, Twinsburg, Ohio USA (www.avid-tech.com)

[6] **NXQ1TXA5 calculation tool —** NXP Semiconductors, contact your sales representative for a copy (salesaddresses@nxp.com)

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