



ADC-AES

ADC-AES Audio Converter card

User manual

Rev. F

A large green circular graphic with a white circle in the center, resembling a stylized 'O' or a ring, located in the bottom right corner of the page.

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Revision history

Current revision of this document is the uppermost in the table below.

Rev.	Repl.	Date	Sign	Change description
F	5	2015-05-11	MB	Cover page update; DoC removed; no other changes to content
5	4	2010-06-10	AA	New template. Updated Appendix A.
4	3	2007-10-23		New front page and removed old logo.
3	2	2007-09-10		Added Materials Declaration and EFUP; updated EC Declaration of Conformity.
2	1	2004-02-10		C2 backplane description
1	B	2002-11-02		Typos, formatting, specifications.
B	A	2002-09-04		Figures, corrected details for first production run.
A	-	2001-01-25		Preliminary version

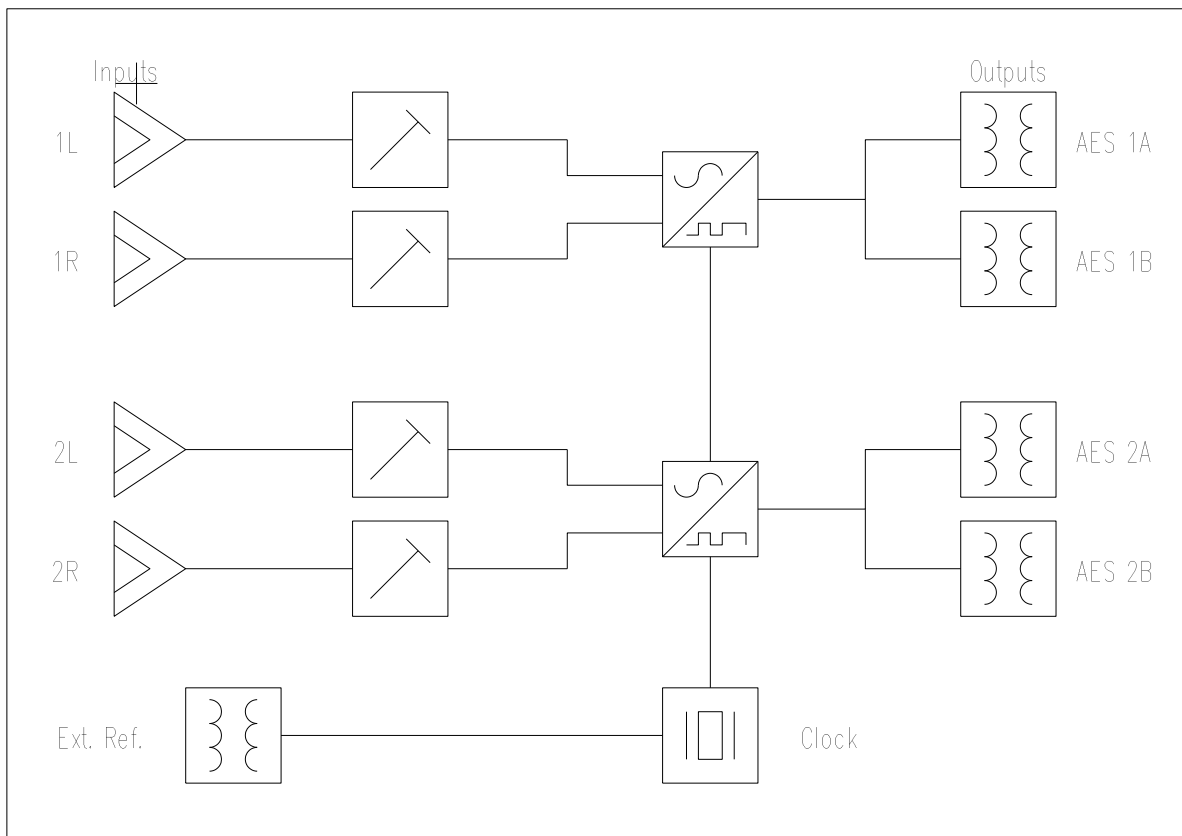
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1 General description

The ADC-AES card is a reference quality audio A/D converter. It is one of the Flashlink series of modules. It will convert four analogue audio channels with the highest possible quality and produce two AES3 stereo digital audio signals. Each converter has dual AES outputs which are available on the C1 backplane connector. Only one output per converter is available on the C2 backplane. The card may be used with, or without an external AES clock signal and may be run at nominal or double sampling rates. The ADC-AES has internal clocks for 48 kHz and 44.1 kHz based rates but can be used with any external sampling rate 29 kHz – 100 kHz.

2 Block diagram



3 Technical description

The ADC-AES card was designed as a reference audio converter with a highly audio optimised signal path. Careful design of the input circuitry was needed to maintain a high dynamic range whilst minimising distortion. Jitter of the sampling clock is kept to a minimum by the use of a two-stage PLL clock recovery circuit as recommended in AES-2id.

The analogue audio input circuit is a DC coupled, electronic differential amplifier with a gain of -6 dB. The use of input coupling capacitors would degrade the common mode rejection ratio of the input amplifiers. The signal is then AC coupled to an inverting variable gain stage with gains ranging from -8 dB to -17 dB. The gain variation is performed by switching extra resistors in parallel with the input resistor. The stage feeds the input of the A/D converter directly and the choice of op-amp is quite important in order to achieve a low output noise. The stage also feeds an inverting amplifier, which feeds the inverting A/D converter input. This last stage must have an output noise that is even lower than the previous one.

The AES transmitter chip is configured as the interface clock master. This means that the AES output chip produces the bit clock and the word clock required for the serial interfaces between itself and the converters.

The A/D converter chip uses the same master clock frequency for both nominal and double sample rates. This means that we can use the same crystal oscillators for both sampling modes. The external sync signal can be nominal or double the sample rate, independent of the sampling mode on the card, i.e. the card may sample at 96 kHz while the external sync signal is a 48 kHz signal. The sampling mode is set with the DIP switch 2-8 for both converters.

Clock jitter in a reference A/D converter must be kept very low. By the time the external clock signals reach the card they often have more jitter than the internal clock oscillator. The best solution is realized when using the external AES signal to lock the internal crystal oscillator. The ADC-AES has an advanced clock management system that locks quickly to an external clock. The master clock is taken temporarily from the AES receiver but switches to the low jitter oscillator when it, in turn, has locked to the received signal. The ADC-AES has oscillators for 48 and 44.1 based sampling rates but only one will be powered up at any time. When power is applied to the card, the sample rate is decided by the DIP switch configuration. If an external AES signal is detected, the input AES circuit reports the received sample rate to the microcontroller which then switches to the appropriate oscillator if necessary or possible. The external sync signal always has priority and the sampling rate of the card will always be derived from the external sync signal, if present.

Each converter has dual independent AES3 transformer isolated 110 Ω outputs which are available on the 15 pin D-sub connector of the C1 backplane module. The optional C2 backplane connector should be used if 75 Ω AES-3id outputs are required. The C2 backplane connector has only one output per converter due to space restrictions.

The card has a microcontroller which controls the clock switching, the AES drivers and controls the LEDs on the front of the card. It also monitors the 5V and ± 15 V power voltages and reports them to the Gyda system controller when present.

4 Configuration

The ADC-AES has two eight-way miniature DIP switches located near the front of the card.

Groups of 3 switches control the input gain of the analogue inputs. Switches marked 1L and 1R control the levels for converter 1 while switches marked 2L and 2R control the levels for converter 2. The settings for the level switches are presented in the following table.

4.1 Analogue input levels

0 corresponds to off. 1 corresponds to on.

The three numbers in the top row should be read as: S2,S1,S0.

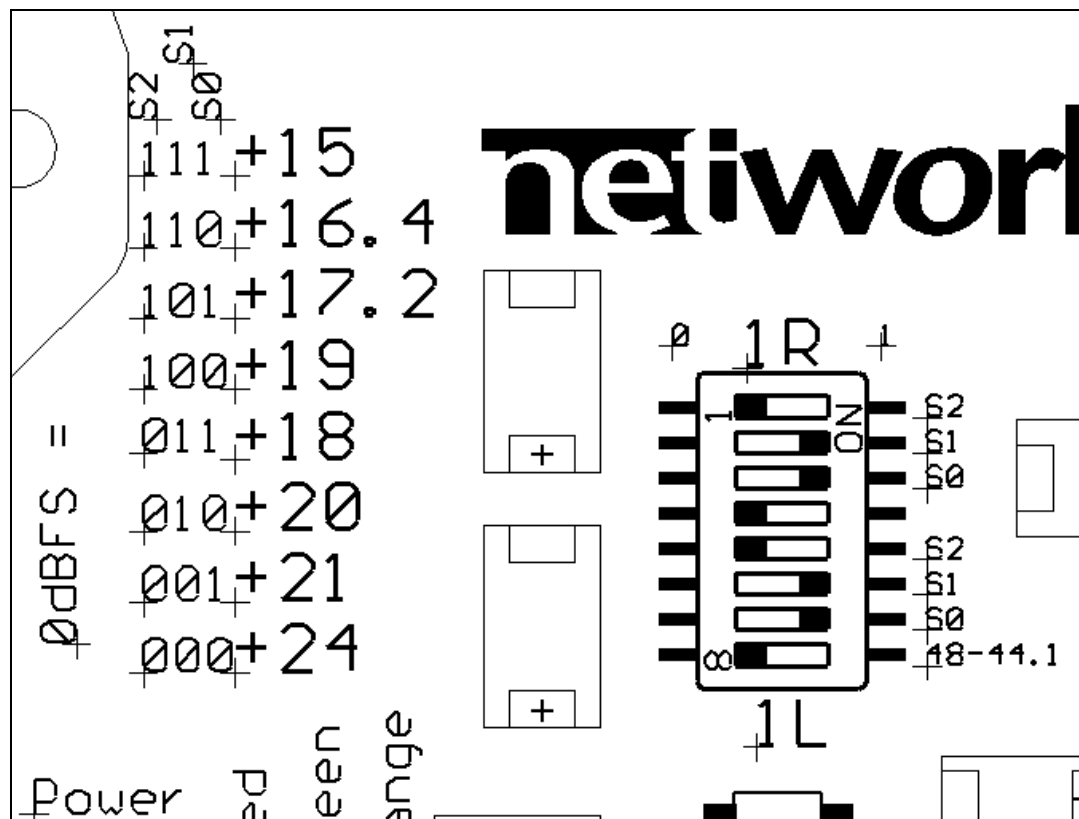
Switches	000	001	010	011	100	101	110	111
dBu @ 0 dBFS	+24	+21	+20	+18	+19	+17.2	+16.4	+15

Switch 1-8 sets the default sample rate. 0 = 48 kHz, 1 = 44.1 kHz.

Switch 2-8 sets the sampling mode. 0 is nominal rate (48 or 44.1 kHz), 1 is double rate (96 or 88.2 kHz).

Note: The external sync input always takes priority for the sampling rate.

The figure below shows the DIP switch SW1 set for + 18 dBu @ 0 dBFS and an internal sampling rate of 48 kHz.



5 Specifications

5.1 Measurement conditions

Sampling rate	48 kHz
Ambient temperature	25 °C
Measurement bandwidth	20 Hz – 20 kHz
Detector	RMS
Input overload level (0 dBFS)	+ 24 dBu

5.2 Analogue inputs

Number of inputs	4 electronically balanced
Common mode voltage tolerance	±30 V
Input impedance (differential)	25 kΩ
Frequency response	10 Hz – 21.5 kHz +0 dB , -1 dB
Passband ripple	±0.001 dB
Group delay	65 samples
Stopband attenuation	110 dB
Dynamic range ¹	Min. 112 dB(A) (0 dBFS @ +15 dBu) Typ. 117 dB(A)
THD+N @ -1 dB FS	Max. –95 dB Typ. –102 dB
Intermodulation distortion ²	@ - 12 dB FS Max. –85 dB Typ. –104 dB
Crosstalk	Max. –100 dB Typ. –110 dB
CMRR (0 Hz – 8 kHz)	Min. 70 dB Typ. 80 dB

5.3 Digital outputs

Internal sampling rates	44.1, 48, 88.2 and 96 kHz
Intrinsic jitter	200 ps peak-peak
JTF corner frequency	2 Hz
JTF peaking	0 dB

5.3.1 ADC-AES-C1 backplane

Number of outputs	2 * 2 transformer balanced
Format	AES3-1992
Output impedance	110Ω

¹ |(THD+N of –60 dB FS signal)| + 60

² SMTE 4:1 60 Hz + 7 kHz

Connector	D-sub 15 pin female.
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5.3.2 ADC-AES-C2 backplane

Number of outputs	2 unbalanced
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Format	AES-3id
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Output impedance	75Ω
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Connector	BNC
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5.4 Digital input

External sampling rates	29 kHz – 100 kHz
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5.4.1 ADC-AES-C1 backplane

Format	AES3-1992
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Input impedance	110Ω
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Connector	D-sub 15 pin female.
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5.4.2 ADC-AES-C2 backplane

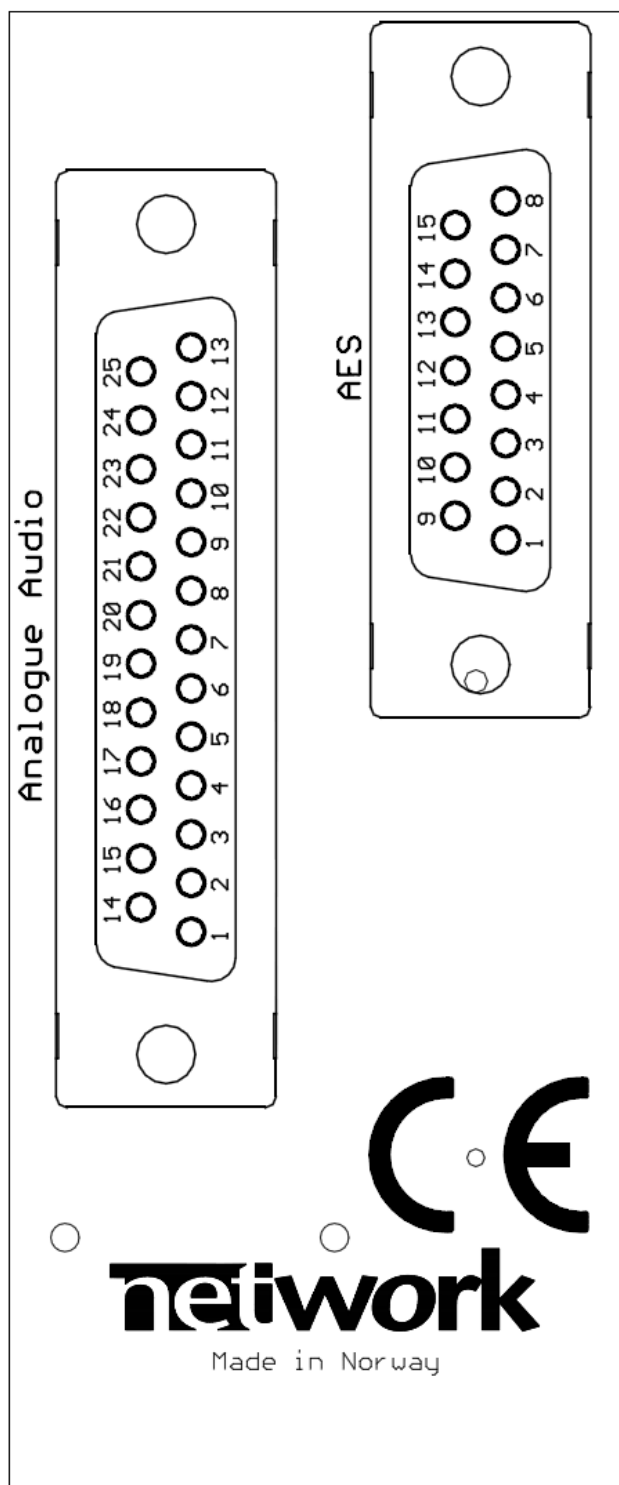
Format	AES-3id
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Input impedance	75Ω
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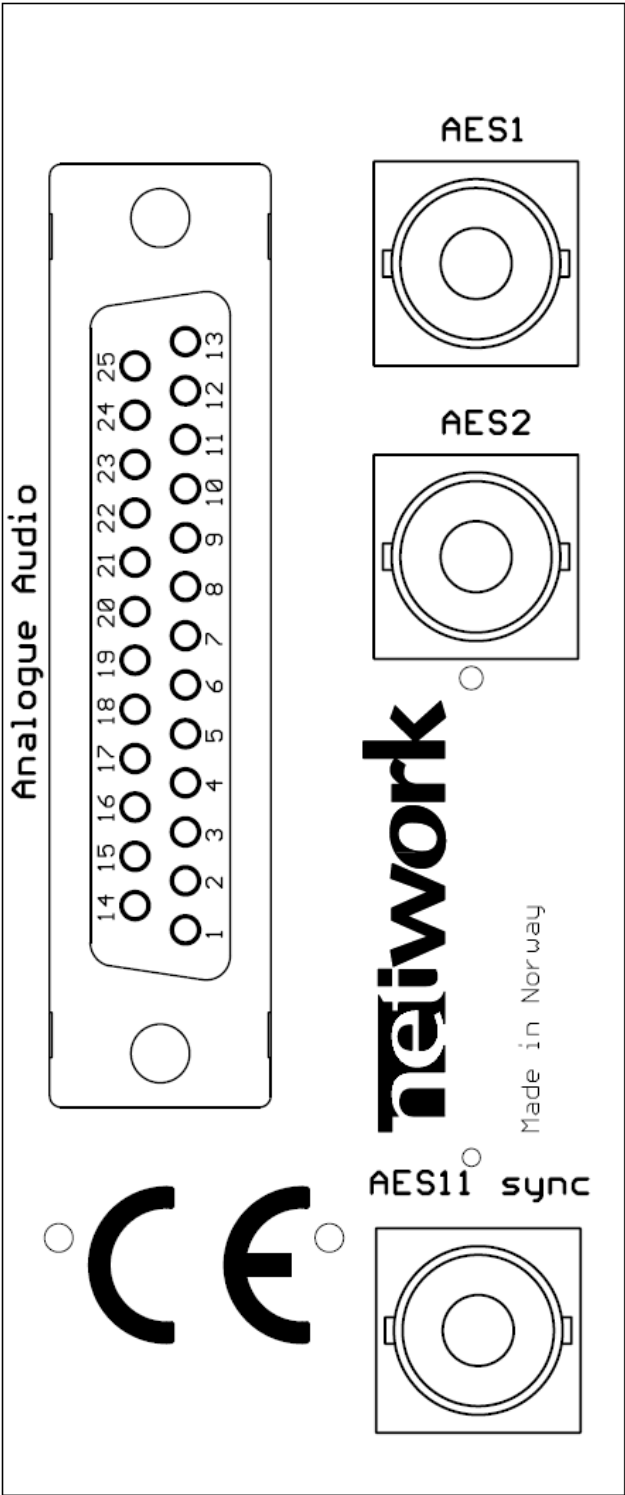
Connector	BNC
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6 Connector modules

6.1 ADC-AES-C1



6.2 ADC-AES-C2



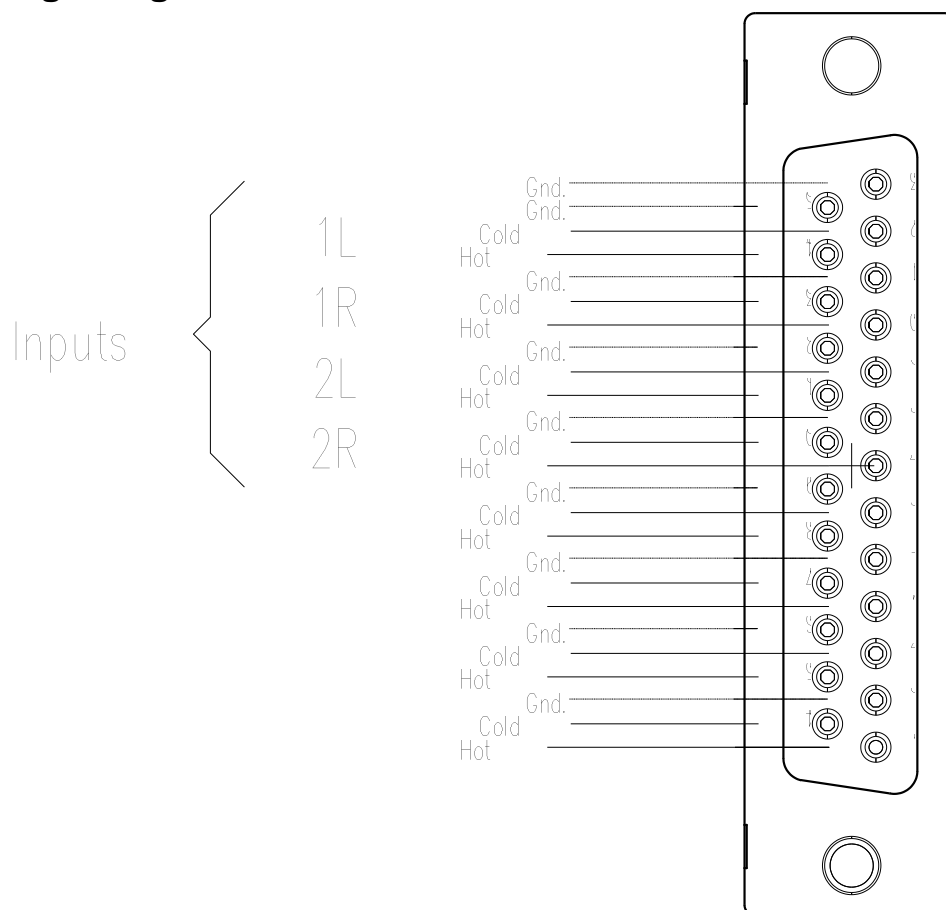
6.3 Mounting of the connector module

Usually, the backplane modules will be delivered mounted in a frame which is part of the order.

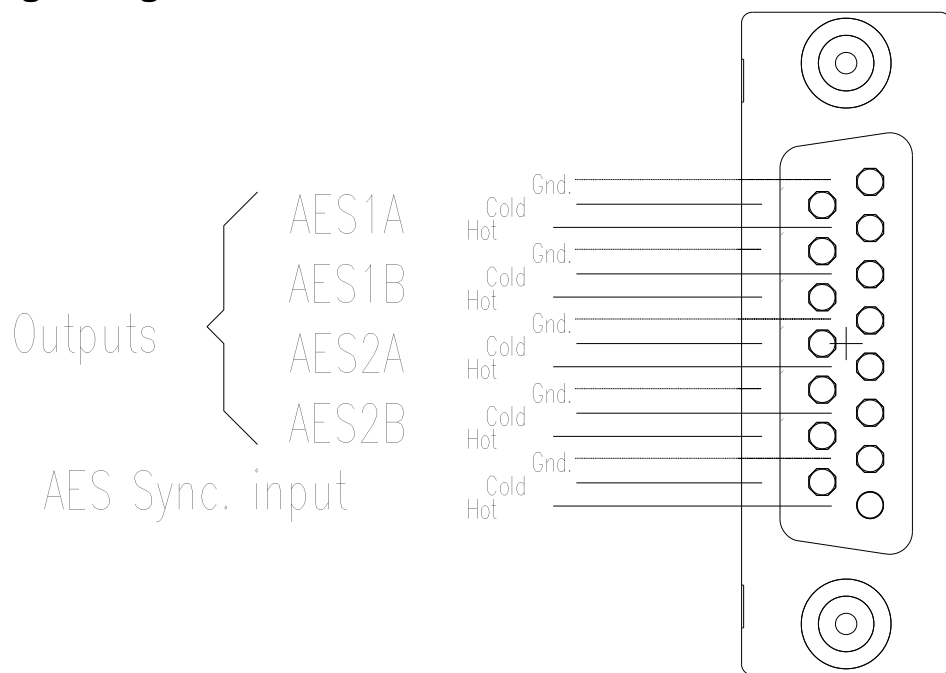
The details of how the connector module is mounted if delivered unmounted, can be found in the user manual for the frame FR-2RU-10-2.

This manual is also available from our web site: <http://www.nevion.com/>

6.4 Analogue signals



6.5 C1 digital signals



7 Module status

The status of the module can be monitored in two ways.

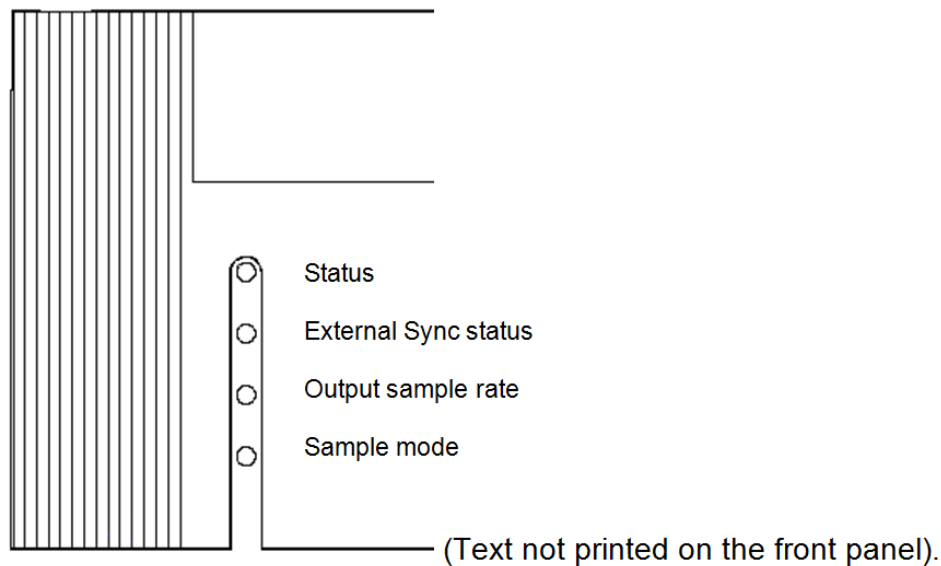
Gyda-SC (system controller).

LED's at the front of the sub-rack.

The LED's are mounted on the module itself, whereas the Gyda-SC is a separate module giving detailed information of the status of the card. The functions of the LED's are described in sections 7.1. The Gyda-SC is described in a separate user manual.

7.1 LED's – Light Emitting Diodes

The status of the module can be easily monitored visually by the LED's at the front of the module. The LED's are visible through the front panel as shown below.



Diode overview of ADC-AES

The ADC-AES has 4 LED's each showing a status. The position of the different LED's is shown above.

Diode \ state	Red LED	Green LED	Orange
Status	Module is faulty: Replace	Module is OK Module power is OK	Card has not been programmed
External Sync. status	Loss of sync. signal No electrical input signal.	Input signal present and identical to the DIP setting	Input signal present but different to the DIP setting
Output Sample rate	Other sample rate	48 kHz / 96 kHz	44.1 kHz / 88.2 kHz
Sample mode	NA	Normal mode	Double rate

General environmental requirements for Nevion equipment

1. The equipment will meet the guaranteed performance specification under the following environmental conditions:
 - Operating room temperature range: 0°C to 50°C
 - Operating relative humidity range: <90% (non-condensing)
2. The equipment will operate without damage under the following environmental conditions:
 - Temperature range: -10°C to 55°C
 - Relative humidity range: <95% (non-condensing)

Product Warranty

The warranty terms and conditions for the product(s) covered by this manual follow the General Sales Conditions by Nevion, which are available on the company web site:

www.nevion.com

Appendix A Materials declaration and recycling information

A.1 Materials declaration

For product sold into China after 1st March 2007, we comply with the “Administrative Measure on the Control of Pollution by Electronic Information Products”. In the first stage of this legislation, content of six hazardous materials has to be declared. The table below shows the required information.

組成名稱 Part Name	Toxic or hazardous substances and elements					
	鉛 Lead (Pb)	汞 Mercury (Hg)	鎘 Cadmium (Cd)	六价铬 Hexavalent Chromium (Cr(VI))	多溴联苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenyl ethers (PBDE)
ADC-AES	○	○	○	○	○	○
O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.						
X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.						

This is indicated by the product marking:



A.2 Recycling information

Nevion provides assistance to customers and recyclers through our web site <http://www.nevion.com/>. Please contact Nevion's Customer Support for assistance with recycling if this site does not show the information you require.

Where it is not possible to return the product to Nevion or its agents for recycling, the following general information may be of assistance:

- Before attempting disassembly, ensure the product is completely disconnected from power and signal connections.
- All major parts are marked or labeled to show their material content.
- Depending on the date of manufacture, this product may contain lead in solder.
- Some circuit boards may contain battery-backed memory devices.