MB835

Intel® EP80579
Motherboard

USER'S MANUAL

Version 1.0

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Introduction
Product Description

The MB835 motherboard incorporates the Intel® EP80579 Integrated Processor for embedded computing. The EP80579 System on a Chip (SoC) is a new generation processor that is cost optimized for a wide range of applications. EP80579 delivers the balance of a powerful IA-32 processor core, standards-based chipset, and acceleration /communications-focused I/O capabilities.

The EP80579 SoC integrates features into a single device with memory controller hubs (IMCH) and I/O controller hubs (IICH). The IMCH has built-in memory controllers for external memory and the IICH has standard IA I/O peripheral capabilities.

The MB835's EP80579 IA-32 core is a derivative of the Intel® Pentium® M processor. This low power IA-32 core is based on 90-nm process technology featuring 256-Kbyte L2 cache and 400/533 MHz quad-pumped internal front-side bus (FSB). With two DDR2 DIMM sockets on board, the board supports up to 2GB of DDR2 system memory. It integrates three Gigabit Ethernet MAC interfaces. The MAC fully implements the IEEE 802.3z, Carrier Sense Multiple Access with Collision Detection (CSMA/CD) method and physical layer specifications The GbE features include RGMII/RMII interface to PHY devices Multi-speed operation 10/100/1000 Mbps.

The main features of the ECX810 board are:
- Supports Intel EP80579 processors in 600/1066/1200MHz.
- EP80579 built-in USB 2.0 host controller supports 2 ports.
- EP80579 built-in SATA controller supports 2 ports.
- Two DDR2 SDRAM DIMM, Max. 2GB memory.
- Integrated Three Gigabit Ethernet MACs + PHY.
- Intel 82574L PCI-E X1 Controller.
- 2x SATA, 2x USB 2.0, 4x COM, Watchdog timer.
- Interface connector for daughter board (ID835/IBP835).

Checklist

Your ECX810 package should include the items listed below.

- The MB835 Mother board
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Optional cables for: Keyboard/mouse, Serial port, Serial ATA

MB835 Specifications

Model	MB835 Motherboard
Form Factor	Custom Size
Processor	Intel EP80579 SOC processor with ASU & SSU Frequency: 600 / 1000 /1200 MHz L2 cache: 256kb
Memory	2x DDR2 sockets, supporting DDR2 400,533,667 and 800 Max 2GB memory with ECC (600Mhz CPU at DDR2 533 only)
Chipset	Integrated Intel® Architecture (IA) and chipset (MCH/ICH) technology; 1088-Ball FCBGA package
BIOS	Award BIOS
PCIe Switch	PEX8509 of PLX: Gen1 8Lanes / 8Ports PCIe switch (up: 4 lanes /down:1lanes) Connect from: PCIeX4 bus of EP80579 Connect to : Intel 82574L GbE 　　　JM368 PCIe to PATA bridge 　　　PEX8112 PCIe to PCI bridge 　　　PCIeX1 golden finger
PCI bridge	PEX8112 of PLX: PCIe to PCI bridge, max for 4PCI Connect from: PCIeX1 bus of PEX8509 downstream Connect to: HIFN 7964 IPSec onboard MiniPCI slot PCI32 golden finger
Ethernet controller	Intel EP80579 integrated 3x GbE MACs(RGMII) link to Marvell 88E1145 Quad PHYs with 3x RJ45 on the edge connector Onboard Intel 82574L GbE with RJ45 on the edge connector
Ethernet bypass	Default ETH0 ~ ETH3 with bypass, optional function, can be controlled by GPIO and WDT)
IPSec	HIFN 7964 (pin to pin compatible with 7965 and 7966, optional function) Connect from: PCI bus from PEX8112 (PCI bus must be 32bit / 66Mhz)
USB	Intel EP80579 build-in 2X USB2.0 host controller with 1x USB stack connector on edge connector
SATA	Intel EP80579 build-in 2X SATA controller with 2XSATA onboard 7-pin shrouded vertical connector
Compact flash (PATA)	Jmicron JM368 PCIe to PATA bridge Connect from: PCIeX1 bus of PEX8509 downstream Connect to: onboard CF type II socket, support UDMA mode
LPC I/O	Winbond W83627DHG COM1 with RJ45 on edge connector for console redirection COM2 for LCM function, Hardware monitor, COM3 & COM4 from EP80579 built in UART with box header
Keyboard / mouse	PS/2 keyboard & mouse support with pitch 2.54mm pin header
Expansion slot & connector	1x onboard MiniPCI slot 1x LAN module expansion connector 1x pitch 2.0mm 44-pin HDD connector for ID370 LED board
Edge connector	4x RJ45 connector with LED for GbE, 1x USB vertical connector 1x console redirection via RJ45 without LED
Onboard connector	ATX 20P connector, 3x 3P fan header with Smart FAN function 2x SATA controller with 2x SATA onboard 7-pin shrouded vertical connector 1x COM2 port for LCM, 2x COM ports for COM3 & 4 1x PS/2 keyboard/mouse, 1x USB2.0, 1x right angle SAMTEC MEC1-140-02-L-D-RA1-SL Hi-Speed connector for LAN module IBP835
TDM	Intel EP80579 Integrated Processor with QuickAssist Technology Reserved interface (headers) for future connection to proprietary E1/T1 board
Power	ATX
WDT	Yes (256 segments: 0, 1, 2,..., 255 sec/min)

Model	IBP835 LAN Module
Form Factor	Custom size
Golden finger	PCIeX4 bus of M/B
PCIe switch	PEX8509 of PLX: Gen1 5 lanes / 8 ports PCIe switch (up: 4lanes /down:1lanes) Connect from: PCIeX4 bus of M/B Connect to 4x Intel 82574L GbE
Ethernet controller	4x onboard Intel 82574L GbE (optional 2x GbE) Connect from: PCIeX1 bus of PEX8509 downstream Connect to: RJ45 on edge connector
Edge connector	4x RJ45 with LED connector

Model	ID835 Riser Card
Form Factor	Custom size
Expansion slot (M/B side)	1x PCI and 1x PCIeX1 slot, connect from M/B
Expansion slot	Top: PCI slot, for additional card Bottom: PCIeX4 slot, for additional card

Board Dimensions
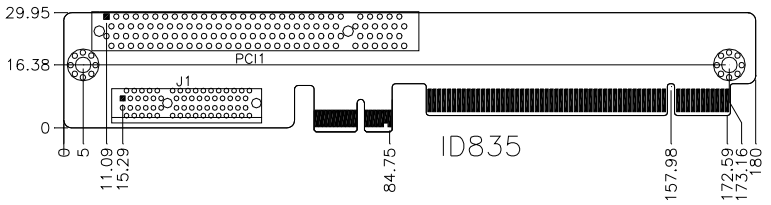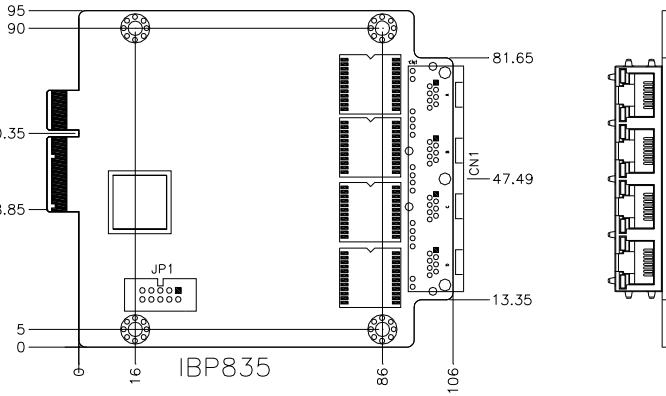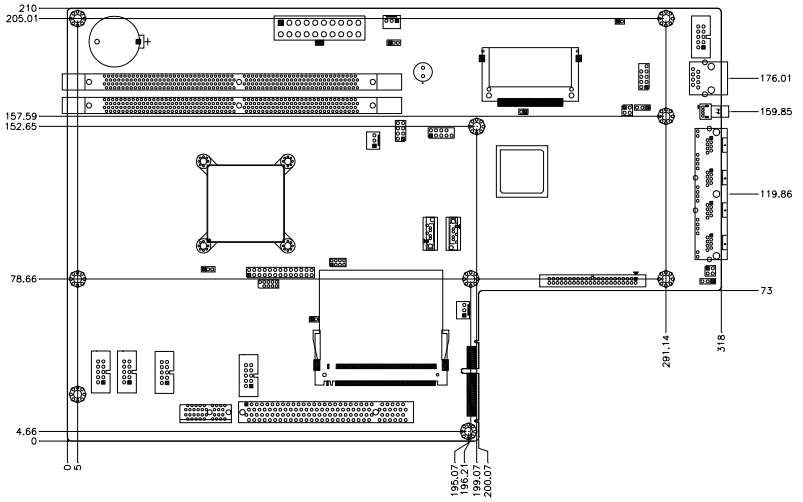
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Installations

This section provides information on how to use the jumpers and connectors on the MB835 in order to set up a workable system. The topics covered are:
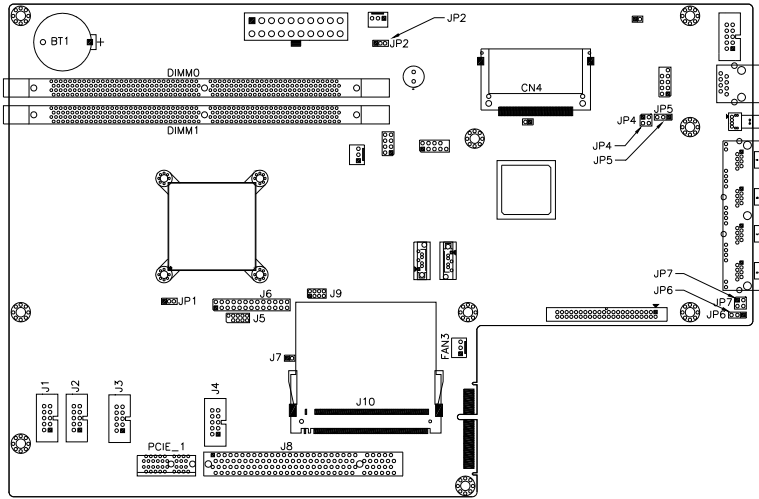
Setting the Jumpers

Jumpers are used on MB835 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on MB835 and their respective functions.

Jumper Locations on MB835

JP1: Clear CMOS Setting

JP1	Setting
□ □ □ 1 2 3	Normal
□ □ □ 1 2 3	Clear CMOS

JP2: AT (Emulation)/ATX Power Selection

JP2	Power Select
□ □ □ 1 2 3	AT (Emulation)
□ □ □ 1 2 3	ATX

Note: AT (Emulation) does not require pressing the power button to turn on the system; plugging the AC power will turn on the system.

JP3: CF Card Master / Slave Selection

JP3	CF Card Setting
□ □ Short	Master
□ □ Open	Slave

JP4, JP5: Watchdog Timer & LAN1/LAN2 Bypass Settings

JP4, JP5 Setting	Function
JP4 Pin 1-2 & 3-4 Open JP5 Pin 1-2 Closed	System will bypass LANs upon the time out of watchdog timer.
JP4 Pin 1-2 & 3-4 Open JP5 Pin 2-3 Closed	System LANs bypass function controlled by SIO GPIO27.
JP4 Pin 1-2 & 3-4 Closed JP5 Pin 1-2 Closed (Default)	System will reboot upon the time out of watchdog timer.

JP6, JP7: Watchdog Timer & LAN3/LAN4 Bypass Settings

JP6, JP7 Setting	Function
JP7 Pin 1-2 & 3-4 Open JP6 Pin 1-2 Closed	System will bypass LANs upon the time out of watchdog timer.
JP7 Pin 1-2 & 3-4 Open JP6 Pin 2-3 Closed	System LANs bypass function controlled by SIO GPIO28.
JP7 Pin 1-2 & 3-4 Closed JP6 Pin 1-2 Closed (Default)	System will reboot upon the time out of watchdog timer.

Connectors on MB835

The connectors on MB835 allows you to connect external devices such as keyboard, floppy disk drives, hard disk drives, printers, etc. The following table lists the connectors on MB835 and their respective functions.

Connector Locations on MB835

CN1: ATX Power Supply Connector

Signal Name	Pin #	Pin #	Signal Name
3.3V	11	1	3.3V
-12V	12	2	3.3V
Ground	13	3	Ground
PS-ON	14	4	+5V
Ground	15	5	Ground
Ground	16	6	+5V
Ground	17	7	Ground
-5V	18	8	Power good
+5V	19	9	5VSB
+5V	20	10	+12V

CN2, CN3: Serial ATA Connector

CN4: Compact Flash Connector

CN5: Front Side Bridge Board to ID370
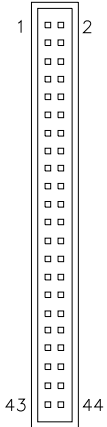
Signal Name	Pin #	Pin #	Signal Name
PWR-SW	1	2	GND
Reset-SW	3	4	GND
Speaker	5	6	VCC
VCC	7	8	VCC
GND(PWR LED)	9	10	Pull up to VCC
HDD LED	11	12	Pull up to VCC
RELAY LED	13	14	Pull up to VCC
GND	15	16	GND
GND	17	18	GND
GPO0	19	20	GPI0
GPO1	21	22	GPI1
GPO2	23	24	GPI2
GPO3	25	26	GPI3
GPO4	27	28	GPI4
GPO5	29	30	GPI5
GPO6	31	32	GPI6
GPO7	33	34	GPI7
VCC	35	36	VCC
GP24	37	38	GP34
GP25	39	40	GPIO18
NC	41	42	NC
VCC3	43	44	VCC3

CN8   CN7   CN6
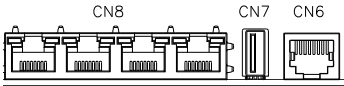
CN6: Console Port
The Console Port is an RJ45 RS-232 port.
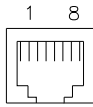
Pin #	Signal Name
1	RTS, Request to send
2	DTR, Data terminal ready
3	TXD, Transmit data
4	Ground
5	DCD, Data carrier detect
6	RXD, Receive data
7	DSR, Data set ready
8	CTS, Clear to send

1   8

CN7: USB0 Port Connector

CN8: RJ45 Gigabit LAN Connectors
These four LAN (LAN1/2/3/4) connectors are used in conjunction with the four Intel 82574L Gigabit Ethernet controllers on the board.

J5: SPI Pin Header (Debug Only)

J6: TDM T1/E1 Connector
J6: The TDM interface for support up to 12 T1/E1 links.
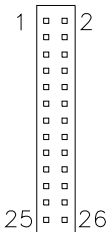
Signal Name	Pin #	Pin #	Signal Name
+3.3V	1	2	Ground
RX_CLK0	3	4	RX_CLK2
TX_CLK0	5	6	TX_CLK2
RX_FRAME0	7	8	RX_FRAME2
TX_FRAME0	9	10	TX_FRAME2
RX_DATA_IN0	11	12	RX_DATA_IN2
TX_DATA_OUT0	13	14	TX_DATA_OUT2
RX_CLK1	15	16	SSP_EXCTCLK
TX_CLK1	17	18	SSP_SCLK
RX_FRAME1	19	20	SSP_SFRM
TX_FRAME1	21	22	SSP_RXD
RX_DATA_IN1	23	24	SSP_TXD
TX_DATA_OUT1	25	N/A	N/A

1   2

25   26

J8, PCIE_1: PCI Slot and PCIE X1 Slot for ID835 add-on card

J10: Mini PCI Connector

J11: LPC 80 Port Pin Header (Debug Use Only)
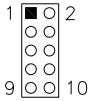
Signal Name	Pin	Pin	Signal Name
LAD0	1	2	PLTRST_N
LAD1	3	4	L_FRAME_N
LAD2	5	6	+3.3V
LAD3	7	8	GND
CLK33	9	10	Cut Pin

J13: PS/2 Keyboard and Mouse Connector
J13, a 10-pin header, has functions for both keyboard and mouse.
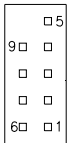
Signal Name	Pin #	Pin #	Signal Name
N.C.	10	5	N.C.
KB clock	9	4	Mouse clock
KB data	8	3	Mouse data
Vcc	7	2	Vcc
Ground	6	1	Ground

J14: USB1 Connector
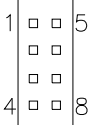
Signal Name	Pin #	Pin #	Signal Name
VCC	1	2	NC
USB2-	3	4	NC
USB2+	5	6	NC
Ground	7	8	NC

J15, J1, J2: COM2, COM3, COM4 Serial Port
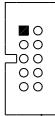
Pin #	Signal Name
1	DCD, Data carrier detect
2	RXD, Receive data
3	TXD, Transmit data
4	DTR, Data terminal ready
5	Ground
6	DSR, Data set ready
7	RTS, Request to send
8	CTS, Clear to send
9	RI, Ring indicator

J16: PCIE X4 Slot For IBP835 Gigabit LAN Add-on Card

FAN1, FAN2, FAN3: CPU Fan & System Fan Power Connectors

FAN1, FAN2, FAN3 is a 3-pin header for system fans. The fan must be a 12V (500mA).

Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

DIMM0, DIMM1: DDR2 DIMM Socket

MB835 supports two DDR2 DIMM sockets for a maximum memory of 2GB, DDR2 400/533/667/800.

Note:

Used 600MHz processor will support DDR2 400/533/667MHz

Used 1200MHz & 1066MHz processors will support DDR2 400/533/667/800MHz.

(x1: One DIMM, x2: Two DIMM, DS: Double Side, SS: Single Side)

	DIMM0	DIMM1
x1 SS Memory Modules	✓	X
x1 DS Memory Modules	✓	X
x2 SS Memory Modules	✓	✓

J1: PCIE X4 Slot (Signal only support PCIE X1)

PCI1: PCI Slot

## CONNECTOR LOCATIONS ON IBP835

CN1: RJ45 Gigabit LAN Connectors
These four LAN (LAN1/2/3/4) connectors are used in conjunction with the four Intel 82574L Gigabit Ethernet controllers on the board.
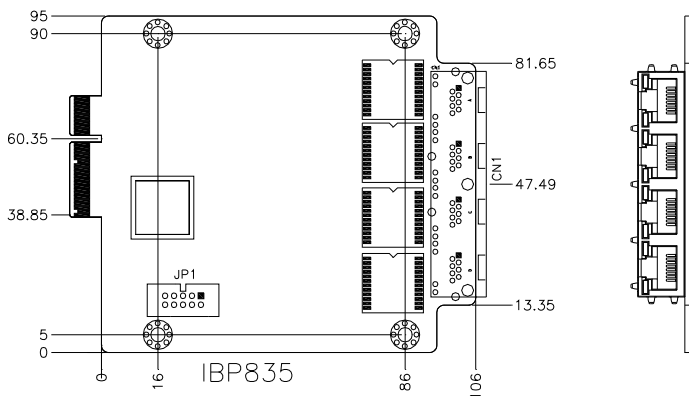
BIOS Setup

This chapter describes the different settings available in the Award BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The Award BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also adds virus and password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The Award BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the Award BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

```
          Press  <DEL>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Phoenix - AwardBIOS CMOS Setup Utility

Standard CMOS Features	Frequency/Voltage Control
Advanced BIOS Features	Load Fail-Safe Defaults
Advanced Chipset Features	Load Optimized Defaults
Integrated Peripherals	Set Supervisor Password
Power Management Setup	Set User Password
PnP/PCI Configurations	Save & Exit Setup
PC Health Status	Exit Without Saving
ESC : Quit	↑ ↓ → ← : Select Item
F10 : Save & Exit Setup	
Time, Date, Hard Disk Type…	

The section below the setup items of the Main Menu displays the
control keys for this menu. At the bottom of the Main Menu just below
the control keys section, there is another section, which displays
information on the currently highlighted item in the list.

Note: *If the system cannot boot after making and saving system
changes with Setup, the Award BIOS supports an override to
the CMOS settings that resets your system to its default.*

Warning: *It is strongly recommended that you avoid making any
changes to the chipset defaults. These defaults have been
carefully chosen by both Award and your system
manufacturer to provide the absolute maximum performance
and reliability. Changing the defaults could cause the system
to become unstable and crash in some cases.*

Standard CMOS Setup

"Standard CMOS Setup" choice allows you to record some basic hardware configurations in your computer system and set the system clock and error handling. If the motherboard is already installed in a working system, you will not need to select this option. You will need to run the Standard CMOS option, however, if you change your system hardware configurations, the onboard battery fails, or the configuration stored in the CMOS memory was lost or damaged.

<div align="center">

Phoenix - AwardBIOS CMOS Setup Utility
Standard CMOS Features

</div>

		Item Help
Date (mm:dd:yy)	Tue, Jul 1 , 2008	
Time (hh:mm:ss)	12 : 00 : 00	Menu Level >
IDE Channel 0 Master	None	Change the day, month,
IDE Channel 0 Slave	None	Year and century
IDE Channel 1 Master	None	
IDE Channel 1 Slave	None	
Video	EGA/VGA	
Halt On	All Errors	
Base Memory	640K	
Extended Memory	1046528K	
Total Memory	1047552K	

At the bottom of the menu are the control keys for use on this menu. If you need any help in each item field, you can press the <F1> key. It will display the relevant information to help you. The memory display at the lower right-hand side of the menu is read-only. It will adjust automatically according to the memory changed. The following describes each item of this menu.

Date
The date format is:

Day :	**Sun to Sat**
Month :	**1 to 12**
Date :	**1 to 31**
Year :	**1999 to 2099**

To set the date, highlight the "Date" field and use the PageUp/ PageDown or +/- keys to set the current time.

Time

The time format is: **Hour   : 00 to 23**
Minute : 00 to 59
Second : 00 to 59

To set the time, highlight the "Time" field and use the <PgUp>/ <PgDn> or +/- keys to set the current time.

IDE Channel Master/Slave

The onboard PCI IDE connector provides Primary and Secondary channels for connecting up to two IDE hard disks or other IDE devices.

Press <Enter> to configure the hard disk. The selections include Auto, Manual, and None. Select 'Manual' to define the drive information manually. You will be asked to enter the following items.

Capacity :	Capacity/size of the hard disk drive
Cylinder :	Number of cylinders
Head :	Number of read/write heads
Precomp :	Write precompensation
Landing Zone :	Landing zone
Sector :	Number of sectors

The Access Mode selections are as follows:
CHS   (HD < 528MB)
LBA   (HD > 528MB and supports Logical Block Addressing)
Large   (for MS-DOS only)
Auto

Video

This field selects the type of video display card installed in your system. You can choose the following video display cards:

EGA/VGA	For EGA, VGA, SEGA, SVGA or PGA monitor adapters. (default)
CGA 40	Power up in 40 column mode.
CGA 80	Power up in 80 column mode.
MONO	For Hercules or MDA adapters.

Halt On

This field determines whether or not the system will halt if an error is detected during power up.

No errors	The system boot will not be halted for any error that may be detected.
All errors	Whenever the BIOS detects a non-fatal error, the system will stop and you will be prompted.
All, But Keyboard	The system boot will not be halted for a keyboard error; it will stop for all other errors
All, But Diskette	The system boot will not be halted for a disk error; it will stop for all other errors.
All, But Disk/Key	The system boot will not be halted for a keyboard or disk error; it will stop for all others.

Advanced BIOS Features

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Phoenix - AwardBIOS CMOS Setup Utility
Advanced BIOS Features

CPU Feature	Press Enter	ITEM HELP
Hard Disk Boot Priority	Press Enter	
Virus Warning	Disabled	Menu Level >
CPU L1 & L2 Cache	Enabled	
Quick Power On Self Test	Enabled	
First Boot Device	Removable	
Second Boot Device	Hard Disk	
Third Boot Device	USB-CDROM	
Boot Other Device	Enabled	
Boot Up NumLock Status	On	
Gate A20 Option	Fast	
Typematic Rate Setting	Disabled	
Typematic Rate (Chars/Sec)	6	
Typematic Delay (Msec)	250	
Security Option	Setup	
APIC Mode	Enabled	
MPS Version Control for OS	1.4	
OS Select For DRAM>64MB	Non-OS2	
Small Logo (EPA) Show	Disabled	

CPU Feature
Press Enter to configure the settings relevant to CPU Feature.

Hard Disk Boot Priority
With the field, there is the option to choose, aside from the hard disks connected, "Bootable add-in Cards" which refers to other external devices.

Virus Warning
If this option is enabled, an alarm message will be displayed when trying to write on the boot sector or on the partition table on the disk.

CPU L1 and L2 Cache
Cache memory is additional memory that is faster than conventional DRAM (system memory). CPUs from 486-type on up contain internal cache memory, and most, but not all, modern PCs have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU. These allow you to enable (speed up memory access) or disable the cache function.

Quick Power On Self Test
When enabled, this field speeds up the Power On Self Test (POST) after the system is turned on. If it is set to *Enabled*, BIOS will skip some items.

First/Second/Third Boot Device
These fields determine the drive that the system searches first for an operating system. The options available include *Removable, Hard Disk*, *CDROM, USB-CDROM* and *Disable*.

Boot Other Device
These fields allow the system to search for an OS from other devices other than the ones selected in the First/Second/Third Boot Device.

Boot Up NumLock Status
This allows you to activate the NumLock function after you power up the system.

Gate A20 Option
This field allows you to select how Gate A20 is worked. Gate A20 is a device used to address memory above 1 MB.

Typematic Rate Setting
When disabled, continually holding down a key on your keyboard will generate only one instance. When enabled, you can set the two typematic controls listed next. By default, this field is set to *Disabled.*

Typematic Rate (Chars/Sec)
When the typematic rate is enabled, the system registers repeated keystrokes speeds. Settings are from 6 to 30 characters per second.

Typematic Delay (Msec)
When the typematic rate is enabled, this item allows you to set the time interval for displaying the first and second characters. By default, this item is set to *250msec.*

Security Option
This field allows you to limit access to the System and Setup. The default value is *Setup*. When you select *System,* the system prompts for the User Password every time you boot up. When you select *Setup,* the system always boots up and prompts for the Supervisor Password only when the Setup utility is called up.

APIC Mode
APIC stands for Advanced Programmable Interrupt Controller. The default setting is *Enabled*.

MPS Version Control for OS
This option is specifies the MPS (Multiprocessor Specification) version for your operating system. MPS version 1.4 added extended configuration tables to improve support for multiple PCI bus configurations and improve future expandability. The default setting is *1.4*.

OS Select for DRAM > 64MB
This option allows the system to access greater than 64MB of DRAM memory when used with OS/2 that depends on certain BIOS calls to access memory. The default setting is *Non-OS/2*.

Small Logo (EPA) Show
The EPA logo appears at the right side of the monitor screen when the system is boot up. The default setting is *Disabled*.

Advanced Chipset Features

This Setup menu controls the configuration of the chipset.

Phoenix - AwardBIOS CMOS Setup Utility
Advanced Chipset Features

		ITEM HELP
System BIOS Cacheable	Enabled	
Video BIOS Cacheable	Disabled	Menu Level >
Memory Hole at 15M-16M	Disabled	
IICH PCI Express Root Port	Press Enter	

System BIOS Cacheable

The setting of *Enabled* allows caching of the system BIOS ROM at F000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may result.

Video BIOS Cacheable

The Setting *Enabled* allows caching of the video BIOS ROM at C0000h-F7FFFh, resulting in better video performance. However, if any program writes to this memory area, a system error may result.

Memory Hole At 15M-16M

In order to improve performance, certain space in memory can be reserved for ISA cards. This memory must be mapped into the memory space below 16 MB. The choices are *Enabled* and *Disabled*.

Integrated Peripherals

This section sets configurations for your hard disk and other integrated peripherals. The first screen shows three main items for user to select. Once an item selected, a submenu appears. Details follow.

Phoenix - AwardBIOS CMOS Setup Utility
Integrated Peripherals

		ITEM HELP
OnChip IDE Device	Press Enter	Menu Level >
Onboard Device	Press Enter	
SuperIO Device	Press Enter	
****IICH Serial Port Device****		
ICH Serial Port 1	3E8/IRQ5	
ICH Serial Port 2	2E8/IRQ7	

Phoenix - AwardBIOS CMOS Setup Utility
OnChip IDE Device

		ITEM HELP
IDE HDD Block Mode	Enabled	Menu Level >
IDE DMA transfer access	Enabled	
On-Chip Primary PCI IDE	Enabled	
IDE Primary Master PIO	Auto	
IDE Primary Slave PIO	Auto	
IDE Primary Master UDMA	Auto	
IDE Primary Slave UDMA	Auto	
On-Chip Secondary PCI IDE	Enabled	
IDE Secondary Master PIO	Auto	
IDE Secondary Slave PIO	Auto	
IDE Secondary Master UDMA	Auto	
IDE Secondary Slave UDMA	Auto	
*** On-Chip Serial ATA Setting ***		
On-Chip Serial ATA	IDE	

Phoenix - AwardBIOS CMOS Setup Utility
Onboard Device

		ITEM HELP
USB Controller	Enabled	Menu Level >
USB 2.0 Controller	Enabled	
USB Keyboard Function	Disabled	
USB Mouse Function	Disabled	

Phoenix - AwardBIOS CMOS Setup Utility
SuperIO Device

		ITEM HELP
POWER ON Function	BUTTON ONLY	Menu Level >
KB Power ON Password	Enter	
Hot Key power ON	Ctrl-F1	
Onboard Serial Port 1	3F8/IRQ4	
Onboard Serial Port 2	2F8/IRQ3	
PWRON After PWR-Fail	Off	

IDE HDD Block Mode
This field allows your hard disk controller to use the fast block mode to transfer data to and from your hard disk drive.

IDE DMA transfer access
Use this field to enable or disable IDE DMA transfer access.

On-chip Primary PCI IDE Enabled
This field, by default, is enabled

On-chip Primary/Secondary PCI IDE
The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select *Enabled* to activate each channel separately.

IDE Primary/Secondary Master/Slave PIO
These fields allow your system hard disk controller to work faster. Rather than have the BIOS issue a series of commands that transfer to or from the disk drive, PIO (Programmed Input/Output) allows the BIOS to communicate with the controller and CPU directly.

The system supports five modes, numbered from 0 (default) to 4, which primarily differ in timing. When Auto is selected, the BIOS will select the best available mode.

IDE Primary/Secondary Master/Slave UDMA
These fields allow your system to improve disk I/O throughput to 33Mb/sec with the Ultra DMA/33 feature. The options are *Auto* and *Disabled*.

USB Controller
The options for this field are *Enabled* and *Disabled*. By default, this field is set to *Enabled*.

USB 2.0 Controller
The options for this field are *Enabled* and *Disabled*. By default, this field is set to *Enabled*. In order to use USB 2.0, necessary OS drivers must be installed first.

USB Keyboard/Mouse Support
The options for this field are *Enabled* and *Disabled*. By default, this field is set to *Disabled***.**

Power ON Function
This field is related to how the system is powered on – such as with the use of conventional power button, keyboard or hot keys. The default is *BUTTON ONLY*.

KB Power ON Password
This field allows users to set the password when keyboard power on is the mode of the Power ON function.

Hot Key Power ON
This field sets certain keys, also known as hot keys, on the keyboard that can be used as a 'switch' to power on the system.

Onboard Serial Port/ICH Serial Port
These fields allow you to select the onboard serial and parallel ports and their addresses. The default values for these ports are:

Onboard Serial Port 1	3F8/IRQ4
Onboard Serial Port 2	2F8/IRQ3
ICH Serial Port 1	3E8/IRQ5
ICH Serial Port 2	2E8/IRQ7

PWRON After PWR-Fail
This field sets the system power status whether *on or off* when power returns to the system from a power failure situation.

Power Management Setup

Phoenix - AwardBIOS CMOS Setup Utility
Power Management Setup

ACPI Function	Enabled	ITEM HELP
Power Management	User Define	Menu Level >
Video Off Method	V/H SYNC+Blank	
Video Off In Suspend	Yes	
Suspend Type	Stop Grant	
Modem Use IRQ	3	
Suspend Mode	Disabled	
HDD Power Down	Disabled	
Soft-Off by PWR-BTTN	Instant-Off	
Wake-Up by PCI card	Enabled	
Resume by Alarm	Disabled	
Date (of Month) Alarm	0	
Time (hh:mm:ss) Alarm	0 : 0 : 0	
** Reload Global Timer Events **		
Primary IDE 0	Disabled	
Primary IDE 1	Disabled	
Secondary IDE 0	Disabled	
Secondary IDE 1	Disabled	
FDD, COM, LPT Port	Disabled	
PCI PIRQ[A-D] #	Disabled	

ACPI Function
Enable this function to support ACPI (Advance Configuration and Power Interface).

Power Management
This field allows you to select the type of power saving management modes. There are four selections for Power Management.

Min. Power Saving	Minimum power management
Max. Power Saving	Maximum power management.
User Define	Each of the ranges is from 1 min. to 1hr. Except for HDD Power Down which ranges from 1 min. to 15 min.

Video Off Method
This field defines the Video Off features. There are three options.

V/H SYNC + Blank	Default setting, blank the screen and turn off vertical and horizontal scanning.
DPMS	Allows BIOS to control the video display.
Blank Screen	Writes blanks to the video buffer.

Video Off In Suspend
When enabled, the video is off in suspend mode. The default setting is *Yes*.

Suspend Type
The default setting for the Suspend Type field is ***Stop Grant***.

Modem Use IRQ
This field sets the IRQ used by the Modem. By default, the setting is *3*.

Suspend Mode
When enabled, and after the set time of system inactivity, all devices except the CPU will be shut off.

HDD Power Down
When enabled, and after the set time of system inactivity, the hard disk drive will be powered down while all other devices remain active.

Soft-Off by PWRBTN
This field defines the power-off mode when using an ATX power supply. The *Instant Off* mode allows powering off immediately upon pressing the power button. In the *Delay 4 Sec* mode, the system powers off when the power button is pressed for more than four seconds or enters the suspend mode when pressed for less than 4 seconds.

Wake up by PCI Card
By default, this field is disabled.

Resume by Alarm

This field enables or disables the resumption of the system operation. When enabled, the user is allowed to set the *Date* and *Time*.

Reload Global Timer Events

The HDD, FDD, COM, LPT Ports, and PCI PIRQ are I/O events that can prevent the system from entering a power saving mode or can awaken the system from such a mode. When an I/O device wants to gain the attention of the operating system, it signals this by causing an IRQ to occur. When the operating system is ready to respond to the request, it interrupts itself and performs the service.

PNP/PCI Configurations

This option configures the PCI bus system. All PCI bus systems on the system use INT#, thus all installed PCI cards must be set to this value.

Phoenix - AwardBIOS CMOS Setup Utility
PnP/PCI Configurations

Init Display First	PCI Slot	ITEM HELP
Reset Configuration Data	Disabled	Menu Level >
Resources Controlled By	Auto (ESCD)	
IRQ Resources	Press Enter	
PCI/VGA Palette Snoop	Disabled	
PCI Express relative items		
Maximum Payload Size	4096	

Init Display First
The default setting is *PCI Card*.

Reset Configuration Data
This field allows you to determine whether to reset the configuration data or not. The default value is *Disabled.*

Resources Controlled by
This PnP BIOS can configure all of the boot and compatible devices with the use of a PnP operating system such as Windows 95.

PCI/VGA Palette Snoop
Some non-standard VGA display cards may not show colors properly. This field allows you to set whether or not MPEG ISA/VESA VGA cards can work with PCI/VGA. When this field is enabled, a PCI/VGA can work with an MPEG ISA/VESA VGA card. When this field is disabled, a PCI/VGA cannot work with an MPEG ISA/VESA card.

Maximum Payload Size
The default setting of the PCI Express Maximum Payload Size is 4096.

PC Health Status

This section shows the parameters in determining the PC Health Status. These parameters include temperatures, fan speeds and voltages.

Phoenix - AwardBIOS CMOS Setup Utility
PC Health Status

CPU Warning Temperature	Disabled	ITEM HELP
Current System Temp	34°C/93°F	Menu Level >
Current CPU1 Temperature	42°C/107°F	
Current CPU2 Temperature	41°C/105°F	
FAN3 Speed	0 RPM	
FAN1 Speed	7031 RPM	
FAN2 Speed	0 RPM	
Vcore	1.30 V	
12 V	12.34 V	
1.8V	1.89V	
5V	4.99 V	
3.3V	3.15V	
VBAT (V)	3.15 V	
5VSB(V)	5.31 V	

CPU Warning Temperature

This field allows the user to set the temperature so that when the temperature is reached, the system sounds a warning. This function can help prevent damage to the system that is caused by overheating.

Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

Frequency/Voltage Control

This section shows the user how to configure the processor frequency.

Phoenix - AwardBIOS CMOS Setup Utility
Frequency/Voltage Control

Auto Detect PCI Clk	Disabled	ITEM HELP
Spread Spectrum Modulated	Disabled	Menu Level >

Auto Detect PCI Clk

This field enables or disables the auto detection of the PCI clock.

Spread Spectrum Modulated

This field sets the value of the spread spectrum. The default setting is *Disabled*. This field is for CE testing use only.

Load Fail-Safe Defaults

This option allows you to load the troubleshooting default values permanently stored in the BIOS ROM. These default settings are non-optimal and disable all high-performance features.

Load Optimized Defaults

This option allows you to load the default values to your system configuration. These default settings are optimal and enable all high performance features.

Set Supervisor Password

These two options set the system password. Supervisor Password sets a password that will be used to protect the system and Setup utility. User Password sets a password that will be used exclusively on the system. To specify a password, highlight the type you want and press <Enter>. The Enter Password: message prompts on the screen. Type the password, up to eight characters in length, and press <Enter>. The system confirms your password by asking you to type it again. After setting a password, the screen automatically returns to the main screen.

To disable a password, just press the <Enter> key when you are prompted to enter the password. A message will confirm the password to be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

Save & Exit Setup

This option allows you to determine whether or not to accept the modifications. If you type "Y", you will quit the setup utility and save all changes into the CMOS memory. If you type "N", you will return to Setup utility.

Exit Without Saving

Select this option to exit the Setup utility without saving the changes you have made in this session. Typing "Y" will quit the Setup utility without saving the modifications. Typing "N" will return you to Setup utility.

Drivers Installation

Intel® EP80579 Software Drivers for Embedded Applications

Intel® EP80579 Software Drivers for Embedded Applications contains all software drivers needed to utilize hardware features on the Intel® EP80579 Integrated Processor.

In addition to the standard OS drivers offered with other Intel architecture platforms, this software package contains drivers specific to developing embedded applications. These drivers provide access to and control of the three Ethernet MACs and two Controller Area Network (CAN) interfaces, as well as internal processor items such as Enhanced Direct Memory Access (EDMA).

Because the core of the Intel EP80579 Integrated Processor is based on Intel architecture, operating systems currently supporting Intel architecture will function without this software package.

For the most recent software package updates from Intel, please visit downloadcenter.intel.com.

• The following operating systems are supported on the Intel EP80579 Integrated Processor:
  – Microsoft Windows XP* Embedded SP2
  – Red Hat Enterprise Linux* 5
  – Wind River Linux* 2.0
  – Wind River VxWorks* 6.6
  – FreeBSD* 6.2

The Driver CD that comes with the board contains software drivers for Windows XP Embedded. The path location of the drivers in the CD is \intel\EP80579.

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Appendix

Bypass and WDT

The bypass function is used to link (or short) two independent Ethernet ports when user's application software halt or when power is off.

Block Diagram:
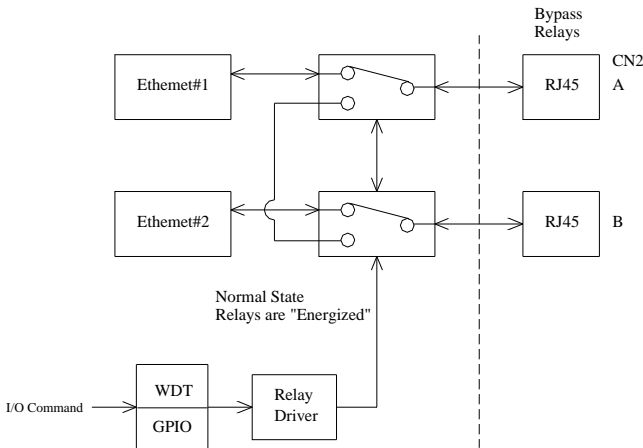
Communication States:
There are two communications states for the bypass function: (1) Normal State, (2) Bypass State. A watchdog timer (WDT) or a GPIO are used to control and switch the communication between the two states.

The block diagram in the section above shows the Normal State, where the two Ethernet ports work independently. The following diagram shows the Bypass State, where the two Ethernet ports are bypassed together.

Bypass
Relays

CN2
A

Ethemet#1 ⇠⇢ ○ ○ ⟵ RJ45

Ethemet#2 ⇠⇢ ○ ○ ⟵ RJ45 B

Bypass State
Relays are "Dis-energized"

I/O Command ⟶ WDT GPIO ⟶ Relay Driver
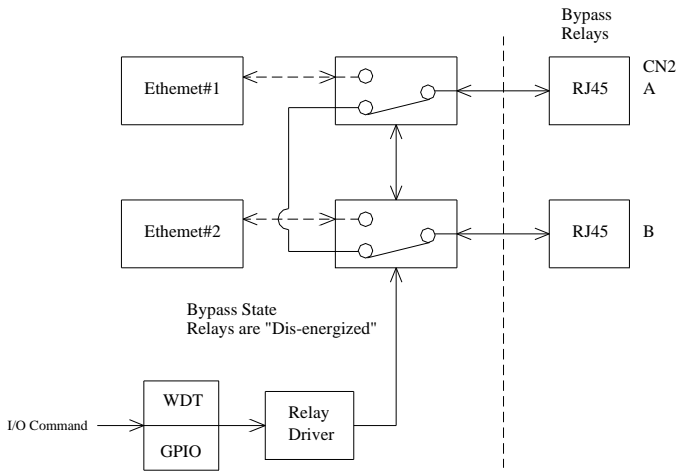
Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//=========================================================================
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=========================================================================
#include <stdio.h>
#include <stdlib.h>
#include "W627EHG.H"
//=========================================================================
int main (int argc, char *argv[]);
void copyright(void);
void EnableWDT(int);
void DisableWDT(void);
//=========================================================================
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        copyright();

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return 1;
        }

        if (Init_W627EHG() == 0)
        {
                printf(" Winbond 83627HF is not detected, program abort.\n");
                return 1;
        }
        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        EnableWDT(bTime);

        return 0;
}
//=========================================================================
```

```
void copyright(void)
{
        printf("\n======= Winbond 83627EHG Watch Timer Tester (AUTO DETECT) =======\n"\
                "      Usage : W627E_WD reset_time\n"\
                "      Ex : W627E_WD 3  => reset system after 3 second\n"\
                "         W627E_WD 0  => disable watch dog timer\n");
}
//============================================================================
void EnableWDT(int interval)
{
        unsigned char bBuf;

        bBuf = Get_W627EHG_Reg( 0x2D);
        bBuf &= (!0x01);
        Set_W627EHG_Reg( 0x2D, bBuf);                //Enable WDTO

        Set_W627EHG_LD( 0x08);                       //switch to logic device 8
        Set_W627EHG_Reg( 0x30, 0x01);                //enable timer

        bBuf = Get_W627EHG_Reg( 0xF5);
        bBuf &= (!0x08);
        Set_W627EHG_Reg( 0xF5, bBuf);                //count mode is second

        Set_W627EHG_Reg( 0xF6, interval);            //set timer
}
//============================================================================
void DisableWDT(void)
{
        Set_W627EHG_LD(0x08);                        //switch to logic device 8
        Set_W627EHG_Reg(0xF6, 0x00);                 //clear watchdog timer
        Set_W627EHG_Reg(0x30, 0x00);                 //watchdog disabled
}
//============================================================================
```

```
//=============================================================================
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=============================================================================
#include "W627EHG.H"
#include <dos.h>
//=============================================================================
unsigned int W627EHG_BASE;
void Unlock_W627EHG (void);
void Lock_W627EHG (void);
//=============================================================================
unsigned int Init_W627EHG(void)
{
        unsigned int result;
        unsigned char ucDid;

        W627EHG_BASE = 0x2E;
        result = W627EHG_BASE;

        ucDid = Get_W627EHG_Reg(0x20);
        if (ucDid == 0x88)
        {       goto Init_Finish;       }

        W627EHG_BASE = 0x4E;
        result = W627EHG_BASE;
        ucDid = Get_W627EHG_Reg(0x20);
        if (ucDid == 0x88)
        {       goto Init_Finish;       }

        W627EHG_BASE = 0x00;
        result = W627EHG_BASE;

Init_Finish:
        return (result);
}
//=============================================================================
void Unlock_W627EHG (void)
{
        outportb(W627EHG_INDEX_PORT, W627EHG_UNLOCK);
        outportb(W627EHG_INDEX_PORT, W627EHG_UNLOCK);
}
//=============================================================================
void Lock_W627EHG (void)
{
        outportb(W627EHG_INDEX_PORT, W627EHG_LOCK);
}
//=============================================================================
void Set_W627EHG_LD( unsigned char LD)
{
        Unlock_W627EHG();
        outportb(W627EHG_INDEX_PORT, W627EHG_REG_LD);
        outportb(W627EHG_DATA_PORT, LD);
        Lock_W627EHG();
}
```

```
//=========================================================================
void Set_W627EHG_Reg( unsigned char REG, unsigned char DATA)
{
      Unlock_W627EHG();
      outportb(W627EHG_INDEX_PORT, REG);
      outportb(W627EHG_DATA_PORT, DATA);
      Lock_W627EHG();
}
//=========================================================================
unsigned char Get_W627EHG_Reg(unsigned char REG)
{
      unsigned char Result;
      Unlock_W627EHG();
      outportb(W627EHG_INDEX_PORT, REG);
      Result = inportb(W627EHG_DATA_PORT);
      Lock_W627EHG();
      return Result;
}
//=========================================================================




//=========================================================================
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=========================================================================
#ifndef __W627EHG_H
#define __W627EHG_H                    1
//=========================================================================
#define      W627EHG_INDEX_PORT        (W627EHG_BASE)
#define      W627EHG_DATA_PORT         (W627EHG_BASE+1)
//=========================================================================
#define      W627EHG_REG_LD            0x07
//=========================================================================
#define W627EHG_UNLOCK                 0x87
#define      W627EHG_LOCK              0xAA
//=========================================================================
unsigned int Init_W627EHG(void);
void Set_W627EHG_LD( unsigned char);
void Set_W627EHG_Reg( unsigned char, unsigned char);
unsigned char Get_W627EHG_Reg( unsigned char);
//=========================================================================
#endif //__W627EHG_H
```