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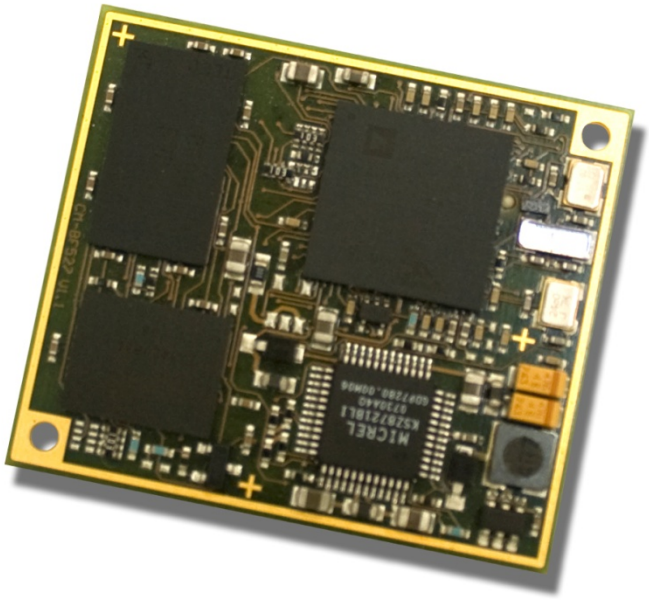

Hardware User Manual

CM-BF527 v1.x

...maximum performance at minimum space

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Due to technical requirements components may contain dangerous substances.

The Core Modules and development systems contain ESD (electrostatic discharge) sensitive devices. Electro-static charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused Core Modules and Development Boards should be stored in the protective shipping

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Core Modules:

CM-BF533:	Blackfin Processor Module powered by Analog Devices' single core ADSP-BF533 processor; up to 600MHz, 32MB SDRAM, 2MB flash, 2x60 pin expansion connectors and a size of 36.5x31.5mm.
CM-BF537E:	Blackfin Processor Module powered by Analog Devices' single core ADSP-BF537 processor; up to 600MHz, 32MB SDRAM, 4MB flash, integrated TP10/100 Ethernet physical transceiver, 2x60 pin expansion connectors and a size of 36.5x31.5mm.
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CM-BF527:	The new Blackfin Processor Module is powered by Analog Devices' single core ADSP-BF527 processor; key features are USB OTG 2.0 and Ethernet. The 2x60 pin expansion connectors are backwards compatible with other Core Modules.
CM-BF548:	The new Blackfin Processor Module is powered by Analog Devices' single core ADSP-BF548 processor; key features are 64MB DDR SD-RAM 2x100 pin expansion connectors.
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EVAL-BF5xx:	Low cost Blackfin processor Evaluation Board with one socket for any Bluetechnix Blackfin Core Module. Additional interfaces are available, e.g. an SD-Card.
DEV-BF5xxDA-Lite:	Get ready to program and debug Bluetechnix Core Modules with this tiny development platform including an USB-Based Debug Agent. The DEV-BF5xxDA-Lite is a low cost starter development system including a VDSP++ Evaluation Software License.
DEV-BF548-Lite:	Low-cost development board with one socket for Bluetechnix CM-BF548 Core Module. Additional interfaces are available, e.g. an SD-Card, USB and Ethernet.

DEV-BF548DA-Lite: Get ready to program and debug Bluetechnix CM-BF548 Core Module with this tiny development platform including an USB-Based Debug Agent. The DEV-BF548DA-Lite is a low-cost starter development system including a VDSP++ Evaluation Software License.

EXT-Boards: The following Extender Boards are available: EXT-BF5xx-AUDIO, EXT-BF5xx-VIDEO, EXT-BF5xx-CAM, EXT-BF5xx-EXP-TR, EXT-BF5xx-USB-ETH2, EXT-BF5xx-AD/DA, EXT-BF548-EXP and EXT-BF518-ETH. Furthermore, we offer the development of customized extender boards for our customers.

Software Support:

BLACKSheep: The BLACKSheep VDK is a multithreaded framework for the Blackfin processor family from Analog Devices that includes driver support for a variety of hardware extensions. It is based on the real-time VDK kernel included within the VDSP++ development environment.

LabVIEW: LabVIEW embedded support for Bluetechnix Core Modules is done by Schmid-Engineering AG: http://www.schmid-engineering.ch

uClinux: All the Core Modules are fully supported by uClinux. The required boot loader and uClinux can be downloaded from: http://blackfin.uClinux.org.

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Based on more than five years of experience with Blackfin, Bluetechnix offers development assistance as well as custom design services and software development.

1 Introduction

The CM-BF527 is a member of Blackfin based core modules incorporating the consumer temperature version of the ADSP-BF527 (optional also ADSP-BF525 or ADSP-BF522). It is backwards compatible to the CM-BF537E for most of its interfaces and can be used as a replacement module on any Bluetechnix development or evaluation Board. A special feature of this module is the on-board 10/100Mbit Ethernet interface which includes the physical transceiver chip and USB2.0 OTG Interface. The module allows easy integration into high demanding applications where space and power are very limited.

1.1 Overview

The Core Module CM-BF527 consists of the following components:

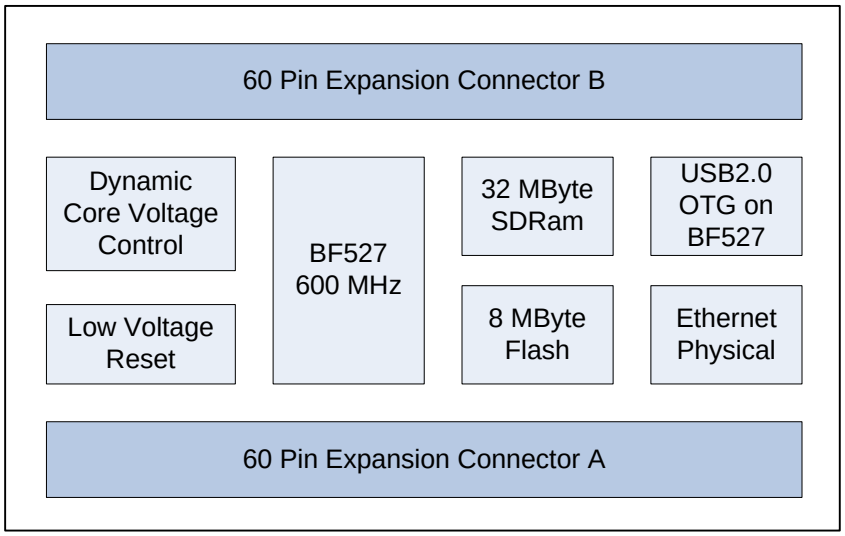

Figure 1-1: Main components of the CM-BF527 Core Module

- **Analog Devices Blackfin Processor ADSP-BF527**
  - ADSP-BF527KBCZ with 525MHz
    (* please see chapter8 for the correct part number)

- **32 MB SDRAM**
  - SDRAM Clock up to 133MHz
  - MT48LC16M16A2BG-7 (16Mx16, 256Mbit at 3.3 V)

- **8 MB of Byte Addressable Flash**
  - PF48F2000P0ZBQ0 (4Mx16, 64Mbit at 3.3V; addressable by 4 banks, 2Mb each, controlled over GPIOs)
  - Additional flash memory can be connected through the expansion board as parallel Flash using asynchronous chip select lines or as a SPI flash.

- **Low Voltage Reset Circuit**
  - Resets module if power supply goes below 2.93 V for at least 140 ms

- **Dynamic Core Voltage Control**
    - Allows adjusting of the core voltage by setting software registers on the Blackfin processor
    - Core voltage range: 0.8 – 1.2V
- **Expansion Connector A**
    - Data Bus
    - Address Bus
    - Control Signals
    - USB2.0 OTG
    - Ethernet Pins
- **Expansion Connector B**
    - PG (0..15) SPI, UART, SPORT, GPIO
    - JTAG
    - TWI (I2C compatible)
    - Power
    - PPI (Parallel Port Interface) , SPORT
    - Boot Mode
    - GPIO's

1.2 Key Features

- The CM-BF527 is a low cost compact core module and measures only 36x31mm
- Allows quick prototyping of product that comes very close to the final design
- Reduces development costs, faster time to market
- Very cost effective for small and medium volumes

1.3 Target Applications

- Mobile Embedded Device
- Generic high performance signal processor module
- Internet Connected Embedded System
- Industrial Control

1.4 Further Information

Further information, and document updates are available on the product homepage: http://www.bluetechnix.com/goto/cm-bf527

2 Specification

2.1 Functional Specification

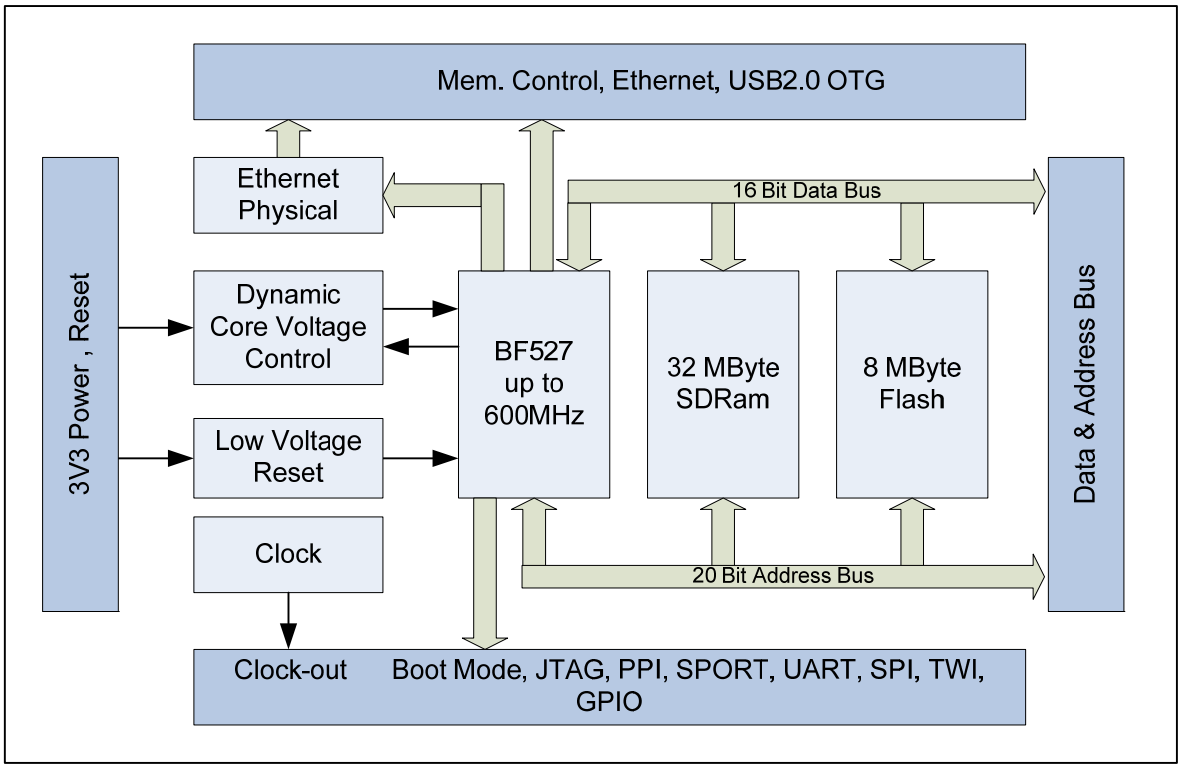

Figure 2-1: Detailed Block Diagram

Figure 2-1 shows a detailed block diagram of the CM-BF527 module. Besides the SDRAM control pins and the Pins used by the Ethernet Physical Transceiver (Port H) the CM-BF527 has all other pins of the Blackfin processor on its two main 60 pin connectors.

A special feature of the CM-BF527 Core Module is the on-board physical Ethernet transceiver from Micrel (KSZ8721BLI).

Dynamic voltage control allows reduction of power consumption to a minimum adjusting the core voltage and the clock frequency dynamically in accordance to the required processing power. A low voltage reset circuit guarantees a power on reset and resets the system when the input voltage drops below 2.93V.

2.2 Boot Mode

By default the boot mode = 0000 (BMODE3 = low, BMODE2 = low, BMODE1 = low, BMODE0 = low). All BMODE pins have internal pull down resistors.

Switch Settings BM3,BM2,BM1,BM0	Boot Mode	Description
0000	0 (default)	Idle - No bootReserved
0001	1	Boot from 8- or 16-bit external flash memory
0010	2	Boot from 16-bit asynchronous FIFO.
0011	3	Boot from serial SPI memory (EEPROM or flash)
0100	4	Boot from SPI host device
0101	5	Boot from serial TWI memory (EEPROM/flash)
0110	6	Boot from TWI host
0111	7	Boot from UART0 Host
1000	8	Boot from UART1 Host
1001	9	Reserved
1010	10	Boot from SDRAM
1011	11	Boot from OTP memory
1100	12	Boot from 8-bit NAND flash via NFC using PORTF data pins
1101	13	Boot from 8-bit NAND flash via NFC using PORTH data pins
1110	14	Boot from 16-Bit Host DMA
1111	15	Boot from 8-Bit Host DMA

Table 2-1: Boot Mode CM-BF527

Connect BMODE0 to Vcc and leave BMODE1, BMODE2 and BMODE3 pins open for Boot Mode 0001 equals to 8 or 16 bit PROM/FLASH boot mode. This is the default boot mode of the BLACKSheep software and uClinux.

Note: Boot Modes 8-15 are not supported with the DEV-BF5xx-DALite or EVAL-BF5xx

2.3 Memory MAP

Memory Type	Start Address	End Address	Size	Comment
FLASH [1)] PH9 Flag **Low** PG11 Flag **Low**	0x20000000	0x201FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S
FLASH [1)] PH9 Flag **High** PG11 Flag **Low**	0x20000000	0x201FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S
FLASH [1)] PH9 Flag **Low** PG11 Flag **High**	0x20000000	0x201FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S
FLASH [1)] PH9 Flag **High** PG11 Flag **High**	0x20000000	0x201FFFFF	2MB	¼ of 8MB Flash, PF48F2000P0ZBQ0S
SD-RAM	0x00000000	0x01FFFFFF	32MB	16Bit Bus, Micron MT48LC16M16A2FG

Table 2-2: Memory Map

*) Please be aware that you have to unlock the flash before starting an erase process!

The maximum amount of memory addressable by a single asynchronous memory bank, of the Blackfin processor is 2MB. In order to be able to use more than 2MB on a single bank, 2 GPIOs are used to select which 2MB section of flash is visible in the memory window of the Blackfin processor. This frees up the remaining banks for the user.

Please do not use the PH9 and PG11 pins as IO flags. You should leave these Pins disconnected! If one or both IO pins are needed and 4MB or 2 MB flash memory is sufficient for your application, remove the 0Ω resistors R26 and R19 from your Core Module. The flash address lines A20 and A21 are pulled Low.

To access more than 8MB flash memory (64MB) you can add the 0Ω resistor array R2. But be aware to not connect the IO pins PG10, PG9 and PG1.

Flash Address Pin	Blackfin Flag	CM Pin Number
A20	PH9	55
A21	PG11	8
A22	PG10	54
A23	PG9	7
A24	PG1	39

Figure 2-2: IO pin to flash address pin assignment

2.4 Electrical Specification

2.4.1 Supply Voltage

- 3.3V DC +/-10%

2.4.2 Supply Voltage Ripple

- 100mV peak to peak 0-20 MHz

2.4.3 On Board Crystal Frequency

- 24 MHz: USB Clock
- 25 MHz: Blackfin Clock

2.4.4 Real Time Clock Crystal

- 32.768kHz

2.4.5 Supply Current

- Maximum current: 350mA @3.3V
- Typical operating conditions:
    - Processor running at 600MHz, Core Voltage 1.2V, SDRAM 20% bandwidth utilization at 130MHz; Ethernet idle: 200mA @ 3.3V
    - Processor running at 300MHz, Core Voltage 0.8V SDRAM 20% bandwidth utilization at 130MHz; Ethernet idle: TBD
    - Processor running at 600MHz, Core Voltage 1.2V, SDRAM 20% bandwidth utilization at 130MHz, Ethernet TX/RX active: TBD

2.5 Environmental Specification

2.5.1 Temperature

- Operating at full 600MHz: 0 to + 70° C

2.5.2 Humidity

- Operating: 10% to 90% (non condensing)

3 CM-BF527

3.1 Mechanical Outline

TOP VIEW

All dimensions are given in millimeters!

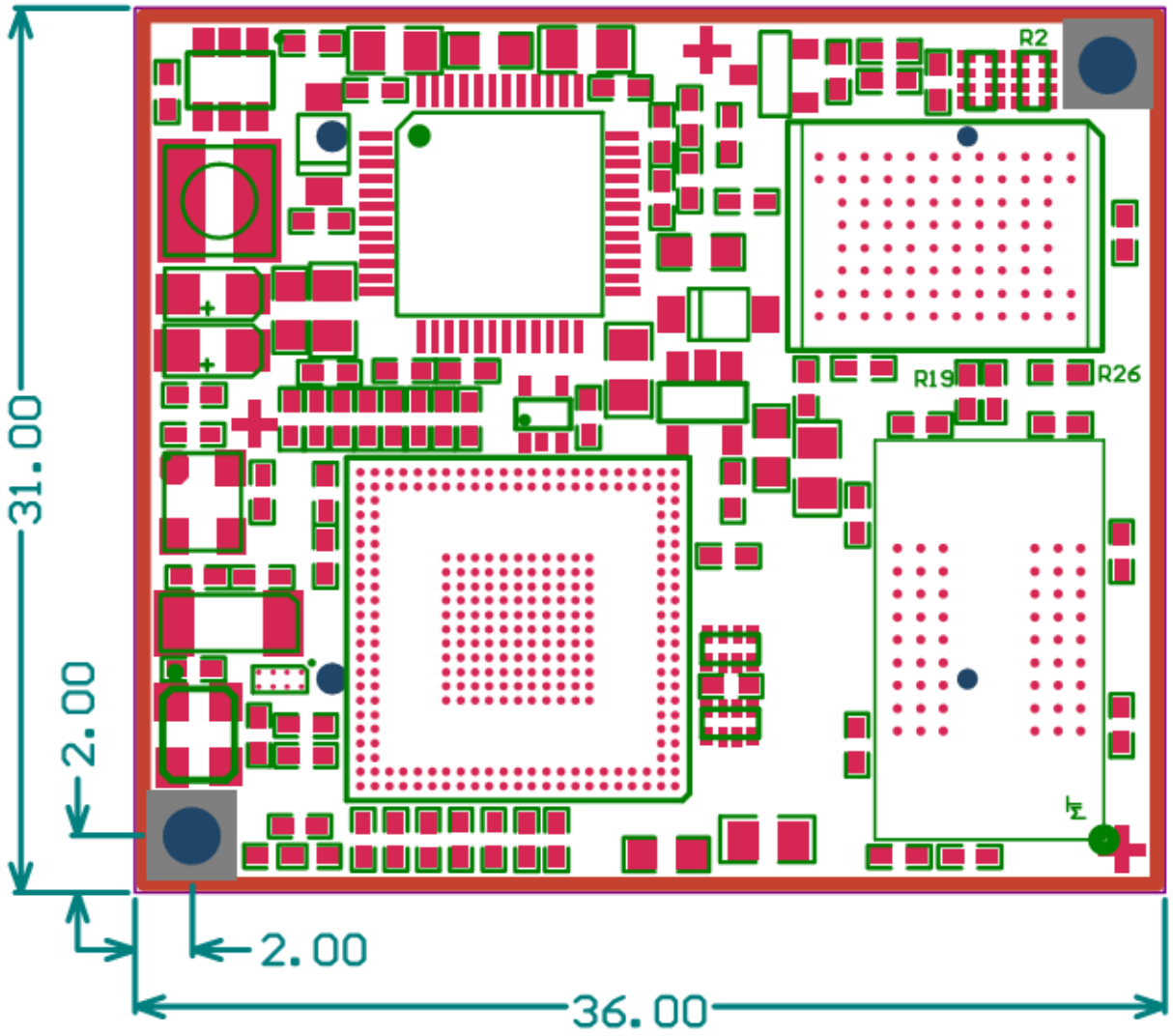

Figure 3-1: Mechanical outline and Components on top side

Take 0.5mm as a tolerance for the boarder of the board since it is broken out from a multi-board panel and some additional boarder may remain.

The module is shipped with two 60pin connectors.

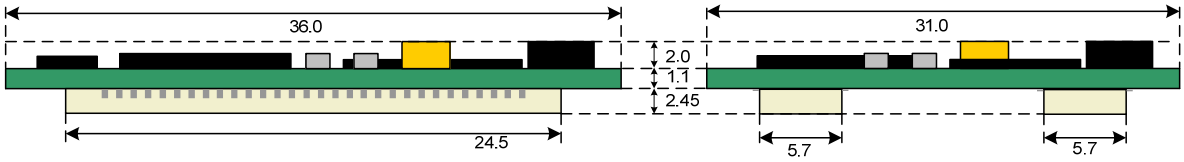

Figure 3-2: Side View with Connector mounted, 0.5mm tolerances

The total minimum mounting height including receptacle at the motherboard is 6.1mm.

Figure 3-3 shows the TOP VIEW of the bottom placed connectors (through the Board View) of the CM-BF527 Core Module. All dimensions are given in millimeters!

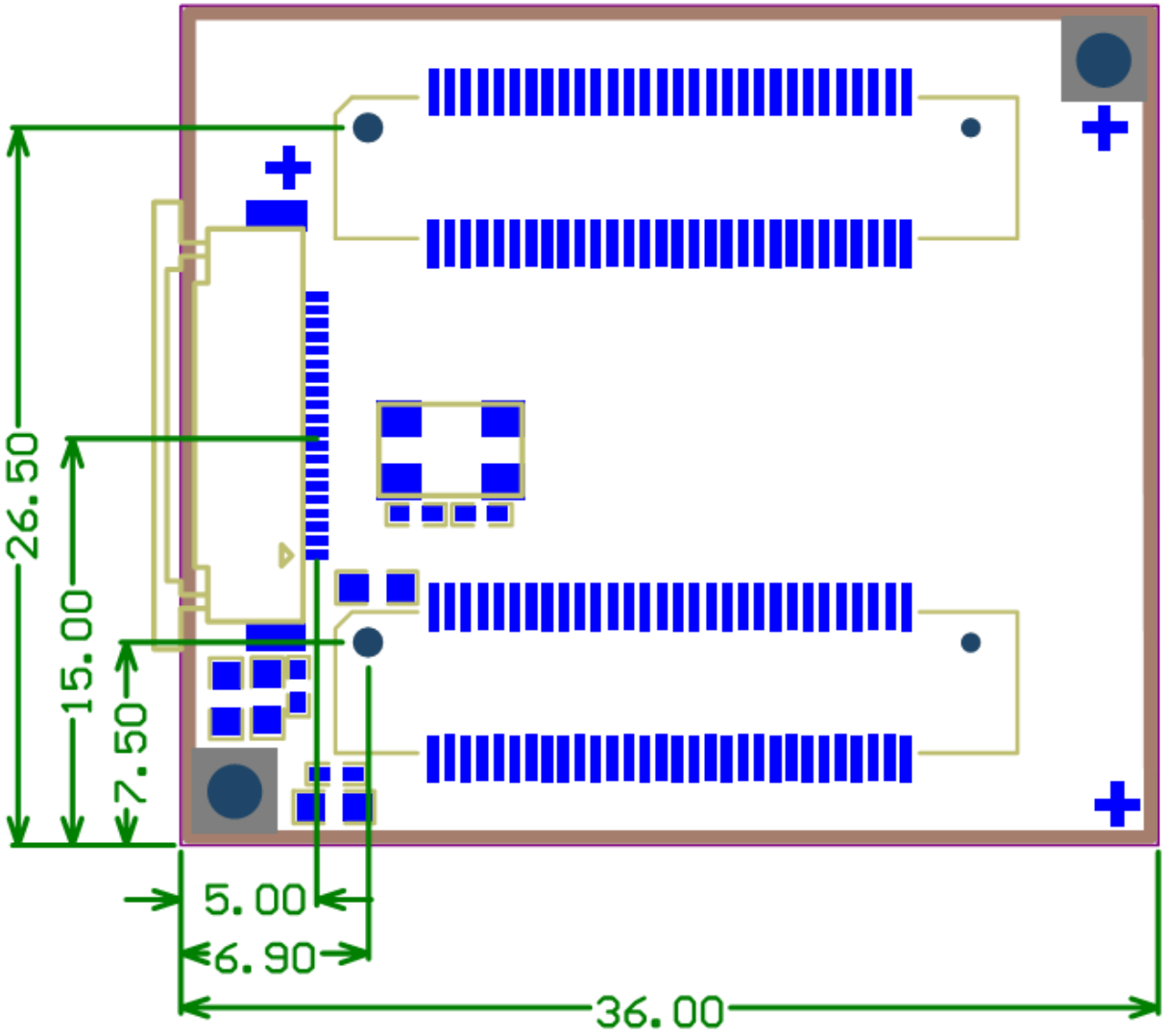

Figure 3-3: Mechanical outline and Bottom Connectors (top view)

The mechanical outline represents a TOP VIEW of the connectors placed at the bottom of the core board.

Note the additional connector X1 (FFC-20) is not supported yet and used for AUDIO functionality in future revisions with the –C variant of the ADSP-BF527 Chip. X1 is not described in this document any further.

The connectors on the CM-BF527 are of the following type:

Part	Manufacturer	Manufacturer Part No.
X2,X3	Hirose 3mm height	FX8-60P-SV

Table 3-1: Module connector types

3.2 Footprint

For the baseboard the following connectors have to be used.

Part Baseboard	Manufacturer	Manufacturer Part No.
X2,X3 mating	Hirose	FX8-60S-SV

Table 3-2: Baseboard connector types

The footprint of the baseboard may look as shown in Figure 3-4.

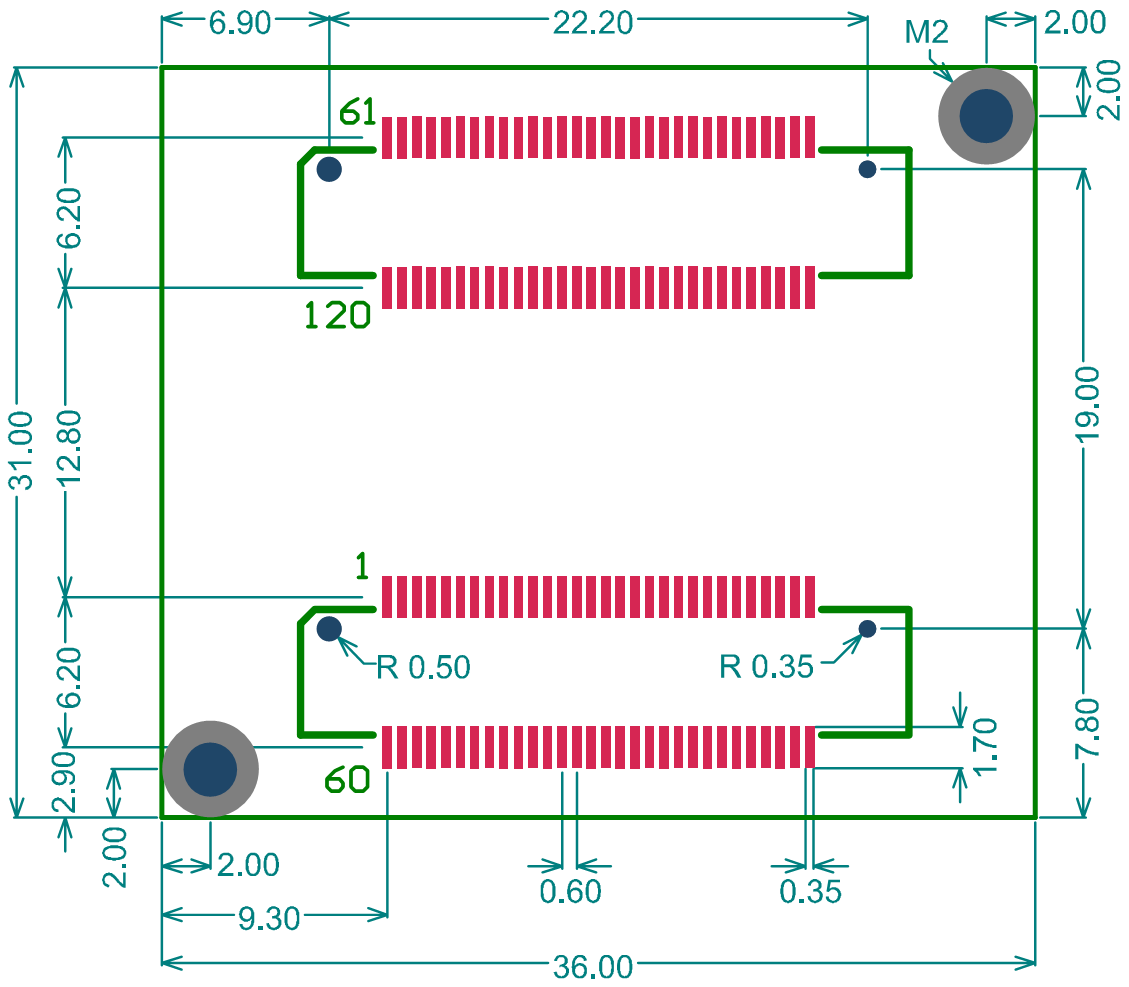

Figure 3-4: Recommended footprint of the Core Module (top view)

If there is no need to affix the Core Module, then you may omit the two M2 screwing holes.

3.3 Schematic Symbol (Signals of X2 and X3)

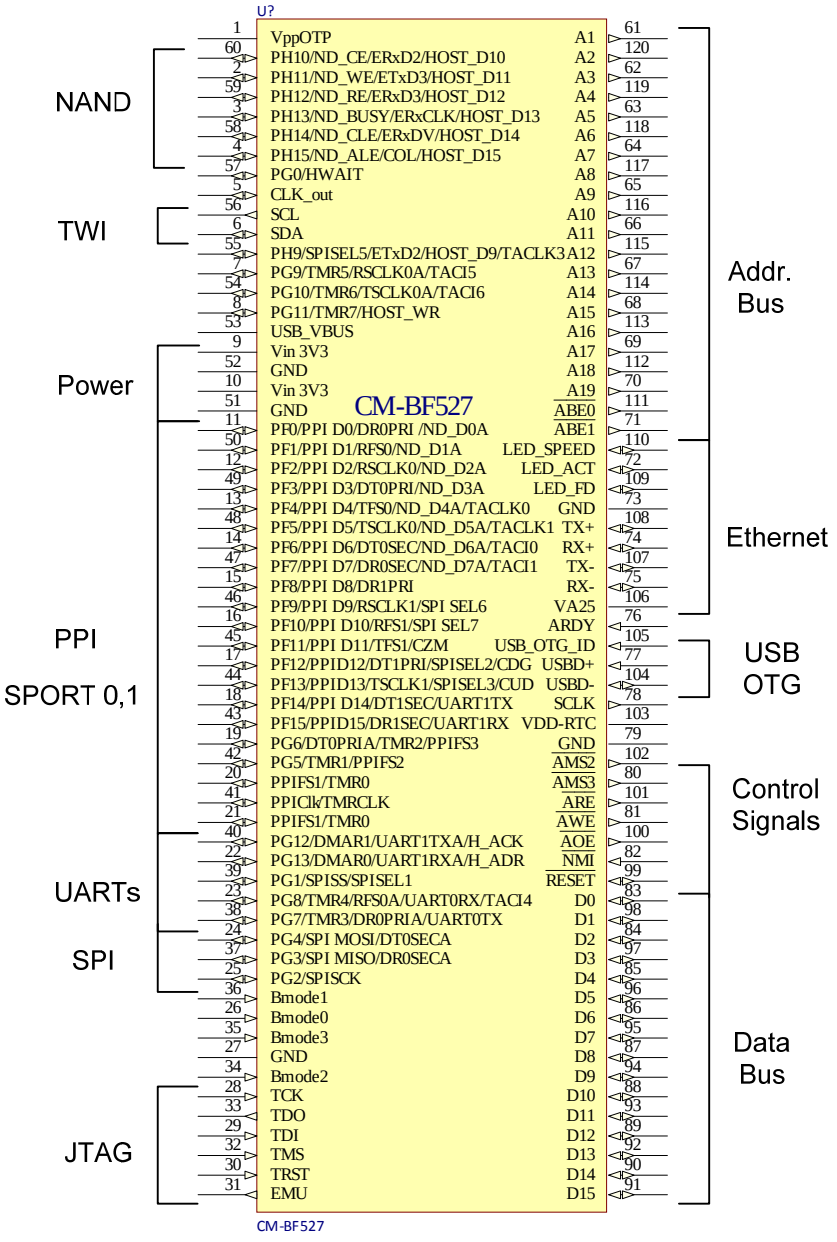

Figure 3-5: Schematic Symbol of Module

Note: For compatibility, some pin names appear twice on the connector. X1 is not supported yet and not shown in the symbol.

3.4 Connector Pin Assignments

In the following tables you will find pin assignments for the Core Module connectors. Most pins are directly connected to the Blackfin processor. If not, please read the Notes below the table.

3.4.1 Connector X2 – (1-60)

Please mind the mounted pull up and pull down resistors on the Core Module. See the third column of Table 3-3.

Pin No.	Signal Name	Signal type
1	VppOTP	Power[1)]
2	PH11/ND_WE/ETxD3/HOST_D11	IO
3	PH13/ND_BUSY/ERxCLK/HOST_D13	IO
4	PH15/ND_ALE/COL/HOST_D15	IO
5	CLKBUF	IO
6	SDA	IO
7	PG9 / RSCLK0A/ TMR5 / TACI5	IO
8	DNU[2)] or PG11 / TMR7 / HOST_WR	IO – 10k pull down
9	Vin 3V3	Power
10	Vin 3V3	Power
11	PF0 / PPID0 / DR0PRI / ND_D0A	IO
12	PF2 / PPI D2 / RSCLK0 / ND_D2A	IO
13	PF4 / PPI D4 / TFS0 / ND_D4A / TACLK0	IO
14	PF6 / PPI D6 / DT0SEC / ND_D6A / TACI0	IO
15	PF8 / PPID8 / DR1PRI	IO
16	PF10 / PPID10 / RFS1 / SPISEL7	IO
17	PF12 / PPID12 / DT1PRI / SPISEL2 / CDG	IO
18	PF14 / PPID14 / DT1SEC / UART1TX	IO
19	PG6 / DT0PRIA / TMR2 / PPIFS3	IO
20	PPIFS1 / TMR0	IO
21	PPIFS1 / TMR0	IO
22	PG13 / DMAR0 / UART1RXA / H_ADR / TACI2	IO
23	PG8 / TMR4 / RFS0A / UART0RX / TACI4	IO
24	PG4 / SPIMOSI / DT0SECA	IO
25	PG2 / SPISCK	IO
26	Bmode0	I - 10k pull down
27	GND	Power
28	TCK	I - 10k pull up
29	TDI	I - 10k pull up
30	TRST	I - 4k7 pull down
31	EMU	O
32	TMS	I – 10k pull up
33	TDO	O
34	Bmode2	I -10k pull down
35	Bmode3	I -10k pull down
36	Bmode1	I -10k pull down
37	PG3 / SPIMISO / DR0SECA	IO
38	PG7 / TMR3 / DR0PRIA / UART0TX	IO
39	PG1 / SPISS / SPISEL1	IO
40	PG12 / DMAR1 / UART1TXA / H_ACK	IO
41	PPICLK / TMRCLK	IO
42	PG5 / TMR1 / PPIFS2	IO

43	PF15 / PPID15 / DR1SEC / UART1RX / TACI3	IO
44	PF13 / PPID13 / TSCLK1 / SPISEL3 / CUD	IO
45	PF11 / PPID11 / TFS1 / CZM	IO
46	PF9 / PPID9 / RSCLK1 / SPISEL6	IO
47	PF7 / PPID7 / DR0SEC / ND_D7A / TACI1	IO
48	PF5 / PPID5 / TSCLK0 / ND_D5A / TACLK1	IO
49	PF3 / PPID3 / DT0PRI / ND_D3A	IO
50	PF1 / PPID1 / RFS0 / ND_D1A	IO
51	GND	Power
52	GND	Power
53	USB_VBUS	I/O
54	PG10 / TMR6 / TSCLK0A / TACI6	IO
55	DNU[2] or PH9/SPISEL5/ETxD2/HOST_D9/TACLK3	IO – 10k pull down
56	SCL	O
57	PG0 / HWAIT	IO
58	PH14/ND_CLE/ERxDV/HOST_D14	IO
59	PH12/ND_RE/ERxD3/HOST_D12	IO
60	PH10/ND_CE/ERxD2/HOST_D10	IO

Table 3-3: Connector X2 pin assignment

[1] Internally connected to 2.5V. If you want to program the OTP memory, just power this pin with 7.0V.

[2] These IO pins are normally used to access more flash memory. They should not be used as general purpose IO pins. For more information please see chapter 2.3.

3.4.2 Connector X3 – (61-120)

Please mind the mounted pull up and pull down resistors on the Core Module. See the third column of Table 3-4.

Pin No.	Signal Name	Signal type
61	A1	O
62	A3	O
63	A5	O
64	A7	O
65	A9	O
66	A11	O
67	A13	O
68	A15	O
69	A17	O
70	A19	O
71	ABE1	O
72	LED_ACT	IO
73	GND	Power
74	RX+	IO – 49R9 pull up to 2V5
75	RX-	IO – 49R9 pull up to 2V5
76	ARDY	I
77	USBD+	I/O
78	SCLK	O

79	GND	Power
80	AMS3	O
81	AWE	O
82	NMI	I -10k pull up
83	D0	IO
84	D2	IO
85	D4	IO
86	D6	IO
87	D8	IO
88	D10	IO
89	D12	IO
90	D14	IO
91	D15	IO
92	D13	IO
93	D11	IO
94	D9	IO
95	D7	IO
96	D5	IO
97	D3	IO
98	D1	IO
99	RESET	I/O see chapter 3.5
100	AOE	O
101	ARE	O
102	AMS2	O
103	VDD-RTC	Power
104	USBD-	I/O
105	USB_OTG_ID	I
106	VA25	Power Out
107	TX-	IO – 49R9 pull up to 2V5
108	TX+	IO – 49R9 pull up to 2V5
109	LED_FD	IO
110	LED_SPEED	IO
111	ABE0	O
112	A18	O
113	A16	O
114	A14	O
115	A12	O
116	A10	O
117	A8	O
118	A6	O
119	A4	O
120	A2	O

Table 3-4: Connector X3 pin assignment

3.5 Reset circuit

The reset of the flash and the processor are connected to a power monitoring IC. The output can be used as power on reset for external devices, see Figure 3-6.

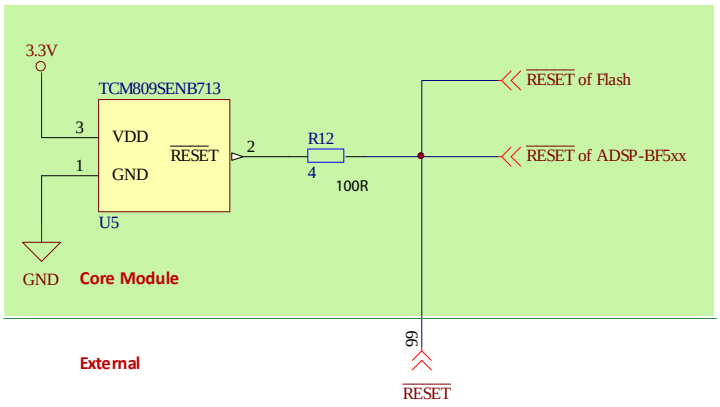

Figure 3-6: Schematic of reset circuit on the Core Module

3.6 RJ45 schematic

The KSZ8721BLI is connected via the RMII to the processor.

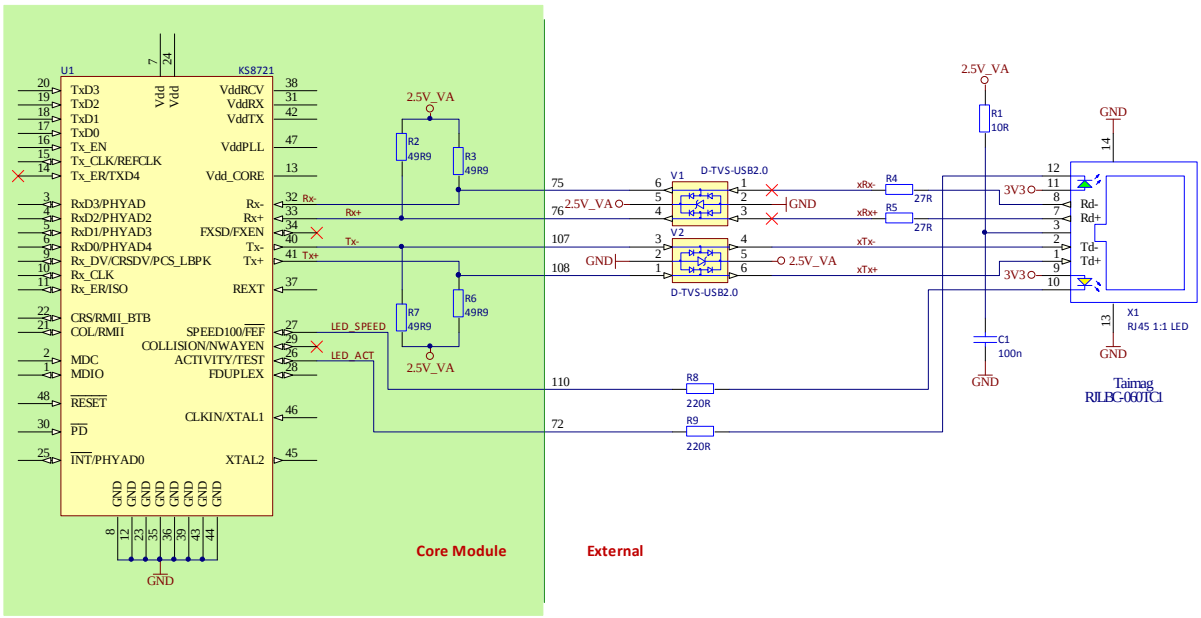

Figure 3-7: Schematic for RJ45 Connection

Designator	Value	Type	Description	Quantity
X1		RJLBC-060TC1	RJ45 with transformer	1
R4, R5	27R		Resistor	2
R8, R9	220R		Resistor	2
V1, V2		USBLC6-2P6	TSV-Diode	2

Table 3-5: Parts List RJ45

4 Software Support

4.1 BLACKSheep

The Core Module is delivered with a pre-flashed basic version of the BLACKSheep VDK multithreaded framework. It contains a boot-loader for flashing the Core Module via the serial port.

The BLACKSheep for the CM-BF527 contains also a web server. By typing http://192.168.0.10 you can see a standard web page installed on the Core Module.

Please consult the software development documents.

4.2 uClinux

The Core Module is fully supported by the open source platform at http://blackfin.uclinux.org. Since the Core Modules are pre-flashed with BLACKSheep you have to flash uBoot first. To flash the uBoot you can use the BLACKSheep boot-loader.

5 Application Examples

5.1 Sample Schematic

In this minimum configuration the CM-BF527 is used as a high performance network connected processor module.

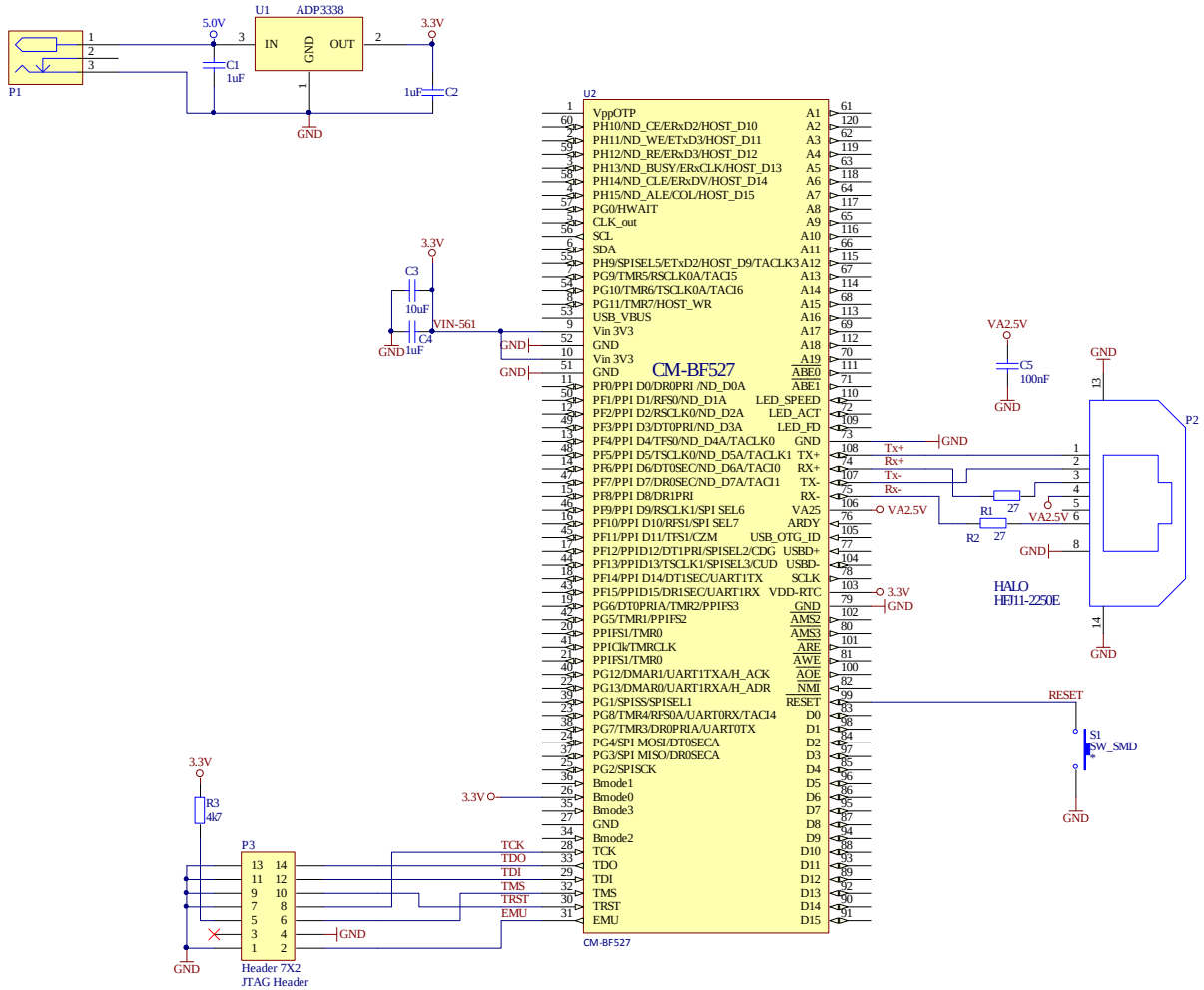

Figure 5-1: Configuration with Ethernet and JTAG Connector

Designator	Value	Type	Description	Quantity
C1, C2, C4	1uF		Capacitor	3
C3	10uF		Capacitor	1
C5	100nF		Capacitor	1
P1		DC-8	Power connector DC-8	1
P2		HFJ11-2250E	RJ45 with transformer	1
P3			Header, 7-Pin, dual row	1
R1, R2	27		Resistor	2
R3	4k7		Resistor	1
S1			Switch	1
U1		ADP3338	Low dropout regulator	1
U2			CM-BF537	1

Table 5-1: Bill of Material of Sample Schematic

5.2 Stand-alone Ethernet based MPEG Webcam

The CM-BF527 module can be used as a stand-alone module for a camera system requiring only power supply and the direct attachment of a compatible video camera. An extender board including a camera is available at Bluetechnix (EXT-BF5xx-CAM).

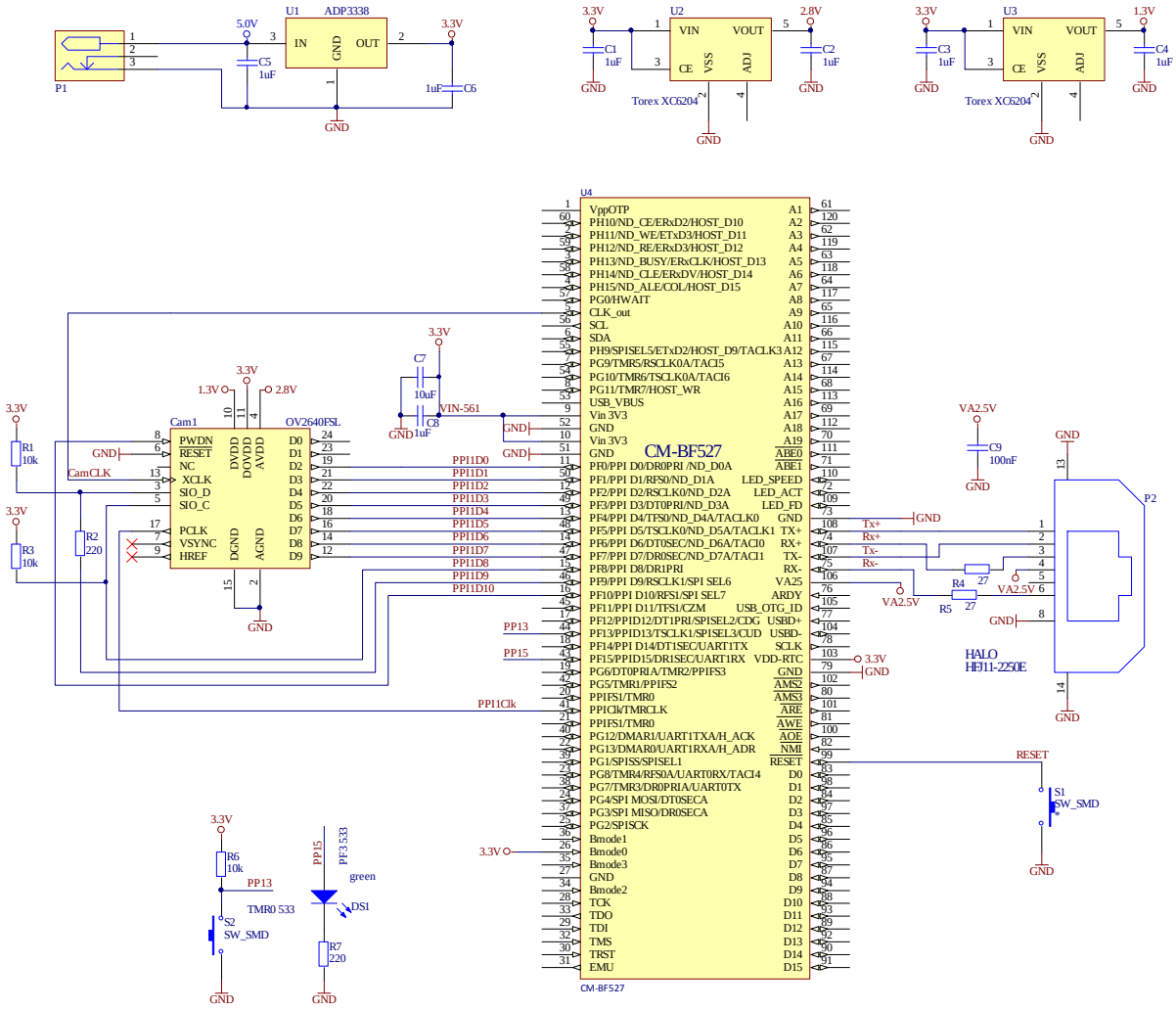

Figure 5-2: Stand-alone Ethernet based MPEG Webcam

Designator	Value	Type	Description	Quantity
C3, C4, C5, C6, C8	1u		Capacitor	6
C7	10u		Capacitor	1
C9	100n		Capacitor	1
Cam1		OV2640FSL	Camera module	1
DS1	green		SMD LED	1
P1		DC-8	Power connector DC-8	1
P2		HFJ11-2250E	RJ45 with transformer	1
R2	220		Resistor	2
R1,R3	10k		Resistor	3
R4, R5	27		Resistor	2

S1, S2			Switch	1
U1		ADP3338	Low dropout regulator	1
U2		XC6204B252MR	XC6204 LDO regulators	1
U3		XC6204B182MR	XC6204 LDO regulators	1
CM1			CM-BF537	1

Table 5-2: Bill of Material of a Stand-alone Ethernet based MPEG Webcam

5.3 Design Services

Bluetechnix offers custom design services and software development.

6 Anomalies

For the latest information regarding anomalies for this product, please consult the product home page:

http://www.bluetechnix.com/goto/cm-bf527

V1.1	Up to V1.1.4: If the load on nReset is too high, the Core Module triggers a reset. As solution use an external reset circuit IC.
V1.0	USB not operating with 25MHz Crystal

Table 6-1: Anomalies

7 Product Changes

For the latest product change information please consult the product web-page at:

http://www.bluetechnix.com/goto/cm-bf527

Version	Changes
V1.1.5	R12 changed from 470R to 100R
V1.1	Fixed Clock supply, now both USB and Ethernet can be used, changed IO Assignment of unused pins
V1.0	Initial Preliminary Version

Table 7-1: Product Changes

8 Production Report

8.1 CM-BF527 (100-1251)

Version	Component	Type
V1.1.5	Processor	ADSP-BF527 KBCZ-6X 1477344.1 0.2 *)
	RAM	MT48LC16M16A2BG-75IT 8UD41 D9DHT
	FLASH	PF48F2000P0XBQ0
V1.1.4	Processor	ADSP-BF527 KBCZ-6X 1477344.1 0.2 *)
	RAM	MT48LC16M16A2BG-75IT 8UD41 D9DHT
	FLASH	PF48F2000P0XBQ0
V1.1.3	Processor	ADSP-BF527 KBCZ-6X 1T1379301.1 0.1*)
	RAM	MT48LC16M16A2BG-75IT 7WD41 D9CHT
	FLASH	PF48F2000P0XBQ0
V1.1.2	Processor	ADSP-BF527 KBCZ-6X 1T1379301.1-B-0.1*)
	RAM	MT48LC16M16A2BG-75IT 7WD41 D9CHT
	FLASH	PF48F2000P0XBQ0
V1.1.1 **)	Processor	ADSP-BF527kBCZ-6X *)
	RAM	MT48LC16M16A2BG-75 IT:D
	FLASH	PF48F2000P0XBQ0

Table 8-1: Production Report CM-BF527

*) As long as X-Grade status is active take notice of the Analog Devices X-Grade information.
**) Only 4MB of Flash is addressable.

9 Document Revision History

Version	Date	Document Revision
13	2010-03-09	RMII information added
12	2010-02-02	Redesign of Manual
11	2009-10-01	production report updated table 3-3, 3-4 updated
10	2009-07-14	product report updated
9	2009-04-20	Boot mode table updated
8	2008-12-02	Chapter 3.5 and 3.6 added Changes on pull up/down in Table 3-4/3-5
7	2008-09-15	Footprint and mechanical drawings updated
6	2008-08-12	English checked for spelling, grammar and clarity.
5	2008-07-21	New Application Examples, Pin Description details
4	2008-05-30	New Picture, x-grade information
3	2008-04-08	Updated to reflect changes from V1.0 to V1.1
2	2008-01-10	Updated USB Bug issue
1	2007-08-28	Preliminary V1.0 of the document

Table 9-1: Revision History

10 List of Figures and Tables

Figures

Tables