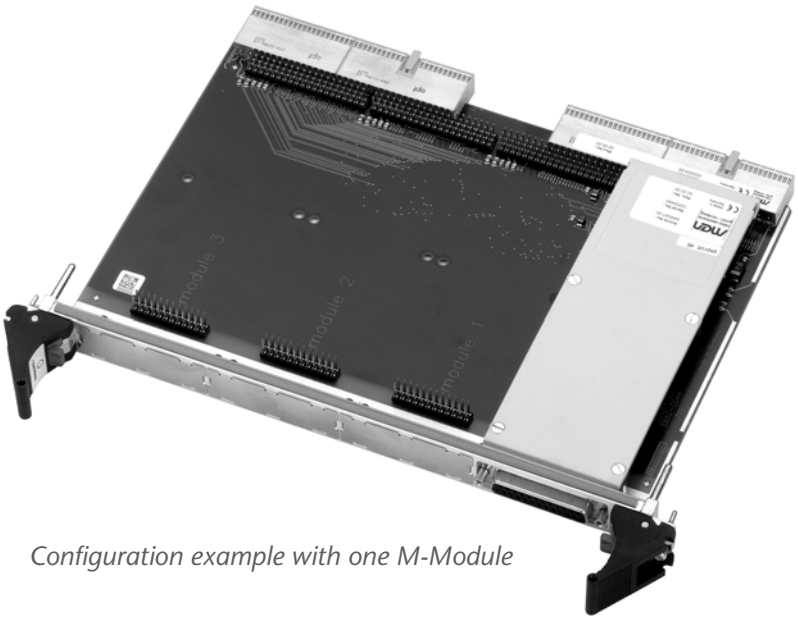
Embedded Solutions

D203 – 6U CompactPCI®/ PXI™ M-Module™ Carrier Board



Configuration example with one M-Module

User Manual

mikro elektronik
gmbh • nürnberg

D203 – 6U CompactPCI®/PXI™ M-Module™ Carrier Board

The D203 is a 6U M-Module™ carrier board for universal I/O on the CompactPCI® bus as well as on PXI™ for automated testing requirements. It allows high flexibility in applications such as data acquisition or process control. The D203 supports all eight PXI™ trigger lines as defined in the PXI™ specification.

You can install up to four M-Modules™ on the D203, which needs only one slot on the CompactPCI® bus or alternatively on the PXI™ bus. All M-Modules™ are screwed tightly on the board and require no separately mounted transition panel.

The D203 offers developers immediate access to more than 70 different M-Modules™ for I/O in fields such as process I/O, measurement, instrumentation, motion control, communication, and development.

Technical Data

M-Module™ Slots

- Four M-Module™ slots
- Compliant with M-Module™ standard
- Characteristics: A08, A24, D08, D16, D32, INTA, TRIGI, TRIGO
- One pass-thru window per M-Module™

Peripheral Connections

- Via front panel
- Via CompactPCI® J4/J5

CompactPCI® Bus

- Compliance with CompactPCI® Specification 2.0 R2.1
- Only one slot required on the 6U CompactPCI® bus
- 32-bit/33-MHz PCI-to-M-Module™ bridge
  - FPGA-based
  - Compliant with PCI Specification 2.2
  - Target on PCI bus
- V(I/O): +5V (+3.3V on request)

PXI™

- Eight trigger lines compliant with PXI™ Specification
- Routing of PXI™ trigger lines to M-Module™ interface TRIGA, TRIGB

Electrical Specifications

- Supply voltage/power consumption:
  - +5V (-3%/+5%), 20mA typ.
  - +3.3V (-3%/+5%), 20mA typ.
- MTBF: 470,000h @ 50°C (derived from MIL-HDBK-217F)

Mechanical Specifications

- Dimensions: conforming to CompactPCI® specification for 6U boards
- Front panel: aluminum with 2 handles, cut-outs for front connectors of 4 M-Modules™
- Weight: 260g

Environmental Specifications

- Temperature range (operation):
  - 0..+60°C or -40..+85°C
  - Airflow: min. 10m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity range (operation): max. 95% non-condensing
- Relative humidity range (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 2g/10..150Hz
- Conformal coating on request

Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

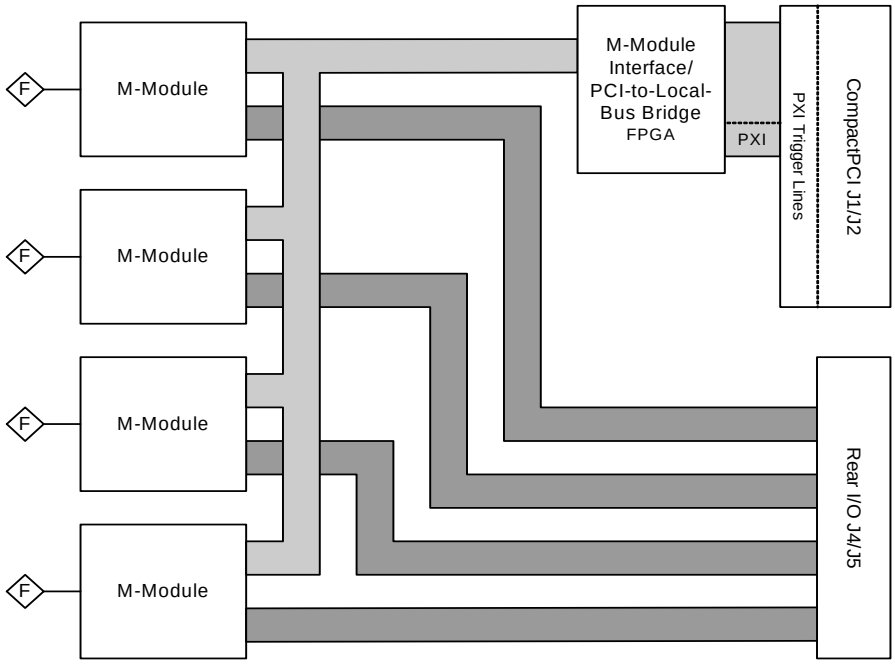
EMC

- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst) with regard to CE conformity

Software Support

- M-Module™ drivers for Windows®, VxWorks®, Linux, QNX®, OS-9®, RTX as supported

Block Diagram



Configuration Options

M-Module™ Characteristics

- A08/D16 or A24/D32

Rear I/O

- With or without J4/J5

Operation Temperature

- 0..+60°C
- -40..+85°C

Product Safety

Electrostatic Discharge (ESD)

Computer boards and components contain electrostatic sensitive devices. Electrostatic discharge (ESD) can damage components. To protect the board and other components against damage from static electricity, you should follow some precautions whenever you work on your computer.

- Power down and unplug your computer system when working on the inside.
- Hold components by the edges and try not to touch the IC chips, leads, or circuitry.
- Use a grounded wrist strap before handling computer components.
- Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
- Store the board only in its original ESD-protected packaging. Retain the original packaging in case you need to return the board to MEN for repair.

About this Document

This user manual describes the hardware functions of the board, connection of peripheral devices and integration into a system. It also provides additional information for special applications and configurations of the board.

The manual does not include detailed information on individual components (data sheets etc.). A list of literature is given in the appendix.

History

Edition	Comments	Technical Content	Date of Issue
E1	First edition	M. Schmitz	2003-01-30
E2	Second edition	T. Eckert	2003-12-11
E3	New board versions with A24/D32 support	B. Nidetzky	2006-10-27

Conventions

This sign marks important notes or warnings concerning proper functionality of the product described in this document. You should read them in any case.

italics — Folder, file and function names are printed in *italics*.

bold — **Bold** type is used for emphasis.

`monospace` — A `monospaced` font type is used for hexadecimal numbers, listings, C function descriptions or wherever appropriate. Hexadecimal numbers are preceded by "0x".

hyperlink — Hyperlinks are printed in blue color.

The globe will show you where hyperlinks lead directly to the Internet, so you can look for the latest information online.

IRQ# /IRQ — Signal names followed by "#" or preceded by a slash ("/") indicate that this signal is either active low or that it becomes active at a falling edge.

in/out — Signal directions in signal mnemonics tables generally refer to the corresponding board or component, "in" meaning "to the board or component", "out" meaning "coming from it".

Vertical lines on the outer margin signal technical changes to the previous edition of the document.

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MEN Mikro Elektronik GmbH
Neuwieder Straße 5-7
90411 Nuremberg
Phone +49-911-99 33 5-0
Fax +49-911-99 33 5-901
E-mail info@men.de
www.men.de

France
MEN Mikro Elektronik SA
18, rue René Cassin
ZA de la Châtelaine
74240 Gaillard
Phone +33 (0) 450-955-312
Fax +33 (0) 450-955-211
E-mail info@men-france.fr
www.men-france.fr

USA
MEN Micro, Inc.
750 Veterans Circle
Warminster, PA 18974
Phone (215) 956-1583
Fax (215) 956-1585
E-mail sales@menmicro.com
www.menmicro.com

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Figures

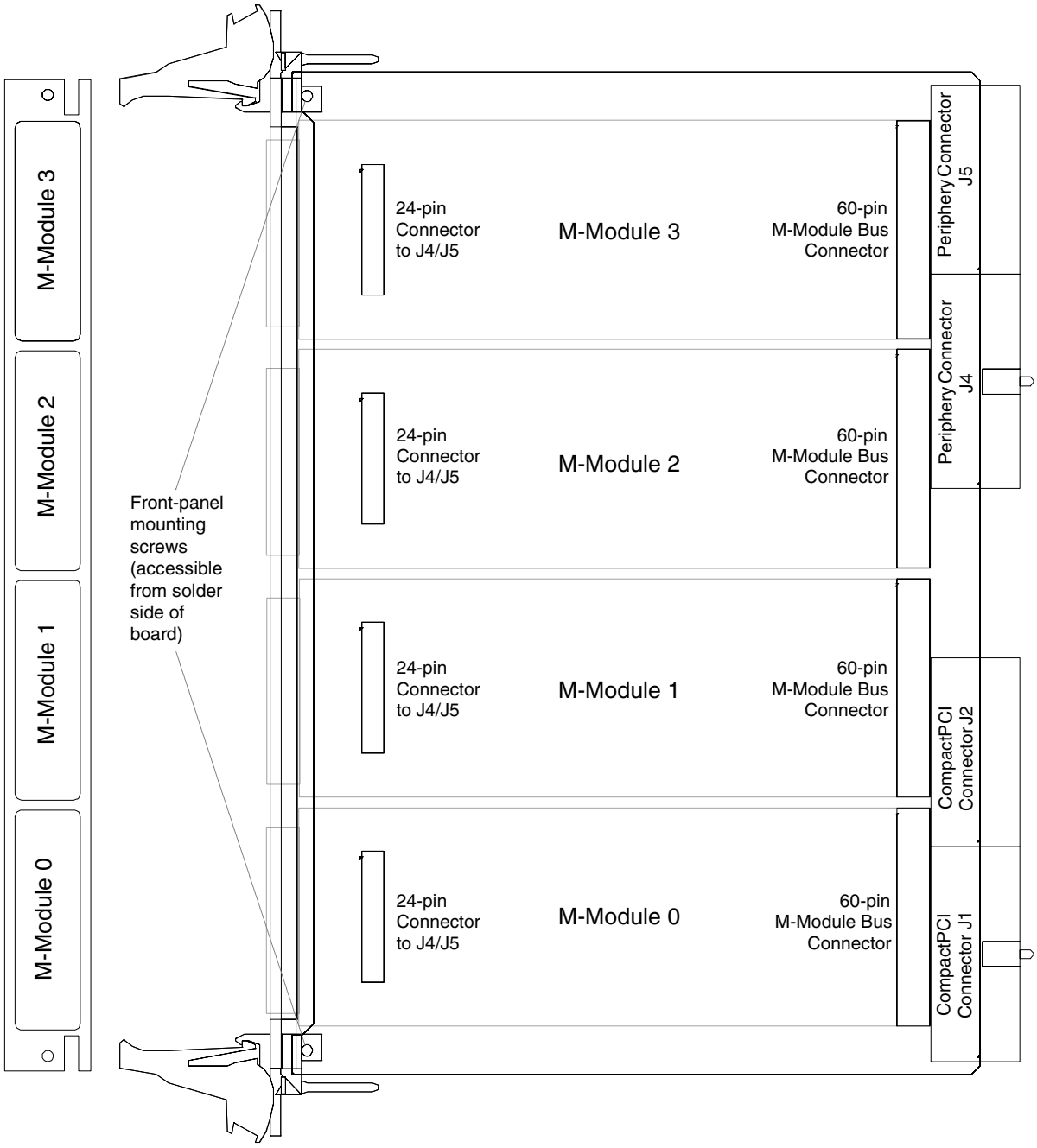
Tables

1 Getting Started

This chapter will give an overview of the carrier board and some hints for first installation in a system as a "check list".

1.1 Map of the Board

Figure 1. *Map of the Board – Front panel and top view*



1.2 Integrating the Board into a System

You can use the following "check list" when installing the D203 in a CompactPCI system for the first time.

Note: The D203 **must not** be inserted into the system slot! The system slot of every CompactPCI system is marked by a △ triangle on the backplane and/or at the front panel.

- ☑ Power-down the system.
- ☑ Install an M-Module on the D203 as described in Chapter 1.3 Installing M-Modules on page 13.
- ☑ Insert the D203 into your CompactPCI system, making sure that the CompactPCI connectors are properly aligned.
- ☑ Power-up the system.
- ☑ You can now install driver software for the D203 and M-Modules.

1.3 Installing M-Modules

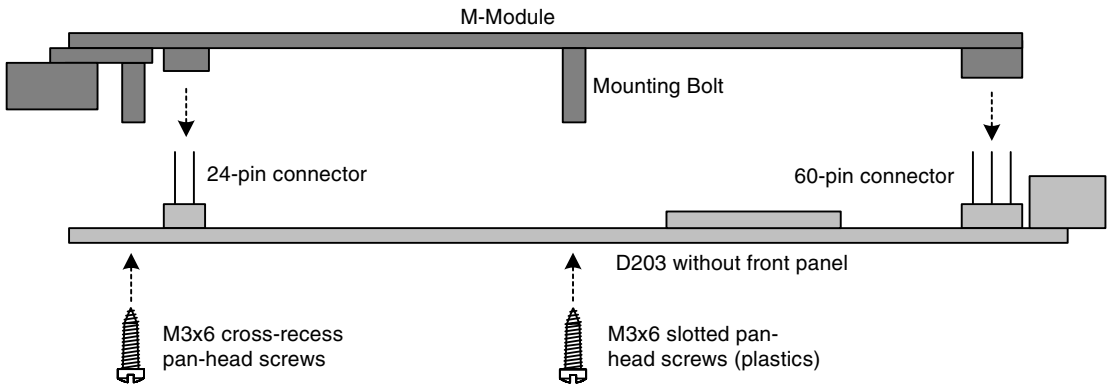
Perform the following steps to install an M-Module:

- ☑ Loosen the two front-panel mounting screws at the solder side of the D203 and remove the whole front panel (see Figure 1, Map of the Board – Front panel and top view, on page 11).
- ☑ Hold the M-Module over the target slot of the D203 with the component sides facing each other.
- ☑ Align the 24-pin and 60-pin connectors of the M-Module and carrier board.
- ☑ Press the M-Module carefully but firmly on the D203, making sure that the connectors are properly linked.
- ☑ Turn the D203 upside down and use four M-Module mounting screws to fasten the M-Module on the solder side of the D203.
- ☑ Re-install the front panel of the D203.

Note: You can order suitable mounting screws from MEN, see MEN's website. In any case, use only the screw types specified in the following figure!

Note: Older M-Modules with a solder side cover may collide with the front panel. If you have any problems, please contact MEN's technical support: support@men.de.

Figure 2. *Installing an M-Module*



1.4 Installing Driver Software

For a detailed description on how to install driver software please refer to the respective documentation.

You can find any driver software available for download on MEN's website.

2 Connecting the Board

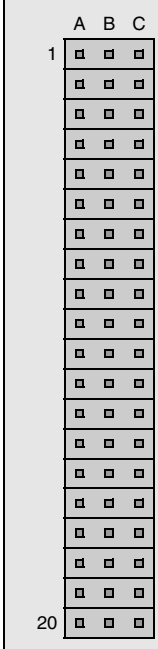
2.1 M-Module Connectors

Connector types:

- Three 20-pin plugs, 2.54mm pitch, square pins ∅ 0.635mm gold
- Mating connector:
  Three 20-pin receptacles, high-precision, 2.54mm pitch, for square pins ∅ 0.635mm gold, 6.9mm height

Note: Signals which are not bussed (i.e. which are applied to each M-Module slot independently) are indexed with "*x*". For each slot, replace "*x*" with the slot number (0..3).

Table 1. *Pin assignment of the 60-pin plug connectors*



	A	B	C
1	/CS*x*	GND	/AS
2	A01	+5V	D16
3	A02	+12V	D17
4	A03	-12V	D18
5	A04	GND	D19
6	A05	/DREQ*x*	D20
7	A06	/DACK*x*	D21
8	A07	GND	D22
9	D08/A16	D00/A08	TRIGA
10	D09/A17	D01/A09	TRIGB
11	D10/A18	D02/A10	D23
12	D11/A19	D03/A11	D24
13	D12/A20	D04/A12	D25
14	D13/A21	D05/A13	D26
15	D14/A22	D06/A14	D27
16	D15/A23	D07/A15	D28
17	/DS1	/DS0	D29
18	/DTACK*x*	/WRITE	D30
19	/IACK*x*	/IRQ*x*	D31
20	/RESET	SYSCLK*x*	/DS2

Due to the characteristics, the following pins are not supported on the carrier board:

- */DREQx*
- */DACKx*

Note: There are different board versions with A08/D16 or A24/D32 M-Module support. If you are not sure which type of addressing your carrier board supports, you can check the different models on MEN's website.

Table 2. *Signal mnemonics of the M-Module connector*

Name	Direction	Function
D00/A08..D15/A23	in/out	Multiplexed data/address bus
D16..D31	in/out	Most significant portion of data bus
A01..A07	out	Address bus
/WRITE	out	Read/write enable
/CS	out	M-Module chip select
/DTACK	in	Data acknowledge
/DS0..1	out	Data bus select signals
/RESET	out	M-Module reset
/IRQ	in	Interrupt request
/IACK	out	Interrupt acknowledge
/DREQ	in	DMA request (not supported)
/DACK	out	DMA acknowledge (not supported)
SYSCLK	out	16-MHz clock
GND	-	Logical reference signal
+5V, +12V, -12V	out	Power supplies
/AS	out	Address strobe for multiplexed address/data bus
TRIGA, TRIGB	in/out	Trigger inputs/outputs

2.2 Peripheral Interface Connectors

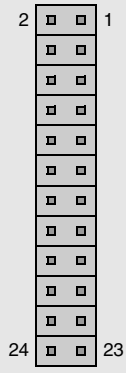
The 24-pin I/O connectors of each M-Module slot are connected to CompactPCI connectors J4/J5 to allow for maximum flexibility in I/O usage. The tables below show the correspondence between the pins on these connectors. "*x*" stands for the respective slot number.

2.2.1 24-pin M-Module I/O Connectors

Connector types:

- Two 12-pin plugs, 2.54mm pitch, square pins ∅ 0.635mm gold
- Mating connector:
  Two 12-pin receptacles, high-precision, 2.54mm pitch, for square pins ∅ 0.635mm gold, 6.9mm height

Table 3. *Pin assignment of the 24-pin peripheral I/O plug connectors*



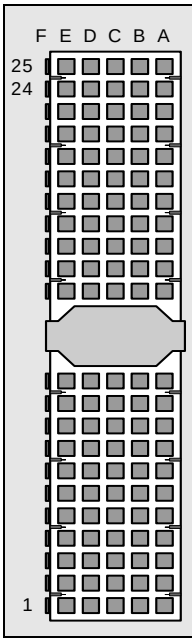
2	M*x*_IO2	1	M*x*_IO1
4	M*x*_IO4	3	M*x*_IO3
6	M*x*_IO6	5	M*x*_IO5
8	M*x*_IO8	7	M*x*_IO7
10	M*x*_IO10	9	M*x*_IO9
12	M*x*_IO12	11	M*x*_IO11
14	M*x*_IO14	13	M*x*_IO13
16	M*x*_IO16	15	M*x*_IO15
18	M*x*_IO18	17	M*x*_IO17
20	M*x*_IO20	19	M*x*_IO19
22	M*x*_IO22	21	M*x*_IO21
24	M*x*_IO24	23	M*x*_IO23

2.2.2 CompactPCI Connectors J4/J5

Connector types of J4/J5:

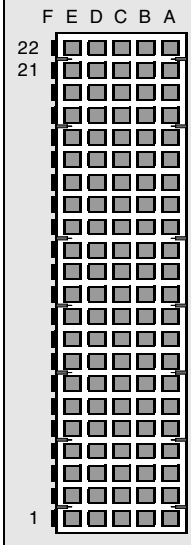
- 110-pin shielded, 2mm-pitch, 5-row receptacle according to IEC 917 and IEC 1076-4-101

Table 4. *Pin assignment of CompactPCI J4 (110-pin type "A")*



	F	E	D	C	B	A
25	GND	M0_IO1	M0_IO2	M0_IO3	M0_IO4	M0_IO5
24	GND	M0_IO6	M0_IO7	M0_IO8	M0_IO9	M0_IO10
23	GND	M0_IO11	M0_IO12	M0_IO13	M0_IO14	M0_IO15
22	GND	M0_IO16	M0_IO17	M0_IO18	M0_IO19	M0_IO20
21	GND	M0_IO21	M0_IO22	M0_IO23	M0_IO24	-
20	GND	-	-	-	-	-
19..1	GND	-	-	-	-	-

Table 5. *Pin assignment of CompactPCI J5 (110-pin type "B" modified)*

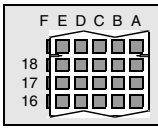


	F	E	D	C	B	A
22	GND	-	-	-	-	-
21	GND	M3_IO1	M3_IO2	M3_IO3	M3_IO4	M3_IO5
20	GND	M3_IO6	M3_IO7	M3_IO8	M3_IO9	M3_IO10
19	GND	M3_IO11	M3_IO12	M3_IO13	M3_IO14	M3_IO15
18	GND	M3_IO16	M3_IO17	M3_IO18	M3_IO19	M3_IO20
17	GND	M3_IO21	M3_IO22	M3_IO23	M3_IO24	-
16	GND	-	-	-	-	-
15	GND	-	-	-	-	-
14	GND	M2_IO1	M2_IO2	M2_IO3	M2_IO4	M2_IO5
13	GND	M2_IO6	M2_IO7	M2_IO8	M2_IO9	M2_IO10
12	GND	M2_IO11	M2_IO12	M2_IO13	M2_IO14	M2_IO15
11	GND	M2_IO16	M2_IO17	M2_IO18	M2_IO19	M2_IO20
10	GND	M2_IO21	M2_IO22	M2_IO23	M2_IO24	-
9	GND	-	-	-	-	-
8	GND	-	-	-	-	-
7	GND	M1_IO1	M1_IO2	M1_IO3	M1_IO4	M1_IO5
6	GND	M1_IO6	M1_IO7	M1_IO8	M1_IO9	M1_IO10
5	GND	M1_IO11	M1_IO12	M1_IO13	M1_IO14	M1_IO15
4	GND	M1_IO16	M1_IO17	M1_IO18	M1_IO19	M1_IO20
3	GND	M1_IO21	M1_IO22	M1_IO23	M1_IO24	-
2	GND	-	-	-	-	-
1	GND	-	-	-	-	-

2.3 PXI Trigger Lines

The carrier board supports PXI trigger lines PXI_TRIG[7:0]. These are located on CompactPCI J2 as shown below:

Table 6. *PXI trigger lines on CompactPCI J2 (110-pin type "B" modified)*



	F	E	D	C	B	A
18	GND	PXI_TRIG6	GND	PXI_TRIG5	PXI_TRIG4	PXI_TRIG3
17	GND	-	-	-	GND	PXI_TRIG2
16	GND	PXI_TRIG7	-	-	PXI_TRIG0	PXI_TRIG1

3 Functional Description

3.1 Power Supply

Power supply is fed via the CompactPCI backplane. The board operates on +5V and +3.3V. +12V/-12V may be required by one of the M-Modules installed. Power consumption is 20 mA typ. plus the current drawn by M-Modules stacked on the carrier board.

3.2 Identifying the Board

You can identify the carrier board as follows:

Note: MEN drivers will also identify the board in this way.

☑ Scan all PCI buses in the system for

- the vendor ID: `0x1172`, and
- the FPGA's device ID:
  `0xD203` with A08 M-Module access boards, or
  `0x203D` with A24 M-Module access boards.

Note: There are different board versions for A08 or A24 M-Module addressing. If you are not sure which type of addressing your carrier board supports, you can check the different models on MEN's website.

☑ Check if the Subsystem Vendor ID is set to `0xFF00` and the Subsystem ID is set to `0xFF00` in the PCI config state (see Table 7, PCI configuration registers, on page 25).

3.3 CompactPCI Interface

The D203 carrier board has a 32-bit CompactPCI interface on connectors J1/J2. It uses a 5V signaling voltage on CompactPCI. For a pinout of the 32-bit CompactPCI interface on J1/J2 and a general description of ComapctPCI, please refer to the CompactPCI specification.

Connector types of J1/J2:

- 110-pin shielded, 2mm-pitch, 5-row receptacle according to IEC 917 and IEC 1076-4-101

The interface is implemented using an FPGA and is compliant to the PCI Specification Rev. 2.2.

3.3.1 Delayed Transactions

The D203 supports delayed transactions across the CompactPCI bus, i.e. if the D203 cannot deliver (on a read cycle) or accept (for a write cycle) data within 16 PCI clock cycles, it responds to the current bus master with a retry. In response to the retry, the bus master relinquishes the CompactPCI bus, which can now be used by another bus master. In the meantime, the D203 processes the retried transaction on the M-Module interface. When the bus master retries the bus cycle on PCI, the D203 will terminate the cycle with zero wait states. This will improve overall system throughput. Even slow M-Modules do not tie up the whole CompactPCI bus.

3.4 M-Module Interfaces

The M-Module interfaces of the D203 comply with the M-Module specification. They support the following M-Module characteristics: D08, D16, D32, A08, A24, INTA, TRIGI, TRIGO. It depends on the board version whether the D203 supports A08/D16 or A24/D32 accesses.

If you are not sure which type of addressing your carrier board supports, you can check the different models on MEN's website.

The D203 does not support burst mode, since this leads to conflicts with the PCI architecture.

3.4.1 Configuring the M-Module Interfaces

M-Module Control/Status Register (read/write)

31..18	17	16
-	GIEN	GIRQ

15..4	3	2	1	0
-	TOUT	PCI RET	IEN	IRQ

GIEN Global interrupt enable bit (common to all M-Modules)
0 = Disable interrupt
1 = Enable interrupt

GIRQ Global interrupt pending (common to all M-Modules) (read-only)
1 = Interrupt pending

TOUT Timeout
1 = Timeout occurred. Write 1 to clear.

PCIRET PCI retries
0 = PCI retries during access (slower)
1 = No PCI retries during access (faster) (default)
You should change this setting to 0 ("slower") if you can expect the M-Module access to be slower than 450 ns. Otherwise, leave the default setting as is.

IEN Interrupt enable bit
0 = Disable interrupt
1 = Enable interrupt

IRQ Interrupt pending (read-only)
1 = Interrupt pending

3.5 Using Triggers

There are 8 internal trigger lines, the "internal trigger bus". Every PXI trigger line can drive one and can be driven by one dedicated internal trigger line. This is set in the PXI Trigger Source and Destination Registers for each M-Module.

Every M-Module trigger line (*TRIGA*/*TRIGB*) can be driven by and can drive every internal trigger line. If there is more than one source for an internal trigger, all connected sources are ORed.

There is one Trigger Source Register and one Trigger Destination Register per M-Module. Bits 31..16 of the Trigger Source and Destination Registers are global, i.e. the PXI trigger lines can only be accessed for all M-Modules together.

The maximum propagation delay between a trigger source and trigger destination amounts to 25 ns.

Figure 3. *Trigger routing*

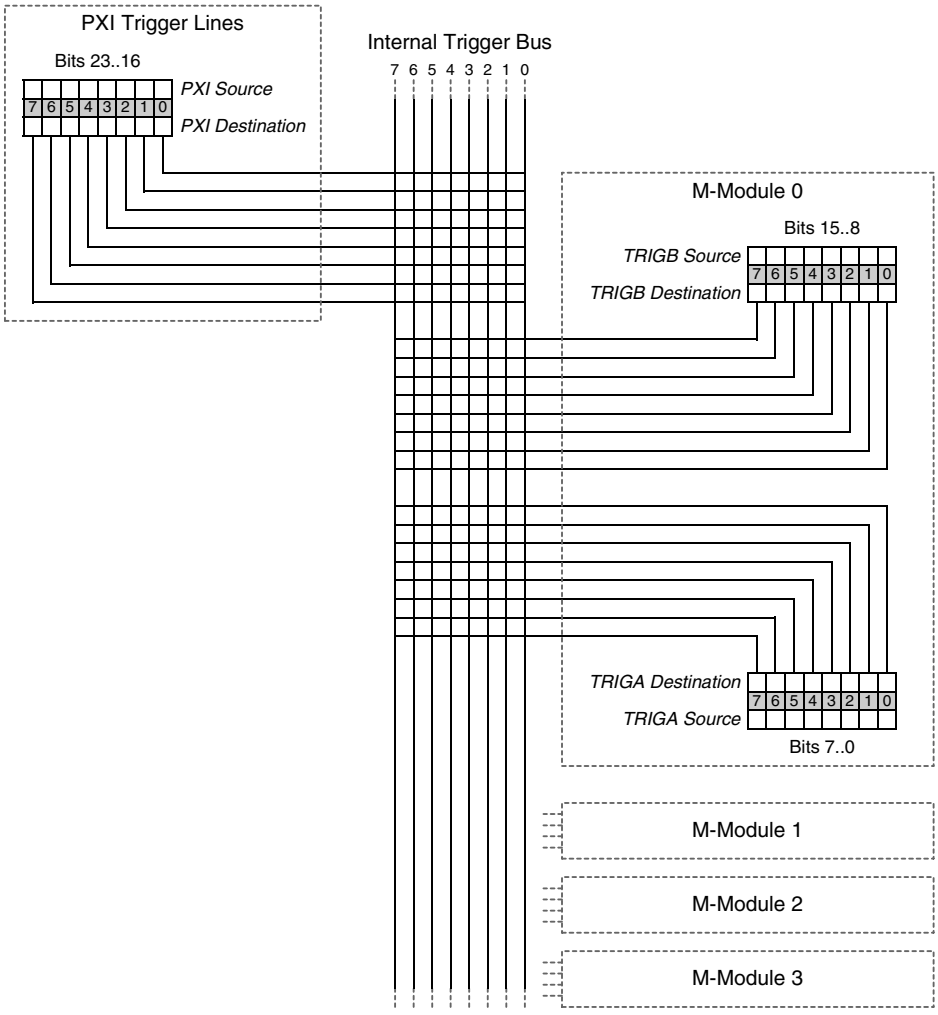
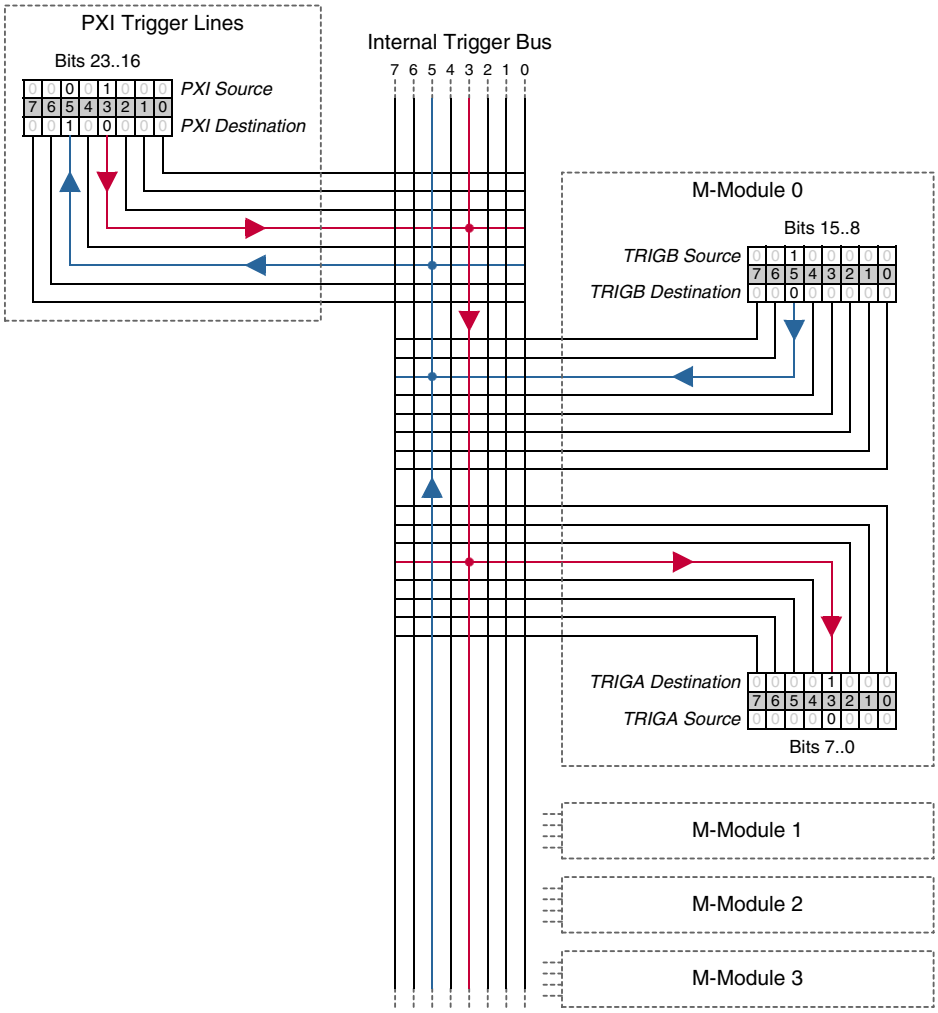


Figure 4. *Trigger routing – examples*



Trigger Source Register (read/write)

31..24	23..16
-	PXI Source 7..0

15..8	7..0
M-Module Source TRIGB 7..0	M-Module Source TRIGA 7..0

PXI Source	1 =	The corresponding PXI input is connected to internal trigger line 7..0. (Common to all M-Modules)
M-Module Source TRIGB	1 =	Trigger input *TRIGB* of the addressed M-Module is connected to the corresponding internal trigger line 7..0.
M-Module Source TRIGA	1 =	Trigger input *TRIGA* of the addressed M-Module is connected to the corresponding internal trigger line 7..0.

Trigger Destination Register (read/write)

31..24	23..16
-	PXI Destination 7..0

15..8	7..0
M-Module Destination TRIGB 7..0	M-Module Destination TRIGA 7..0

PXI Destination	1 =	The corresponding internal trigger line is connected to PXI trigger line 7..0. This line becomes an output and no longer an input line. (Common to all M-Modules)
M-Module Destination TRIGB	1 =	The corresponding internal trigger line is connected to *TRIGB* of the addressed M-Module. This *TRIGB* line becomes an output and no longer an input line.
M-Module Destination TRIGA	1 =	The corresponding internal trigger line is connected to *TRIGA* of the addressed M-Module. This *TRIGA* line becomes an output and no longer an input line.

Note: It is not forbidden but may make no sense to activate a trigger line as an output and use this line as an input as well. Care shall be taken to prevent loops! If you use PXI 0 as an input connected to internal line 0, and activate PXI as an output as well might cause heavy oscillation or any other non-deterministic behavior.

4 Organization of the Board

The D203 complies with PCI specification 2.2. All resources requested by the D203 are mapped through the PCI configuration space. For a detailed description of the PCI configuration space, please refer to the PCI specification.

4.1 PCI Configuration Registers

4.1.1 Address Map

The following register map is shown for reference only.

Table 7. *PCI configuration registers*

Address	D31..D24	D23..D16	D15..D8	D7..D0	R/W
0x00	Device ID (A08: 0xD203 / A24: 0x203D)[1]		Vendor ID (0x1172)		R
0x04	Status (0x0400)		Command (0x0007)		R/W
0x08	Class Code (0x068000)			Revision ID	R
0x0C	BIST (0x00)	Header Type (0x00)	Latency Timer (0x40)	Cache Line Size	R/W
0x10	PCI Base Address 0 for Memory Mapped FPGA Registers				R/W
0x14	PCI Base Address 1 — Not used				R/W
0x18	PCI Base Address 2 — Not used				R/W
0x1C	PCI Base Address 3 — Not used				R/W
0x20	PCI Base Address 4 — Not used				R/W
0x24	PCI Base Address 5 — Not used				R/W
0x28	CardBus CIS Pointer (0x00000000)				R
0x2C	Subsystem ID (0xFF00)		Subsystem Vendor ID (0xFF00)		R
0x30	Expansion ROM Register (0x00000000)				R/W
0x34	Reserved (0x00000000)				R
0x38	Reserved (0x00000000)				R
0x3C	Max_Lat (0x00)	Min_Gnt (0x00)	Interrupt Pin (0x01)	Interrupt Line	R/W

[1] There are different board versions for A08 or A24 M-Module addressing. If you are not sure which type of addressing your carrier board supports, you can check the different models on MEN's website.

4.2 M-Module Slot Address Spaces

Each M-Module slot is provided with a 1-KB address space with A08 access or a 32-MB address space with A24 access. (See also Chapter 3.4 M-Module Interfaces on page 21.) The base address within the PCI address space is set by the corresponding base address registers in the PCI configuration space. Each of the M-Module address spaces is divided into three distinct areas:

- An area for A24 access cycles (depending on the board version).
- An area for A08 access cycles.
- An area for accesses to additional control registers.

Table 8. *M-Module address map for board versions with A08/D16 support*

M-Module	Offset Address Range	Function
M-Module 0	0x0000..0x00FF	Reserved
	0x0100..0x01FF	Reserved
	0x0200..0x02FF	A08/D16 access
	0x0300..0x0303	A08/D16 IACK
	0x0304..0x0307	Control/Status Register
	0x0308..0x030B	Trigger Source Register
	0x030C..0x030F	Trigger Destination Register
M-Module 1	0x0400..0x04FF	Reserved
	0x0500..0x05FF	Reserved
	0x0600..0x06FF	A08/D16 access
	0x0700..0x0703	A08/D16 IACK
	0x0704..0x0707	Control/Status Register
	0x0708..0x070B	Trigger Source Register
	0x070C..0x070F	Trigger Destination Register
M-Module 2	0x0800..0x08FF	Reserved
	0x0900..0x09FF	Reserved
	0x0A00..0x0AFF	A08/D16 access
	0x0B00..0x0B03	A08/D16 IACK
	0x0B04..0x0B07	Control/Status Register
	0x0B08..0x0B0B	Trigger Source Register
	0x0B0C..0x0B0F	Trigger Destination Register
M-Module 3	0x0C00..0x0CFF	Reserved
	0x0D00..0x0DFF	Reserved
	0x0E00..0x0EFF	A08/D16 access
	0x0F00..0x0F03	A08/D16 IACK
	0x0F04..0x0F07	Control/Status Register
	0x0F08..0x0F0B	Trigger Source Register
	0x0F0C..0x0F0F	Trigger Destination Register

Table 9. *M-Module address map for board versions with A24/D32 support*

M-Module	Offset Address Range	Function
M-Module 0	0x000 0000..0x0FF FFFF	A24/D32 access
	0x100 0000..0x1FF FCFF	A24/D16 access
	0x1FF FD00..0x1FF FDFF	A08/D32 access
	0x1FF FE00..0x1FF FEFF	A08/D16 access
	0x1FF FF00..0x1FF FF03	A08/D16 IACK
	0x1FF FF04..0x1FF FF07	Control/Status Register
	0x1FF FF08..0x1FF FF0B	Trigger Source Register
	0x1FF FF0C..0x1FF FF0F	Trigger Destination Register
M-Module 1	0x200 0000..0x2FF FFFF	A24/D32 access
	0x300 0000..0x3FF FCFF	A24/D16 access
	0x3FF FD00..0x3FF FDFF	A08/D32 access
	0x3FF FE00..0x3FF FEFF	A08/D16 access
	0x3FF FF00..0x3FF FF03	A08/D16 IACK
	0x3FF FF04..0x3FF FF07	Control/Status Register
	0x3FF FF08..0x3FF FF0B	Trigger Source Register
	0x3FF FF0C..0x3FF FF0F	Trigger Destination Register
M-Module 2	0x400 0000..0x4FF FFFF	A24/D32 access
	0x500 0000..0x5FF FCFF	A24/D16 access
	0x5FF FD00..0x5FF FDFF	A08/D32 access
	0x5FF FE00..0x5FF FEFF	A08/D16 access
	0x5FF FF00..0x5FF FF03	A08/D16 IACK
	0x5FF FF04..0x5FF FF07	Control/Status Register
	0x5FF FF08..0x5FF FF0B	Trigger Source Register
	0x5FF FF0C..0x5FF FF0F	Trigger Destination Register
M-Module 3	0x600 0000..0x6FF FFFF	A24/D32 access
	0x700 0000..0x7FF FCFF	A24/D16 access
	0x7FF FD00..0x7FF FDFF	A08/D32 access
	0x7FF FE00..0x7FF FEFF	A08/D16 access
	0x7FF FF00..0x7FF FF03	A08/D16 IACK
	0x7FF FF04..0x7FF FF07	Control/Status Register
	0x7FF FF08..0x7FF FF0B	Trigger Source Register
	0x7FF FF0C..0x7FF FF0F	Trigger Destination Register

5 Appendix

5.1 Literature and Web Resources

- D203 data sheet with up-to-date information and documentation:
  www.men.de
- M-Module Standard:
  ANSI/VITA 12-1996, M-Module Specification;
  VMEbus International Trade Association
  www.vita.com
- CompactPCI Specification Revision 2.0 R2.1:
  1997; PCI Industrial Computers Manufacturers Group (PICMG)
  www.picmg.org

5.2 Restrictions

MEN's M67 M-Module, hardware revision ≤01.xx, is not operable on the D203.

You can request the circuit diagrams for the current revision of the product described in this manual by completely filling out and signing the following non-disclosure agreement.

Please send the agreement to MEN by mail. We will send you the circuit diagrams along with a copy of the completely signed agreement by return mail.

MEN reserves the right to refuse sending of confidential information for any reason that MEN may consider substantial.

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gmbh • nürnberg

Non-Disclosure Agreement

for Circuit Diagrams provided by MEN Mikro Elektronik GmbH

between

MEN Mikro Elektronik GmbH
Neuwieder Straße 5-7
D-90411 Nürnberg

("**MEN**")

and

_____
_____
_____
_____

("**Recipient**")

We confirm the following Agreement:

MEN		**Recipient**	
Date:	_____	Date:	_____
Name:	_____	Name:	_____
Function:	_____	Function:	_____

Signature: _____

Signature: _____

The following Agreement is valid as of the date of the MEN signature.

MEN Mikro Elektronik GmbH

Neuwieder Straße 5-7
90411 Nürnberg
Deutschland

Tel. +49-911-99 33 5-0
Fax +49-911-99 33 5-901

E-Mail info@men.de
www.men.de

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This Agreement is only effective if signed by both parties.

Amendments to this Agreement can be adopted only in writing. There are no supplementary oral agreements.

This Agreement shall be governed by German Law.

The court of jurisdiction shall be Nuremberg.

MEN Mikro Elektronik GmbH

Neuwieder Straße 5-7
90411 Nürnberg
Deutschland

Tel. +49-911-99 33 5-0
Fax +49-911-99 33 5-901

E-Mail info@men.de
www.men.de