SERVICE MENUAL

MODEL: L32K6RW MST6E16

L37K6RW MST6E16

L42K6RW MST6E16

This manual is the latest at the time of printing, and does not include the modification which may be made after the printing, by the constant improvement of product.

CONTENTS

Safety Precaution

CAUTION

RISK OF ELECTRIC SHOCK
DO NOT OPEN

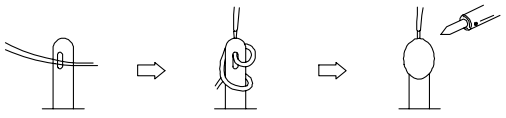
CAUTION: TO REDUCE THE RISK OF ELECTRIC SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER-SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of uninsulated “dangerous voltage” within the product’s enclo sure that may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

PRECAUTIONS DURING SERVICING

1. In addition to safety, other parts and assemblies are specified for conformance with such regulations as those applying to spurious radiation. These must also be replaced only with specified replacements.
   Examples: RF converters, tuner units, antenna selection switches, RF cables, noise-blocking capacitors, noise-blocking filters, etc.
2. Use specified internal Wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads
3. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulating Tape
   2) PVC tubing
   3) Spacers (insulating barriers)
   4) Insulating sheets for transistors
   5) Plastic screws for fixing micro switches
4. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.), wrap ends of wires securely about the terminals before soldering.



5. Make sure that wires do not contact heat generating parts (heat sinks, oxide metal film resistors, fusible resistors, etc.)
6. Check if replaced wires do not contact sharply edged or pointed parts.
7. Make sure that foreign objects (screws, solder droplets, etc.) do not remain inside the set.

MAKE YOUR CONTRIBUTION TO PROTECT THE ENVIRONMENT

Used batteries with the ISO symbol  for recycling as well as small accumulators (rechargeable batteries), mini-batteries (cells) and starter batteries should not be thrown into the garbage can.

Please leave them at an appropriate depot.

WARNING:

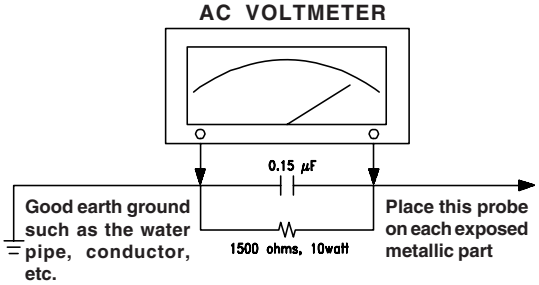
Before servicing this TV receiver, read the SAFETY INSTRUCTION and PRODUCT SAFETY NOTICE.

SAFETY INSTRUCTION

The service should not be attempted by anyone unfamiliar with the necessary instructions on this apparatus. The following are the necessary instructions to be observed before servicing.

1. An isolation transformer should be connected in the power line between the receiver and the AC line when a service is performed on the primary of the converter transformer of the set.
2. Comply with all caution and safety related provided on the back of the cabinet, inside the cabinet, on the chassis or picture tube.
3. To avoid a shock hazard, always discharge the picture tube's anode to the chassis ground before removing the anode cap.
4. Completely discharge the high potential voltage of the picture tube before handling. The picture tube is a vacuum and if broken, the glass will explode.

5. When replacing a MAIN PCB in the cabinet, always be certain that all protective are installed properly such as control knobs, adjustment covers or shields, barriers, isolation resistor networks etc.
6. When servicing is required, observe the original lead dressing. Extra precaution should be given to assure correct lead dressing in the high voltage area.
7. Keep wires away from high voltage or high tempera ture components.
8. Before returning the set to the customer, always perform an AC leakage current check on the exposed metallic parts of the cabinet, such as antennas, terminals, screwheads,metal overlay, control shafts, etc., to be sure the set is safe to operate without danger of electrical shock. Plug the AC line cord directly to the AC outlet (do not use a line isolation transformer during this check). Use an AC voltmeter having 5K ohms volt sensitivity or more in the following manner.
   Connect a 1.5K ohm 10 watt resistor paralleled by a 0.15μF AC type capacitor, between a good earth ground (water pipe, conductor etc.,) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination of the 1.5K ohm resistor and 0.15 uF capacitor. Reverse the AC plug at the AC outlet and repeat the AC voltage measurements for each exposed metallic part.
   The measured voltage must not exceed 0.3V RMS.
   This corresponds to 0.5mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.
   The resistance measurement should be done between accessible exposed metal parts and power cord plug prongs with the power switch "ON". The resistance should be more than 6M ohms.



AC Leakage Current Check

PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in this apparatus have special safety-related characteristics.

These characteristics are offer passed unnoticed by visual spection and the protection afforded by them cannot necessarily be obtained by using replacement components rates for a higher voltage, wattage, etc.

The replacement parts which have these special safety characteristics are identified by ⚠ marks on the schematic diagram and on the parts list.

Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts which do not have the same safety characteristics as specified in the parts list may create shock, fire, or other hazards.

9. Must be sure that the ground wire of the AC inlet is connected with the ground of the apparatus properly.

CAUTION

Danger of explosion if battery is incorrectly replaced.
Replace only with the same or equivalent type.
Batteries shall not be exposed to excessive heat such as sunshine, fire or the like.
Used batteries should not be thrown into the garbage can, please leave them at an appropriate depot.

CAUTION

Where the MAINS plug or an appliance coupler is used as the disconnect device, the disconnect device shall remain readily operable.

CAUTION

These servicing instructions are for use by qualified service personnel only. To reduce the risk of electric shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

Attention:

Motionless picture might cause permanent destruction to the display.

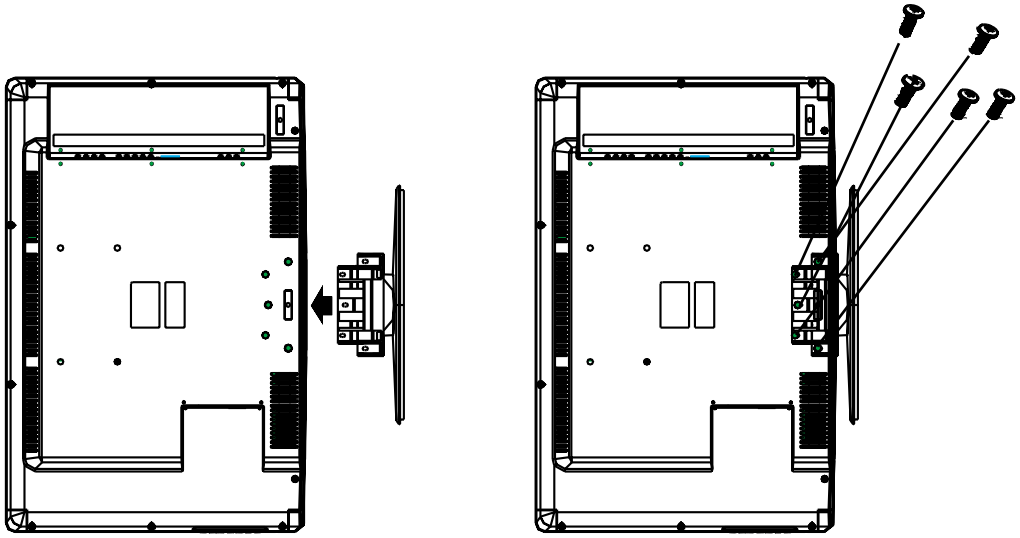
- Be sure not to display motionless picture on the LCD TV for more than 2 hours, because it would cause picture remnants to appear, which is called "screen burns". To avoid such picture remnants, please decrease the "contrast" and "brightness" of the display when displaying motionless picture.
- While watching TV program in 4:3 size mode for a long time, there would be traces on the edge of the screen's left, right and center parts because of different transmition of the light on the screen.Similar impact on the screen will occur when playing DVD or connecting games control. Products destroyed by these reasons can't be guaranteed for maintenance.
- It might cause picture remnants to display electronic games and motionless picture of PC more than a period of time.To avoid such effect, please decrease the "contrast" and "brightness" when displaying motionless picture.

1. Connection and Preparation of TV

1.1 Accessories

- ✶ User Manual x 1
- ✶ Power Cord x 1
- ✶ Remote Control x 1
- ✶ Battery (UM-4/R03P/AAA) x 2
- ✶ Stand x 1 (Pre-assembled)(Optional)
- ✶ Wall Mount Kit x 1 (Pre-assembled)(Optional)

1.2 Installation of Stand



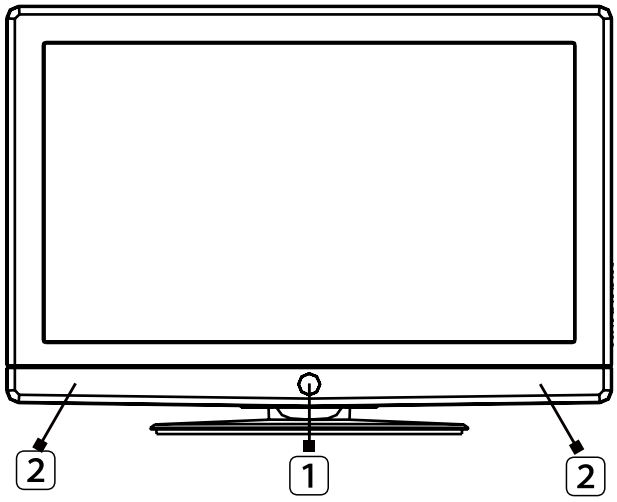
1. Place the TV with the front panel facing downwards on the soft cloth or soft pads on a desk.
2. Insert the stand into the bottom socket of the TV.
3. Insert the screws into the sockets and tighten them.

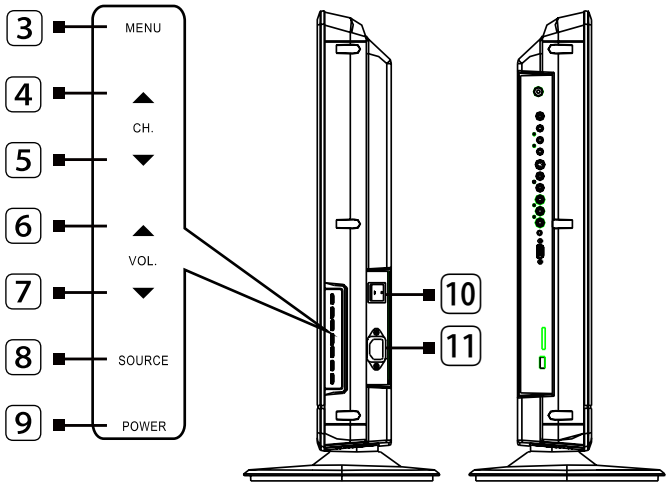
1.3 Installation of Wall Mount Kit(Optional)

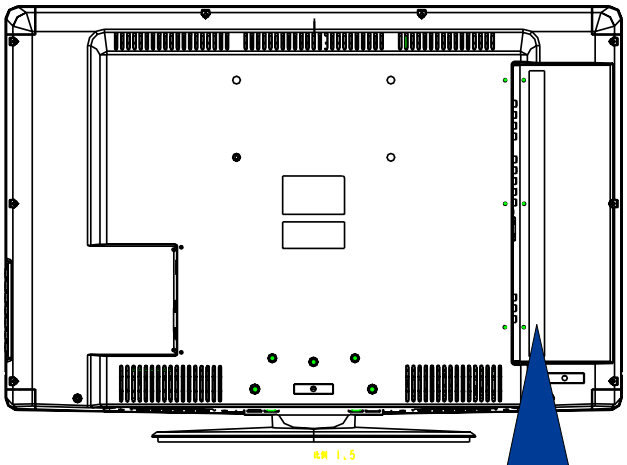
The Wall Mount Kit can help install the TV on the wall.
For more information about wall mounting, please refer to the instructions provided along with the wall mount kit.
When wall mounting the product, please contact qualified personnel.
If users choose to install the TV by themselves, the producer is irresponsible for any possible damages caused either to the product or to persons .

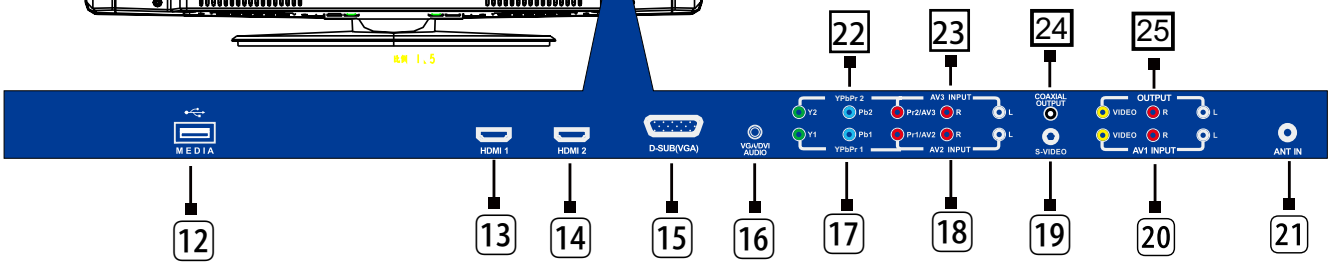
1.4 Keys and Interfaces

- L32K6/L37K6/L42K6



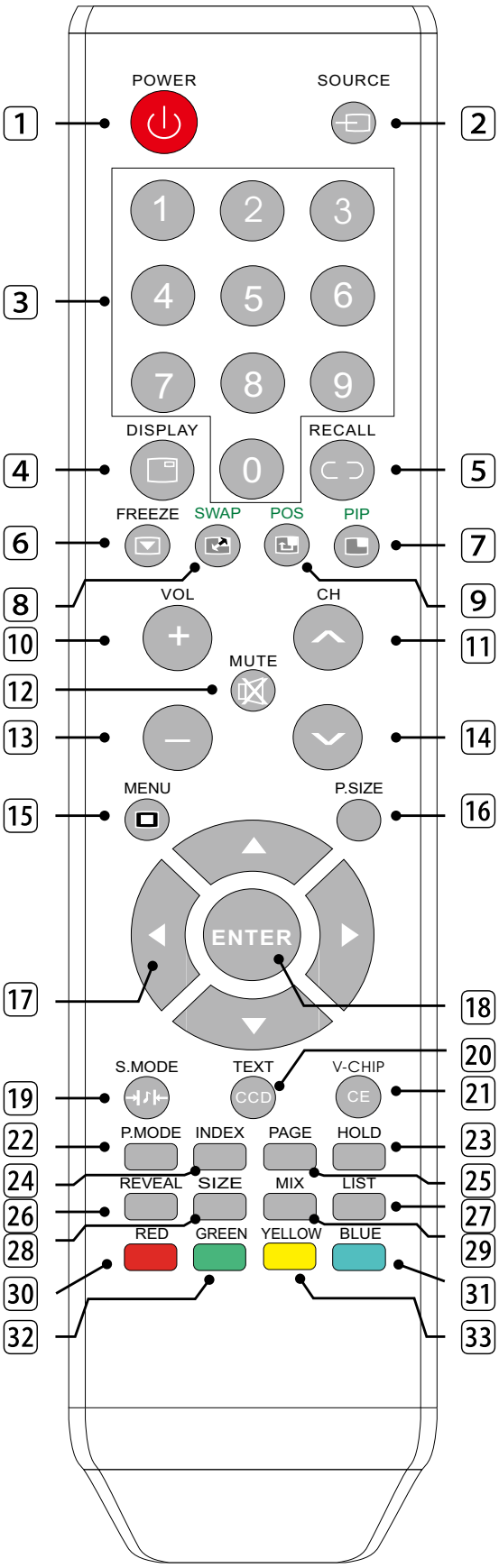






1. Remote sensor window& Power indicator
2. Speaker
3. Menu key
4. Channel “▲” key
5. Channel “▼” key
6. Volume “▲” key
7. Volume “▼” key
8. Source key
9. Power (Standby) key
10. Power switch
11. AC input
12. MEDIA
13. HDMI 1 input
14. HDMI 2 input
15. D-SUB(VGA) input
16. VGA/DVI audio input
17. YPbPr 1 and audio input
18. AV2(video and audio) input
19. S-Video input
20. AV1(video and audio) input
21. Antenna input
22. YPbPr 2 and audio input
23. AV3(video and audio) input
24. Coaxial output
25. AV(Video and audio) output

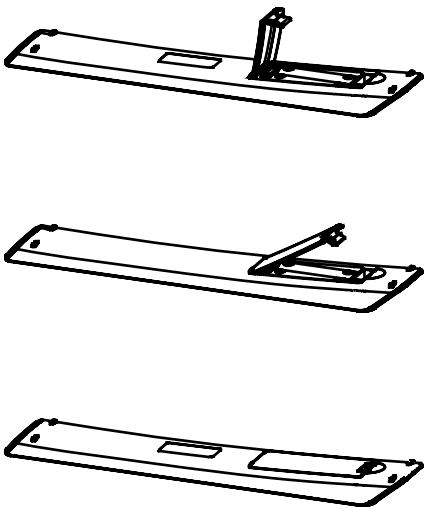
1.5 Remote Control



1. POWER: Standby turn on and off.
2. SOURCE: Select the signal source.
3. 0~9: Continue to press the keys to select a channel.
4. DISPLAY: Display the information of current video and audio.
5. RECALL: Return to previous channel.
6. FREEZE: Freeze the picture.
7. PIP: Open or close PIP.
8. SWAP: Swap the position of the main picture and sub picture.
9. POS: Change the PIP position.
10. VOL+: Increase the volume.
11. CH∧: Select the channel forward.
12. MUTE: Mute sound.
13. VOL-: Decrease the volume.
14. CH∨: Select the channel backward.
15. MENU: Enter or exit menu.
16. P.SIZE: Change the picture size.
17. ▲,▼,◀,▶ key: The menu item selection.
18. ENTER: Confirm or enter.
19. S.MODE: Select the sound mode.
20. TEXT(optioal): Enter or exit teletext.
21. CE: Hide teletext contents,press again to reappear.
22. P.MODE: Select the picture mode.
23. HOLD: Hold the current page.
24. INDEX: Display the index page.
25. PAGE: Enter the sub page mode.
26. REVEAL: Reveal the hidden information.
27. LIST: Enter the teletext list mode.
28. SIZE: Change the teletext size.
29. MIX: Press repeatedly to turn on Teletext
    ➔Teletext blending with TV program
    ➔Teletext mode.
30. RED: Access the red item or page.
31. BLUE: Access the blue item or page.
32. GREEN: Access the green item or page.
33. YELLOW: Access the yellow item or page.

Note: The INDEX, CE, PAGE, HOLD, REVEAL, SIZE, MIX, LIST, RED, GREEN, YELLOW, BLUE keys related to teletext are optional.

1.6 Installation of Batteries



1. Open the back lid of the remote control.
2. Install two 7#(AAA)1.5V batteries.
   Ensure the correct polarity of the batteries.
3. Cover the back lid.
   Please take out of the batteries from the remote control for long time of no use.

If the remote control doesn't work properly, please carry out the following checks.

- Check the TV is turned on.
- Check the polarity of the batteries are correct.
- Check the batteries are not drained.
- Check the power supply is normal or the power cord is correctly connected.
- Check there are no special fluorescent light or neon light around.

2. Basic Operation

2.1 Power ON/OFF

- Connect the power cord to the **AC Input**. Insert the power cord into the appropriate socket.
- Press the **Power switch** to switch on the TV, then press **Power** button to turn on the unit.
- Press the **Power switch** again to switch off the TV.

Note: After switch off the TV, please don't immediately re-open the power switch ,should be delayed one minute more to re-open the power switch.

2.2 Setting of Standby Mode

- Press **Power** (⏻) button to turn on the unit.
- Press **Power** (⏻) button again to return the display to standby mode. The power indicator turns red.
- Be sure not to set your TV in standby mode for a long period of time.

2.3 Selection of Input Mode

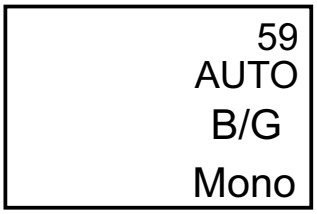
- Press the **Source** button, and then press ▲ or ▼ to select the signal source you desire, then press **Enter** or ▶ button to confirm.

The signal sources are displayed in the following sequence :

TV → AV1 → AV2 → AV3 → S-VIDEO → YPbPr1 → YPbPr2 → VGA → HDMI1 → HDMI2 → MEDIA

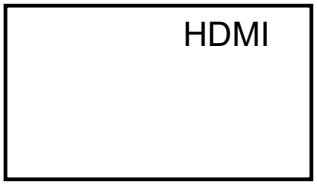
When selecting the signal source, the screen will display the information.

TV mode

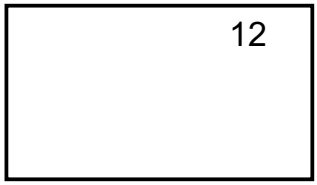


When there is no signal from the selected source, the warning message will be displayed as per illustration. Either change the channel in TV mode or press **Source** button to change source.

HDMI mode



TV mode



2.4 Menu Option Adjustment

After you have installed the batteries into the remote control, you will need to set some preferences on the LCD TV, using the menu system.

- The buttons for menu option adjustment include: **Menu,** ▲ , ▼ , ◄ , ► **Enter** buttons.
- Press the **Menu** button to open the OSD Menu, then press ◄ , ► button to select the pages. The pages are displayed in the following sequence (circular display):

Picture → Sound → System → Advance → TV → PIP

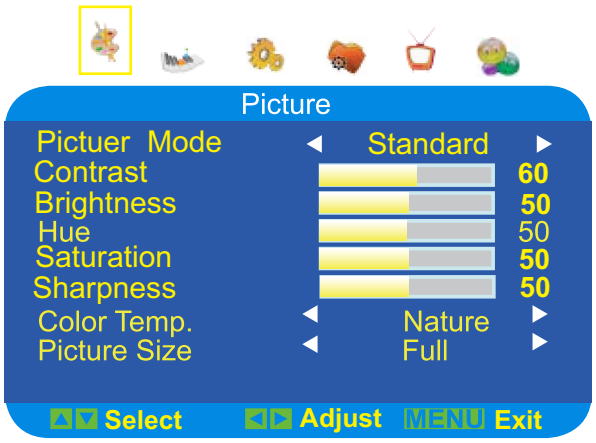
1. Press the **Menu** button to display the menu system.
2. Press ◄ , ► button to select the menu pages.
3. Press ▲ , ▼ button to select an item.
4. Press ▲ , ▼ , ◄ , ► button to select or adjust a setting.
5. If you do not make a selection within 15 seconds, the menu will close automatically.
6. Press the **Menu** button to return or exit OSD menu.

2.5 Menu Functions

2.5.1 Picture Function

※ Adjustment of the Picture.

1. Press the **Menu** button, and then press ◄ or ► button until the “Picture” menu appears.
2. Press ▲ or ▼ button to highlight the “Picture Mode”,“Contrast”,“Brightness”, “Hue”,“Saturation” “Sharpness”,“Color Temp”,“Picture Size”item.
3. Press ◄ or ► button to adjust.
4. Press the **Menu** button to return or exit.

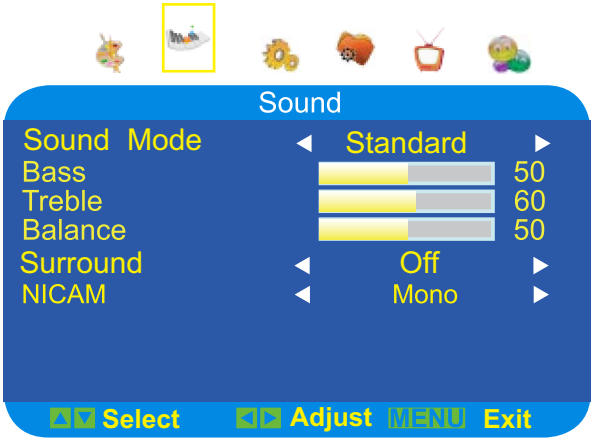


2.5.2 Sound Function

※ Adjustment of the Sound

1. Press the **Menu** button, and then press ◄ or ► button until the “Sound” menu appears.
2. Press ▲ or ▼ button to highlight the “Sound Mode”, “Bass”, “Treble”, “Balance”,“Sourround”, “NICAM” item.
3. Press ◄ or ► button to adjust.
4. Press the **Menu** button to return or exit.

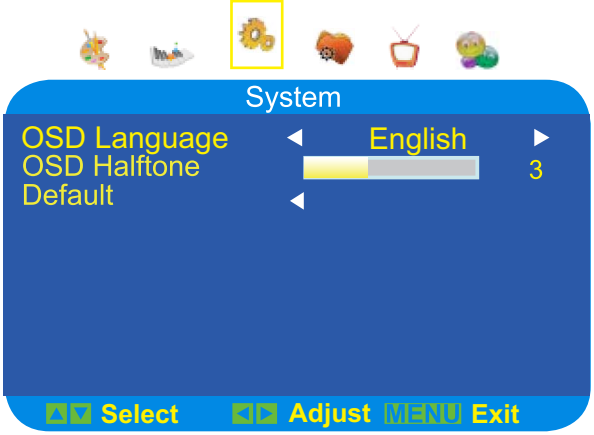
Note: “NICAM” item is optional.



2.5.3 System Function

※ Adjustment of the System

1. Press the **Menu** button, and then press ◄ or ► button until the “System” menu appears.
2. Press ▲ or ▼ button to highlight the “OSD Language”,“OSD Halftone”, “Default” item.
3. Press ◄ or ► button to adjust.
4. Press the **Menu** button to return or exit.



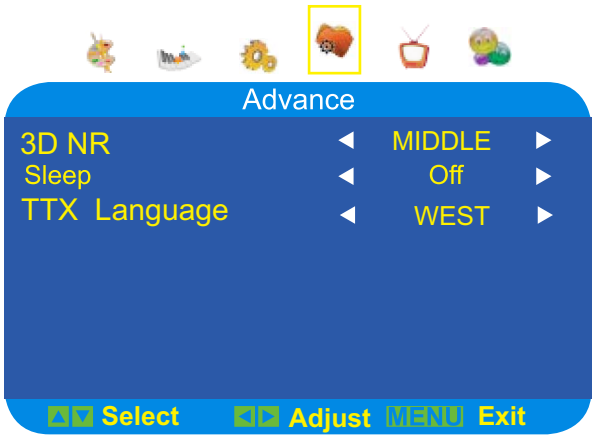
2.5.4 Advance Function

※ Adjustment of the Advance

To control the noise reduction.

1. Press the **Menu** button, and then press ◄ or ► button until the “Advance” menu appears.
2. Press ▲ or ▼ button to highlight the “3D NR”, “Sleep”,“TTX Language” item.
3. Press ◄ or ► button to select .
4. Press the **Menu** button to return or exit.

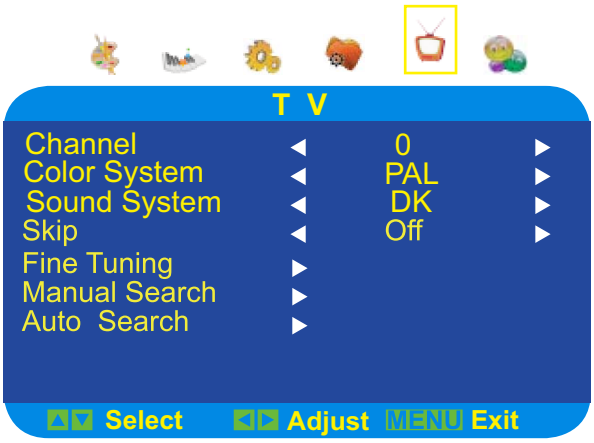
Note: Inactive for VGA and DVI→HDMI.



2.5.5 TV Function (Optional) (Only for TV)

※ Adjustment of the TV

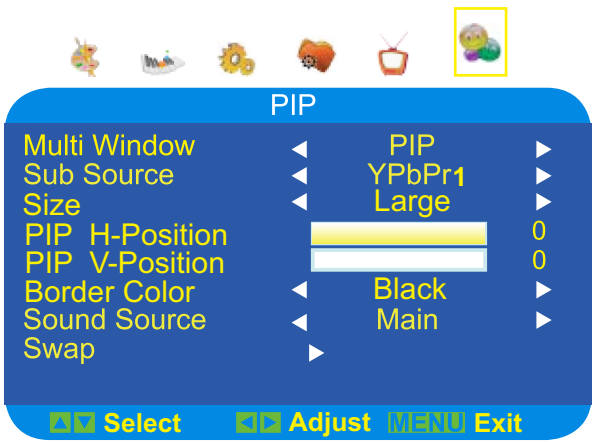
1. Press the **Menu** button, and then press ◄ or ► button until the “TV” menu appears.
2. Press ▲ or ▼ button to highlight the “Channel”, “Color System”, “Sound System”, “Skip”, , “FineTuning”, “Manual Search”, “Auto Search” item.
3. Press ◄ or ► button to select .
4. Press the **Menu** button to return or exit.



2.5.6 PIP Function

※ Adjustment of the PIP

1. Press the **Menu** button, and then press ◄ or ► button until the “PIP” menu appears.
2. Press ▲ or ▼ button to highlight the “Multi Window”,“Sub Source”,“Size”, “PIP H-Position”,“PIP V-Position”, “Border Color”,“Sound Source”, “Swap” item.
3. Press ◄ or ► button to adjust.
4. Press the **Menu** button to return or exit.



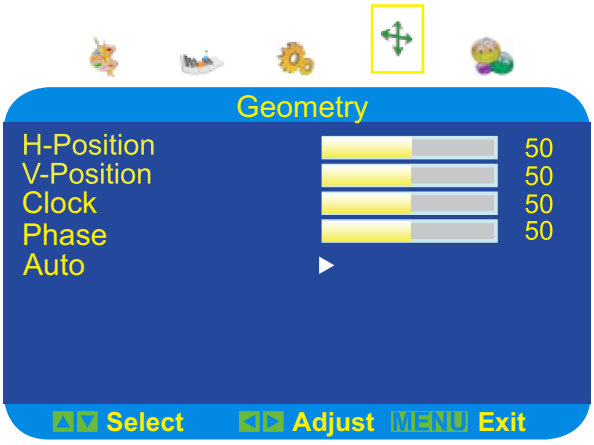
PIP Setting(O, PIP function, X, non-PIP function)

Sub / Main	TV	AV	S-Video	YPbPr	VGA	HDMI
TV	X	X	X	O	O	O
AV	X	X	X	O	O	O
S-Video	X	X	X	O	O	O
YPbPr	O	O	O	X	X	X
VGA	O	O	O	X	X	X
HDMI	O	O	O	X	X	X

2.5.7 Geometry Function (Only for VGA)

※ Adjustment of the Geometry

1. Press the **Menu** button, and then press ◄ or ► button until the “Geometry” menu appears.
2. Press ▲ or ▼ button to highlight the “H-Position”,“V-Position”,“Clock”, “Phase”, “Auto” item.
3. Press ◄ or ► button to adjust.
4. Press the **Menu** button to return or exit.



2.5.8 MEDIA Function (Option)

※ Adjustment of the MEDIA

1. In MEDIA Source.the MEDIA MENU will always appear as right.
2. Press ▲ or ▼ button to select JPEG,MP3 or DEVICE function,The JPEG only support.jpg format data,MP3 only support.mp3 format data the device only support FAT32 format hard disk.
3. Press ◄ or ► button to highlight the JPEG or MP3 file,the press ► button to play music or decording picture.
4. Press the **Menu** button to return or exit.

2.6 Using the Teletext Function (Optional)

Note: When pressing the Teletext function keys on the remote control, if the word "NO TTX" is displayed onscreen, it means the related function can't be used.

Teletext is a free service broadcast by most TV stations which give up-to-the-minute information news,weather,television programs, share price,subtitles,and many other topics.

To operate TELETEXT

※ Select a TV station on which Teletext is being transmitted.

※ Press the **Text** button once to bring up the teletext screen.Two page numbers are displayed on the screen headline.The first page number indicates your selection,while the second shows the current page displayed.

Teletext Page Selection

※ Enter the required Teletext page as a three digit numbers. The selected page number is displayed at the top left corner of the screen. The Teletext page counter searches until the selected page number is located,so that the desired page is displayed on the screen.

※ The ▲ , ▼ buttons can be used to select the preceding or following page.

※ Fast find using the **4 coloured buttons**.Four subject-headed pages can be selected quickly by pressing the corresponding coloured buttons **Red**,**Green**,**Yellow**,or **Blue** on the remote control.

Useful features for Teletext

Mix

※ Press repeatedly to turn on Teletext⟶Teletext blending with TV program ⟶Teletext mode.

Index

※ Press this button to select the index page that displays the list of teletext contents.

Hold

※ The teletext page you have selected may contain more information than is on the screen;The rest of the information will be displayed after a period of time on a sub page.

※ Press **Hold** button to stop the automatic page change.The hold symbol will be displayed at the top left-hand corner on the screen and the automatic page change will be stopped.

※ Press **Hold** button again to continue.

Reveal

※ Press this button once to display concealed information,such as solutions of riddles,puzzles or a quiz.

※ Press this button again to conceal the revealed answers.

Size

※ Press repeatedly to double the character size in the following order:Upper half of the page, Lower half of the page, Return to normal size.

Page

※ Press this button to enter the sub page mode.You can use ▲, ▼ button to display sub page; Press again to exit.

CE

※ Press to hide teletext contents, press again to reappear.

List

※ Press this button to list mode, press again to exit.

3. Technical Specification

Product Model	L32K6	L37K6	L42K6
Screen Size	32” diagonal	37” diagonal	42” diagonal
Aspect Ratio	16:9		
Power Supply	AC 100-240V~ , 50/60 Hz		
Power Consumption	140 W	200 W	280 W
TV System	PAL B/G D/K I, SECAM B/G D/K		
Audio Output Power (Internal)	6W x 2	6W x 2	8W x 2
Input Terminal	✦ Antenna Input (DIN Type) x 1 ✦ VGA (D-Sub 15 Pin Type) x 1 ✦ HDMI (Ver. 1.3) Connector x 2 ✦ S-Video Input Mini Din 4 Pin Terminals x 1 ✦ Video Input RCA Terminals x 3 ✦ Component Video - YPbPr x 2 RCA Terminals ✦ Stereo Audio x 3RCA,x 1（ Phone Jack for VGA/DVI） ✦ MEDIA(USB Type) x 1		
Output Terminal	✦ 1 set of Audio Output Terminals (RCA, L&R) ✦ 1 set of Video Output RCA Terminals ✦ 1 set of S/PDIF Output RCA Terminals		
Outline Size (LxWxH)(mm) without stand with stand	799x88x529 799x236x564	914x93x595 914x236x634	1022x93x657 1022x256x712
Gross Weight	15.2Kg	19.2kg	22.5kg
Working Temperature	0℃~40℃		
Working Humidity	20% ~ 80% Non-condensing		

4. Supported Signal Modes

A. VGA Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
640 x 480	31.50	60.00
800 x 600	35.16	56.25
	37.90	60.00
1024 x 768	48.40	60.00

Note: 1. When in VGA mode, you'd better choose the resolution of 1024 x 768.
2. You're suggested to use the VGA connecting cord of not more than 5 meters to ensure the appropriate picture quality.

B. YPbPr Mode

Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480i	15.734	59.94
480p(720x480)	31.468	59.94
576i	15.625	50.00
576p(720x576)	31.25	50.00
720p(1280x720)	37.50	50.00
	45.00	60.00
1080i	28.13	50.00
	33.75	60.00
1080P(1920x1080)	67.50	60.00
	56.25	50.00

C. HDMI Mode

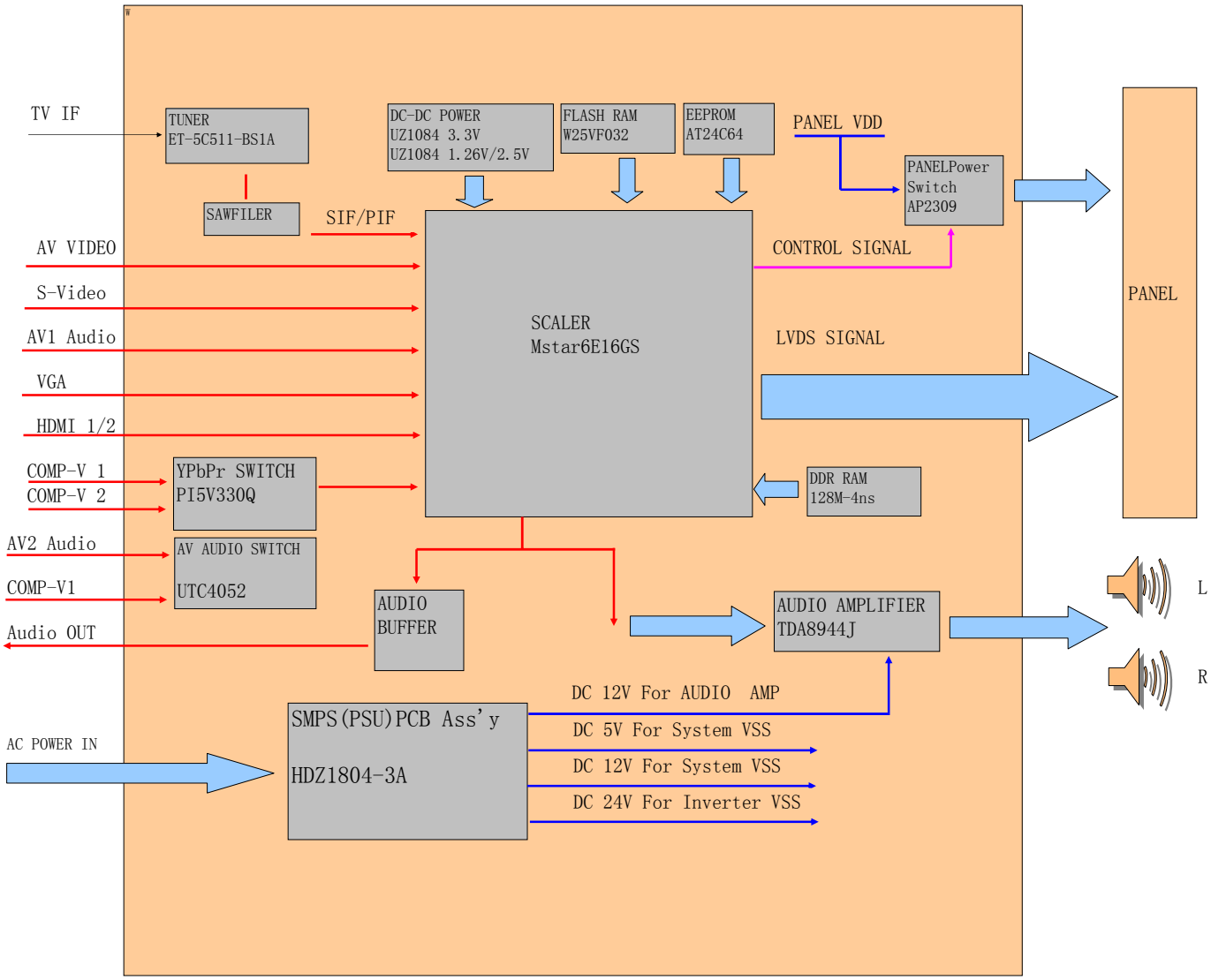
Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)
480p	31.468	59.94
576p	31.25	50.00
720P	45.00	60.00
1080i	33.75	60.00
1080P(1920x1080)	67.50	60.00

Note: HDMI mode can't be applied to PC function.

- When the signal received by the Display exceeds the allowed range, a warning message will appear on the screen.
- You can confirm the input signal format onscreen.

Simplified Functional Block Diagram

Mstar-6E16GS Chassis



MST6E16GS-LF

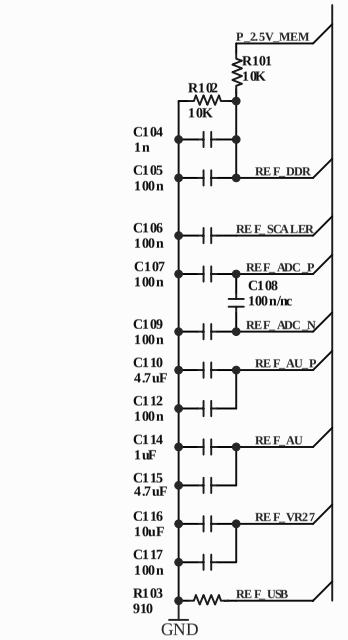
U103

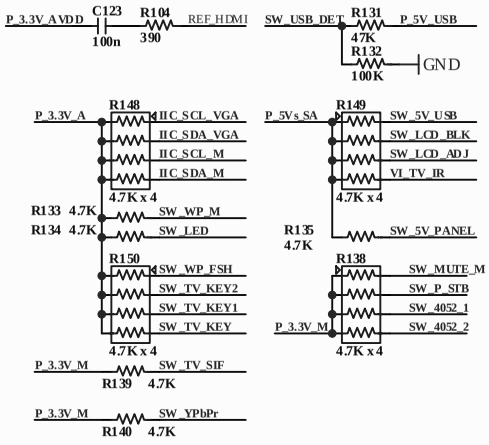
VI_H1_CLK-	1	RXACKN	
VI_H1_CLK+	2	RXACKP	
VI_H1_TX0-	3	RXA0N	
VI_H1_TX0+	4	RXA0P	
P_3.3V_AVDD	5	AVDD_33	
VI_H1_TX1-	6	RXA1N	
VI_H1_TX1+	7	RXA1P	
VI_H1_TX2-	8	RXA2N	
VI_H1_TX2+	9	RXA2P	
SW_H1_HPD	10	HOTPLUGA	
REF_HDMI	11	REXT	
IIC_SDA_H1	12	DDCDA_SDA	
IIC_SCL_H1	13	DDCDA_SCA	
REF_SCALER	14	VCLAMP	
REF_ADC_P	15	REFP	
REF_ADC_N	16	REFM	
VI_SW_BIN+	17	BIN1P	
VI_SW_SOG	18	SOGIN1	
VI_SW_GIN+	19	GIN1P	
VI_SW_RIN+	20	RIN1P	
VI_VGA_BIN-	21	BIN0M	
VI_VGA_BIN+	22	BIN0P	
VI_VGA_GIN-	23	GIN0M	
VI_VGA_GIN+	24	GIN0P	
VI_VGA_SOG	25	SOGIN0	
VI_VGA_RIN+	26	RIN0P	
P_3.3V_AVDD	27	AVDD_33	
GND	28	GND	
VI_VGA_HS	29	HSYNC0	
VI_VGA_VS	30	VSYNC0	
SW_SC2_FB	31	VSYNC2	
VI_S1_Yin	32	Y0	
VI_S1_Cin	33	CVBS3	
VI_AV3_Vin	34	CVBS2	
VI_AV2_Vin+	35	CVBS1	
VI_AV2_Vin-	36	VCOM1	
VI_AV1_Vin+	37	CVBS0	
VI_AV1_Vin-	38	VCOM0	
P_3.3V_AVDD	39	AVDD_33	
VI_CVBS2_Out	40	CVBSOUT1	
VI_CVBS1_Out	41	CVBSOUT0	
GND	42	GND	
X_OUT	43	XOUT	
X_IN	44	XIN	
P_3.3V_MPLL	45	AVDD_MPLL	
REF_VR27	46	GND_VIFPLL	
P_3.3V_SIF	47	VR27	
GND	48	AVDD_RXS	
AU_TV_SIF+	49	GND_RXS	
AU_TV_SIF-	50	SIFP	
VI_TV_VIF-	51	SIFM	
VI_TV_VIF+	52	VIFM	
GND	53	VIFP	
P_3.3V_VIF	54	AVDD_RXV	

SW_TV_AGC	55	TAGC	
P_3.3V_AU	56	AVDD_33	
GND	57	GND	
GND	58	AUVRM	
REF_AU_P	59	AUVRP	
REF_AU	60	AUVAG	
P_3.3V_AU	61	AVDD_AU	
AU_VGA_L	62	LINE_IN_0L	
AU_VGA_R	63	LINE_IN_0R	
AU_MUX_L	64	LINE_IN_1L	
AU_MUX_R	65	LINE_IN_0R	
AU_GND	66	AUCOM	
AU_Out_L3	67	LINE_OUR_3L	
AU_Out_R3	68	LINE_OUT_3R	
AU_Out_L2	69	LINE_OUT_2L	
AU_Out_R2	70	LINE_OUT_2R	
AU_Out_L1	71	LINE_OUT_1L	
AU_Out_R1	72	LINE_OUT_1R	
SW_YPbPr	73	GPIOD[0]	
SW_TV_SIF	74	GPIOD[1]	
SW_MUTE_M	75	GPIOD[2]	
P_3.3V_VDDP	76	VDDP	
GND	77	GND	
P_1.2V_C	78	VDDC	
SW_SCL_FS	79	AD[0]	
SW_P_STB	80	AD[1]	
SW_SC2_FS	81	AD[2]	
SW_SCL_FB	82	AD[3]	
AU_SPDIF_O	83	WRZ	
SW_4052_1	84	RDZ	
SW_4052_2	85	ALE	
DDR_BA1	86	BADR[1]	
DDR_BA0	87	BADR[0]	
DDR_RASZ	88	RASZ	
P_1.2V_C	89	VDDC	
GND	90	GND	
P_2.5V_MEM	91	AVDD_MI	
DDR_CASZ	92	CASZ	
DDR_WEZ	93	WEZ	
DDR_AR11	94	MADR[11]	
DDR_AR10	95	MADR[10]	
DDR_AR9	96	MADR[9]	
DDR_AR8	97	MADR[8]	
DDR_AR7	98	MADR[7]	
DDR_AR6	99	MADR[6]	
DDR_AR5	100	MADR[5]	
DDR_AR4	101	MADR[4]	
DDR_AR3	102	MADR[3]	
DDR_AR2	103	MADR[2]	
DDR_AR1	104	MADR[1]	
DDR_AR0	105	MADR[0]	
GND	106	GND	
P_2.5V_MEM	107	AVDD_MI	
P_3.3V_MPLL	108	AVDD_MIPLL	

DDCDB_SCL	216	IIC_SCL_H2	
DDCDB_SDA	215	IIC_SDA_H2	
HPLUGB	214	SW_H2_HPD	
RXB2P	213	VI_H2_TX2+	
RXB2N	212	VI_H2_TX2-	
GND	211	GND	
RXB1P	210	VI_H2_TX1+	
RXB1N	209	VI_H2_TX1-	
GND	208	GND	
RXB0P	207	VI_H2_TX0+	
RXB0N	206	VI_H2_TX0-	
AVDD_33	205	P_3.3V_AVDD	
RXBCKP	204	VI_H2_CLK+	
RXBCKN	203	VI_H2_CLK-	
VDDC	202	P_1.2V_C	
GPIOM[1]	201	SW_PBP_DISPEN	
GPIOM[0]	200	SW_USB_DET	
GND	199	GND	
VDDP	198	P_3.3V_VDDP	
LVB0M	197	VI_LV_RA0-	
LVB0P	196	VI_LV_RA0+	
LVB1M	195	VI_LV_RB0-	
LVB1P	194	VI_LV_RB0+	
LVB2M	193	VI_LV_RC0-	
LVB2P	192	VI_LV_RC0+	
LVBCKM	191	VI_LV_CK0-	
LVBCKP	190	VI_LV_CK0+	
LVB3M	189	VI_LV_RD0-	
LVB3P	188	VI_LV_RD0+	
LVB4M	187	VI_LV_RE0-	
LVB4P	186	VI_LV_RE0+	
GND	185	GND	
VDDP	184	P_3.3V_VDDP	
LVA0M	183	VI_LV_RA1-	
LVA0P	182	VI_LV_RA1+	
LVA1M	181	VI_LV_RB1-	
LVA1P	180	VI_LV_RB1+	
LVA2M	179	VI_LV_RC1-	
LVA2P	178	VI_LV_RC1+	
LVACKM	177	VI_LV_CK1-	
LVACKP	176	VI_LV_CK1+	
LVA3M	175	VI_LV_RD1-	
LVA3P	174	VI_LV_RD1+	
LVA4M	173	VI_LV_RE1-	
LVA4P	172	VI_LV_RE1+	
VDDC	171	P_1.2V_C	
GND	170	GND	
HWRESET	169	SW_RESET	
GPIOT[1]	168	SW_5V_USB	
VDDP	167	P_3.3V_VDDP	
PWM3	166	SW_LCD_BLK	
PWM2	165	SW_LCD_ADJ	
VDDP	164	P_3.3V_AVDD	
IRIN	163	VI_TV_IR	

INT	162	SW_5V_PANEL	
DDCA_SCL	161	IIC_SCL_VGA	
DDCA_SDA	160	IIC_SDA_VGA	
DDCR_SCL	159	IIC_SCL_M	
DDCR_SDA	158	IIC_SDA_M	
PWM1	157	SW_WP_M	
PWM0	156	SW_LED	
SAR3	155	SW_WP_FSH	
SAR2	154	SW_TV_KEY2	
SAR1	153	SW_TV_KEY1	
SAR0	152	SW_TV_KEY	
VDDC	151	P_1.2V_C	
GND	150	GND	
SPI_SDO	149	SPI_DO	
SPI_SCZ	148	SPI_CZ	
SPI_SDI	147	SPI_DI	
SPI_SCK	146	SPI_CK	
VDDP	145	P_3.3V_VDDP	
GND	144	GND	
USB20_DP	143	VI_USB_D+	
USB20_DM	142	VI_USB_D-	
AVDD_USB	141	P_3.3V_VDDP	
USB20_REXT	140	REF_USB	
MVREF	139	REF_DDR	
MCLKE	138	DDR_CKE	
MCLK	137	DDR_MCLK+	
MCLKZ	136	DDR_MCLK-	
DQM1	135	DDR_UDQM	
DQS1	134	DDR_DQS1	
AVDD_MI	133	P_2.5V_MEM	
MDATA[15]	132	DDR_DATA15	
MDATA[14]	131	DDR_DATA14	
MDATA[13]	130	DDR_DATA13	
MDATA[12]	129	DDR_DATA12	
AVDD_MI	128	P_2.5V_MEM	
MDATA[11]	127	DDR_DATA11	
MDATA[10]	126	DDR_DATA10	
GND	125	GND	
MDATA[9]	124	DDR_DATA9	
MDATA[8]	123	DDR_DATA8	
AVDD_MI	122	P_2.5V_MEM	
MDATA[7]	121	DDR_DATA7	
MDATA[6]	120	DDR_DATA6	
MDATA[5]	119	DDR_DATA5	
MDATA[4]	118	DDR_DATA4	
AVDD_MI	117	P_2.5V_MEM	
MDATA[3]	116	DDR_DATA3	
MDATA[2]	115	DDR_DATA2	
GND	114	GND	
MDATA[1]	113	DDR_DATA1	
MDATA[0]	112	DDR_DATA0	
AVDD_MI	111	P_2.5V_MEM	
DQS0	110	DDR_DQS0	
DQM0	109	DDR_LDQM	





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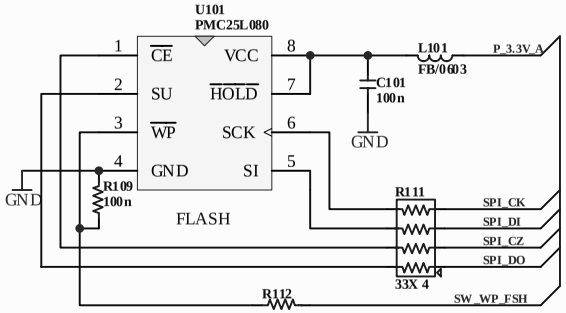

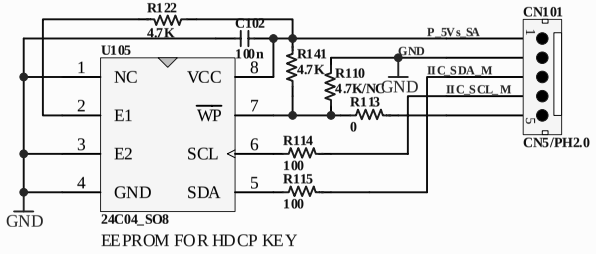

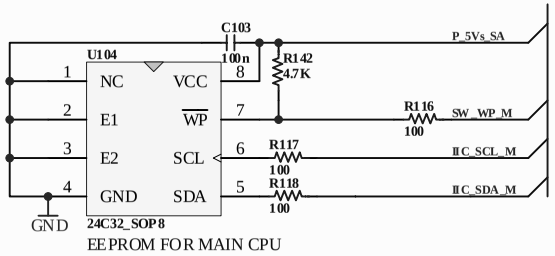

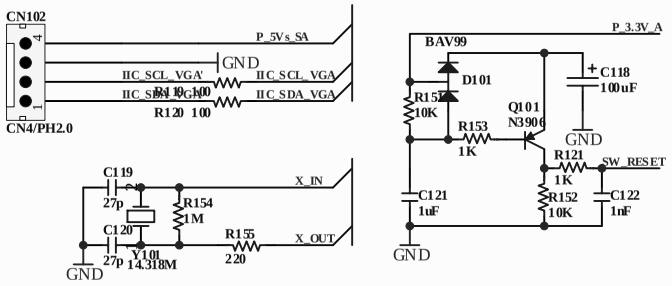

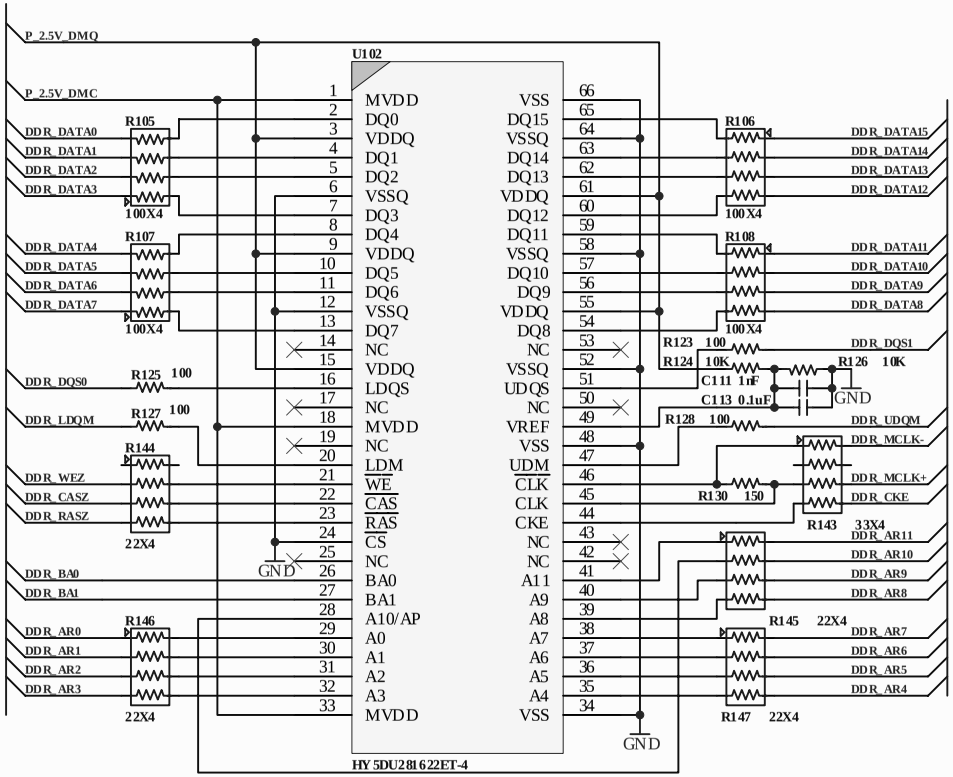

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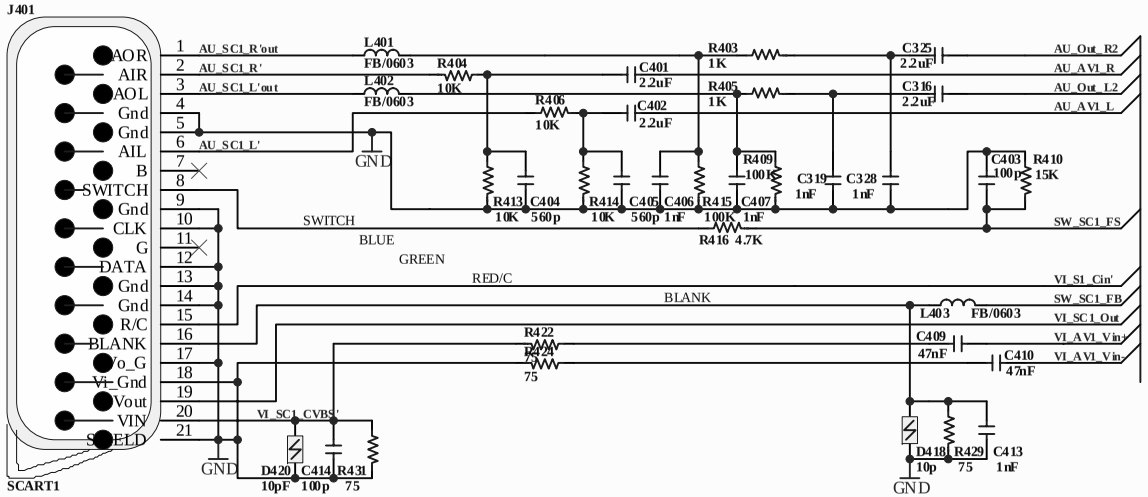

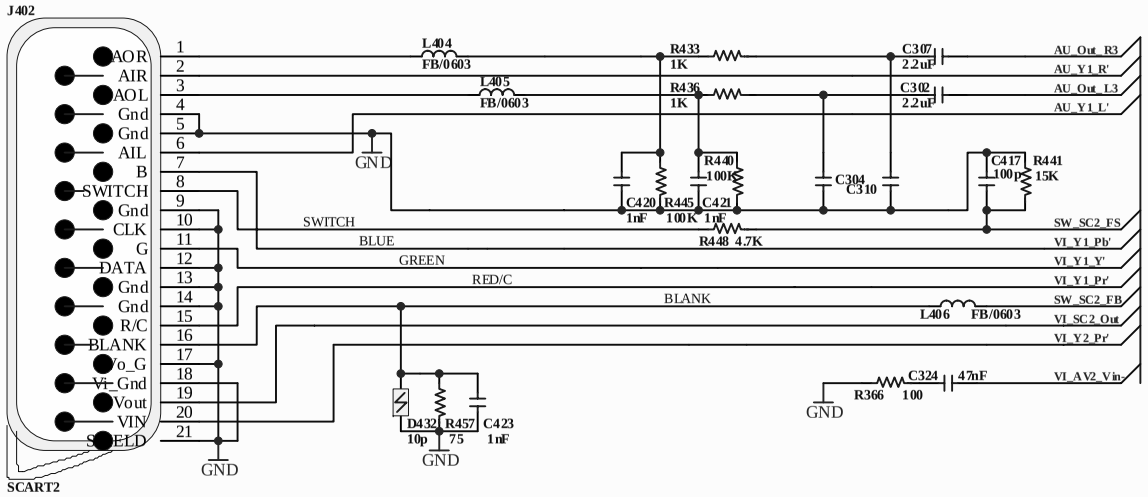

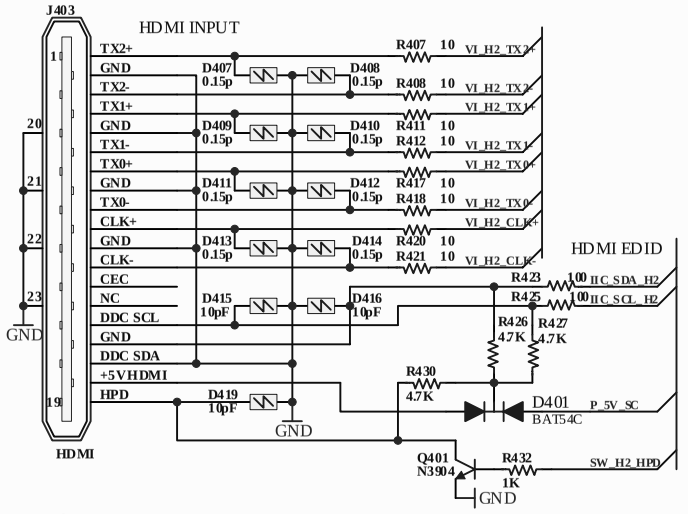

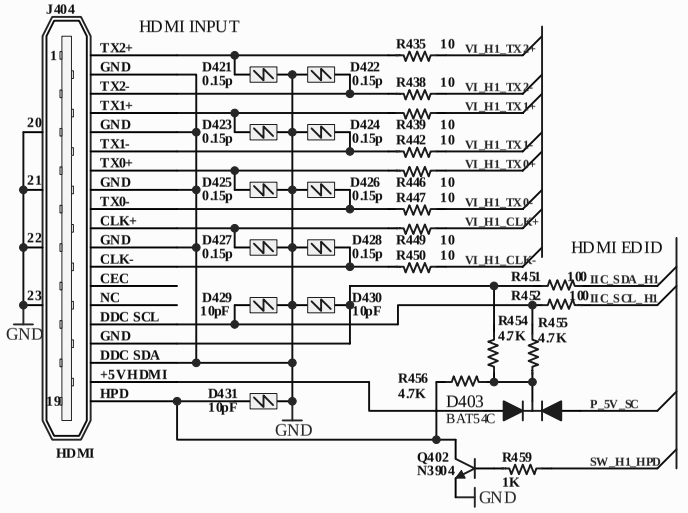

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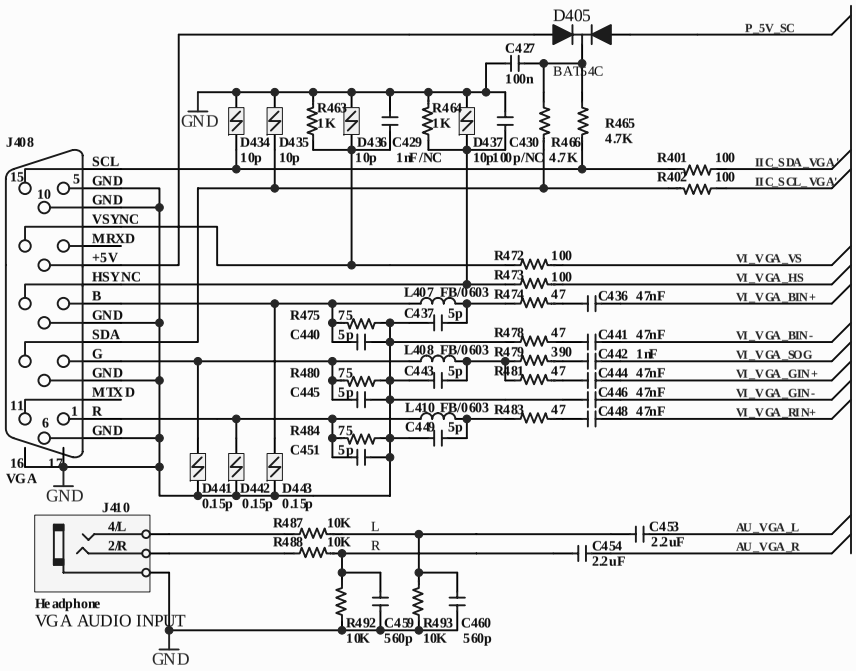

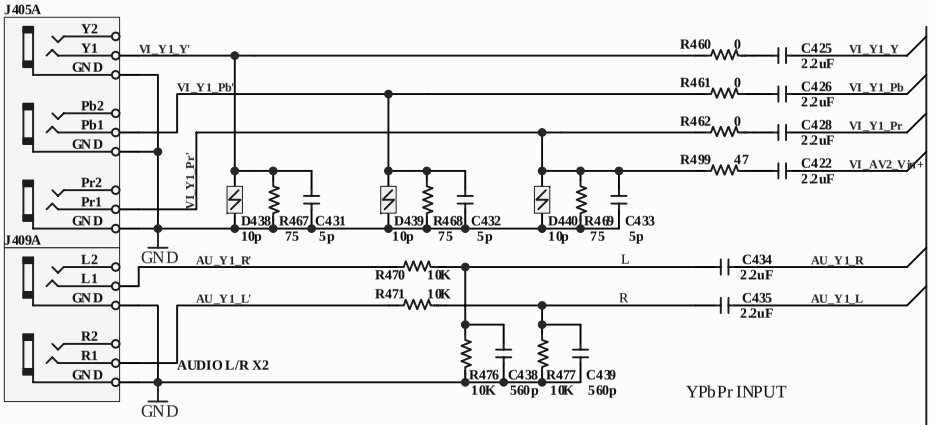

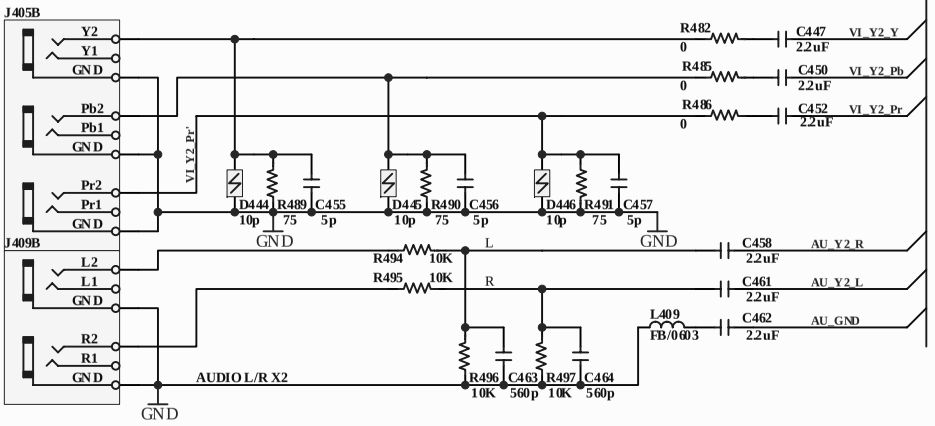

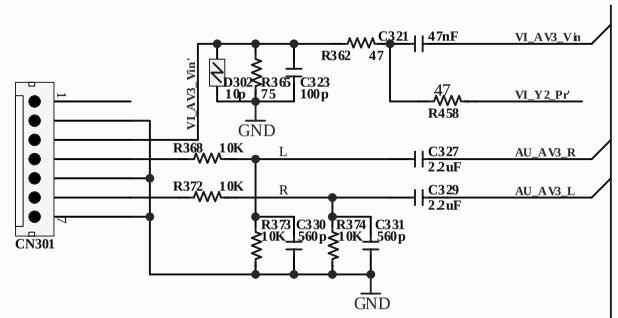

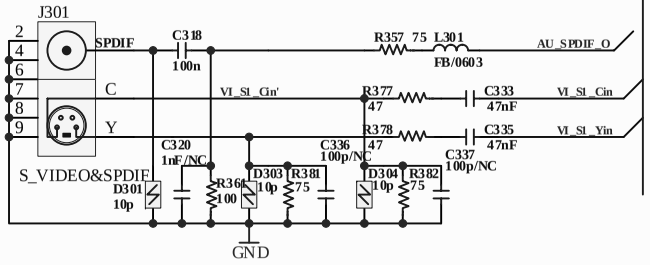

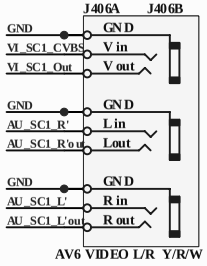

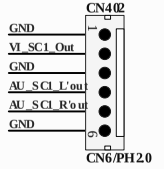

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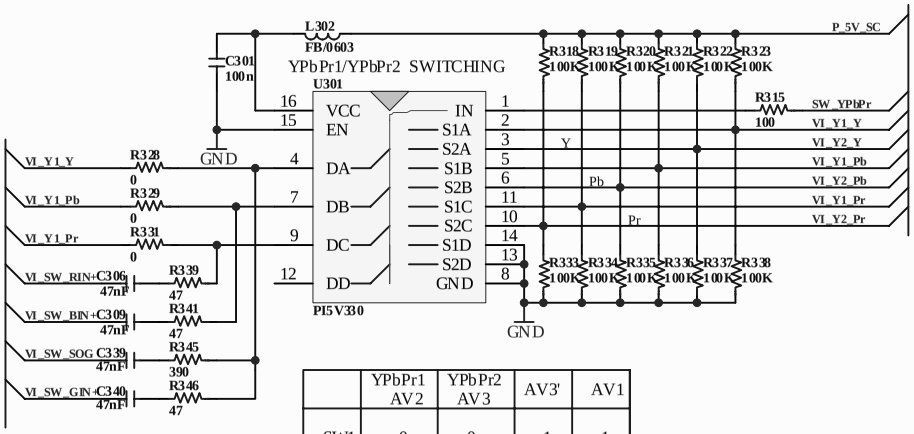
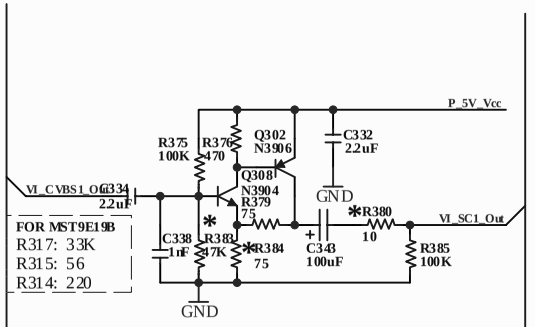
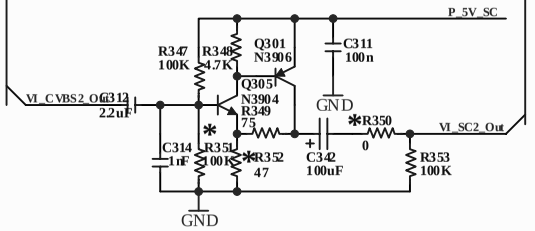
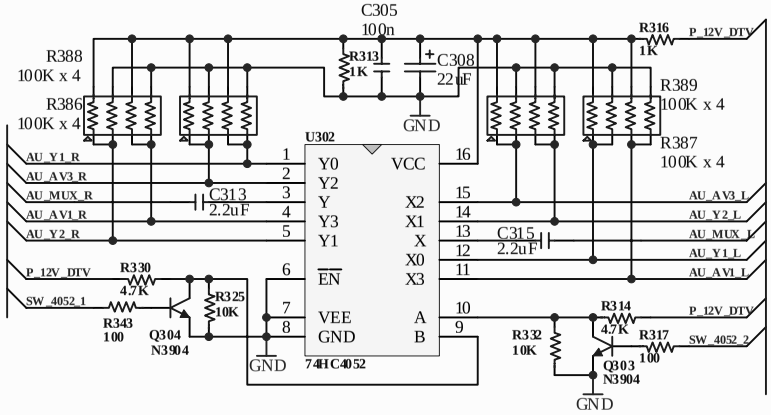
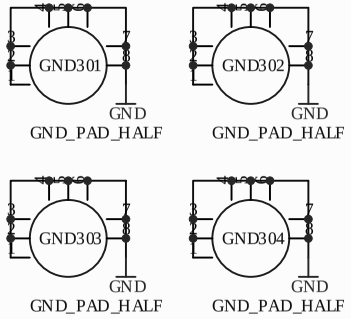


	YPbPr1 AV2	YPbPr2 AV3	AV3'	AV1
SW1	0	0	1	1
SW2	0	1	0	1









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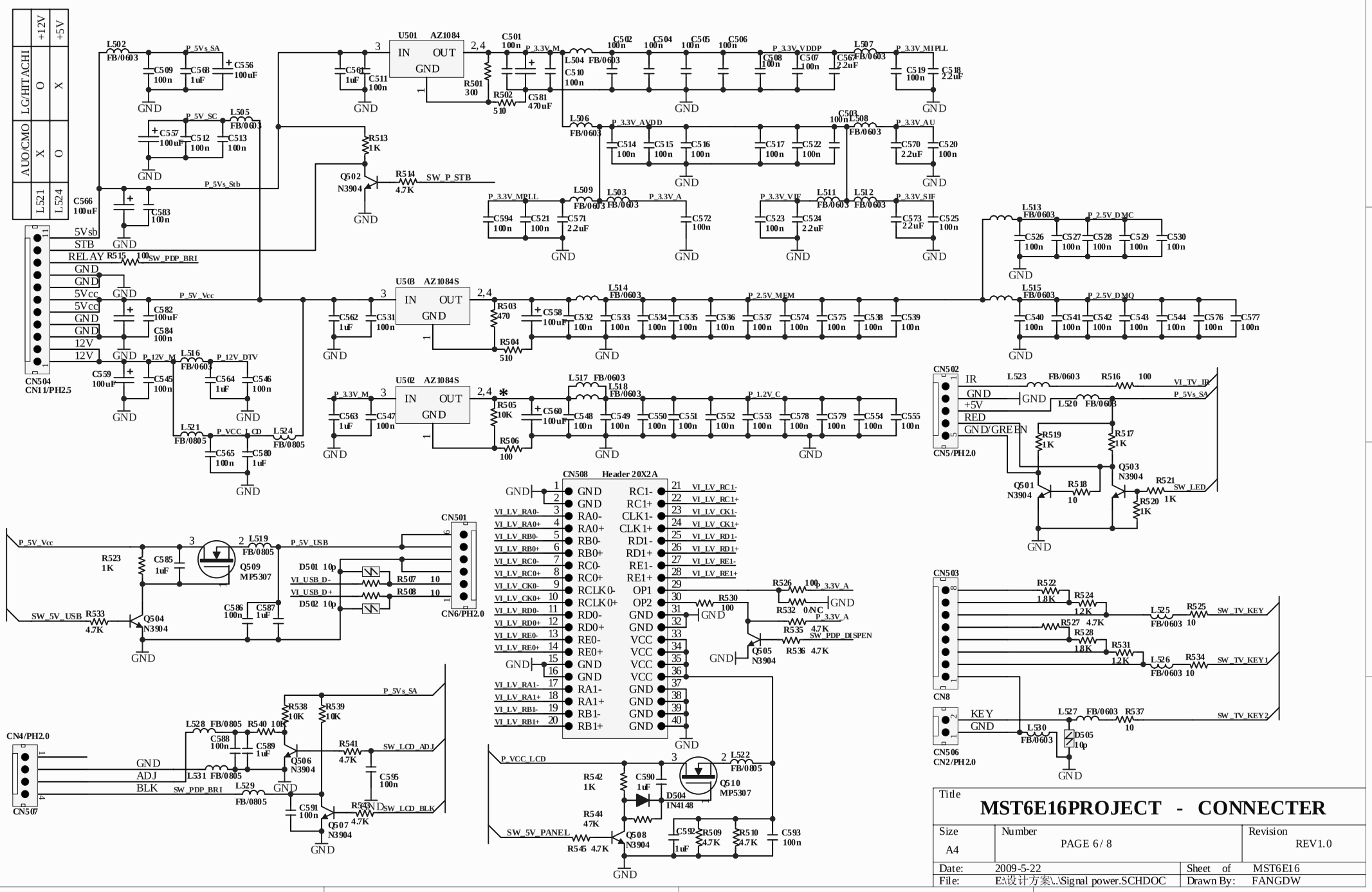

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MST6E16PROJECT - CONNECTER

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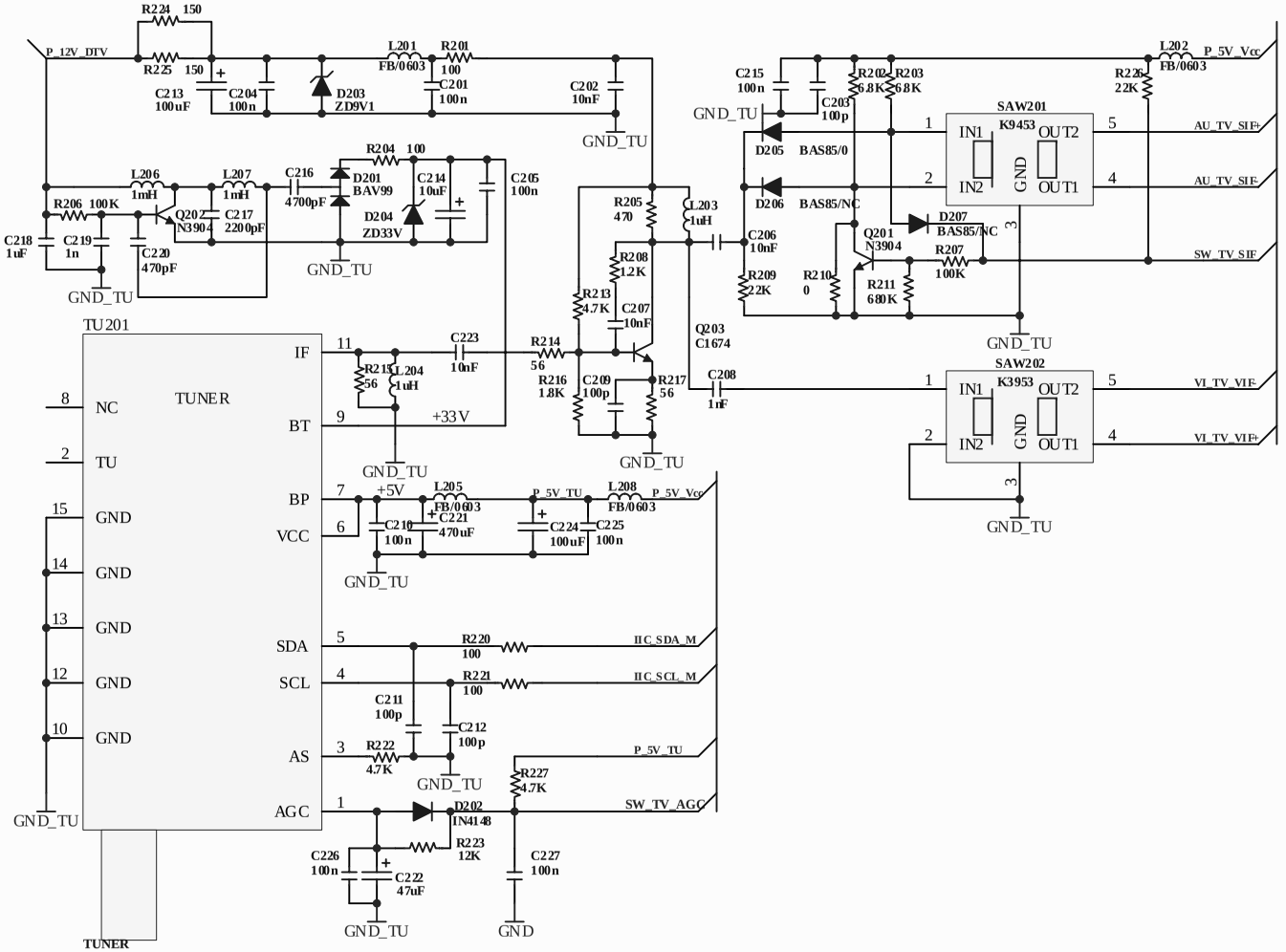

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Date: 2009-5-22		Sheet of	MST6E16
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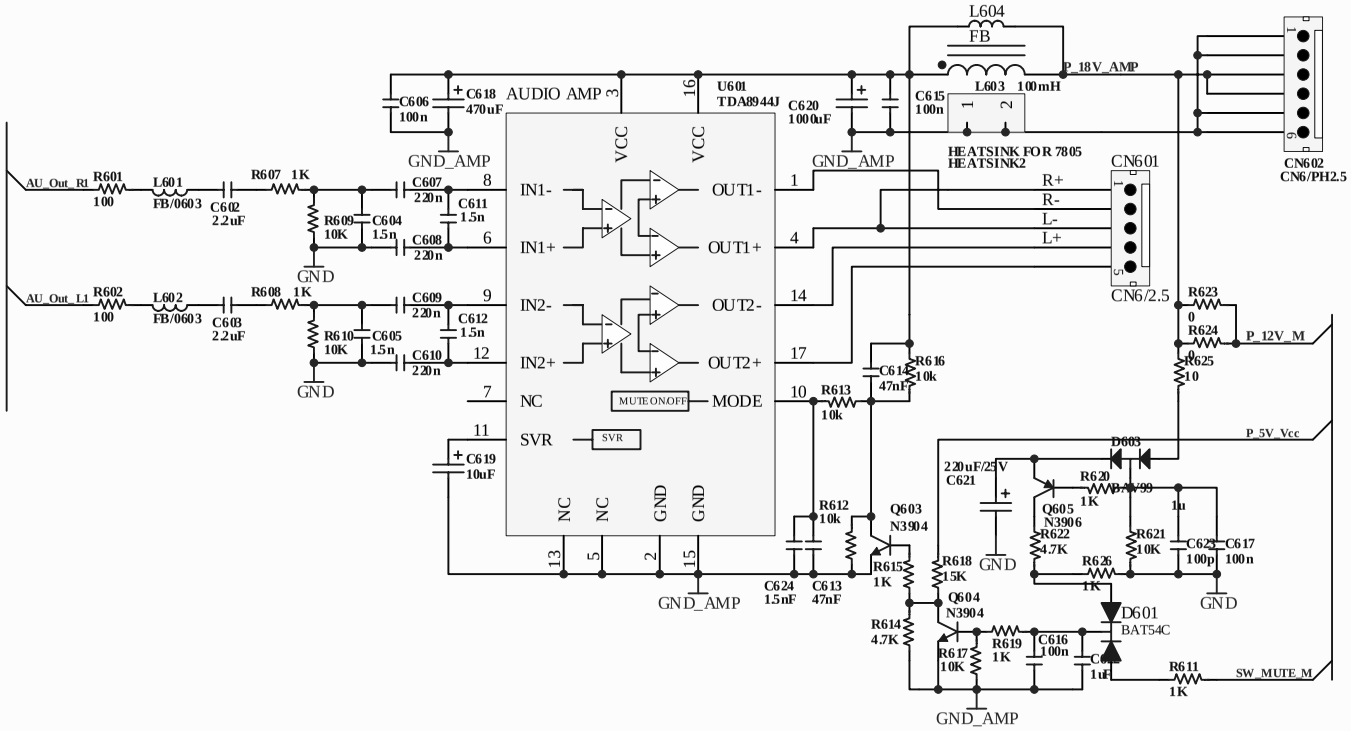

Title: **MST6E16 PROJECT - AUDIO AMP**		
Size: A4	Number: PAGE 8/ 8	Revision: REV1.0
Date: 2009-5-22	Sheet of MST6E16	
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Basic Operations & Circuit Description

Main Electric Components

(1). MODULE:

There are 1 pc. panel and 3 pcs. PCB including 1 pc. INVERTER board(L), 1 pc. INVERTER board(R),1 pc. T-CONTROL board,

(2).SIGNAL PROCESS

There are 3 pcs. PCBs including

1 pc. Main digital board, With Tuner board Ass'y
1 pc. Keypad board,
1 pc. Remote Control Receiver board

(3).POWER

There are 1 pc. PCB for power.

PCB function

1. Power board:

(1). Input voltage: AC 100V~240V, 50~60Hz.
Input range: AC 90V(Min)~250V(Max) auto regulation.
(2). To provide power for PCBs.
a). +24V for Inverter.
b). +5Vsb for standby,
c). +5V for signal power,
d). +12V for Audio Amp power
e). +12V for Tuner power and LCD pannel.

2. Main (Video InterFace) board:

(1).Decoder the video signal (TV,CVBS,S-VIDEO) from analog to digital signal.
(2).Converter the Video signals(TV,CVBS,S-VIDEO) and graphics signal (HDMI,VGA,YPbPr) from internace to progressive,
(3).Converter the Digital to fit the panel display mode and output the LVDS signal to Panel.
(4).Converter the TV input signal from IF to video and SIF signal ,
(5).Converter the digital and analog audio signal to tone controlled signal to audio AMPFILER. .

4. KEY board

To get the main button control on LCD_TV as
SOURCE,MENU, CHANEL +,CHANEL -,VOL +,VOL-, STANDBY functions.

5. Remote Control board

Receive the remote signal and active for the control.

6. T-CONTROL board

Converter the LVDS signal to the digital signal for fitting the PANEL.

7. INVERTER board

Converter the low DC voltage +24V to high AC voltage to drive the backlight.

PCB failure analysis

1. CONTROL:

a. Abnormal noise on screen.

b. No picture.

2. MAIN (VIDEO):

a. Lacking color, Bad color scale.

b. No voice.

c. No picture but with signals output, OSD and back light.

d. Abnormal noise on screen.

3. POWER:

No picture, no power output.

Basic operation of LCD-TV

1. After turning on power switch, power board sends 5Vst-by Volt to Micro Processor IC waiting for ON signals from Key Switch or Remote Receiver.

2. When the ON signal from Key Switch or Remote Receiver is detected, Micro Processor will send ON Control signals to Power. Then Power sends (5Vsc, 12Vsc, 24V and RLY ON, Vs ON) to PCBs working. This time VIF will send signals to display back light, OSD on the panel and start to search available signal sources. If the audio signals input, them will be amplified by Audio AMP and transmitted to Speakers.

3. If some abnormal signals are detected (for example: over volts, over current, over temperature and under volts), the system will be shut down by Power off.

LCD basic display theory.

When an electrical field is applied to the LC planes, the LC molecules re-align themselves so that they are parallel to the electrical field. This electrical process is known as **twisted nematic field effect** or **TNFE**. In this alignment, polarized light is not twisted as it passes through the LC material (see Diagram 3A and 3B). If the front polarizer is oriented perpendicular to the rear polarizer, light will pass through the energized display but will be blocked by the rear polarizer. An LCD in this form is acting as a light shutter.

Displays with variable characters are created by selectively etching away the conductive surface that was originally deposited on the glass. Etched areas become the display's background; unetched areas become the display's characters.

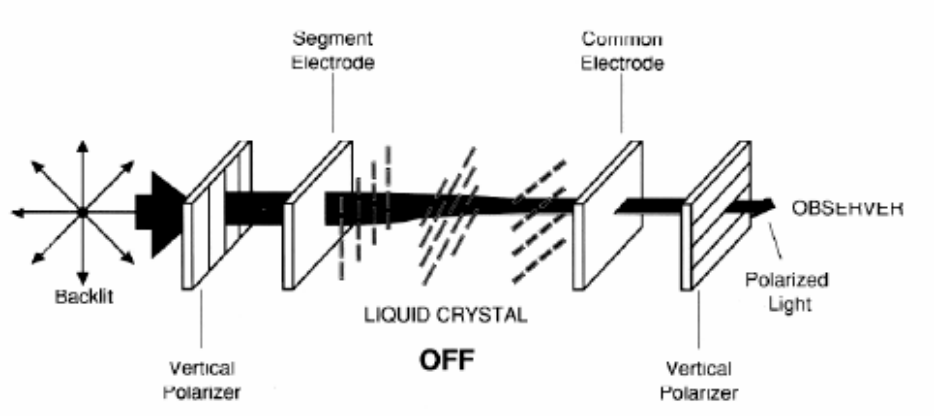

Diagram 3A. The "off" state of a TN LCD-the LC molecules form a twist and therefore cause polarized light to twist as it passes through.

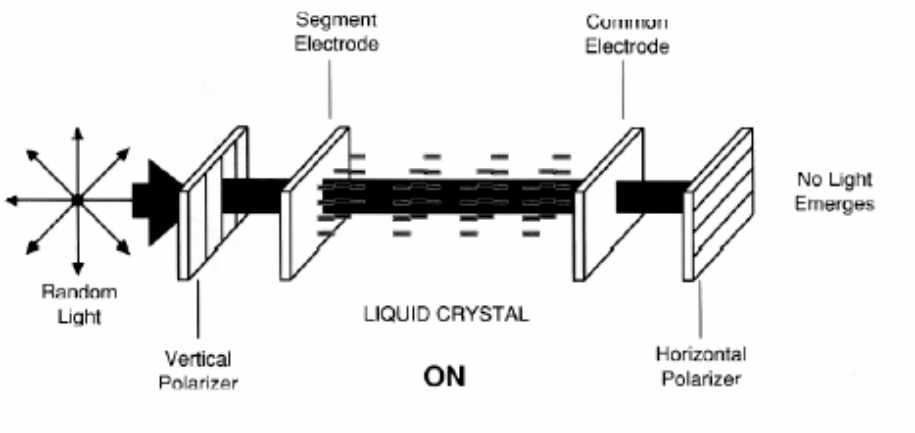

Diagram 3B. The "on" state-the electrical field re-aligns the LC molecules so they do not twist the polarized light.

Simple Troubleshooting

If the display fails or the performance changes dramatically, check the Display in accordance with the following instructions. Remember to check the peripherals to pinpoint the source of the failure.

Symptom	Solution
Power cannot be turned on.(Power indicator does not light.)	-Check that both ends of the power cable are plugged into the socket appropriately and the wall socket is operational.
No Input Signal message appears.	-Check that the signal line is connected properly. -Check that the power of the relevant peripherals is turned on. -Check that the Input option that has been selected matches with the input signal.
The remote control does not function properly.	-Check the batteries are not drained.(Use new batteries.) -Check that the remote control is within the operating range. -Check that the remote control is pointed to the remote control window on the display. -Check that there are no obstacles between the remote control and the remote control window.
Flashing spots or stripes appear on the screen.	-Check that there are no emission (Car, HV cable or Neon lamp) or other possible interference sources.
Image colour or quality deteriorates.	-Check that all the video settings are adjusted appropriately, such as brightness, contrast, colour etc. -For more information about video settings, refer to OSD Functions in Chapter 2.
Screen position and size are incorrect.	-Check that the screen position and size is adjusted appropriately.
Image or colour is incorrect.	-Check that the signal line is connected properly. -When connecting to a PC, you can change the resolution of the PC to acquire the correct image. The discrepancy of the PC output signal may affect the display of the image.
Display warning message.	-Check that the input signal line is properly fixed. -Select the correct input signal. -For more information, refer to Supported Signal Modes in Chapter 4.

FACTORY MODE INSTRUSTION：

1. Enter into foctory mode.

In TV normal mode ,Press key " S.MODE, 5,8,0 "will go into factory mode。Select the item by "Up" and "Down" keys, Adjust by "Left" and "Right" keys, Press "MENU" key to exit factory mode !

2. Factory mode function.

a. SHOP OUT and HEAT RUN function: This two mode is for factory production. After writing into the Flash data, should shop out the EEROM data and HEAT RUN for mass production.

Enter into factory mode and go into OPTION item, Press LEFT of remote control to use SHOP OUT, the power LED will flash for about 5 seconds, the TV will auto power down when complete. Power again will be normal.

Enter into factory mode and select HEAT RUN item, Press LEFT of remote control to HEAT RUN, The TV set will display 7 pure color picture circulate, Only Press the STANDARDBY key of the front key board can go back to normal mode.

b. Other factory setting and function.

FACTORY MODE						
SOURCE	TV	AV	S-VIDEO	YPbPr	VGA	HDMI
ADC ADJ		YPbPr	VGA			
	R OFF	127	127			For design using。
	G OFF	127	127			
	B OFF	127	127			
	R GAIN	78	78			
	G GAIN	69	69			
	B GAIN	78	78			
	AUTOTUNE					
PIC MODE		SOFT	STANDARD	BRIGHT		Set the value of different picture mode
	CONTRAST	50	60	70		
	BRIGHTNESS	40	50	60		
	HUE	50	50	50		
	SATURATION	40	50	50		
	SHARPNESS	40	50	50		
SND MODE		NEWS	MUSIC	STANDARD		
	BASS	40	75	50		
	TREBLE	70	75	50		
COL TEMP		NORMAL	WARM	COOL		
	R OFF	10	10	10		
	G OFF	10	10	10		
	B OFF	10	10	10		

	R GAIN	103		117		123		White balance setting.	
	G GAIN	108		114		129			
	B GAIN	115		110		129			
NON LINEAR		X0	X1		X2		X3		X4
For design using.	VOL	0	25		50		75		100
	BASS	0	25		50		75		100
	TREBLE	0	25		50		75		100
	SD.CON	80	100		120		140		160
	SD.BRI	18	63		109		154		200
	SD.HUE	0	25		50		75		100
	SD.SAT	0	63		127		191		255
	SD.SHP	0	5		10		15		20
	PC.CON	80	113		147		180		214
	PC.BRI	18	57		96		135		174
SSC SETTING									
	MEMORY CLOCK SSC								
		MODURATION	21						
		PERCENTAGE	0						
	PANNEL CLOCK SSC								
		MODURATION	1						
		PERCENTAGE	0						
EEPROM:	ADDR	00							
	DATA	00							
	SAVE								
OPTION:	HDCP KEY		0007A124A5F0						
	SHOP OUT								
	PRESET CHANNEL								
HEAT RUN									
S5	RW_	AU2601_	0U		C_		02		
(CHASSIS)	(MARKET AREA)	(PANNEL)	(LOGO)		(LANGUAGE)		VERSION		
VERSION V2.51 15:37:49 01/19/08					(TIME)				

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FEATURES

- LCD TV controller with PIP display functions
- Input supports up to UXGA & 1080P
- Panel supports up to full HD (1920x1080)
- TV decoder with 3-D comb filter
- Multi-standard TV sound demodulator and decoder
- 10-bit triple-ADC for TV and RGB/YPbPr
- 10-bit video data processing
- Integrated DVI/HDCP/HDMI compliant receiver
- High-quality dual scaling engines & dual 3-D video de-interlacers
- 3-D video noise reduction
- MStarACE-3 picture/color processing engine
- Embedded On-Screen Display (OSD) controller engine
- Built-in MCU supports PWM & GPIO
- Built-in dual-link 8/10-bit LVDS transmitter
- 5-volt tolerant inputs
- Low EMI and power saving features
- 216-pin LQFP

■ NTSC/PAL/SECAM Video Decoder
- Supports NTSC M, NTSC-J, NTSC-4.43, PAL (B,D,G,H,M,N,I,Nc), and SECAM
- Automatic TV standard detection
- 3-D Comb filter for NTSC/PAL
- 5 configurable CVBS & Y/C S-video inputs
- Supports Teletext level-1.5, WSS, VPS, Closed-caption, and V-chip
- CVBS video output

■ Video IF for Multi-Standard Analog TV
- Digital low IF architecture
- Stepped-gain PGA with 26 dB tuning range and 1 dB tuning resolution
- Maximum IF analog gain of 37dB in addition to digital gain
- Programmable TOP to accommodate different tuner gain to optimize noise and linearity performance

■ Multi-Standard TV Sound Decoder
- Supports BTSC/NICAM/A2/EIA-J demodulation and decoding
- FM stereo & SAP demodulation
- L/Rx2 and SIF audio inputs
- L/Rx2 loudspeaker and line outputs
- Supports sub-woofer output
- Built-in audio output DAC's
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, and P/G EQ
- Support MP3 decode
- Optional advanced surround available (Dolby[1], SRS[2], BBE[3]... etc) **Note**

■ Digital Audio Interface
- S/PDIF digital audio input & output
- HDMI audio channel processing capability
- Programmable delay for audio/video synchronization

■ Analog RGB Compliant Input Ports
- Two analog ports support up to UXGA
- Fast blanking and function selection switch support full SCART functions
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

■ DVI/HDCP/HDMI Compliant Input Port
- Two DVI/HDMI input ports with built-in switch
- Supports TMDS clock up to 225MHz @ 1080P 60Hz with 12-bit deep-color resolution
- Single link on-chip DVI 1.0 compliant receiver
- High-bandwidth Digital Content Protection (HDCP) 1.1 compliant receiver
- High Definition Multimedia Interface (HDMI) 1.3 compliant receiver with CEC support

[1] **Trademark of Dolby Laboratories**
[2] **Trademark of SRS Labs, Inc.**
[3] **Registered trademark of BBE Sound, Inc.**

- Long-cable tolerant robust receiving
- Support HDTV up to 1080P

■ Auto-Configuration/Auto-Detection
- Auto input signal format and mode detection
- Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
- Sync detection for H/V Sync

■ High-Performance Scaling Engines
- Fully programmable shrink/zoom capabilities
- Nonlinear video scaling supports various modes including Panorama

■ Video Processing & Conversion
- 3-D motion adaptive video de-interlacer
- Edge-oriented adaptive algorithm for smooth low-angle edges
- Automatic 3:2 pull-down & 2:2 pull-down detection and recovery
- PIP with programmable size and location, supports multi-video applications
- MStar 3rd Generation Advanced Color Engine (MStarACE-3) automatic picture enhancement gives:
  - Brilliant and fresh color
  - Intensified contrast and details
  - Vivid skin tone
  - Sharp edge
  - Enhanced depth of field perception
  - Accurate and independent color control
- sRGB compliance allows end-user to experience the same colors as viewed on CRTs and other displays
- Programmable 12-bit RGB gamma CLUT
- 3-D video noise reduction
- Frame rate conversion

■ On-Screen OSD Controller
- 16/256 color palette
- 512 1/2/4/8-bit per pixel fonts
- Supports texture function
- Supports 4K attribute/code
- Horizontal and vertical stretch of OSD menus
- Pattern generator for production test
- Supports OSD MUX and alpha blending capability
- Supports blinking and scrolling for closed caption applications

■ LVDS Panel Interface
- Supports 8/10-bit dual link LVDS up to full HD (1920x1080)
- Supports 2 data output formats: Thine & TI data mappings
- Compatible with TIA/EIA
- Dithering with 6/8 bits options
- Reduced swing for LVDS for low EMI
- Supports flexible spread spectrum frequency with 360Hz~11.8MHz and up to 25% modulation

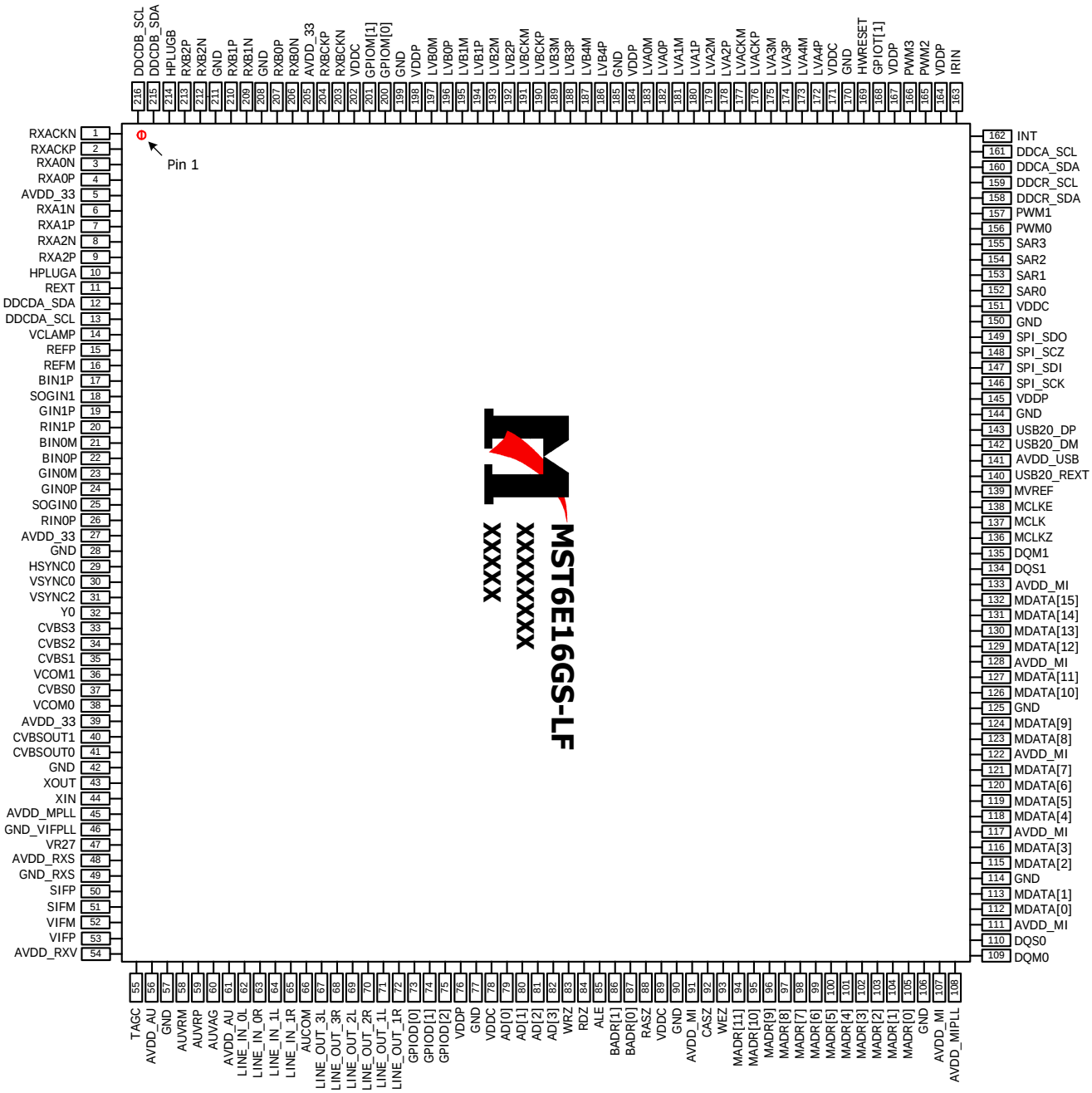
■ Integrated Micro Controller
- Embedded 8032 micro controller
- Configurable PWM's and GPIO's
- Low-speed ADC inputs for system control
- SPI bus for external flash
- Supports external MCU option controlled through 4-wire double-data-rate direct MCU bus

■ External Connection/Component
- USB 2.0 port with internal switch to host controller
- 16-bit data bus for external frame buffer (DDR DRAM)
- All system clocks synthesized from a single external clock

GENERAL DESCRIPTION

The MST6E16GS is a high performance and fully integrated IC for multi-function LCD monitor/TV with resolutions up to full HD (1920x1080). It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, a multi-standard TV video and audio decoder, a video de-interlacer, a scaling engine, the MStarACE-3 color engine, an on-screen display controller, an 8-bit MCU and a built-in output panel interface. By use of external frame buffer, PIP/POP is provided for multimedia applications. Furthermore, 3-D video decoding and processing are fulfilled for high-quality TV applications. To further reduce system costs, the MST6E16GS also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

PIN DIAGRAM (MST6E16GS)



PIN DESCRIPTION

MCU Interface

Pin Name	Pin Type	Function	Pin
AD[3]	I/O w/5V-tolerant	MCU 4-bit DDR Direct Bus; 4mA driving strength	82
AD[2:0]	I/O (not 5V-tolerant)	MCU 4-bit DDR Direct Bus; 4mA driving strength	81-79
WRZ	I/O w/ 5V-tolerant	MCU Bus WDZ, active low	83
RDZ	I/O w/ 5V-tolerant	MCU Bus RDZ, active	84
ALE	I/O w/ 5V-tolerant	MCU Bus ALE, active high	85
SPI_SCK	Output (not 5V-tolerant)	SPI Flash Serial Clock	146
SPI_SDI	Output (not 5V-tolerant)	SPI Flash Serial Data Input	147
SPI_SCZ	Output (not 5V-tolerant)	SPI Flash Chip Select	148
SPI_SDO	Input w/ 5V-tolerant	SPI Flash Serial Data Output	149
INT	I/O w/ 5V-tolerant	External Interrupt Input/Output	162
HWRESET	Schmitt Trigger Input w/ 5V-tolerant	Hardware Reset; active high	169

Analog Video Interface

Pin Name	Pin Type	Function	Pin
REXT	Analog Input	External Resister 390 ohm to AVDD_33	11
VCLAMP		CVBS/YC Mode Clamp Voltage Bypass	14
REFP		Internal ADC Reference Top De-coupling Pin	15
REFM		Internal ADC Reference Bottom De-coupling Pin	16
HSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog HSYNC Input from Channel 0	29
VSYNC0	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC Input from Channel 0	30
BIN0M	Analog Input	Reference Ground for Analog Blue Input from Channel 0	21
BIN0P	Analog Input	Analog Blue Input from Channel 0	22
GIN0M	Analog Input	Reference Ground for Analog Green Input from Channel 0	23
GIN0P	Analog Input	Analog Green Input from Channel 0	24
SOGIN0	Analog Input	Sync-On-Green Input from Channel 0	25
RIN0P	Analog Input	Analog Red Input from Channel 0	26
BIN1P	Analog Input	Analog Blue Input from Channel 1	17
SOGIN1	Analog Input	Sync-On-Green Input from Channel 1	18
GIN1P	Analog Input	Analog Green Input from Channel 1	19

Pin Name	Pin Type	Function	Pin
RIN1P	Analog Input	Analog Red Input from Channel 1	20
VSYNC2	Schmitt Trigger Input w/ 5V-tolerant	Analog VSYNC Input from Channel 2	31
Y0	Analog Input	Luma Video Input 0 / CVBS Input Channel 4 (CVBS4)	32
CVBS3	Analog Input	Analog CVBS (Composite) / S-Video (Y/C) Input Channel 3	33
CVBS2	Analog Input	Analog CVBS (Composite) / S-Video (Y/C) Input Channel 2	34
CVBS1	Analog Input	Analog CVBS (Composite) / S-Video (Y/C) Input Channel 1	35
CVBS0	Analog Input	Analog CVBS (Composite) / S-Video (Y/C) Input Channel 0	37
VCOM1	Analog Input	Common Analog Input Reference Ground 1 (for CVBS/ADCB)	36
VCOM0	Analog Input	Common Analog Input Reference Ground 0 (for CVBS/ADCB)	38
CVBSOUT1	Analog Output	CVBS (Composite) Video Output Channel 1	40
CVBSOUT0	Analog Output	CVBS (Composite) Video Output Channel 0	41

Analog Audio Interface

Pin Name	Pin Type	Function	Pin
AUVRM	Analog Output	Negative Reference Voltage for Audio ADC	58
AUVRP	Analog Output	Positive Reference Voltage for Audio ADC	59
AUVAG	Analog Output	Reference Voltage for Audio Common Mode	60
LINE_IN_0L	Analog Input	Audio Line Input Left Channel 0	62
LINE_IN_0R	Analog Input	Audio Line Input Right Channel 0	63
LINE_IN_1L	Analog Input	Audio Line Input Left Channel 1	64
LINE_IN_1R	Analog Input	Audio Line Input Right Channel 1	65
AUCOM	Analog Input	Reference Ground for Audio Line Input	66
LINE_OUT_1L	Analog Output	Main Audio Output Left Channel 1 (DA0)	71
LINE_OUT_1R	Analog Output	Main Audio Output Right Channel 1 (DA0)	72
LINE_OUT_2L	Analog Output	Main Audio Output Left Channel 2 (AA1)	69
LINE_OUT_2R	Analog Output	Main Audio Output Right Channel 2 (AA1)	70
LINE_OUT_3L	Analog Output	Main Audio Output Left Channel 3 (AA0)	67
LINE_OUT_3R	Analog Output	Main Audio Output Right Channel 3 (AA0)	68

DVI/HDMI Interface

Pin Name	Pin Type	Function	Pin
RXACKN	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Clock Channel	1
RXACKP	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Clock Channel	2
RXA0N	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Data Channel 0	3
RXA0P	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Data Channel 0	4
RXA1N	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Data Channel 1	6
RXA1P	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Data Channel 1	7
RXA2N	DVI/HDMI Input	Negative DVI/HDMI Input for A Link Data Channel 2	8
RXA2P	DVI/HDMI Input	Positive DVI/HDMI Input for A Link Data Channel 2	9
RXBCKN	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Clock Channel	203
RXBCKP	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Clock Channel	204
RXB0N	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Data Channel 0	206
RXB0P	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Data Channel 0	207
RXB1N	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Data Channel 1	209
RXB1P	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Data Channel 1	210
RXB2N	DVI/HDMI Input	Negative DVI/HDMI Input for B Link Data Channel 2	212
RXB2P	DVI/HDMI Input	Positive DVI/HDMI Input for B Link Data Channel 2	213

LVDS Interface

Pin Name	Pin Type	Function	Pin
LVA0M	Output	LVDS A-Link Channel 0 Negative Data Output	183
LVA0P	Output	LVDS A-Link Channel 0 Positive Data Output	182
LVA1M	Output	LVDS A-Link Channel 1 Negative Data Output	181
LVA1P	Output	LVDS A-Link Channel 1 Positive Data Output	180
LVA2M	Output	LVDS A-Link Channel 2 Negative Data Output	179
LVA2P	Output	LVDS A-Link Channel 2 Positive Data Output	178
LVA3M	Output	LVDS A-Link Channel 3 Negative Data Output	175
LVA3P	Output	LVDS A-Link Channel 3 Positive Data Output	174
LVA4M	Output	LVDS A-Link Channel 4 Negative Data Output	173
LVA4P	Output	LVDS A-Link Channel 4 Positive Data Output	172
LVACKM	Output	LVDS A-Link Negative Clock Output	177
LVACKP	Output	LVDS A-Link Positive Clock Output	176
LVB0M	Output	LVDS B-Link Channel 0 Negative Data Output	197

Pin Name	Pin Type	Function	Pin
LVB0P	Output	LVDS B-Link Channel 0 Positive Data Output	196
LVB1M	Output	LVDS B-Link Channel 1 Negative Data Output	195
LVB1P	Output	LVDS B-Link Channel 1 Positive Data Output	194
LVB2M	Output	LVDS B-Link Channel 2 Negative Data Output	193
LVB2P	Output	LVDS B-Link Channel 2 Positive Data Output	192
LVB3M	Output	LVDS B-Link Channel 3 Negative Data Output	189
LVB3P	Output	LVDS B-Link Channel 3 Positive Data Output	188
LVB4M	Output	LVDS B-Link Channel 4 Negative Data Output	187
LVB4P	Output	LVDS B-Link Channel 4 Positive Data Output	186
LVBCKM	Output	LVDS B-Link Negative Clock Output	191
LVBCKP	Output	LVDS B-Link Positive Clock Output	190

GPIO Interface

Pin Name	Pin Type	Function	Pin
GPIOD[2:0]	I/O (not 5V-tolerant)	General Purpose Input/Output	75-73
GPIOT[1]	I/O w/ 5V-tolerant	General Purpose Input/Output	168
GPIOM[1:0]	I/O w/ 5V-tolerant	General Purpose Input/Output	201, 200
SAR0	I/O (not 5V-tolerant)	SAR Low Speed ADC Input 0	152
SAR1	I/O (not 5V-tolerant)	SAR Low Speed ADC Input 1	153
SAR2	I/O (not 5V-tolerant)	SAR Low Speed ADC Input 2	154
SAR3	I/O (not 5V-tolerant)	SAR Low Speed ADC Input 3	155
PWM0	I/O (not 5V-tolerant)	Pulse Width Modulation Output; 4mA driving strength / MCU Configuration Input 0 During Reset / General Purpose Input/Output	156
PWM1	I/O (not 5V-tolerant)	Pulse Width Modulation Output; 4mA driving strength / MCU Configuration Input 1 During Reset / General Purpose Input/Output	157
PWM2	I/O (not 5V-tolerant)	Pulse Width Modulation Output; 4mA driving strength / General Purpose Input/Output	165
PWM3	I/O (not 5V-tolerant)	Pulse Width Modulation Output; 4mA driving strength / General Purpose Input/Output	166
IRIN	Input w/5V-tolerant	IR Receiver Input / General Purpose Input/Output	163

DRAM Interface

Pin Name	Pin Type	Function	Pin
BADR[1:0]	Output	DRAM Memory Bank Address	86, 87
RASZ	Output	Row Address Strobe; active low	88
CASZ	Output	Column Address Strobe; active low	92
WEZ	Output	Write Enable; active low	93
MADR[11:0]	Output	DRAM Memory Address	94-105
DQM[1:0]	Output	Data Mask for Low Byte; active high	135, 109
DQS[1:0]	I/O	Data Strobe	134, 110
MDATA[15:0]	I/O	DRAM Memory Data Bus	132-129, 127, 126, 124, 123, 121-118, 116, 115, 113, 112
MCLKZ	Output	DRAM Memory Negative Differential Clock	136
MCLK	Output	DRAM Memory Positive Differential Clock	137
MCLKE	Output	DRAM Memory Clock Enable	138
MVREF	Input	Reference Voltage for DDR SDRAM Interface	139

USB Interface

Pin Name	Pin Type	Function	Pin
USB20_REXT		USB External Resistor Pin; Connected through 900 ohm (±1%) Resistor to GND	140
USB20_DM	Analog I/O	USB 2.0 Inverting Data Input/Output	142
USB20_DP	Analog I/O	USB 2.0 Non-inverting Data Input/Output	143

VIF Interface

Pin Name	Pin Type	Function	Pin
VR27		Compensation Capacitor for Regulator	46
SIFP	Analog Input	Positive Sound IF Input	49
SIFM	Analog Input	Negative Sound IF Input	50
VIFM	Analog Input	Negative Video IF Input	51
VIFP	Analog Input	Positive Video IF Input	52
TAGC	Analog Output	Tuner Automatic Gain Control Output	55

Misc Interface

Pin Name	Pin Type	Function	Pin
XOUT	Analog Output	Crystal Oscillator Output	43
XIN	Analog Input	Crystal Oscillator Input	44
DDCR_SDA	I/O w/ 5V-tolerant	DDC Data for ROM	158
DDCR_SCL	I/O w/ 5V-tolerant	DDC Clock for ROM	159
DDCA_SDA	I/O w/ 5V-tolerant	DDC Data for Analog Interface; 4mA driving strength	160
DDCA_SCL	Input w/ 5V-Tolerant	DDC Clock for Analog Interface	161
HPLUGA	I/O w/ 5V-tolerant	Hot-plug control for DVI/HDMI Port A	10
HPLUGB	I/O w/ 5V-tolerant	Hot-plug control for DVI/HDMI Port B	214
DDCDA_SDA	I/O w/ 5V-Tolerant	DDC Data and HDCP Slave Serial Bus Data I/O for DVI/HDMI Port A; 4mA driving strength	12
DDCDA_SCL	Input w/ 5V-tolerant	DDC Clock and HDCP Slave Serial Bus Clock Input for DVI/HDMI Port A	13
DDCDB_SDA	I/O w/ 5V-Tolerant	DDC Data and HDCP Slave Serial Bus Data I/O for DVI/HDMI Port B; 4mA driving strength	215
DDCDB_SCL	Input w/ 5V-tolerant	DDC Clock and HDCP Slave Serial Bus Clock Input for DVI/HDMI Port B	216

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_33	3.3V Power	Analog Power	5, 27, 39, 205
AVDD_MPLL	3.3V Power	MPLL Power	45
AVDD_RXS	3.3V Power	Sound Path Receiver Power	48
GND_RXS	Ground	Sound Path Receiver Ground	49
GND_RXV	Ground	Video Path Receiver Ground	53
AVDD_RXV	3.3V Power	Video Path Receiver Power	54
AVDD_AU	3.3V Power	Audio Power	56, 61
AVDD_MI	2.5V Power	Memory Interface Power	91, 107, 111, 117, 122, 128, 133
AVDD_MIPLL	3.3V Power	Memory Interface PLL Power	108
AVDD_USB	3.3V Power	USB Power	141
VDDC	1.26V Power	Digital Core Power	78, 89, 151, 171, 202
VDDP	3.3V Power	Digital Input/Output Power	76, 145, 164, 167, 184, 198
GND	Ground	Ground	28, 42, 57, 77, 90, 106, 114, 125, 144, 150, 170, 185, 199, 208, 211

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
DC ACCURACY				
Differential Nonlinearity		TBD	TBD	LSB
Integral Nonlinearity		TBD		LSB
VIDEO ANALOG INPUT				
Input Voltage Range				
Minimum			0.5	V p-p
Maximum	1.0			V p-p
Input Bias Current			1	uA
Input Full-Scale Matching		1.5		%FS
Brightness Level Adjustment		62		%FS
SWITCHING PERFORMANCE				
Maximum Conversion Rate	165			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		165	MHz
PLL Jitter		500		ps p-p
Sampling Phase Tempco		15		ps/°C
DYNAMIC PERFORMANCE				
Analog Bandwidth, Full Power		250		MHz
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
VIDEO ANALOG OUTPUT				
CVBS Buffer Output				
Output Low		1.5		V
Output High		2.0		V

Parameter	Min	Typ	Max	Unit
AUDIO				
ADC Input		2.0		V p-p
DAC Output		2.0		V p-p
SIF Input Range				
Minimum			0.1	V p-p
Maximum	1.0			V p-p
FSSW Input[1]	0		1.8	V
SAR ADC Input	0		3.3	V
FB ADC Input[2]	0		1.25	V

Specifications subject to change without notice.
Notes:
1. **Input full scale is typically 1.8V, but input range is 0 ~ 3.3V.**
2. **Input full scale is 1.25V, but input range is 0 ~ 3.3V.**

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}			3.6	V
2.5V Supply Voltages	V_{VDD_25}			2.75	V
1.26V Supply Voltages	V_{VDD_126}			1.32	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$			5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}			V_{VDD_33}	V
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		150	°C
Junction Temperature	T_J			150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
MST6E16GS	0°C to +70°C	LQFP	216
MST6E16GS-LF	0°C to +70°C	LQFP	216
MST6E16GS-S1	0°C to +70°C	LQFP	216
MST6E16GS-LF-S1	0°C to +70°C	LQFP	216
MST6E16GS-S2	0°C to +70°C	LQFP	216
MST6E16GS-LF-S2	0°C to +70°C	LQFP	216
MST6E16GS-S3	0°C to +70°C	LQFP	216
MST6E16GS-LF-S3	0°C to +70°C	LQFP	216
MST6E16GS-S4	0°C to +70°C	LQFP	216
MST6E16GS-LF-S4	0°C to +70°C	LQFP	216
MST6E16GS-S5	0°C to +70°C	LQFP	216
MST6E16GS-LF-S5	0°C to +70°C	LQFP	216

Note on product suffix:
1. "LF": Lead-free version.
2. "S1" ~ "S5": Advanced surround features.

Code	Description
S1	SRS TruSurround XT™
S2	Dolby® ProLogic® II + Dolby® Virtual Speaker
S3	Dolby® ProLogic® II + Virtual Dolby® Surround
S4	BBE®
S5	BBE® ViVA™

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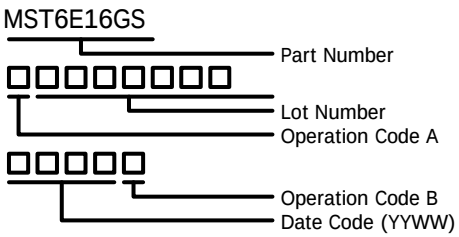
MARKING INFORMATION



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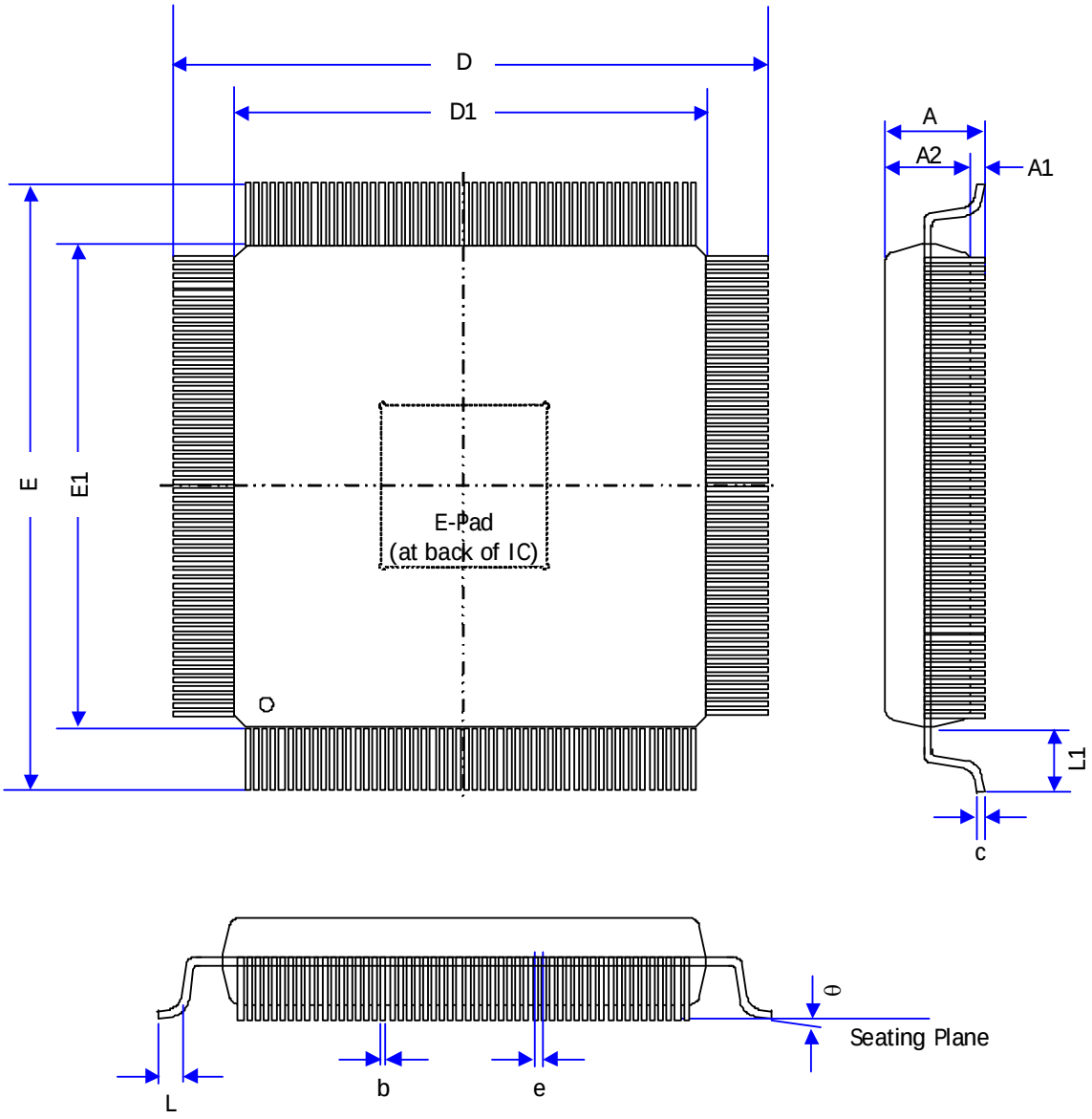
Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST6E16GS comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
MST6E16GS_ds_v01	• Initial release	Jun 2008
MST6E16GS_ds_v02	• Added 3-D Comb and Advanced Sound Technology related information • Updated Features / Digital Audio Interface • Updated to DDR DRAM in Features • Updated Mechanical Dimensions	Jul 2008
MST6E16GS_ds_v03	• Revised Pin #56 in Pin Diagram and Pin Description	Aug 2008
MST6E16GS_ds_v04	• Updated Pin 46-53 in Pin Diagram and Pin Description • Updated voltage of VDDC pins	Oct 2008

MECHANICAL DIMENSIONS



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	26.00			1.024		
D1	24.00			0.945		
E	26.00			1.024		
E1	24.00			0.945		

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
θ	0°	-	7°	0°	-	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
b	-	0.18	-	-	0.007	-
c	-	0.14	-	-	0.006	-
e	0.40 BSC			0.016 BSC		

FEATURES

- **Family of Serial Flash Memories**
  - W25X20: 2M-bit / 256K-byte (262,144) 1024 pages
  - W25X40: 4M-bit /512K-byte (524,288) 2048 pages
  - W25X80: 8M-bit / 1M-byte (1,048,576) 4,096 pages
  - 256-bytes per programmable page
  - Uniform 4K-byte Sectors and 64K-byte Blocks
- **SPI Serial Interface with Single or Dual Outputs**
  - Clock, Chip Select, Data I/O, Data Out
  - Optional Hold function for SPI flexibility
- **Fast Data Transfer up to 136M-bits / second**
  - Clock operation to 68MHz
  - Fast Read Dual Output instruction
  - Auto-increment Read capability
- **Flexable Array Architecture with 4KB sectors**
  - Sector Erase (4K-bytes)
  - Block Erase (64K-byte)
  - Page program up to 256 bytes <2ms
  - 100,000 erase/write cycles, 20-year retention
- **Low Power Consumption, Wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 5mA active current, 1µA Power-down (typ)
  - -40° to +85°C operating range
- **Software and Hardware Write Protection**
  - Write-Protect all or portion of memory via software
  - Enable/Disable protection with WP pin
  - Top or bottom array protection
- **Space Efficient Packaging**
  - 8-pin SOIC 150-mil
  - 8-pin SOIC 208-mil

8-Pin SOIC 150-mil
W25X20 and W25X40
(Package Code SN)

8-Pin SOIC 208-mil
W25X80
(Package Code SS)

GENERAL DESCRIPTION

The W25X20 (2M-bit), W25X40 (4M-bit) and W25X80 (8M-bit) Serial Flash memories provide a storage solution for systems with limited space, pins and power. The 25X series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code download applications as well as storing voice, text and data. The devices operate on a single 2.7V to 3.6V power supply with current consumption as low as 5mA active and 1µA for power-down. All devices are offered in space-saving packages.

The W25X20/40/80 array is organized into 2048/4096/8192 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instruction. Pages can be erased in groups of 16 (sector erase), groups of 256 (block erase) or the entire chip (chip erase). The W25X20/40/80 has 128/256/512 erasable sectors and 8/16/32 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage. (See figure 1.)

The W25X20/40/80 support the standard Serial Peripheral Interface (SPI), and a high performance dual output SPI using four pins: Serial Clock, Chip Select, Serial Data I/O and Serial Data Out. SPI clock frequencies of up to 68MHz are supported allowing read transfer rates of 136MHz when using the Fast Read Dual Output instruction. These transfer rates are comparable to those of 8 and 16-bit Parallel Flash memories.

A hold pin, write Protect pin and programmable write protect, with top or bottom array control features, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification.

NEXFLASH® Technologies, Inc.

Continuity
The Winbond W25X40 and W25X80 are fully compatible with the previous NexFlash NX25X40 and NX25X80 Serial Flash memories.

PIN DESCRIPTIONS

Package Types
At the time this data sheet was published not all package types had been finalized. Contact Winbond to confirm availability of these packages before designing to this specification. The W25X20 and W25X40 are offered in an 8-pin plastic 150mil width SOIC (package code SN) as shown in figure 2A. The W25X80 is offered in an 8-pin plastic 208mil width SOIC (package code SS) as shown in figure 2B. Package diagrams and dimensions are illustrated at the end of this data sheet

Serial Data Input / Output (DIO)
The SPI Serial Data Input/Output (DIO) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin. The DIO pin is also used as an output when the Fast Read Dual Output instruction is executed.

Serial Data Output (DO)
The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

Serial Clock (CLK)
The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI "Operations")

Chip Select ($\overline{CS}$)
The SPI Chip Select ($\overline{CS}$) pin enables and disables device operation. When $\overline{CS}$ is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When $\overline{CS}$ is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, $\overline{CS}$ must transition from high to low before a new instruction will be accepted. The $\overline{CS}$ input must track the Vcc supply level at power-up (see "Write Protection" and figure 19). If needed a pull-up resister on $\overline{CS}$ can be used to accomplish this.

Hold ($\overline{HOLD}$)
The $\overline{HOLD}$ pin allows the device to be paused while it is actively selected. When $\overline{HOLD}$ is brought low, while $\overline{CS}$ is low, the DO pin will be at high impedance and signals on the DIO and CLK pins will be ignored (don't care). When $\overline{HOLD}$ is brought high, device operation can resume. The hold function can be useful when multiple devices are sharing the same SPI signals. ("See Hold function")

Write Protect ($\overline{WP}$)
The Write Protect ($\overline{WP}$) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0 and BP1) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The $\overline{WP}$ pin is active low.

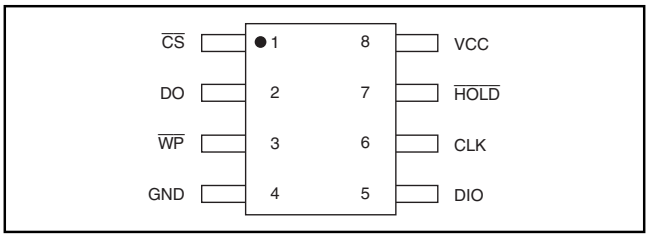


Figure 2A. W25X20 and W25X40 Pin Assignments, 8-pin SOIC (Package Code SN)

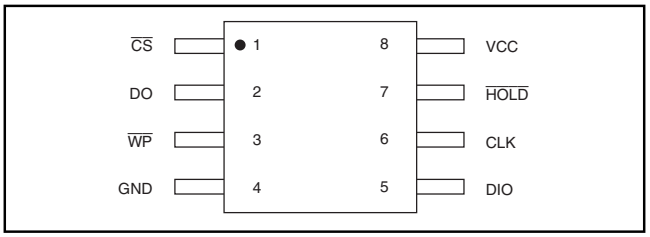


Figure 2B. W25X80 Pin Assignments, 8-pin SOIC (Package Code SS)

Table 1. Pin Descriptions

DIO	Data Input/Output
DO	Data Output
CLK	Serial Clock Input
$\overline{CS}$	Chip Select Input
$\overline{WP}$	Write Protect Input
$\overline{HOLD}$	Hold Input
Vcc, GND	Power Supply
N/C	No Connect

SPECIFICATIONS AND TIMING DIAGRAMS

Table 5. Absolute Maximum Ratings (1)

Symbol	Parameters	Conditions	Range	Unit
Vcc	Supply Voltage		–0.6 to +4.0	V
VIO	Voltage Applied to Any Pin	Relative to Ground	–0.6 to Vcc + 0.4	V
TSTG	Storage Temperature		–65 to +150	°C
TLEAD	Lead Temperature		See Note 2	°C
VESD	Electrostatic Discharge Voltage	Human Body Model(3)	–2000 to +2000	V

Note:
1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure beyond absolute maximum ratings (listed above) may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

Table 6. Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage(1)		2.7	3.6	V
TA	Ambient Temperature, Operating	Industrial	–40	+85	°C

Note:
1. Vcc voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

Table 7. Power-up Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit
tVSL(1)	VCC(min) to $\overline{CS}$ Low	10		µs
tPUW(1)	Time Delay Before Write Instruction	1	10	ms
VWI(1)	Write Inhibit Threshold Voltage	1	2	V

Note:
1. These parameters are characterized only.

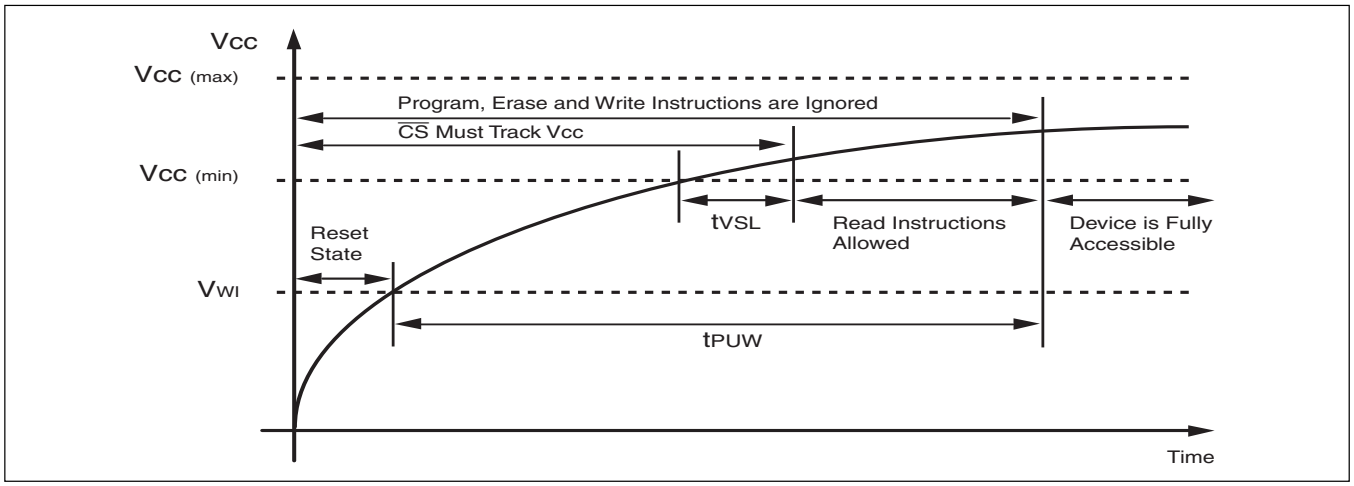


Figure 20. Power-up Timing and Voltage Levels

Table 8. DC Electrical Characteristics (Preliminary) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V(2)			6	pf
Cout(2)	Output Capacitance	V_{OUT} = 0V(2)			8	pf
I_{LI}	Input Leakage				±2	µA
I_{LO}	I/O Leakage				±2	µA
I_{CC1}	Standby Current	$\overline{CS}$ = VCC, VIN = GND or VCC		25	50	µA
I_{CC2}	Power-down Current	$\overline{CS}$ = VCC, VIN = GND or VCC		<1	5	µA
I_{CC3}	Current Read Data 1MHz(3)	C = 0.1VCC / 0.9 VCC DO = Open		5	8	mA
	Current Read Data 50MHz(3)	C = 0.1VCC / 0.9 VCC DO = Open		20	25	mA
	Current Read Data 68MHz(3)	C = 0.1VCC / 0.9 VCC DO = Open		25	30	mA
I_{CC4}	Current Page Program	$\overline{CS}$ = VCC		15	25	mA
I_{CC5}	Current Write Status Register	$\overline{CS}$ = VCC		20	25	mA
I_{CC6}	Current Sector Erase	$\overline{CS}$ = VCC		20	25	mA
I_{CC7}	Current Chip Erase	$\overline{CS}$ = VCC		20	25	mA
V_{IL}	Input Low Voltage		–0.5		Vccx0.3	V
V_{IH}	Input High Voltage		Vccx0.7		Vcc +0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{CC}–0.2			V

Notes:
1. See Preliminary Designation.
2. Tested on sample basis and specified through design and characterization data. TA=25° C, Vcc 3V, Frequency 20MHz.
3. Checker Board Pattern.

Table 9. AC Measurement Conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30	30	pF
T_R, T_F	Input Rise and Fall Times		5	ns
V_{IN}	Input Pulse Voltages	0.2VCC to	0.8VCC	V
O_{UT}	Output Timing Reference Voltages	0.5VCC to	0.5VCC	V

Note:
1. Output Hi-Z is defined as the point where data out is no longer driven.

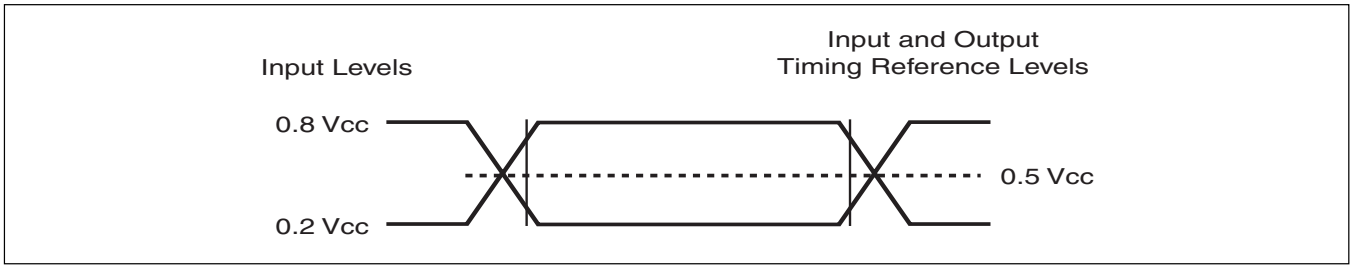


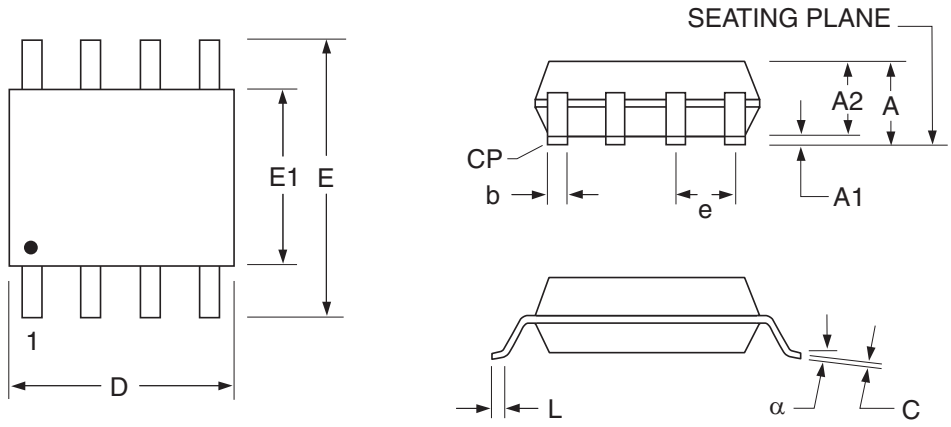
Figure 21. AC Measurement I/O Waveform

Table 10. AC Electrical Characteristics (Preliminary)

Symbol	Alt	Description	Min	Typ	Max	Unit
F_R	f_C	Clock frequency, for Fast Read (0Bh, 3Bh) and all other instructions except Read Data (03h)	D.C.		68	MHz
f_R		Clock freq. Read Data instruction (03h)	D.C.		33	MHz
t_{CLH}, t_{CLL}(1)		Clock High, Low Time, for Fast Read (0Bh, 3Bh) and all other instructions except Read Data (03h)	7			ns
t_{CRLH}, t_{CRLL}(1)		Clock High, Low Time for Read Data instruction	8			ns
t_{CLCH}(2)		Clock Rise Time peak to peak	0.1			V / ns
t_{CHCL}(2)		Clock Fall Time peak to peak	0.1			V / ns
t_{SLCH}	t_{CSS}	CS Active Setup Time relative to CLK	5			ns
t_{CHSL}		CS Not Active Hold Time relative to CLK	5			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{CHSH}		CS Active Hold Time relative to CLK	5			ns
t_{SHCH}		CS Not Active Setup Time relative to CLK	5			ns
t_{SHSL}	t_{CSH}	CS Deselect Time	100			ns
t_{SHQZ}(2)	t_{DIS}	Output Disable Time			7	ns
t_{CLQV}	t_V	Clock Low to Output Valid			6	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{HLCH}		HOLD Active Setup Time relative to CLK	5			ns
t_{CHHH}		HOLD Active Hold Time relative to CLK	5			ns
t_{HHCH}		HOLD Not Active Setup Time relative to CLK	5			ns
t_{CHHL}		HOLD Not Active Hold Time relative to CLK	5			ns
t_{HHQX}(2)	t_{LZ}	HOLD to Output Low-Z			7	ns
t_{HLQZ}(2)	t_{HZ}	HOLD to Output High-Z			7	ns
t_{WHSL}(4)		Write Protect Setup Time Before CS Low	20			ns
t_{SHWL}(4)		Write Protect Hold Time After CS High	100			ns
t_{DP}(2)		CS High to Power-down Mode			3	µs
t_{RES1}(2)		CS High to Standby Mode without Electronic Signature Read			3	µs
t_{RES2}(2)		CS High to Standby Mode with Electronic Signature Read			1.8	µs
t_W		Write Status Register Cycle Time		5	15	ms
t_{PP}		Page Program Cycle Time 2.7V-3.6V Vcc		1.5	5	ms
t_{SE}		Sector Erase Cycle Time (4KB)		150	300	ms
t_{BE}		Block Erase Cycle Time (64KB)		1	2	s
t_{CE}		Chip Erase Cycle Time 25X20 Chip Erase Cycle Time 25X40 Chip Erase Cycle Time 25X80		3 5 10	6 10 20	s s s

Notes:
1. Clock high + Clock low must be less than or equal to 1/f_C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set at 1.

PACKAGING INFORMATION
8-Pin SOIC 150-mil (Package Code SN)



Package Dimensions(1)

	Millimeters			Inches		
Symbol	**Min**	**Typ.**	**Max**	**Min**	**Typ.**	**Max**
A	1.47	1.60	1.72	0.058	0.063	0.068
A1	0.10		0.24	0.004		0.009
A2		1.45			0.057	
b	0.33	0.41	0.50	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D(3)	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.19	0.228	0.236	0.244
E1(3)	3.80	3.90	4.00	0.150	0.154	0.157
e(2)		1.27 BSC			0.050 BSC	
L	0.40	0.71	1.27	0.015	0.028	0.050
α	0°		8°	0°		8°
CP			0.10			0.004

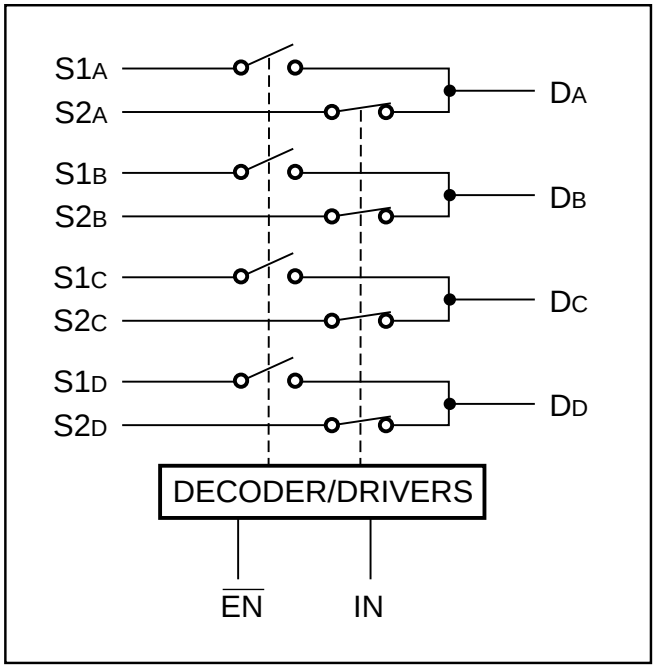
Notes:
1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within .0004 inches at the seating plane.

Low ON Resistance Wideband/Video Quad 2-Channel MUX/DEMUX

Product Features:

- High-performance, low-cost solution to switch between video sources
- Wide bandwidth: 200 MHz
- Low ON-resistance: 3Ω
- Low crosstalk at 10 MHz: –58 dB
- Ultra-low quiescent power (0.1 µA typical)
- Single supply operation: +5.0V
- Fast switching: 10 ns
- High-current output: 100 mA
- Packages available:
  - 16-pin 300-mil wide plastic SOIC (S)
  - 16-pin 150-mil wide plastic SOIC (W)
  - 16-pin 150-mil wide plastic QSOP (Q)

Functional Block Diagram



Truth Table

$\overline{EN}$	IN	ON Switch
0	0	$S1_A$, $S1_B$, $S1_C$, $S1_D$
0	1	$S2_A$, $S2_B$, $S2_C$, $S2_D$
1	X	Disabled

Product Description:

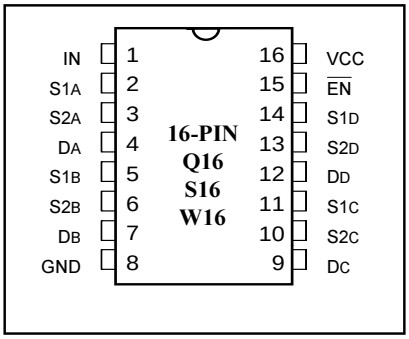
Pericom Semiconductor's PI5V series of mixed signal video circuits are produced in the Company's advanced CMOS low-power technology, achieving industry leading performance.

The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications. The VideoSwitch™ can be driven from a current output RAMDAC or voltage output composite video source.

Low ON-resistance and wide bandwidth make it ideal for video and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today. A single 5V supply is all that is required for operation.

The PI5V330 offers a high-performance, low-cost solution to switch between video sources. The application section describes the PI5V330 replacing the HC4053 multiplier and buffer/amplifier.

16-Pin Product Configuration



Product Pin Description

Pin Name	Description
$S1_A$, $S2_A$ $S1_B$, $S2_B$ $S1_C$, $S2_C$ $S1_D$, $S2_D$	Analog Video I/O
IN	Select Input
$\overline{EN}$	Enable
D_A, D_B, D_C, D_D	Analog Video I/O
GND	Ground
V_{CC}	Power

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5V ±5%)

Parameters	Description	Test Conditions[1]	Min.	Typ[2]	Max.	Units
V_{ANALOG}	Analog Signal Range		0	—	2.0	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	–0.5	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND	—	—	±1	µA
I_O	Analog Output Leakage Current	0 ≤ S1, S2 or D ≤ V_{CC}, Switch Off	—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA	—	–0.7	–1.2	V
I_{OS}	Short Circuit Current[3]	S1, S2, D = 0V V_{CC}	100	—	—	mA
V_H	Input Hysteresis at Control Pins		—	150	—	mV
R_{ON}	Switch On Resistance[4]	V_{CC} = Min., V_{IN} = 1.0V R_L = 75ohm, I_{ON} = 13 mA	—	3	7	ohm
		V_{CC} = Min., V_{IN} = 2.0V R_L = 75ohm, I_{ON} = 26 mA	—	7	10	ohm

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, T_A = 25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Measured by the voltage drop between S1, S2, and D I/O pins at indicated current through the switch. ON resistance is determined by the lower of the voltages on the S1, S2, and D I/O pins.

Dynamic Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5V ±5%)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn On Time	R_L = 75ohm, C_L = 20 pF, see Fig. 6	—	2.5	5	ns
t_{OFF}	Turn Off Time	R_L = 75ohm, C_L = 20 pF, see Fig. 6	—	1.1	5	ns
B_W(1)	–3 dB Bandwidth	R_L = 150ohm, see Fig. 7	180	—	—	MHz
X_{TALK}	Crosstalk	R_{IN} = 10ohm; R_L = 150ohm, 10 MHz, see Fig. 7	—	–58	—	dB
D_G	Differential Gain	R_L = 150ohm, f = 3.58 MHz, see Fig. 5	—	0.64	—	%
D_P	Differential Phase	R_L = 150ohm, f = 3.58 MHz, see Fig. 5	—	0.27	—	Deg.
C_{IN}(1)	Input/Enable Capacitance	V_{IN} = 0V, f = 1 MHz	—	—	6	pF
C_{OFF}(1)	Capacitance, Switch Off	V_{IN} = 0V, f = 1 MHz	—	—	6	pF
C_{ON}(1)	Capacitance, Switch On	V_{IN} = 0V, f = 1 MHz	—	—	8	pF
O_{IRR}	Off Isolation	R_L = 150ohm, 10 MHz, see Fig. 7	—	–38	—	dB

Notes:
1. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

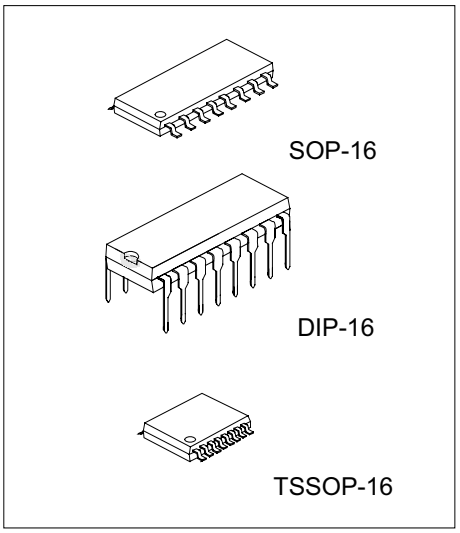
Parameters	Description	Test Conditions(1)		Min.	Typ(2)	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	IN = GND or V_{CC}	—	0.1	3.0	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	IN = 3.4V(3)	—	—	2.5	mA
I_{CCD}	Supply Current per Input per MHz(4)	V_{CC} = Max., S1, S2, and D Pins Open $\overline{EN}$ = GND Control Input Toggling 50% Duty Cycle		—	—	0.25	mA/ MHz

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V, control inputs only); S1, S2, and D pins do not contribute to Icc.
4. This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The S1, S2, and D I/O pins generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

4052

CMOS IC

DIFFERENTIAL 4-CHANNEL ANALOG MULTIPLEXERS/ DEMULTIPLEXERS



*Pb-free plating product number: 4052L

■ DESCRIPTION

The UTC **4052** is differential 4-channel analog multiplexers/ demultiplexers for application as digitally–controlled analog switches.

The device has two binary control inputs and an inhibit input. It feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

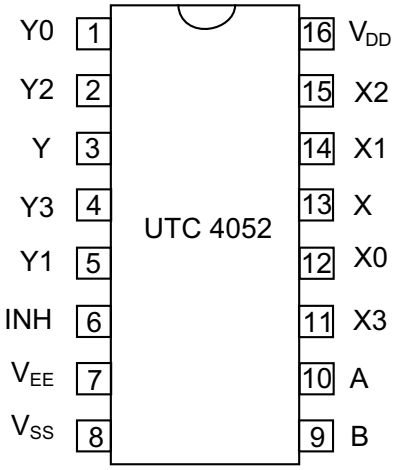
■ FEATURES

* Wide Analog Voltage Range: V_{DD}–V_{EE} = 3V~18V.
  (Note: V_{EE} must be $\leqq V_{SS}$)
* Break-Before-Make Switching Eliminates Channel Overlap.
* Linearized Transfer Characteristics
* Implement an DP4T Switch Effectively.
* Pin–to–Pin Replacement for CD4052

■ ORDERING INFORMATION

Order Number		Package	Packing
Normal	Lead Free Plating		
4052-S16-R	4052L-S16-R	SOP-16	Tape Reel
4052-S16-T	4052L-S16-T	SOP-16	Tube
4052-P16-R	4052L-P16-R	TSSOP-16	Tape Reel
4052-P16-T	4052L-P16-T	TSSOP-16	Tube
4052-D16-T	4052L-D16-T	DIP-16	Tube

■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN No.	SYMBAL	NAME AND FUNCTION
13, 3	X,Y	Commons Input/Output
6	INH	Inhibit Input
7	V_{EE}	Supply Voltage
8	V_{SS}	Ground
10,9	A,B	Binary Control Inputs
12,14,15,11	X0~X3	X Channel Inputs/Outputs
1,5,2,4	Y0~Y3	Y Channel Inputs/Outputs
16	V_{DD}	Positive Supply Voltage

Note: Control Inputs referenced to V_{SS}. Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be $<V_{SS}$.

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage (Referenced to V_{EE}, $V_{SS} \geqq V_{EE}$)	V_{DD}	-0.5 ~ +18	V
Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	V_{IN}, V_{OUT}	-0.5 ~ V_{DD} +0.5	V
Input Current (DC or Transient), per Control Pin	I_{IN}	±10	mA
Switch Through Current	I_{SW}	±25	mA
Power Dissipation Derating above 65℃	P_D	700 7	mW mW/℃
Junction Temperature	T_J	125	℃
Operating Temperature Range	T_{OPR}	-40 ~ +125	℃
Storage Temperature Range	T_{STG}	-40 ~ +150	℃

Note: 1.Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2.The device is guaranteed to meet performance specification within 0℃~70℃ operating temperature range and assured by design from –40℃~125℃.

■ ELECTRICAL CHARACTERISTICS (Ta=25℃, unless otherwise specified.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})							
Power Supply Voltage Range		V_{DD}	$V_{DD} - 3 \geqq V_{SS} \geqq V_{EE}$	3		18	V
Quiescent Current per Package	V_{DD}=5V	I_Q	Control Inputs: $V_{IN} = V_{SS}$ or V_{DD} Switch I/O: $V_{EE} \leqq V_{I/O} \leqq V_{DD}$, and $\Delta Vsw \leqq 500mV$(Note 2)		0.005	5	μA
	V_{DD}=10V				0.010	10	
	V_{DD}=15V				0.015	20	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	V_{DD}=5V	$I_{D(AV)}$	T_a=25℃ only (The channel component, $(V_{IN}-V_{OUT})/R_{ON}$, is excluded.)		(0.07 μA/kHz) f + I_Q		μA
	V_{DD}=10V				(0.20 μA/kHz) f + I_Q		
	V_{DD}=15V				(0.36 μA/kHz) f + I_Q		
SWITCHES IN/OUT AND COMMONS OUT/IN -- X, Y, Z (Voltages Referenced to V_{EE})							
Recommended Peak–to–Peak Voltage Into or Out of the Switch		$V_{I/O}$	Channel On or Off	0		V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch (Note2)		ΔVsw	Channel On	0		600	mV
Output Offset Voltage		$V_{O(OFF)}$	V_{IN} = 0V, No Load		10		μV
ON Resistance	V_{DD}=5V	R_{ON}	$\Delta Vsw \leqq 500mV$ (Note2) $V_{IN} = V_{IL}$ or V_{IH} (Control), and V_{IN} = 0 to V_{DD} (Switch)		250	1050	Ω
	V_{DD}=10V				120	500	
	V_{DD}=15V				80	280	
△ON Resistance Between Any Two Channels in the Same Package	V_{DD}=5V	ΔR_{ON}			25	70	Ω
	V_{DD}=10V				10	50	
	V_{DD}=15V				10	45	
Off–Channel Leakage Current		I_{OFF}	$V_{IN} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel, V_{DD}=15V		±0.05	±100	nA
Capacitance, Switch I/O		$C_{I/O}$	Inhibit = V_{DD}		10		pF
Capacitance, Common O/I		$C_{O/I}$	Inhibit = V_{DD}		17		pF
Capacitance, Feedthrough (Channel Off)		$C_{I/O}$	Pins Not Adjacent Pins Adjacent		0.15 0.47		pF

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V_{SS})							
Low Level Input Voltage	V_{DD}=5V	V_{IL}	R_{ON}= per spec, I_{OFF} = per spec		2.25	1.5	V
	V_{DD}=10V				4.50	3.0	
	V_{DD}=15V				6.75	4.0	
High Level Input Voltage	V_{DD}=5V	V_{IH}	R_{ON}= per spec, I_{OFF} = per spec	3.5	2.75		V
	V_{DD}=10V			7.0	5.50		
	V_{DD}=15V			11	8.25		
Input Leakage Current		I_{LEAK}	V_{IN}= 0 or V_{DD}, V_{DD}=15V		±0.00001	±0.1	μA
Input Capacitance		C_{IN}			5.0	7.5	pF

■ DYNAMIC ELECTRICAL CHARACTERISTICS

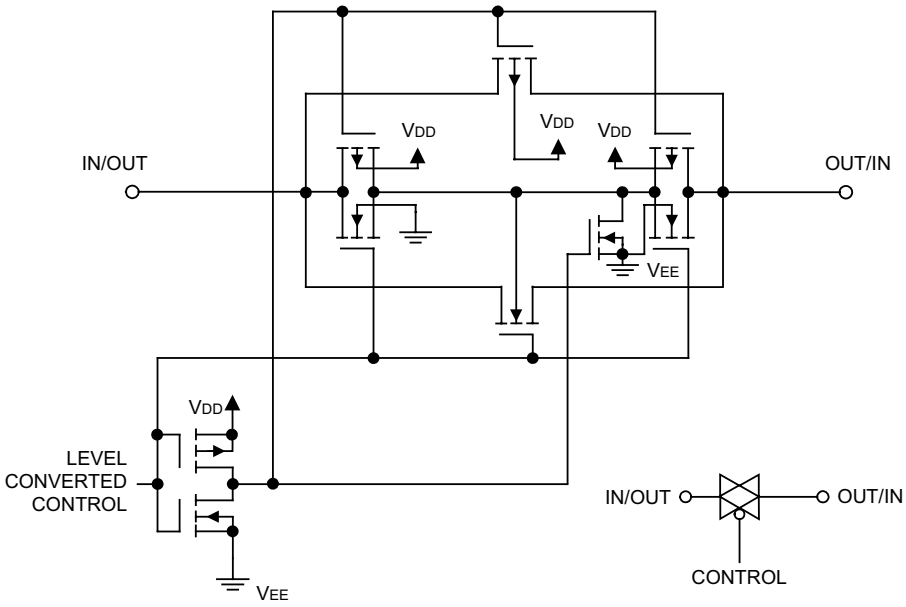
(C_L = 50pF, T_a=25℃, $V_{EE} \leqq V_{SS}$, unless otherwise specified)

PARAMETER	SYMBOL	V_{DD}–V_{EE} Vdc	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Times Switch Input to Switch Output (R_L = 10 kΩ)	t_{PLH}, t_{PHL}	5 10 15	t_{PLH}, t_{PHL} =(0.17 ns/pF)C_L + 21.5ns t_{PLH}, t_{PHL} =(0.08 ns/pF)C_L + 8.0ns t_{PLH}, t_{PHL} =(0.06 ns/pF)C_L + 7.0ns		30 12 10	75 30 25	ns
Inhibit to Output	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	5 10 15	(R_L=10kΩ, V_{EE}=V_{SS}) Output “1” or “0” to High Impedance, or High Impedance to “1” or “0” Level		300 155 125	600 310 250	ns
Control Input to Output	t_{PLH}, t_{PHL}	5 10 15	R_L = 10 kΩ, V_{EE} = V_{SS}		325 130 90	650 260 180	ns
Total Harmonic Distortion	THD	10	R_L = 10KΩ, f = 1 kHz, V_{IN} = 5 V_{PP}		0.07		%
Bandwidth	BW	10	R_L = 1kΩ, V_{IN} = 1/2 (V_{DD}–V_{EE}) p–p, C_L = 50pF, 20 Log (V_{OUT}/V_{IN}) = -3dB)		17		MHz
Off Channel Feedthrough Attenuation		10	R_L=1KΩ, V_{IN} = 1/2 (V_{DD}–V_{EE}) p–p f_{IN} = 30MHz		-50		dB
Channel Separation		10	R_L = 1kΩ, V_{IN} = 1/2 (V_{DD}–V_{EE}) p–p f_{IN} = 3MHz		-50		dB
Crosstalk, Control Input to Common O/I		10	R_1 = 1kΩ, R_L = 10kΩ Control t_{TLH} = t_{THL} = 20ns, Inhibit = V_{SS}		75		mV

Note 1. Data of “TYP” is intended as an indication of the IC’s potential performance.

2. For voltage drops across the switch(ΔVsw)>600mV (>300mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded.

■ TEST CIRCUIT



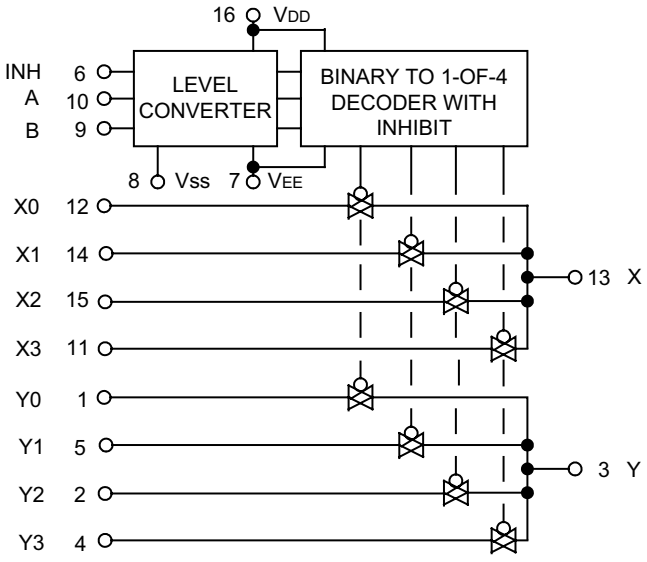
Switch Circuit Schematic

■ TRUTH TABLE

TRUTH TABLE

Control Inputs			ON Switches
	Select		
Inhibit	B	A	
0	0	0	Y0 X0
0	0	1	Y1 X1
0	1	0	Y2 X2
0	1	1	Y3 X3
1	X	X	None

* X=Don't Care



UTC 4052 Functional Diagram

Features

- **Medium-voltage and Standard-voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
- **Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)**
- **2-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bi-directional Data Transfer Protocol**
- **100 kHz (2.7V) and 400 kHz (5V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **8-byte Page (1K, 2K), 16-byte Page (4K, 8K, 16K) Write Modes**
- **Partial Page Writes are Allowed**
- **Self-timed Write Cycle (10 ms max)**
- **High-reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **8-lead PDIP and 8-lead JEDEC SOIC Packages**

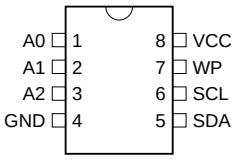
Description

The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many automotive applications where low-power and low-voltage operation are essential. The AT24C01A/02/04/08/16 is available in space-saving 8-lead PDIP and 8-lead JEDEC SOIC packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V) and 2.7V (2.7V to 5.5V) versions.

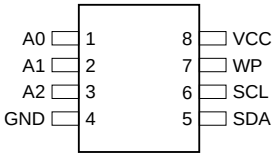
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

8-lead PDIP



8-lead SOIC



2-wire Automotive Serial EEPROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

AT24C01A
AT24C02
AT24C04
AT24C08(1)
AT24C16(2)

Note: 1. This device is not recommended for new designs. Please refer to AT24C08A.

2. This device is not recommended for new designs. Please refer to AT24C16A.

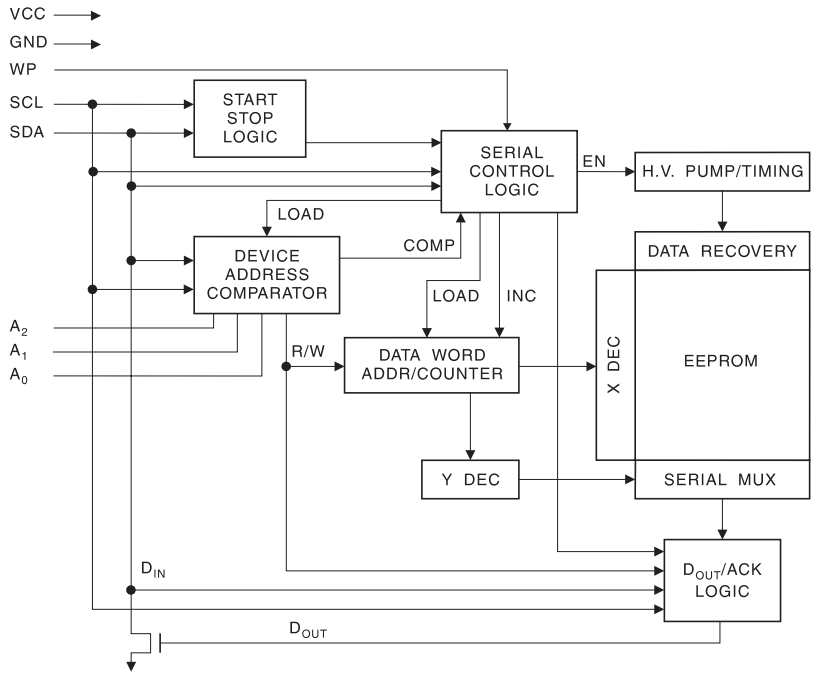
3256D–SEEPR–11/03

Absolute Maximum Ratings

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

DC Characteristics

Applicable over recommended operating range from: T_A = -40°C to +125°C, V_{CC} = +2.7V to +5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		2.7		5.5	V
V_{CC2}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB2}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level[1]		-0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

AC Characteristics

Applicable over recommended operating range from T_A = -40°C to +125°C, V_{CC} = +2.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted).

Symbol	Parameter	2.7V		5.0V		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		100		400	kHz
t_{LOW}	Clock Pulse Width Low	4.7		1.2		µs
t_{HIGH}	Clock Pulse Width High	4.0		0.6		µs
t_I	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.1	4.5	0.1	0.9	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	4.7		1.2		µs
$t_{HD.STA}$	Start Hold Time	4.0		0.6		µs
$t_{SU.STA}$	Start Setup Time	4.7		0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Setup Time	200		100		ns
t_R	Inputs Rise Time(1)		1.0		0.3	µs
t_F	Inputs Fall Time(1)		300		300	ns
$t_{SU.STO}$	Stop Setup Time	4.7		0.6		µs
t_{DH}	Data Out Hold Time	100		50		ns
t_{WR}	Write Cycle Time		10		10	ms
Endurance(1)	5.0V, 25°C, Byte Mode	1M		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (refer to Data Validity timing diagram). Data changes during SCL high periods will indicate a start or stop condition as defined below.

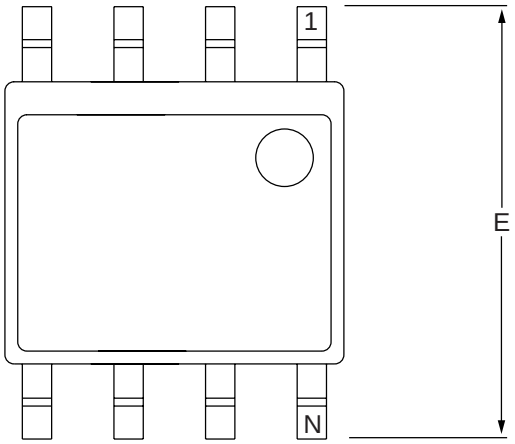
START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (refer to Start and Stop Definition timing diagram).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Start and Stop Definition timing diagram).

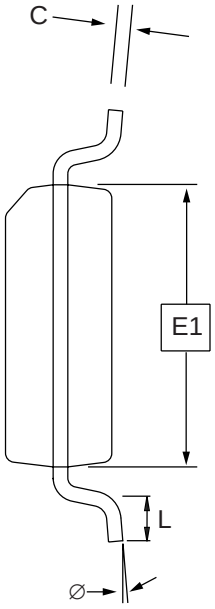
ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The AT24C01A/02/04/08/16 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

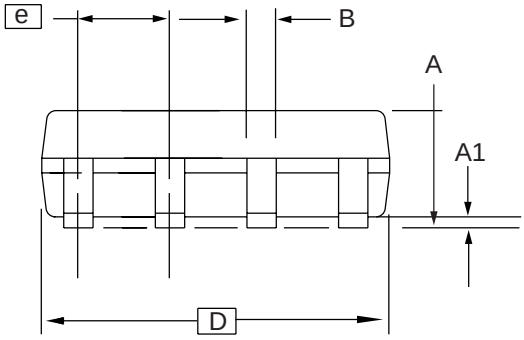
8S1 – JEDEC SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

10/7/03

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** B

FAIRCHILD SEMICONDUCTOR TM

May 1999

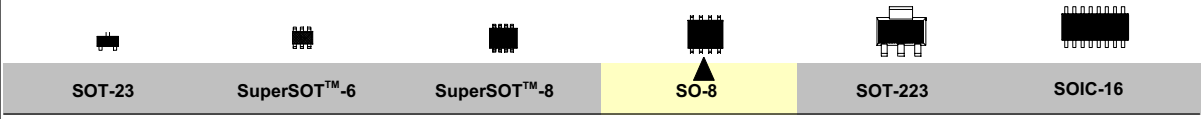
FDS9435A
Single P-Channel Enhancement Mode Field Effect Transistor

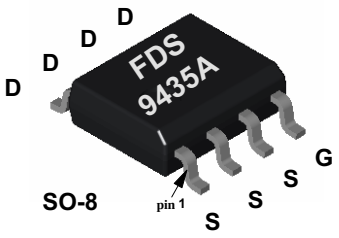
GeneralDescription

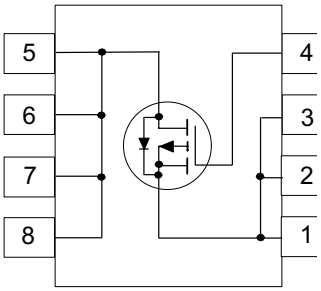
SO-8 P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -5.3 A, -30 V, $R_{DS(ON)}$ = 0.045 Ω @ V_{GS} = -10 V,
  $R_{DS(ON)}$ = 0.075 Ω @ V_{GS} = - 4.5 V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.







Absolute Maximum Ratings T_A = 25°C unless otherwise noted

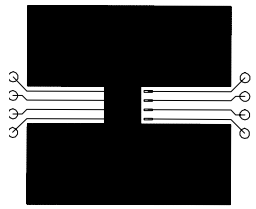
Symbol	Parameter		FDS9435A	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		-20	V
I_D	Drain Current - Continuous	(Note 1a)	- 5.3	A
	- Pulsed		-50	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

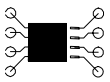
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
BV_{DSS}/T_J	Breakdown Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25 °C		-25		mV/ °C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			-100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-1.5	-3	V
$V_{GS(th)}/T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25 °C		-3.2		mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -5.3 A		0.035	0.045	Ω
		T_J =125°C		0.052	0.072	
		V_{GS} = -4.5 V, I_D = -4.0 A		0.059	0.075	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-25			A
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -4 A		9.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		730		pF
C_{oss}	Output Capacitance			400		pF
C_{rss}	Reverse Transfer Capacitance			90		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DS} = -10 V, I_D = -1 A		11	20	ns
t_r	Turn - On Rise Time	V_{GS} = -10 V , R_{GEN} = 6 Ω		10	18	
$t_{D(off)}$	Turn - Off Delay Time			90	125	
t_f	Turn - Off Fall Time			55	80	
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -4 A,		19	27	nC
Q_{gs}	Gate-Source Charge	V_{GS} = -10 V		3.5		
Q_{gd}	Gate-Drain Charge			3.6		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.1 A (Note 2)		-0.77	-1.2	V

Notes:

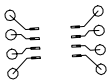
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W on a 1 in² pad of 2oz copper.



b. 105°C/W on a 0.04 in² pad of 2oz copper.



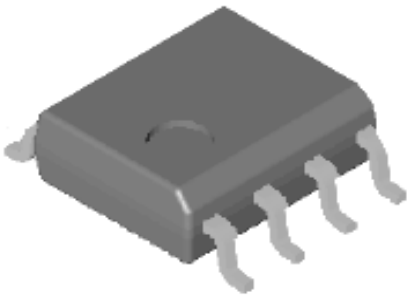
c. 125°C/W on a 0.006 in² pad of 2oz copper.

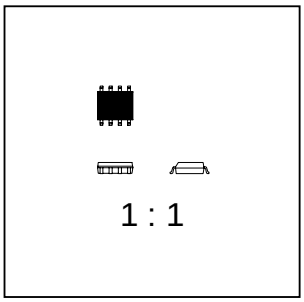
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC-8 (FS PKG Code S1)

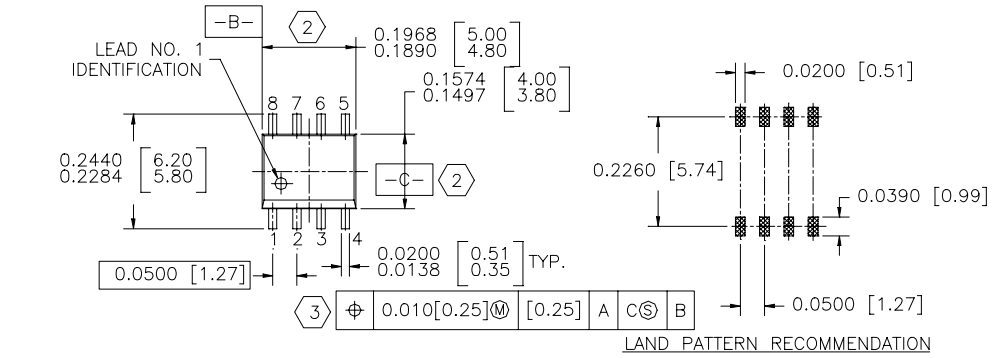


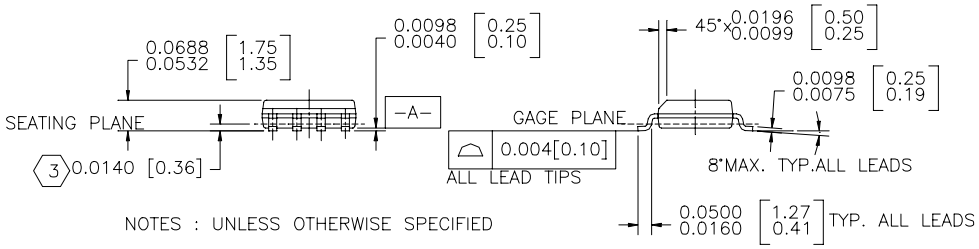


Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774





NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   200 MICROINCHES / 5.08 MICRONS MINIMUM
   LEAD / TIN (SOLDER) ON COPPER.

SO 0.150 WIDE 8 LEADS

2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

3. MAXIMUM LEAD 0.024 [0.609]

September 1998, Rev. A

TDA8944J

2 x 7 W stereo Bridge Tied Load (BTL) audio amplifier

Rev. 02 — 14 February 2000 **Product specification**

1. General description

The TDA8944J is a dual-channel audio power amplifier with an output power of 2×7 W at an 8 Ω load and a 12 V supply. The circuit contains two Bridge Tied Load (BTL) amplifiers with an all-NPN output stage and standby/mute logic. The TDA8944J comes in a 17-pin DIL-bent-SIL (DBS) power package. The TDA8944J is printed-circuit board (PCB) compatible with all other types in the TDA894x family. One PCB footprint accommodates both the mono and the stereo products.

2. Features

- Few external components
- Fixed gain
- Standby and mute mode
- No on/off switching plops
- Low standby current
- High supply voltage ripple rejection
- Outputs short-circuit protected to ground, supply and across the load
- Thermally protected
- Printed-circuit board compatible.

3. Applications

- Mains fed applications (e.g. TV sound)
- PC audio
- Portable audio.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		6	12	18	V
I_q	quiescent supply current	V_{CC} = 12 V; $R_L = \infty$	-	24	36	mA
I_{stb}	standby supply current		-	-	10	µA

Table 1: Quick reference data...*continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_o	output power	THD = 10%; R_L = 8 Ω; V_{CC} = 12 V	6	7	-	W
THD	total harmonic distortion	P_o = 1 W	-	0.03	0.1	%
G_v	voltage gain		31	32	33	dB
SVRR	supply voltage ripple rejection		50	65	-	dB

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8944J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

6. Block diagram

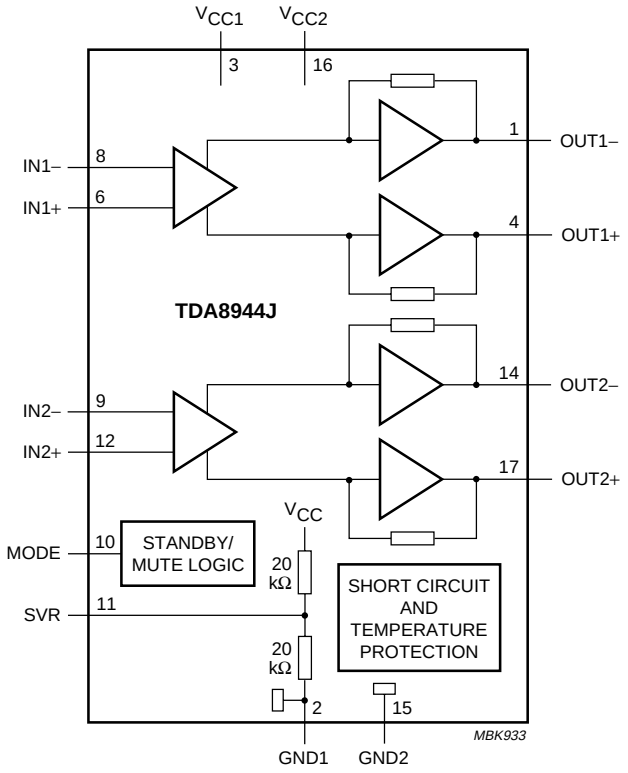


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

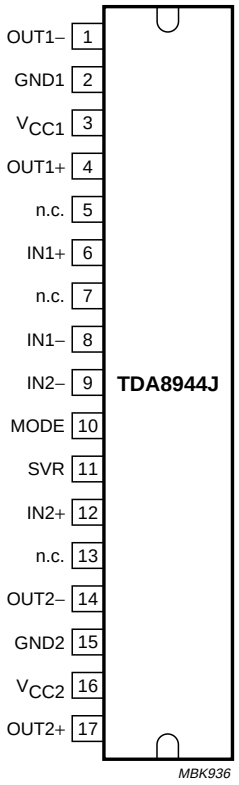


Fig 2. Pin configuration.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
OUT1–	1	negative loudspeaker terminal 1
GND1	2	ground channel 1
V_{CC1}	3	supply voltage channel 1
OUT1+	4	positive loudspeaker terminal 1
n.c.	5	not connected
IN1+	6	positive input 1
n.c.	7	not connected
IN1–	8	negative input 1
IN2–	9	negative input 2
MODE	10	mode selection input (standby, mute, operating)
SVR	11	half supply voltage decoupling (ripple rejection)
IN2+	12	positive input 2

Table 3: Pin description...*continued*

Symbol	Pin	Description
n.c.	13	not connected
OUT2–	14	negative loudspeaker terminal 2
GND2	15	ground channel 2
V_{CC2}	16	supply voltage channel 2
OUT2+	17	positive loudspeaker terminal 2

8. Functional description

The TDA8944J is a stereo BTL audio power amplifier capable of delivering 2 × 7 W output power to an 8 Ω load at THD = 10%, using a 12 V power supply and an external heatsink. The voltage gain is fixed at 32 dB.

With the three-level MODE input the device can be switched from ‘standby’ to ‘mute’ and to ‘operating’ mode.

The TDA8944J outputs are protected by an internal thermal shutdown protection mechanism and a short-circuit protection.

8.1 Input configuration

The TDA8944J inputs can be driven symmetrical (floating) as well as asymmetrical. In the asymmetrical mode one input pin is connected via a capacitor to the signal ground which should be as close as possible to the SVR (electrolytic) capacitor ground. Note that the DC level of the input pins is half of the supply voltage V_{CC}, so coupling capacitors for both pins are necessary.

The input cut-off frequency is:

$$f_{i(cut-off)} = \frac{1}{2-(R_i \times C_i)} \quad (1)$$

For R_i = 45 kΩ and C_i = 220 nF:

$$f_{i(cut-off)} = \frac{1}{2-(45 \times 10^{3} \times 220 \times 10^{-9})} = 16\ \text{Hz} \quad (2)$$

As shown in Equation 1 and 2, large capacitor values for the inputs are not necessary; so the switch-on delay during charging of the input capacitors, can be minimized. This results in a good low frequency response and good switch-on behaviour.

Remark: To prevent HF oscillations do not leave the inputs open, connect a capacitor of at least 1.5 nF across the input pins close to the device.

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	no signal	–0.3	+25	V
		operating	–0.3	+18	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		-	2	A
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
P_{tot}	total power dissipation		-	18	W
$V_{CC(sc)}$	supply voltage to guarantee short-circuit protection		-	15	V

10. Thermal characteristics

Table 6: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	both channels driven	6.9	K/W

11. Static characteristics

Table 7: Static characteristics

V_{CC} = 12 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; V_i = 0 V; measured in test circuit Figure 14; unless otherwise specified.

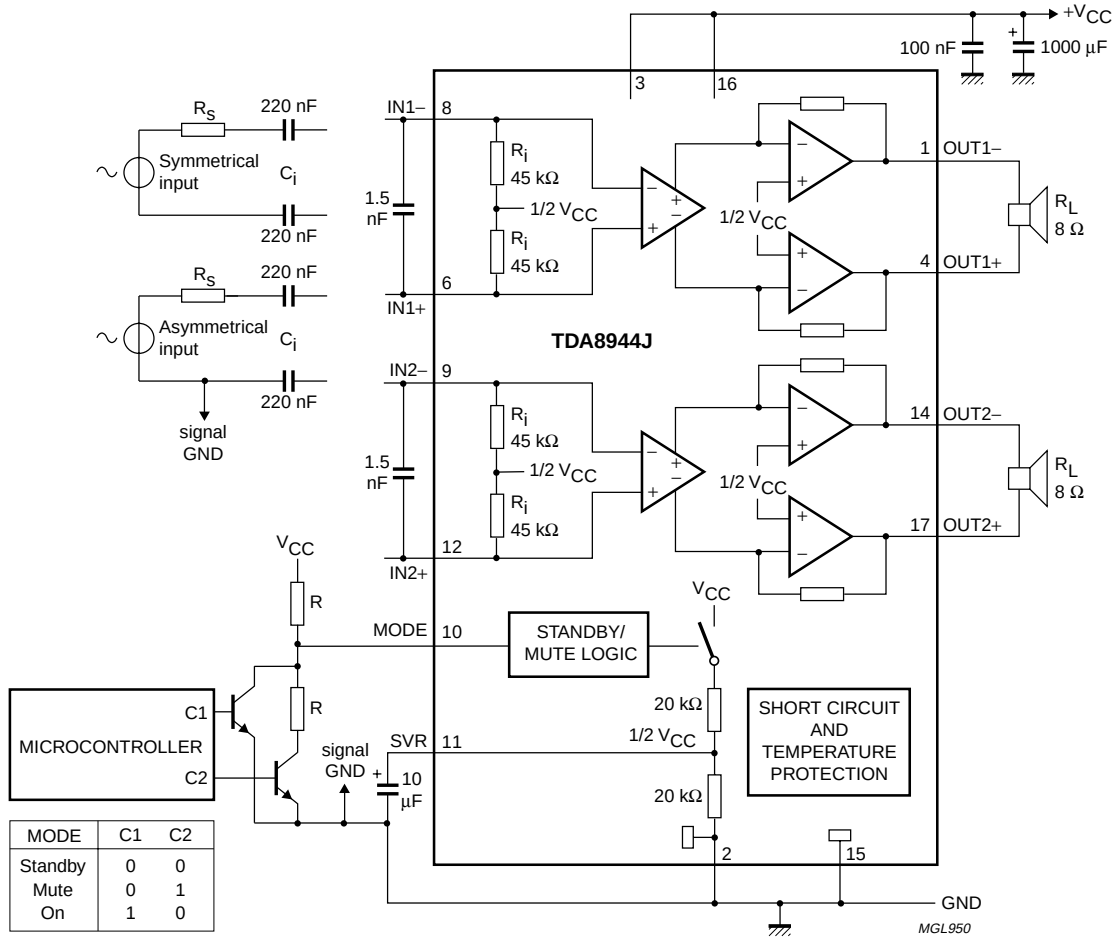
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	operating		6	12	18	V
I_q	quiescent supply current	R_L = ∞	[1]	-	24	36	mA
I_{stb}	standby supply current	V_{MODE} = V_{CC}		-	-	10	µA
V_O	DC output voltage		[2]	-	6	-	V
ΔV_{OUT}	[3] differential output voltage offset			-	-	200	mV
V_{MODE}	mode selection input voltage	operating mode		0	-	0.5	V
		mute mode		3	-	V_{CC} – 1.5	V
		standby mode		V_{CC} – 0.5	-	V_{CC}	V
I_{MODE}	mode selection input current	0 < V_{MODE} < V_{CC}		-	-	20	µA

[1] With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the differential output voltage offset (ΔV_{OUT}) divided by the load resistance (R_L).

[2] The DC output voltage with respect to ground is approximately 0.5V_{CC}.

[3] $\Delta V_{OUT} = |V_{OUT+} - V_{OUT-}|$

14. Application information



MODE	C1	C2
Standby	0	0
Mute	0	1
On	1	0

Fig 14. Application diagram.

14.1 Printed-circuit board (PCB)

14.1.1 Layout and grounding

For a high system performance level certain grounding techniques are essential. The input reference grounds have to be tied with their respective source grounds and must have separate tracks from the power ground tracks; this will prevent the large (output) signal currents from interfering with the small AC input signals.

The small-signal ground tracks should be physically located as far as possible from the power ground tracks. Supply and output tracks should be as wide as possible for delivering maximum output power.

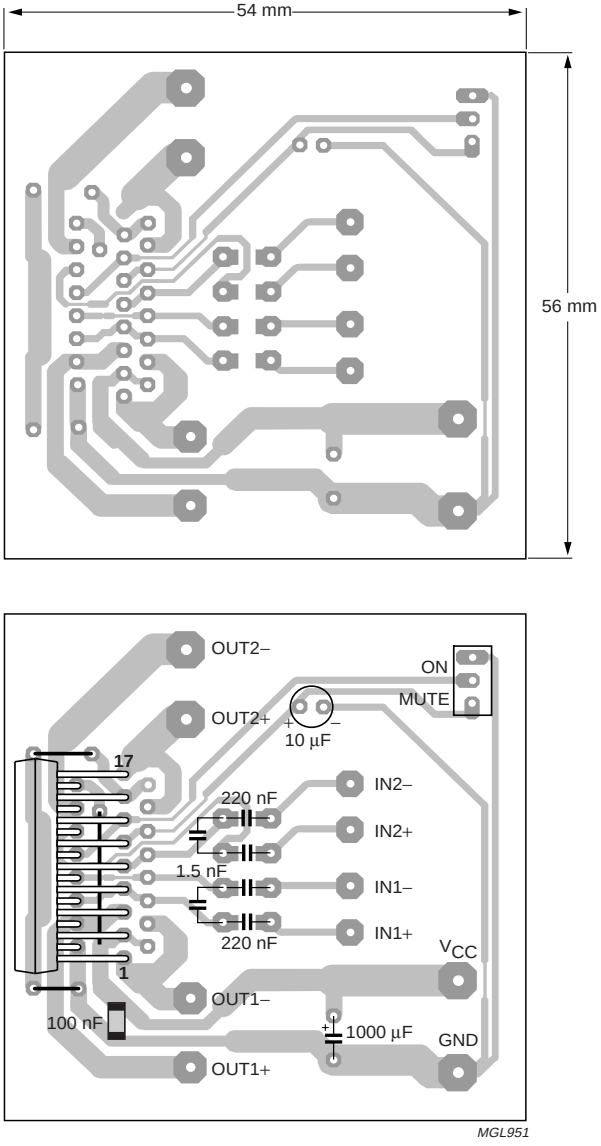


Fig 15. Printed-circuit board layout (single-sided); components view.

14.1.2 Power supply decoupling

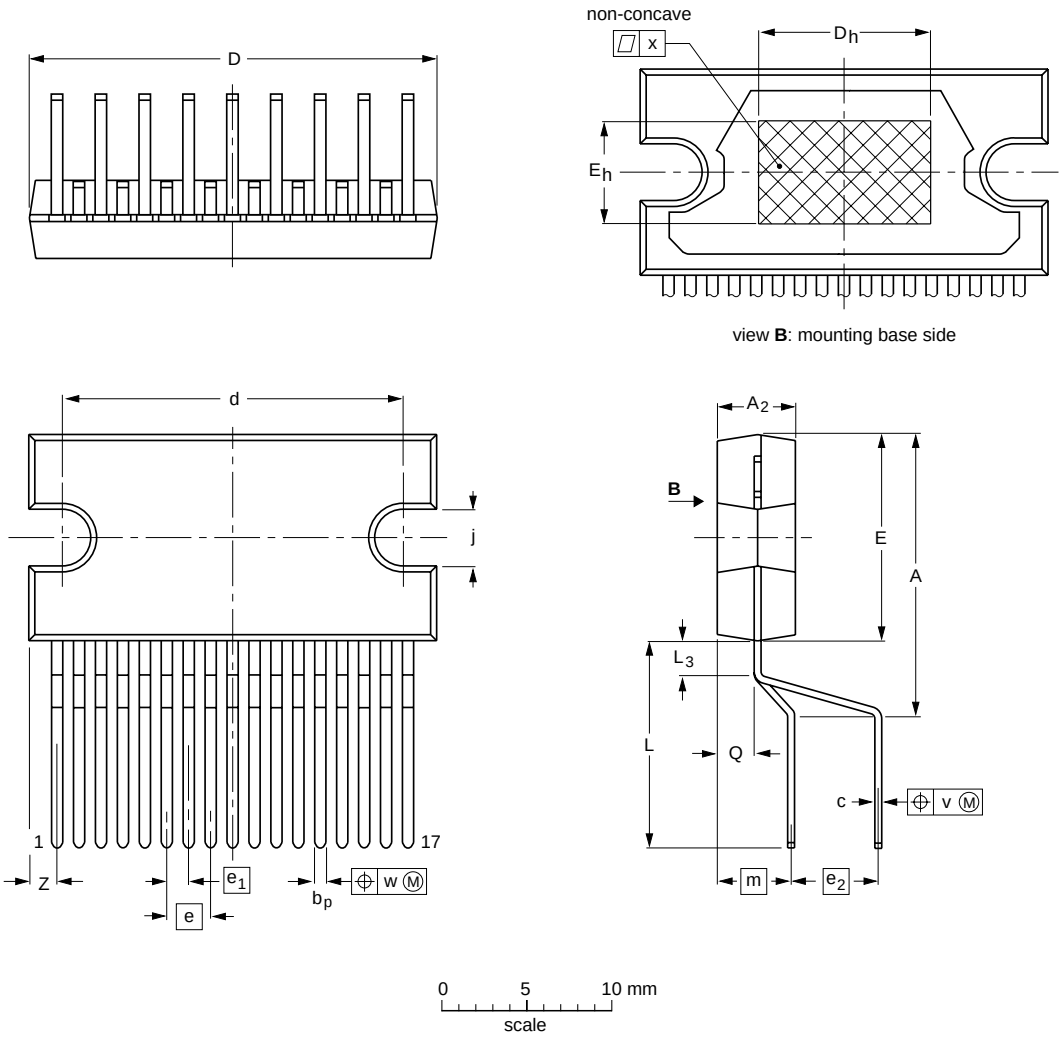
Proper supply bypassing is critical for low-noise performance and high supply voltage ripple rejection. The respective capacitor locations should be as close as possible to the device and grounded to the power ground. Proper power supply decoupling also prevents oscillations.

For suppressing higher frequency transients (spikes) on the supply line a capacitor with low ESR – typical 100 nF – has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor – e.g. 1000 µF or greater – must be placed close to the device.

The bypass capacitor on the SVR pin reduces the noise and ripple on the midrail voltage. For good THD and noise performance a low ESR capacitor is recommended.

16. Package outline

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm) **SOT243-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						~~97-12-16~~ 99-12-17

Fig 16. DBS17P package outline.

I²C-bus controlled single and multistandard alignment-free IF-PLL demodulators

1 FEATURES

- 5 V supply voltage
- Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier, AC-coupled
- Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation, good intermodulation figures, reduced harmonics, and excellent pulse response
- Gated phase detector for L and L-accent standard
- Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free, frequencies switchable for all negative and positive modulated standards via I²C-bus
- Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75, and 58.75 MHz
- 4 MHz reference frequency input: signal from Phase-Locked Loop (PLL) tuning system or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
- External AGC setting via pin OP1
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter, AFC bits readable via I²C-bus
- TakeOver Point (TOP) adjustable via I²C-bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5, 5.5, 6.0, and 6.5 MHz, controlled by FM-PLL oscillator
- Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode, PLL controlled
- SIF-AGC for gain controlled SIF amplifier, single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I²C-bus
- AM demodulator without extra reference circuit
- Alignment-free selective FM-PLL demodulator with high linearity and low noise
- Four selectable I²C-bus addresses
- I²C-bus control for all functions
- I²C-bus transceiver with pin programmable Module Address (MAD).

2 GENERAL DESCRIPTION

The TDA9885 is an alignment-free multistandard (PAL and NTSC) vision and sound IF signal PLL demodulator for negative modulation only and FM processing.

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation, including sound AM and FM processing.

3 APPLICATIONS

- TV, VTR, PC, and STB applications.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9885T/V3	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9885TS/V3	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9885HN/V3	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body $5 \times 5 \times 0.85$ mm	SOT617-3
TDA9886T/V4	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
TDA9886TS/V4	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA9886HN/V4	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body $5 \times 5 \times 0.85$ mm	SOT617-3

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	notes 1 and 2	4.5	5.0	5.5	V
I_P	supply current		52	63	70	mA
Video part						
$V_{i(VIF)(rms)}$	VIF input voltage sensitivity (RMS value)	−1 dB video at output	–	60	100	μV
$G_{VIF(cr)}$	VIF gain control range	see Fig.7	60	66	–	dB
f_{VIF}	vision carrier operating frequencies	see Table 14	–	33.4	–	MHz
			–	33.9	–	MHz
			–	38.0	–	MHz
			–	38.9	–	MHz
			–	45.75	–	MHz
			–	58.75	–	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	related to f_{VIF}; see Fig.10	–	±2.3	–	MHz
$V_{o(v)(p-p)}$	video signal output voltage (peak-to-peak value)	see Fig.5				
		normal mode	1.7	2.0	2.3	V
		trap bypass mode	0.95	1.10	1.25	V
G_{dif}	differential gain	*"CCIR 330"*; note 3				
		B/G standard	–	–	5	%
		L standard	–	–	7	%
φ_{dif}	differential phase	*"CCIR 330"*	–	2	4	deg
$B_{v(-1dB)}$	−1 dB video bandwidth	trap bypass mode; AC load; C_L < 20 pF; R_L > 1 kΩ	5	6	–	MHz
$B_{v(-3dB)(trap)}$	−3 dB video bandwidth including sound carrier trap	note 4				
		f_{trap} = 4.5 MHz	3.95	4.05	–	MHz
		f_{trap} = 5.5 MHz	4.90	5.00	–	MHz
		f_{trap} = 6.0 MHz	5.40	5.50	–	MHz
		f_{trap} = 6.5 MHz	5.50	5.95	–	MHz
α_{SC1}	trap attenuation at first sound carrier	M/N standard	30	36	–	dB
		B/G standard	30	36	–	dB
S/N_W	weighted signal-to-noise ratio	weighted in accordance with *"CCIR 567"*; see Fig.11; note 5	56	59	–	dB
$PSRR_{CVBS}$	power supply ripple rejection at pin CVBS	f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Fig.6	20	25	–	dB
AFC_{stps}	AFC control steepness	definition: $\Delta I_{AFC}/\Delta f_{VIF}$	0.85	1.05	1.25	μA/kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio part						
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	27 kHz FM deviation; 50 μs de-emphasis	430	540	650	mV
THD	total harmonic distortion of audio signal	FM: 27 kHz FM deviation; 50 μs de-emphasis	–	0.15	0.50	%
		AM: m = 54 %	–	0.5	1.0	%
$B_{AF(-3dB)}$	−3 dB AF bandwidth	without de-emphasis; dependent on FM-PLL filter	80	100	–	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	FM: 27 kHz FM deviation; 50 μs de-emphasis; vision carrier unmodulated	52	56	–	dB
		AM: m = 54 %	45	50	–	dB
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	50 μs de-emphasis; AM: f = 1 kHz and m = 54 %; referenced to 27 kHz FM deviation	40	46	–	dB
$PSRR_{AUD}$	power supply ripple rejection on pin AUD	f_{ripple} = 70 Hz; see Fig.6				
		for AM	20	26	–	dB
		for FM	14	20	–	dB
$V_{o(intc)(rms)}$	IF intercarrier output level (RMS value)	QSS mode; SC_1; SC_2 off	90	140	180	mV
		L standard; without modulation	90	140	180	mV
		intercarrier mode; PC/SC_1 = 20 dB; SC_2 off; note 6	–	75	–	mV
Reference frequency						
f_{ref}	reference signal frequency	note 7	–	4	–	MHz
$V_{ref(rms)}$	reference signal voltage (RMS value)	operation as input terminal	80	–	400	mV

Notes

1. Values of video and sound parameters can be decreased at V_P = 4.5 V.
2. For applications without I²C-bus, the time constant (R × C) at the supply must be >1.2 μs (e.g. 1 Ω and 2.2 μF).
3. Condition: luminance range (5 steps) from 0 % to 100 %.
4. AC load: C_L < 20 pF and R_L > 1 kΩ. The sound carrier frequencies (depending on the TV standard) are attenuated by the integrated sound carrier traps (see Figs 13 to 18; $|H(s)|$ is the absolute value of transfer function).
5. S/N_W is the ratio of the black-to-white amplitude to the black level noise voltage (RMS value measured on pin CVBS). B = 5 MHz weighted in accordance with *"CCIR 567"*.

6 BLOCK DIAGRAM

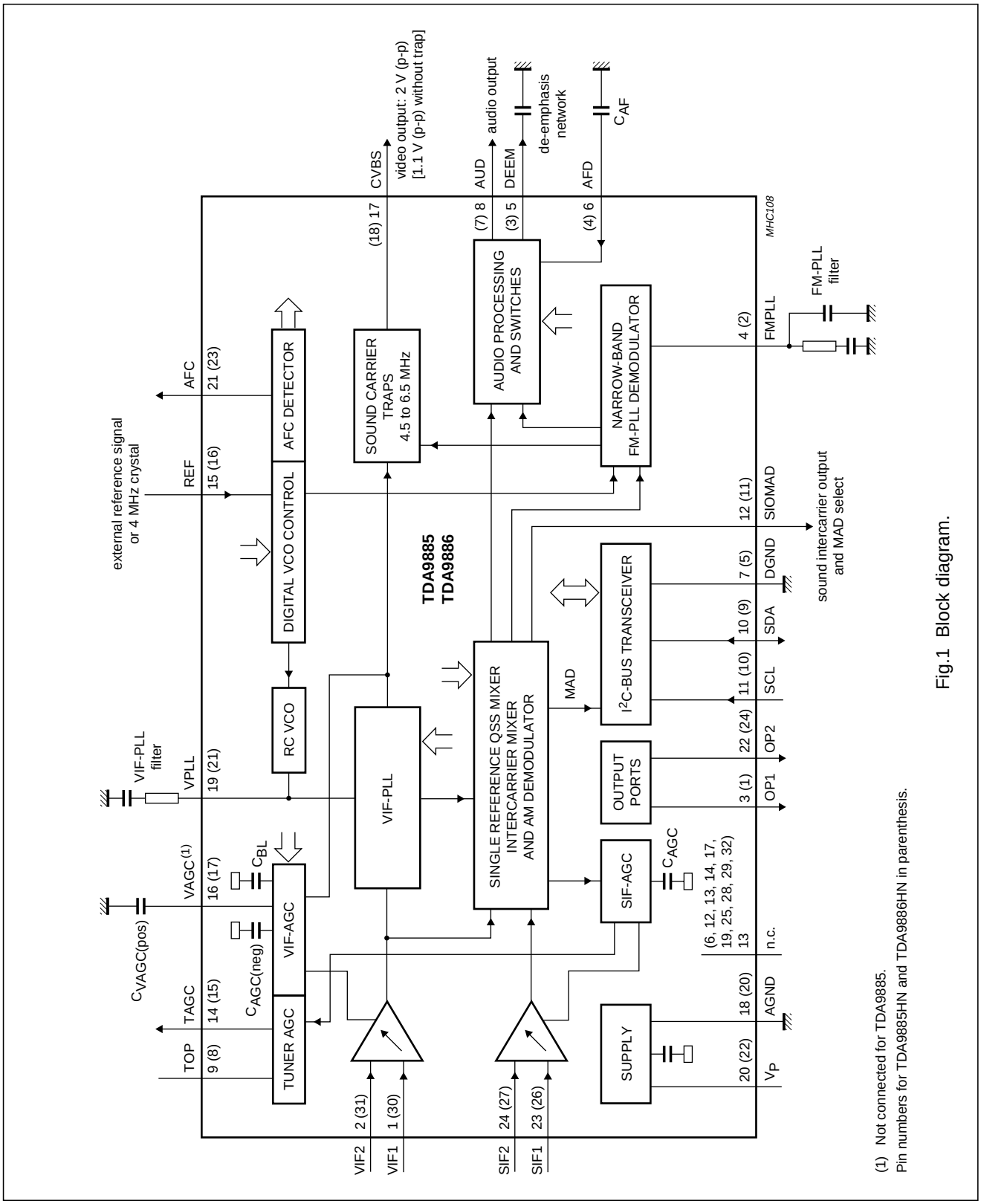
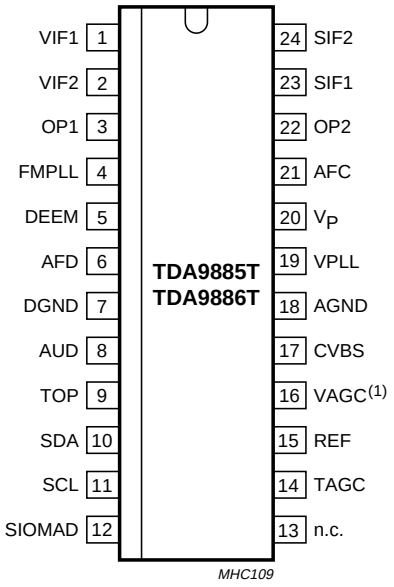


Fig.1 Block diagram.

(1) Not connected for TDA9885.
Pin numbers for TDA9885HN and TDA9886HN in parenthesis.

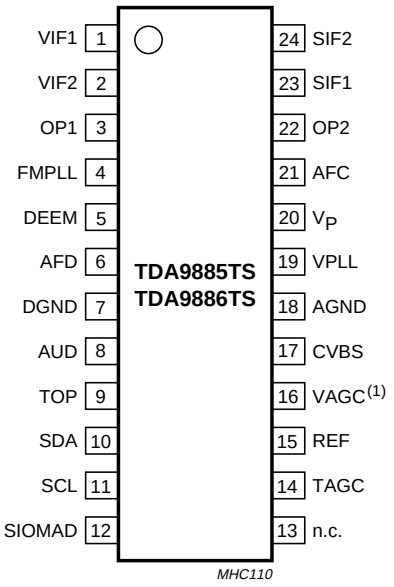
7 PINNING

SYMBOL	PIN				DESCRIPTION
	TDA9885T TDA9885TS	TDA9886T TDA9886TS	TDA9885HN	TDA9886HN	
VIF1	1	1	30	30	VIF differential input 1
VIF2	2	2	31	31	VIF differential input 2
n.c.	–	–	32	32	not connected
OP1	3	3	1	1	output port 1; open-collector
FMPLL	4	4	2	2	FM-PLL for loop filter
DEEM	5	5	3	3	de-emphasis output for capacitor
AFD	6	6	4	4	AF decoupling input for capacitor
DGND	7	7	5	5	digital ground
n.c.	–	–	6	6	not connected
AUD	8	8	7	7	audio output
TOP	9	9	8	8	tuner AGC TakeOver Point (TOP) for resistor adjustment
SDA	10	10	9	9	I²C-bus data input and output
SCL	11	11	10	10	I²C-bus clock input
SIOMAD	12	12	11	11	sound intercarrier output and MAD select with resistor
n.c.	–	–	12	12	not connected
n.c.	13	13	13	13	not connected
n.c.	–	–	14	14	not connected
TAGC	14	14	15	15	tuner AGC output
REF	15	15	16	16	4 MHz crystal or reference signal input
VAGC	–	16	–	17	VIF-AGC for capacitor
n.c.	16	–	17	–	not connected
CVBS	17	17	18	18	composite video output
n.c.	–	–	19	19	not connected
AGND	18	18	20	20	analog ground
VPLL	19	19	21	21	VIF-PLL for loop filter
V_P	20	20	22	22	supply voltage
AFC	21	21	23	23	AFC output
OP2	22	22	24	24	output port 2; open-collector
n.c.	–	–	25	25	not connected
SIF1	23	23	26	26	SIF differential input 1 and MAD select with resistor
SIF2	24	24	27	27	SIF differential input 2 and MAD select with resistor
n.c.	–	–	28	28	not connected
n.c.	–	–	29	29	not connected



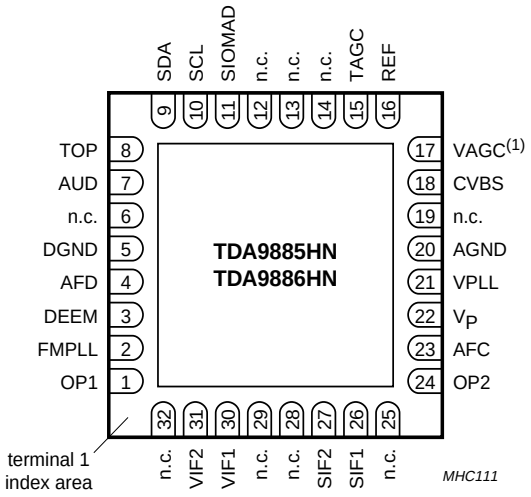
(1) Not connected for TDA9885T.

Fig.2 Pin configuration for SO24.



(1) Not connected for TDA9885TS.

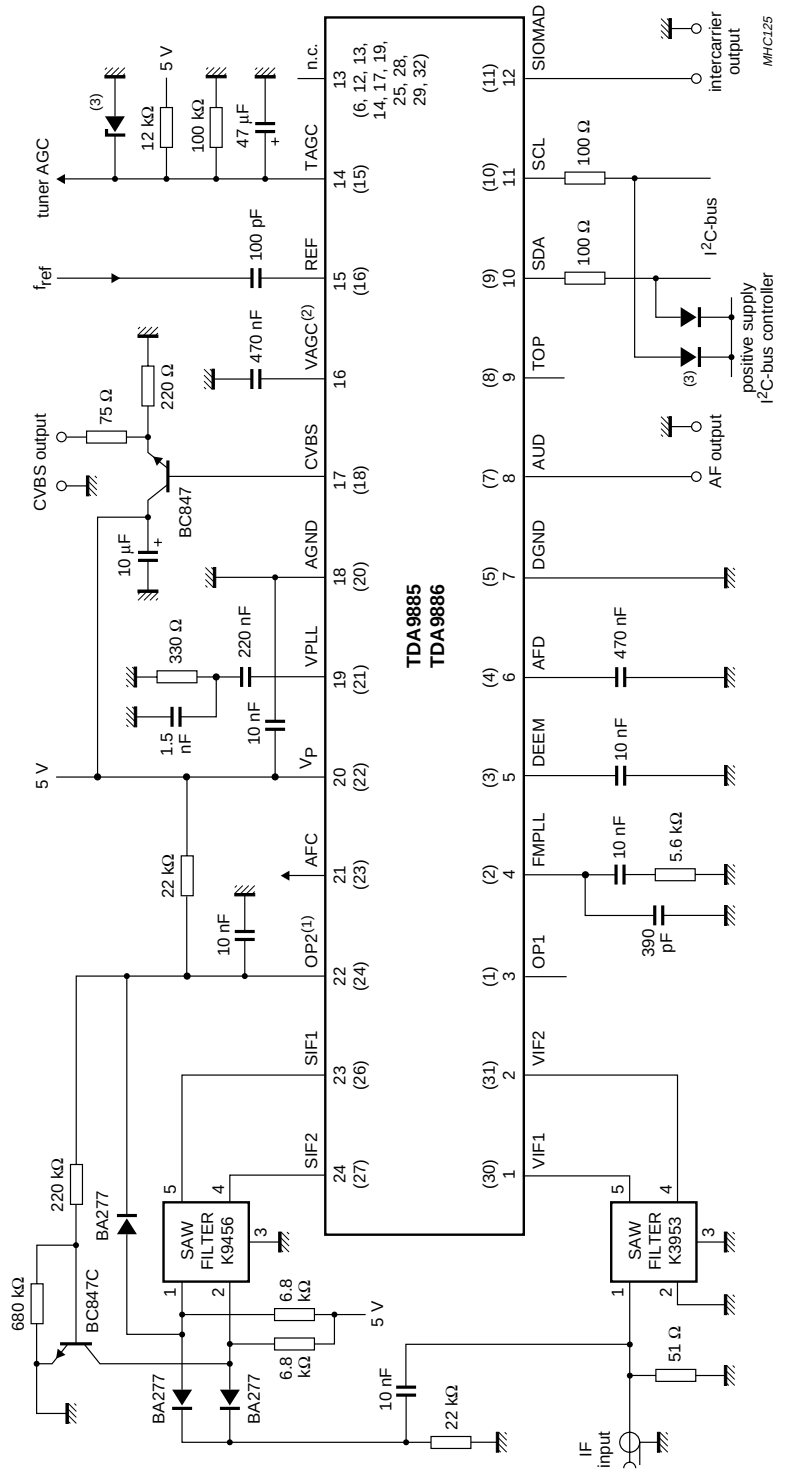
Fig.3 Pin configuration for SSOP24.



Bottom view.

(1) Not connected for TDA9885HN.

Fig.4 Pin configuration for HVQFN32.



Pin numbers for TDA9885HN and TDA9886HN in parenthesis.

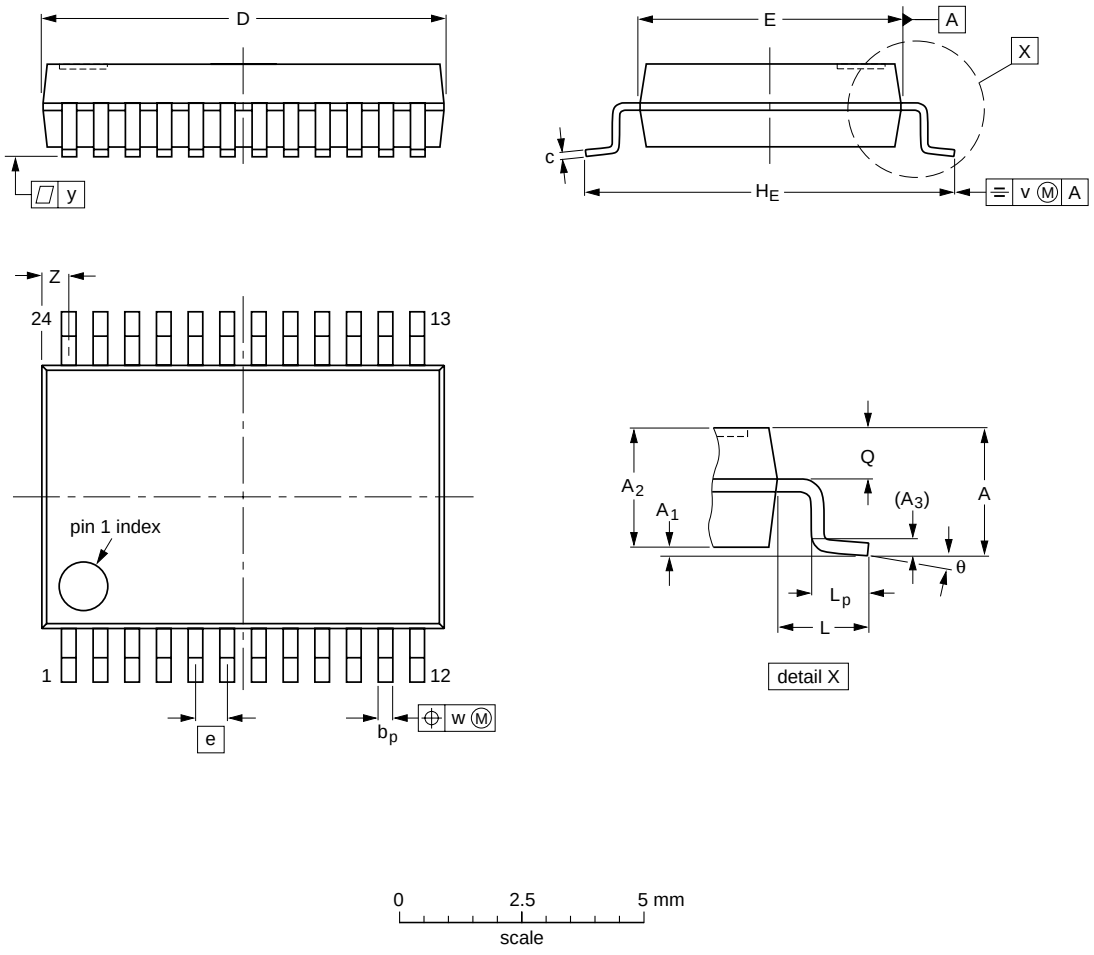
(1) If pin OP2 outputs VIF-AGC voltage, then pin OP1 can be used for SAW switching.

(2) Not connected for TDA9885.

(3) Optional measures to improve ESD performance within a TV-set application.

Fig.24 Application circuit.

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

ZHUHAI JINSHENG ELECTRONICS CO.,LTD	PRODUCT SPECIFICATION	MODEL ET-5C511-BS1A	PAGE
		DESCRIPTION PAL B\G PLL TUNER	

NO.	ITEM	DESCRIPTION
1	GENERAL	
1.1	Supply Voltage	True 5V Device (low power dissipation)。
1.2	Control System	I^2C bus control of tuning
1.3	Tuning System	PLL controlled tuning 。
1.5	Receiving System	PAK B\G
1.6	Receiving Channels	Full frequency range from 45.75MHz to 863.25 MHz.

BAND	ET-5C511-BS1A
Low band	45.75MHz ~160.25MHz
Mid band	168.25MHz ~ 464.25MHz
High band	471.25MHz ~ 863.25MHz

1．7	Intermediate Frequency	System		B\G
		Picture	Carried	38.90
		Color	Carried	34.47
		Sound	Carried	33.40

unit：MHz

1．8	Antenna Input Impedance	VHF/UHF/CATV， 75 ohm unbalanced
1．9	Output Impedance	75ohm unbalanced
1．10	Weight	37g±3g

1.11 端子功能说明

SYMBOL	PIN	SPECIFICATION	CURRENT
AGC	1	AGC supply voltage：+4.5V	20mA
TU	2	Tuning Voltage	1.7mA
AS/CE	3	I^2C-bus address select	
SCL	4	I^2C-bus serial clock	
SDA	5	I^2C-bus serial date	
VCC	6	Tuner supply voltage：+5V	
VCC	7	+B of PLL mixer	115mA
ADC	8	NC	
+33V	9	+33V	
GDN	10	Ground	
IF	11	IF output	

Note: 6. 7 selected by customer。

NO.	ITEM	SPECIFICATION
1.13	Operating Temperature	-10℃ to +60℃: Standard：+25℃
1.14	Relative Humidity	0 to 90% Standard: 60%
1.15	Storage Temperature	-20℃ to +80℃: Standard：+25℃

2. Electrical Characteristics

2．1 Frequency Cover Range Of local Oscillator：

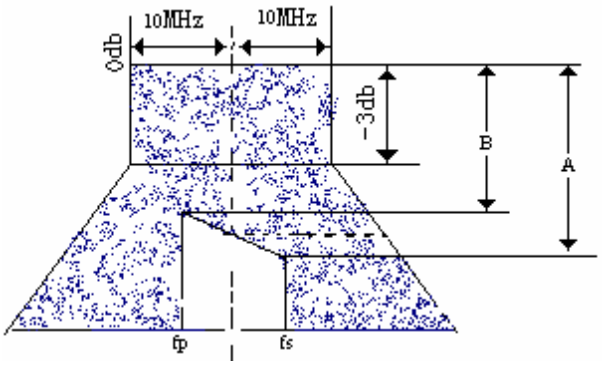
The min adjustable range of local frequency including all freq .of high-low channel nominal local freq .Of each band and the ends is over 2MHz

BAND	Frequency cover range of local oscillator
VHF Low	83.25MHz ~ 202.15MHz
VHF High	205.15MHz ~ 505.15MHz
UHF	500.15MHz ~ 904.15MHz

2.2 Frequency Response

2．2．1 The freq . response shall fall in the hatched area show chart ,and accord with table

。



Frequency range	A	B
VHF Low	-9	-4
VHF High	-8	- -4
UHF	-8	-4

2.3 POWER GAIN

VHF： 30dBMin

UHF： 30dBMin

2.4 DEVIATION OF POWER GAIN

ALL BAND： 8dBMax

2. 6 AGC CHARACTERISTICS

VHF: 40dbMin

UHF: 35dbMin

2.7 NOISE COEFFICIENT

VHF： 8dBMax

UHF： 8dBMax

2.8 IMAGE REJECTION RATION]

VHF： 51dBMin。

UHF： 46dBMin。

2.9 IF REJECTION RATION

55dbMin

2.10 1% CROSS MODULATION

75dBμ V Min

2.11 BEAT INTERFERENCE REJECTION RATIO

DS-2 CH : 45dB

DS-3 CH : 42dB

2.12 COLOR BEAT INTERFERENCE REJECTION RATIO

All Band :45dBMin

2.13 THE MAX INPUT SIGNAL LEVEL

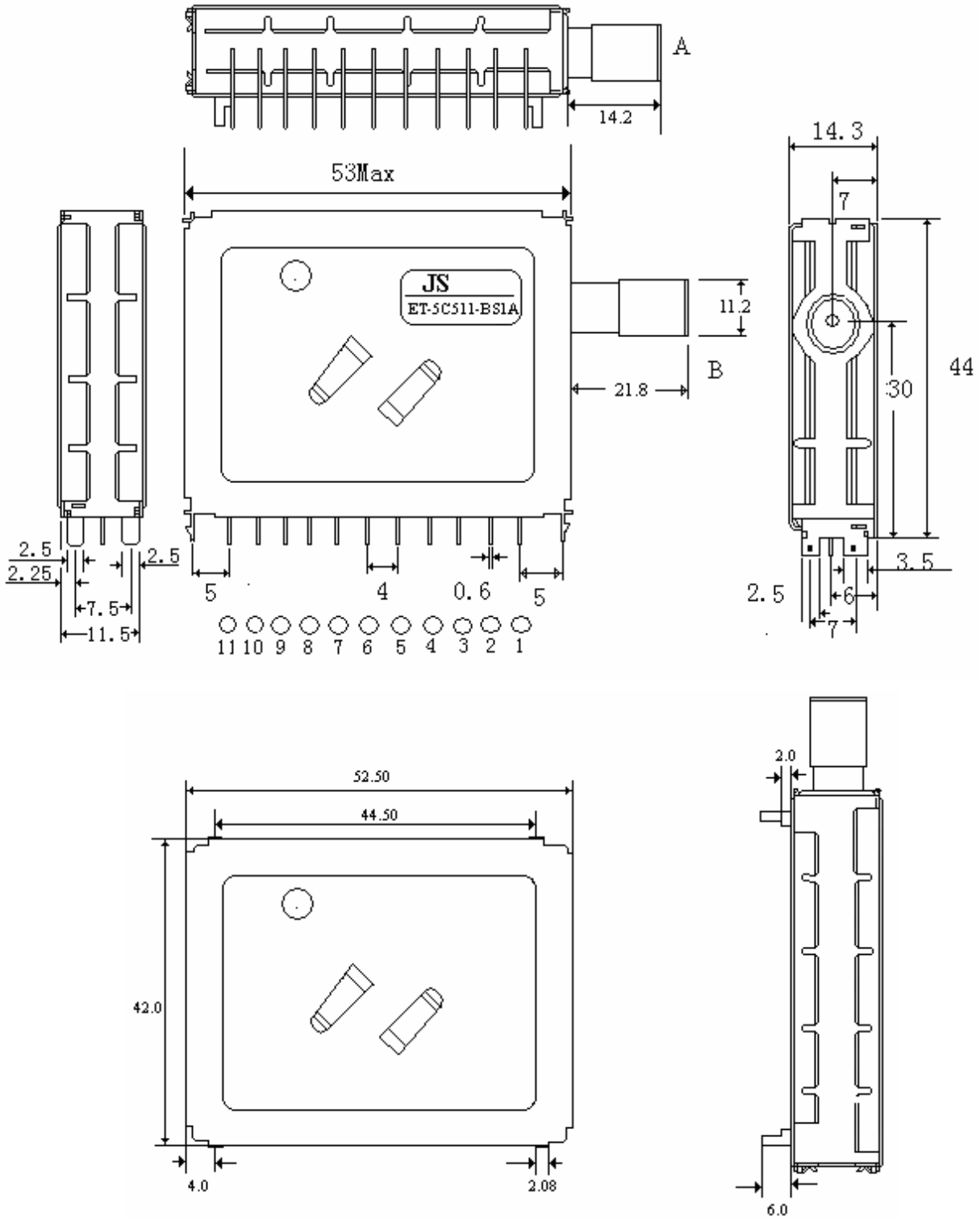
All Band :100dBμV Max

2.14 RF INPUT VSWR

All Band :5dBMax

ZHUHAI JINSHENG ELECTRONICS CO.,LTD	PRODUCT SPECIFICATION	MODEL ET-5C511-BS1A	PAGE
		DESCRIPTION **PAL B\G** **PLL TUNER**	

FEATURES SIZE Dimensions unit（mm）



NOTE: A. B. selected by customer。

HDZ1804-3A LCD TV POWER

Design specification

描　　述 DESCRIPTION	电　源　规　格 书 SPECIFICATION FOR SWITCHING POWER SUPPLY		
型　　号 MODEL NO.	HDZ1804-3A		

目录

TABLE OF CONTENTS

1 电源性能指标 Power supply overview

1.1 输入特性 INPUT ELECTRICAL CHARACTERISTICS

输入电压 Input Voltage Range	90Vac to 264Vac
额定电压 Normal Voltage Range	100Vac to 240Vac
频率范围 Frequency range	50Hz/60Hz±5%
最大输入电流 Max input AC current	2.8A Max at full load condition
浪涌电流 Inrush current (cold start)	50Atyp peak, 120Vac; 100Atyp peak 220Vac
效率 Efficiency (full load)	82%Min. 100Vac; 86% Min. 220Vac
谐波电流 Harmonic current	Meet GB17625 1-1998/IEC61000-3-2 Class D
漏电流 Leakage Current	Less than 0.7mA, 230Vac input
待机功耗 Standby Power Loss	≤1W Max at 264Vac, output power ≤0.1W
输入保险 Input Fuse	T5AH/250Vac

1.2 输出特性 OUTPUT ELECTRICAL CHARACTERISTICS

1.2.1 输出调整率 Output Voltage, Current & Regulation.

输出电压 Output Voltage	调整率 Regulation	最小电流 Min.Current	额定电流 Rated. current	峰值电流或功率 Peak current or power
+24V	±5%	0.1A	5.0A	7.5A
+12V	±5%	0.1A	3.0A	5.0A
+5V	±5%	0.1A	2.5A	5.0A
+5Vsb	±5%	0.02A	1.5A	1.5A

备注: 峰值电流或功率的测试是在其他额定负载时测试,且脉宽小于 100 毫秒. The peak current or power should be test at other of DC output at Rated load, and the peak current pulse width within 100ms.

1.2.2 输出纹波和噪声 DC Output Ripple & Noise.

输出电压 Output Voltage	纹波和噪声 Ripple & Noise V1
+24V	240mVp-p@25℃;240mVp-p@-5℃
+12V	120mVp-p@25℃;150mVp-p@-5℃
+5V	50mVp-p @25℃;50mVp-p@-5℃
+5Vsb	50mVp-p @25℃;50mVp-p@-5℃

备注:1） 示波器须设置在 20 兆赫兹带宽.Measurements shall be made with an oscilloscope with 20MHz bandwidth.

2) 输出须并联 0.1uF 的陶瓷电容和 10uF 的电解电容来模拟负载.Output shall be bypassed at the connector with a 0.1uF ceramic capacitor and a 10uF electrolytic capacitor to simulate system loading.

1.2.3 输出动态响应 Output Transient Response

Voltage Tolerance Limit	Slew Rate	Load Change
+12V +24V/+5V/+5Vsb ±5%	0.2A/uS	Min. to 50% load and 50% to Max load
All output ±10%	0.2A/uS	Min. load to Max load

备注：以 50~10kHz 的频率跳变负载来测试 Transient response measurements shall be made with a load changing repetition rate of 50Hz to 10kHz.

1.2.4 输出保持时间 DC Output Hold-Up Time

Output Voltage	120Vac input	220Vac input
+24V	≥10mS	≥10mS
+12V	≥10mS	≥10mS
+5V	≥10mS	≥10mS
+5Vsb	≥10mS	≥10mS

备注：所有输出带满载 All of dc output at full load.

1.2.5 输出超调 DC Output Overshoot At Turn On & Turn Off

Output Channel	Output(V)	超调电压(V)Over shoot voltage	
		开机 Turn on	关机 Turn off
+24V	+24V	10%	5%
+12V	+12V	10%	5%
+5V	+5V	10%	5%
+5Vsb	+5V	10%	5%

备注：测试时负载范围：最小到最大.All of dc output current from Min. to Max.

1.2.6 输出上升时间 DC output Voltage rise time

Output Voltage	120Vac input &Full Load	220Vac input &Full Load
+24V	≤50mS	≤50mS
+12V	≤50mS	≤50mS
+5V	≤50mS	≤50mS
+5Vsb	≤50mS	≤50mS

备注：输出从10%上升到90%的时间.The output voltages shall rise from 10% to 90% of their output voltage.

1.3 遥控功能 Remto On/Off Control

除+5Vsb 外，其余输出受控于一个 TTL 电平兼容的信号(Ps-on≥2.5V/2.0mA) +5Vsb 上电就存在。The power supply DC outputs(without +5Vsb) shall be enable with an active-high TTL(≥2.5V/2.0mA)-compatible signal(Ps-on, S/T).The +5Vsb is on whenever the AC power is present.

高电平，打开输出；低电平，关闭输出.When Ps-on is pulled to TTL high, the DC outputs are to be enabled. Ps-on When Ps-on is pulled to TTL low or open circuit, the DC outputs are to be disabled. Ps-on

Ps-on Signal	Comments	Outputs
S/T high	≥2.5V&2.0mA(source)	1
S/T low	≤1.0V	×
S/T open	--	×

1.4 保护功能 Protection

1.4.1 输出过压保护 DC output Over Voltage Protection

Output Voltage	Typ.Over Voltage	Comments
+24V	26-32V Type	Power supply latch into shutdown state 输出锁机
+12V	13-18V Type	Power supply latch into shutdown state 输出锁机
+5V	5.5V-9V Type	Power supply latch into shutdown state 输出锁机
+5Vsb	5.5V-9V Type	Power supply latch into shutdown state 输出锁机

备注：应该在最大的交流输入电压 264 伏和轻载、空载下测试 The power supply shall be test at max AC voltage(264Vac) and min load or no load.

1.4.2 输出过流保护 DC Output Over current Protection

Output Voltage	Over Current	Comments
+24V	7.5A-10A Type	Power supply latch into shutdown state 输出锁机
+12V	5A-9A Type	Power supply latch into shutdown state 输出锁机
+5V	5A-10A Type	Hiccup 打嗝保护模式
+5Vsb	2A-8A Type	Hiccup 打嗝保护模式

备注：过流保护测试是在其它额定负载时测试 The over current protection should be test at an Rated load.

1.4.3 输出短路保护 DC Output Short Circuit Protection

Output Voltage	Comments
+24V	Power supply latch into shutdown state 输出锁机
+12V	Power supply latch into shutdown state 输出锁机
+5V	Hiccup 打嗝保护模式
+5Vsb	Hiccup 打嗝保护模式

备注：短路保护测试是在其它额定负载时测试 The Short Circuit protection should be test at other of dc output at Rate load.

1.4.4 保护功能复位 Reset After Shutdown

故障去除后，电源进入保护状态后，AC 输入重置后，电源即可恢复正常工作。After power supply enter into shutdown, the power supply will restart after AC input reset.

2 绝缘性能 Isolation

2.1 绝缘耐压 Dielectric Strength

输入-输出 Input To Output	3000Vac 50Hz 1minute ≤10mA
输入-地 Input To FG	1500Vac 50Hz 1minute ≤10mA
输出-地 Output To FG	Non Isolated

备注：交流地和输出负极要断开 Open FG and Output return.

3 安全规格 Safety

电源安全性满足下列标准 The power supply shall compliance with the following Criterion:

(1) UL60065 (2) EN60065 (3) GB8988-2001

4 电磁兼容性 EMC

4.1 电磁干扰 EMI

电源电磁干扰满足下列规则 The power supply shall compliance with the following Criterion:

(1)传导干扰度 Conduction Emission:

*EN55022,CLASS B *GB9254,CLASS B *FCC PART15 CLASS B

(2)辐射干扰度 Radiated Emission:

*EN55022,CLASS B *GB9254,CLASS B *FCC PART15 CLASS B

备注: 需配合用户电路整机通过上述规则 The power board should be assembled in customer’s product to test for passing the regulations。

4.2 电磁抗扰 EMS

电源电磁抗扰满足下列规则 The power supply shall compliance with the following Criterion:

(1) ESD	（静电抗扰度）	*GB17626.2-1998/1EC61000-4-2	
(2) EFT	（脉冲群抗扰度）	*GB17626.4-1998/1EC61000-4-4	3KV
(3) Surge	（雷击浪涌）	*GB17626.5-1998/1EC61000-4-5	1.5KV/3KV

5 工作环境 Environmental Requirement

5.1 环境温度 Temperature

* 工作环境 Operating Ambient: -5℃ to +50℃
* 储存环境 Non-operating Ambient: -10℃ to +80℃

5.2 环境湿度 Humidity

* 工作环境 Operating: From 10% to 90% relative humidity (non-condensing 无冷凝).
* 储存环境 Non-operating: From 5% to 95% relative humidity (non-condensing 无冷凝)

5.3 海拔高度 Altitude

* 工作环境 Operating: to 10,000 ft.
* 储存环境 Non-operating: to 20,000 ft

5.4 冷却方式 Cooling Method

* Ventilation cooling。 自然冷却

5.5 振动耐受 Vibration

* 10-55Hz, 19.6m/s2(2G), 3mintues period, 60mintues each along X,Y and Z axis.

5.6 冲击耐受

* 49m/s2(5G),11ms,once each X,Y and Z axis.

6 物理尺寸 Dimension

* 长(L)×宽(W)×高(H)：L190mm X W130mm X H26mm

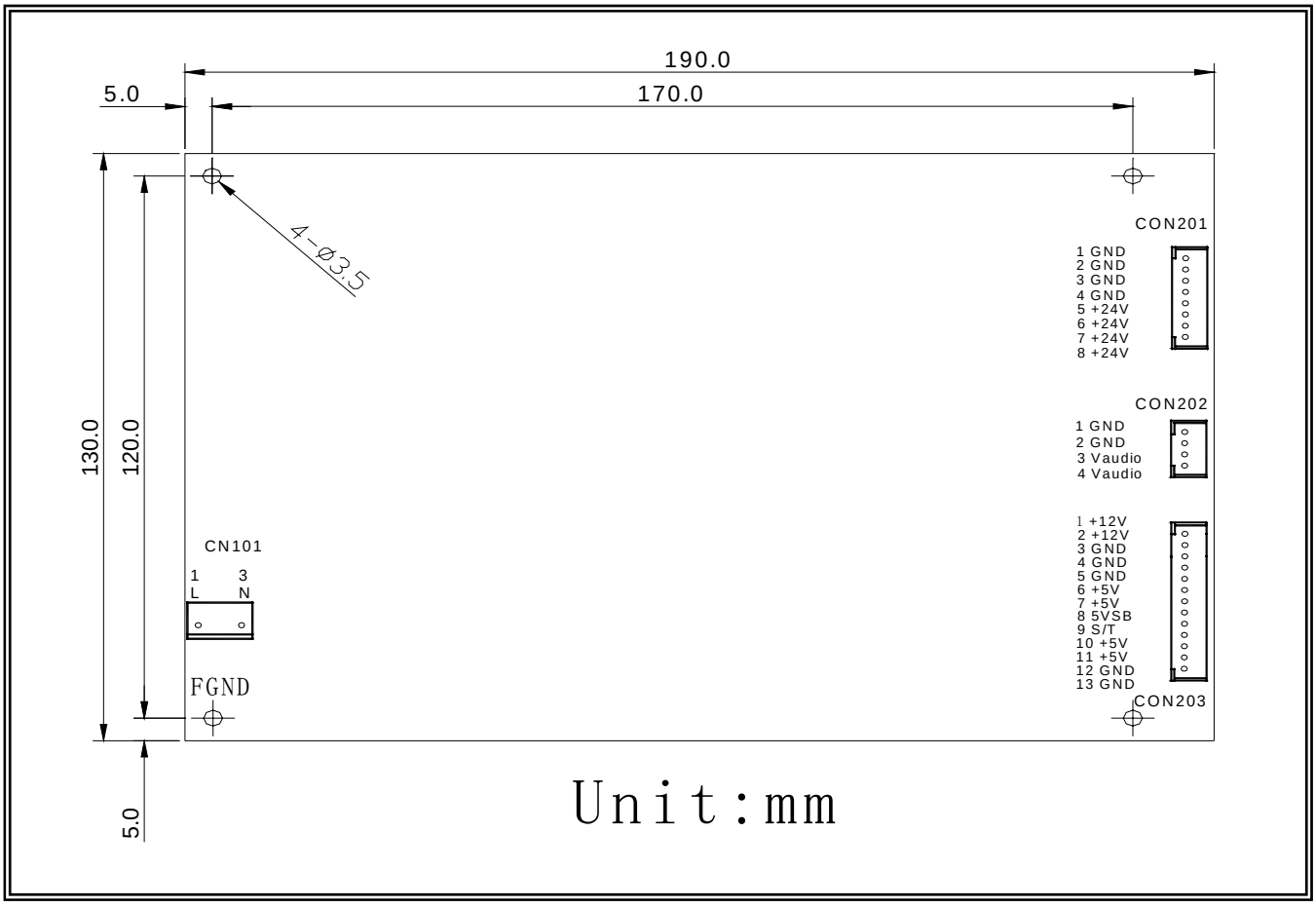
7 重量 Weight

* About650g/PC

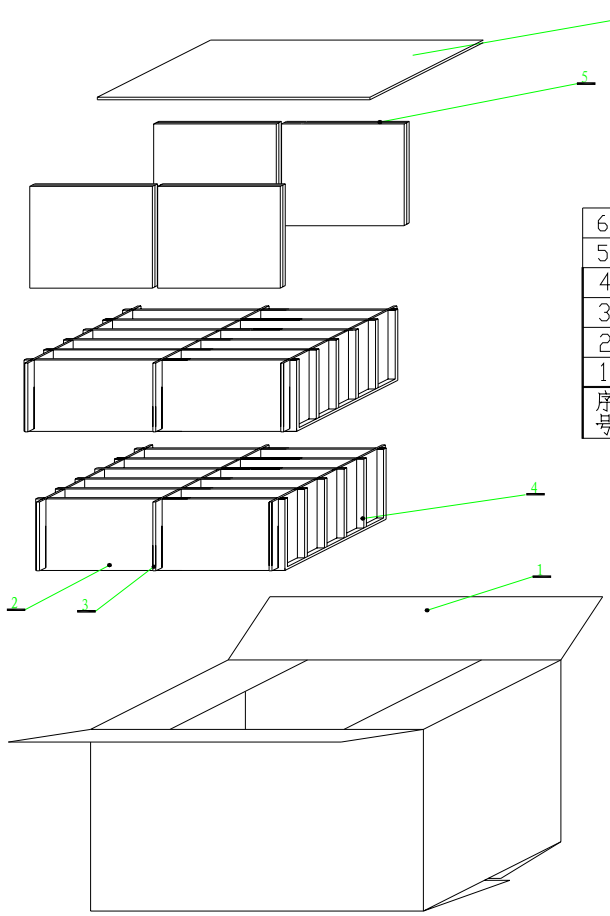
8 连接器脚位定义 Pin Connection

Connector NO.	Pin No.	Function
AC CON101	1	AC/L
	3	AC/N
DC CON201	1~4	GND
	5~8	24V
DC CON 202	1~2	GND
	3~4	Audio
DC CON 203	1~2	12V
	3~5，12~13	GND
	6~7，10~11	5V
	8	5VSB
	9	ON-OFF

9 安装尺寸 Power Supply Mounting

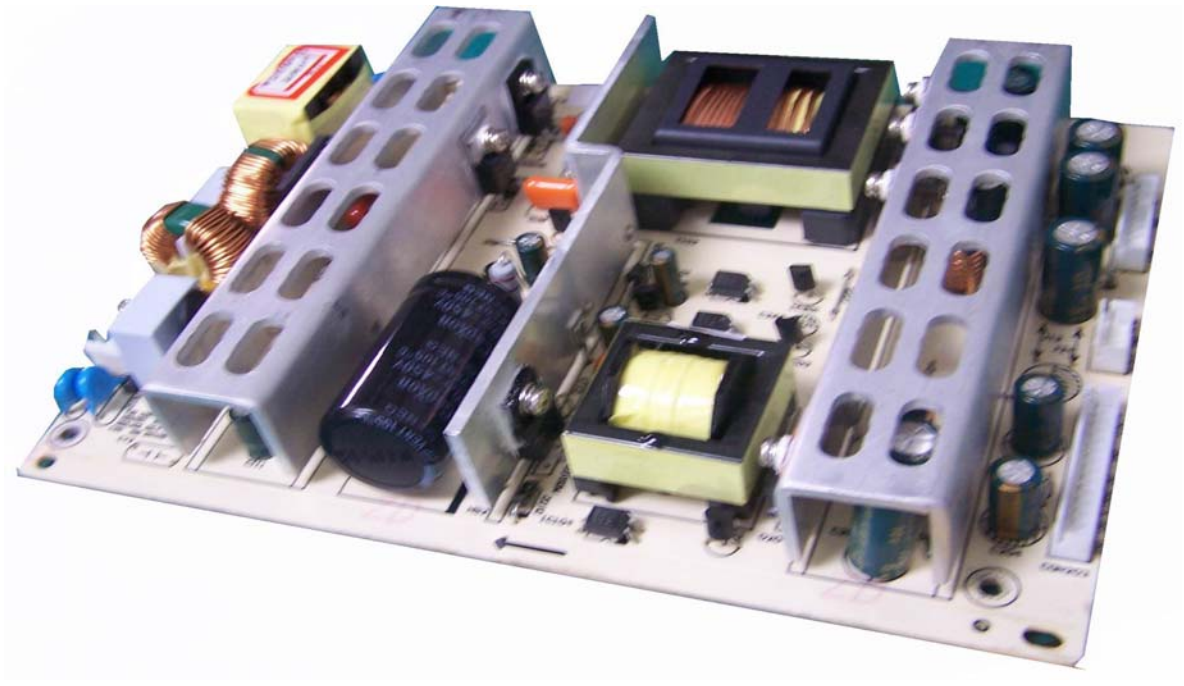


10 包装 Package



序号	代　　号	名　　称	数量	备　注
6		上盖板	1	1版
5		填充板	8	1版
4		横分隔板	8	1版
3		纵分隔板	6	1版
2		托　板	2	1版
1		纸　箱	1	1版

11 样机图片 Picture



1. General Description

This specification applies to the 26.0 inch Color TFT-LCD Module T260XW02 VQ. This LCD module has a TFT active matrix type liquid crystal panel 1366x768 pixels, and diagonal size of 26.0 inch. This module supports 1366x768 XGA-WIDE mode (Non-interlace).

Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot.

The T260XW02 VQ has been designed to apply the 8-bit 1 channel LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important. The T260XW02 VQ model is RoHS verified which can be distinguished on panel label.

* General Information

Items	Specification	Unit	Note
Active Screen Size	26.0	inches	
Display Area	575.769 (H) x 323.712(V)	mm	
Outline Dimension	626.0 (H) x 373.0 (V) x 45.0(D)	mm	With inverter
Driver Element	a-Si TFT active matrix		
Display Colors	16.7M	Colors	
Number of Pixels	1366 x 768	Pixel	
Pixel Pitch	0.4215	mm	
Pixel Arrangement	RGB vertical stripe		
Display Mode	Normally Black		
Surface Treatment	AG, Haze=11%, 3H		

2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

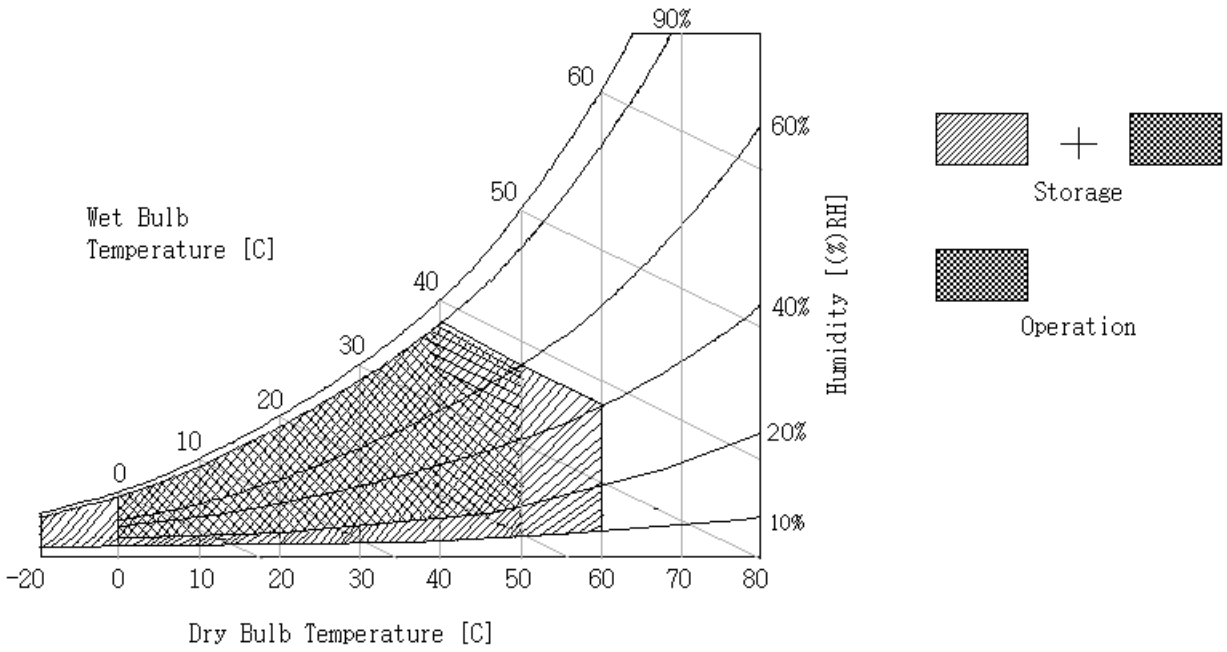
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{CC}	-0.3	13.2	[Volt]	Note 1
Input Voltage of Signal	V_{in}	-0.3	3.6	[Volt]	Note 1
BLU Input Voltage	VDDB	-0.3	27.0	[Volt]	Note 1
BLU Brightness Control Voltage	VDIM	-0.3	6.0	[Volt]	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3

Note 1: Duration = 1 sec

Note 2: Maximum Wet-Bulb should be 39℃ and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

Note 3: Surface temperature is measured at 50℃ Dry condition



3. Electrical Specification

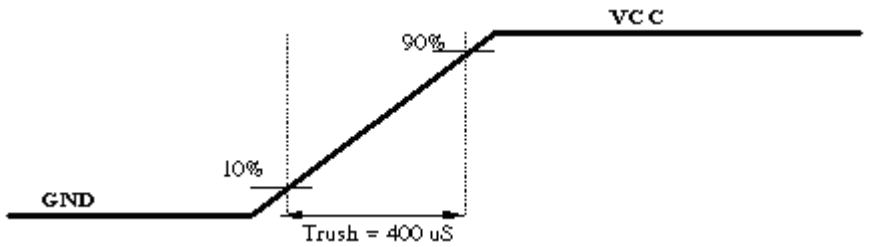
The T260XW02 VQ requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input power for the BLU is to power inverter.

3-1 Electrical Characteristics

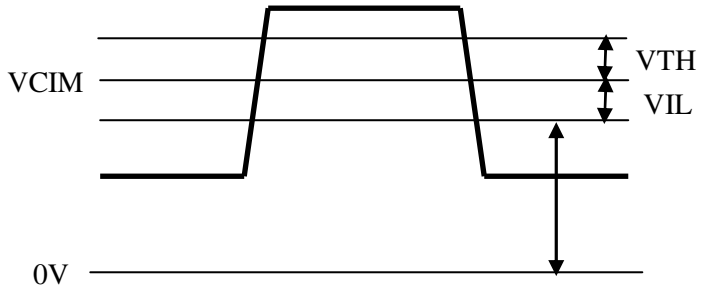
Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
LCD:							
Power Supply Input Voltage		Vcc	10.8	12	13.2	Vdc	1
Power Supply Input Current		Icc	-	0.35		A	2
Power Consumption		Pc	-	4.2		Watt	2
Inrush Current		I_{RUSH}	-	-	3.0	Apeak	3
LVDS Interface	Differential Input High Threshold Voltage	VTH			+100	mV	4
	Differential Input Low Threshold Voltage	VTL	-100			mV	4
	Common Input Voltage	VCIM	1.10	1.25	1.40	V	4
CMOS Interface	Input High Threshold Voltage	VIH (High)	2.4		3.3	Vdc	
	Input Low Threshold Voltage	VIL (Low)	0		0.7	Vdc	
Backlight Power Consumption		PDDB		40		Watt	8
Life Time			50,000	60,000		Hours	9

Note :

1. The ripple voltage should be controlled under 10% of V_{CC}
2. Vcc=12.0V, f_v =60Hz, fCLK=81.5Mhz , 25℃, Test Pattern : White Pattern
3. Measurement condition :



4. VCIM = 1.2V



5. The performance of the Lamp in LCM, for example life time or brightness, is extremely influenced by the characteristics of the DC-AC Inverter. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter. When you design or order the inverter, please make sure unwanted lighting caused by the mismatch of the lamp and the inverter (no lighting, flicker, etc) never occurs. When you confirm it, the LCD Assembly should be operated in the same condition as installed in your instrument.

6. Do not attach a conducting tape to lamp connecting wire. If the lamp wire attach to conducting tape, TFT-LCD Module have a low luminance and the inverter has abnormal action because leakage current occurs between lamp wire and conducting tape.

7. The relative humidity must not exceed 80% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃. When operate at low temperatures, the brightness of CCFL will drop and the life time of CCFL will be reduced.

3-2 Interface Connections

LCD connector (CN1): Starconn 093G30-B0001A-1

Pin No	Symbol	Description	Default
1	VCC	+12V, DC, Regulated	
2	VCC	+12V, DC, Regulated	
3	VCC	+12V, DC, Regulated	
4	VCC	+12V, DC, Regulated	
5	GND	Ground and Signal Return	
6	GND	Ground and Signal Return	
7	GND	Ground and Signal Return	
8	GND	Ground and Signal Return	
9	LVDS Option	Low/Open for Normal (NS), High for JEIDA	NS Mode
10	Reserved	Open or High	AUO internal test
11	GND	Ground and Signal Return for LVDS	
12	RIN0-	LVDS Channel 0 negative	
13	RIN0+	LVDS Channel 0 positive	
14	GND	Ground and Signal Return for LVDS	
15	RIN1-	LVDS Channel 1 negative	
16	RIN1+	LVDS Channel 1 positive	
17	GND	Ground and Signal Return for LVDS	
18	RIN2-	LVDS Channel 2 negative	
19	RIN2+	LVDS Channel 2 positive	
20	GND	Ground and Signal Return for LVDS	
21	RCLK-	LVDS Clock negative	
22	RCLK+	LVDS Clock positive	
23	GND	Ground and Signal Return for LVDS	
24	RIN3-	LVDS Channel 3 negative	
25	RIN3+	LVDS Channel 3 positive	
26	GND	Ground and Signal Return for LVDS	
27	Reserved	Open or High	AUO internal test
28	Reserved	Open or High	AUO internal test
29	GND	Ground and Signal Return	
30	GND	Ground and Signal Return	

Note:

1. All GND (ground) pins should be connected together and should also be connected to the LCD's metal frame.
2. All Vcc (power input) pins should be connected together.

3-3 Signal Timing Specifications

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

* Timing Table

DE only Mode
Vertical Frequency

Signal	Item	Symbol	Min	Type	Max	Unit
Vertical Section	Period	Tv	776	810	1015	Th
	Active	Tdisp (v)		768		Th
	Blanking	Tblk (v)	8	42	247	Th
Horizontal Section	Period	Th	1414	1648	2000	Tclk
	Active	Tdisp (h)		1366		Tclk
	Blanking	Tblk (h)	48	282	634	Tclk
LVDS Clock	Frequency	1/Tclk	50	80	86	MHz
Vertical Frequency	Frequency	Freq	47	60	63	Hz
Horizontal Frequency	Frequency	Freq	43	48	53	KHz

Notes:
1) Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.
Vertical display position is specified by the rise of DE after a “Low” level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise the of 1st DE is displayed at the top line of screen.
2) If a period of DE “High” is less than 1366 DCLK or less than 768 lines, the rest of the screen displays black.
3) The display position does not fit to the screen if a period of DE “High” and the effective data period do not synchronize with each other.

3-7 Backlight Power Specification for LCD Module

3.7.1 Electrical specification

(Ta=25±5℃)

No	ITEM	SYMBOL		CONDITION	MIN	TYP	MAX	UNIT	Note
1	**Input Voltage**	VDDB		---	21.6	24.0	26.4	VDC	
2	**Input Current**	IDDB		VDDB=24V VDIM=3.3V	1.59	1.67	1.75	ADC	1
3	**Input Power**	PDDB		VDDB=24V VDIM=3.3V	38	40	42	W	1
4	**Inrush current**	IRUSH		VDDB=24V VDIM=3.3V	---	---	6	ADC	1,2
6	**ON/OFF Control Voltage**	VBLON	ON	VDDB=24V	2.0	3.3	5.0	VDC	
			OFF	VDDB=24V	0.0	---	0.8		
7	**ON/OFF Control Current**	IBLON		VDDB=24V	-1	---	1.5	mADC	
8	**Dimming Control Voltage**	VDIM	MAX	VDDB=24V	---	3.3	---	VDC	
			MIN	VDDB=24V	---	0.0	---		
9	**Dimming Control Current**	I_DIM	MIN	VDDB=24V	---	---	1.5	mADC	
10	**Internal Dimming Ratio**	DIM_R		---	20		100	%	
11	**PWM Function**	V_PWM	MAX	---	2	---	3.3	VDC	
			MIN	---	0	---	0.8		
12	**External PWM Control Current**	I_EPWM		---	---	---	2	mADC	
13	**External PWM Ratio (Duty)**	D_EPWM		---	10	---	100	%	3
14	**External PWM Frequency**	F_EPWM		---	140	---	240	Hz	

Note 1 : Condition: VDDB=24V (Ta=25±5℃, Turn on for 45minutes), PWM=100%

Note 2 : Measurement condition Rising time = 20 ms (VDDB : 10%~90%)

Note 3 : (a) Uniformity and flicker do not guarantee below 20% dimming control;

(b) 10% dimming control is function okay and no backlight shut down.

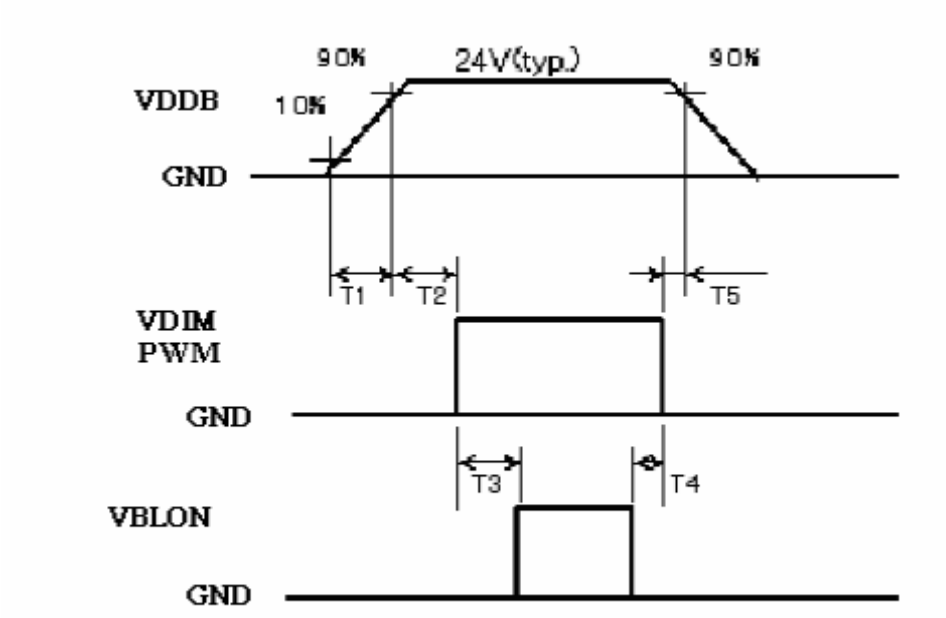
3.7.2 Input Pin Assignment

CN1: CI0114M1HRL-LF (Cvilux)

Pin No	Symbol	Description	Default
Pin No	Symbol	Description	
1	VDDB(main power)	DC input 24V VDC	24V
2	VDDB(main power)	DC input 24V VDC	24V
3	VDDB(main power)	DC input 24V VDC	24V
4	VDDB(main power)	DC input 24V VDC	24V
5	VDDB(main power)	DC input 24V VDC	24V
6	GND	Ground	GND
7	GND	Ground	GND
8	GND	Ground	GND
9	GND	Ground	GND
10	GND	Ground	GND
11	DET	Inverter OK: Low/GND (0-0.8V) Inverter NG: Open collector	-
12	VBLON	BL on-off : Open/High (3.3V) for BL ON, Low(GND) for BL OFF	-
13	ADIM	Internal PWM : 0V=20% ; 3.3V=100% ; OPEN=100% < NC ; When External PWM >	-
14	PDIM	External PWM (10%～100%) < NC ; When Internal PWM >	-

Note: Pin13 and Pin14 can't be used at the same time!

3.7.3 Power Sequence for Inverter

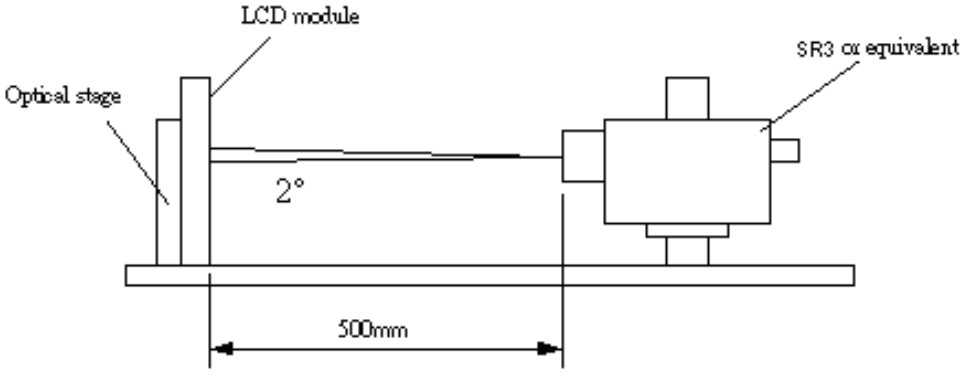


Parameter	Values			Units
	Min.	Typ.	Max.	
T1	20	-	-	ms
T2	10	-	-	ms
T3	0	-	-	ms
T4	50	-	-	ms
T5	0	-	-	ms

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0°. Signal generator used for measurement is "Chroma 2913" and signal setting follows the typical value shown in page 13 with vertical frequency range A (fv=60Hz). Meanwhile, dimmer is 3.3(V) for its maximum setting.

Fig.1 1 presents additional information concerning the measurement equipment and method.



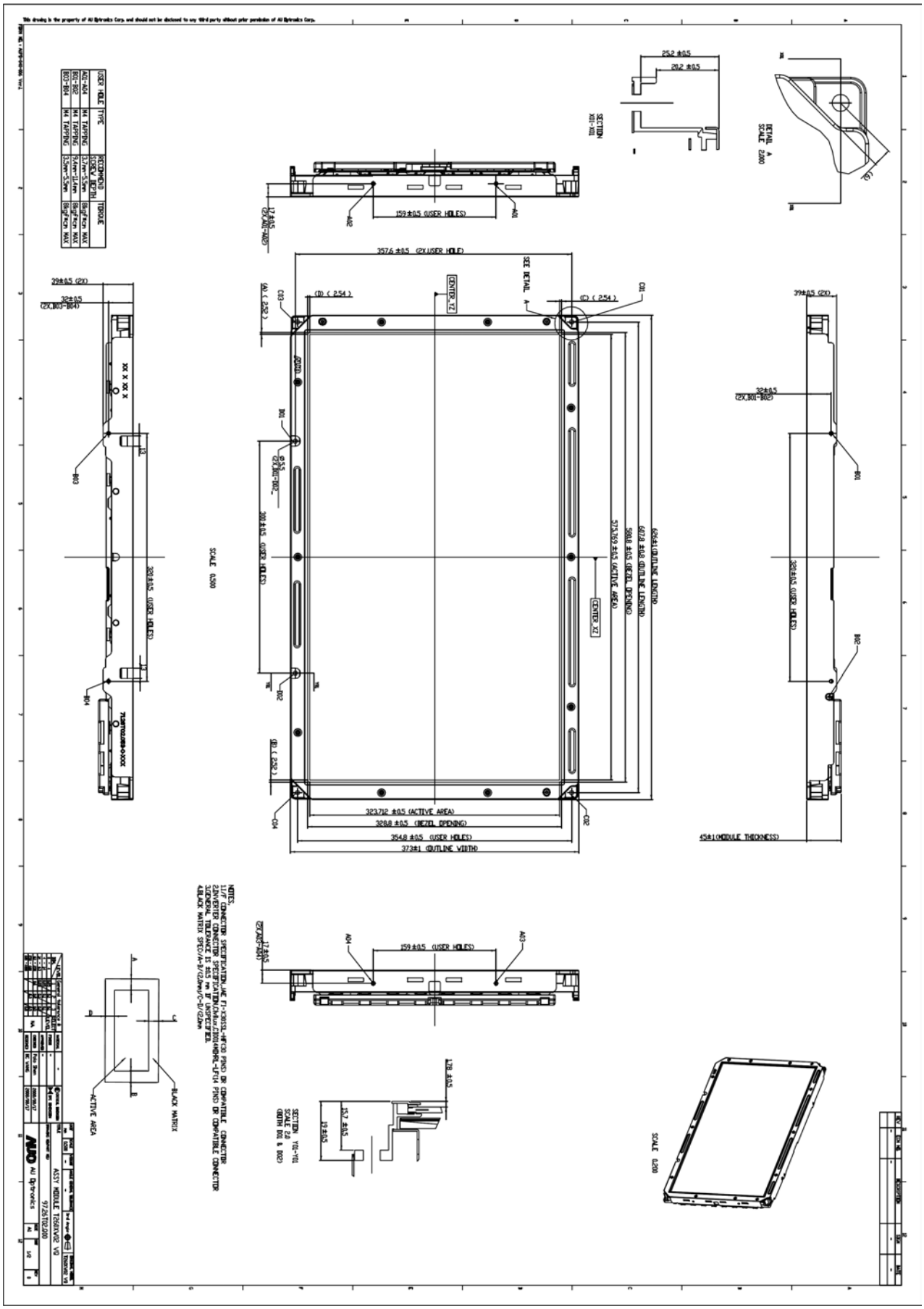
Parameter		Symbol	Values			Units	Notes
			Min.	Typ.	Max.		
Contrast Ratio		CR	2400	3000			1
Surface Luminance, white		LWH	360	450		cd/㎡	2
Luminance Variation		δ_{WHITE} | 9 p			1.3		3
Response Time (G to G)		Ty		6.5		ms	4
Color Gamut		NTSC		72		%	
Color Coordinates							
	RED	R_X	Typ.-0.03	0.64	Typ.+0.03		
		R_Y		0.33			
	GREEN	G_X		0.28			
		G_Y		0.59			
	BLUE	B_X		0.15			
		B_Y		0.05			
	WHITE	W_X		0.28			
		W_Y		0.29			
Viewing Angle							
	x axis, right(φ=0°)	θ_r		89		Degree	6
	x axis, left(φ=180°)	θ_l		89		Degree	
	y axis, up(φ=90°)	θ_u		89		Degree	
	y axis, down (φ=0°)	θ_d		89		Degree	

5. Mechanical Characteristics

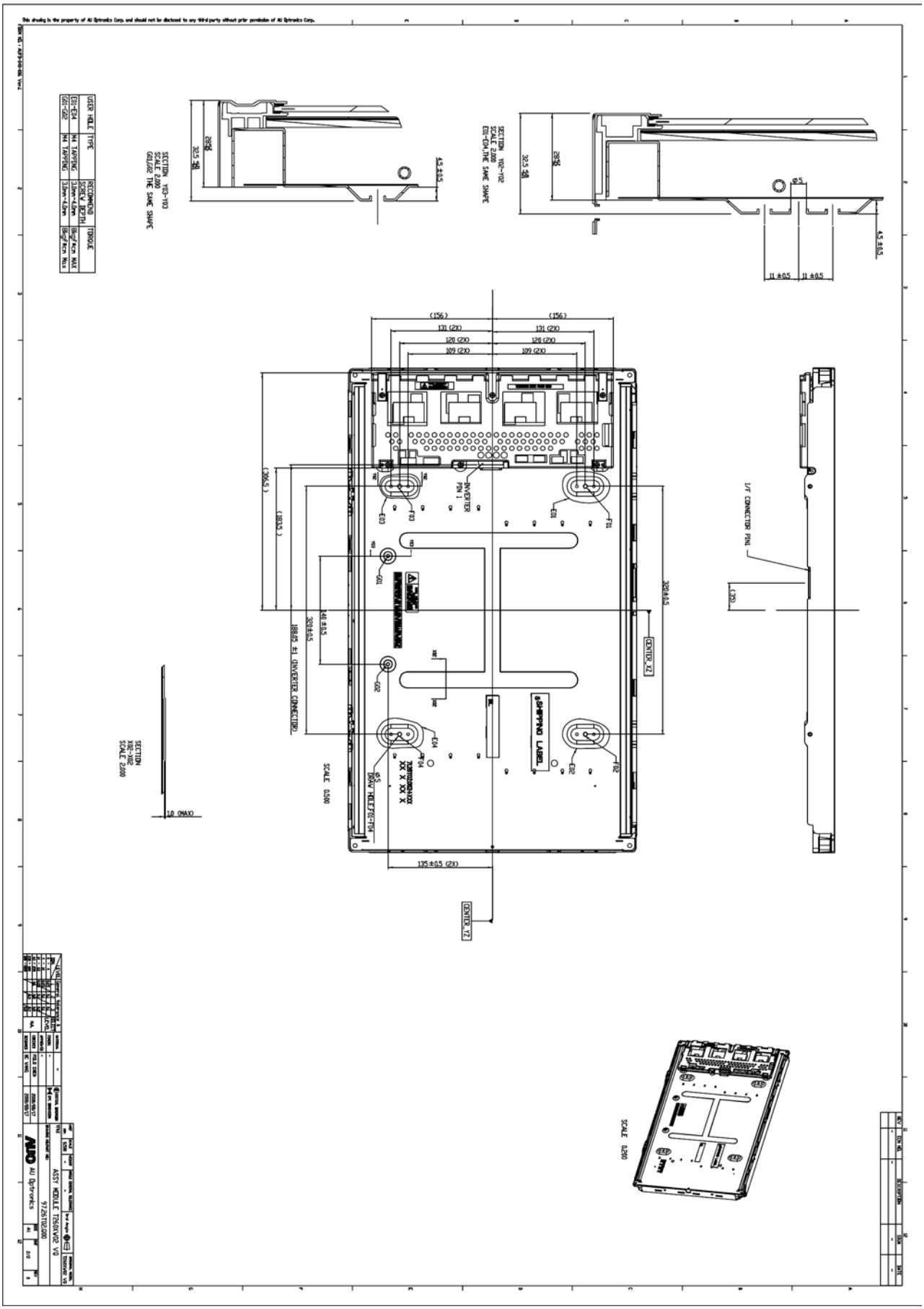
The contents provide general mechanical characteristics for the model T260XW02 VQ. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	626.0mm
	Vertical	373.0mm
	Depth	45.0mm(w/ inverter & shielding) 39.0mm(w/o inverter)
Bezel Area	Horizontal	580.8mm±0.5mm
	Vertical	328.8mm±0.5mm
Active Display Area	Horizontal	575.769mm
	Vertical	323.712mm
Weight	3750g (Typ.)	
Surface Treatment	AG, Haze=11%, 3H	

Front View



Rear View



1. General Description

This specification applies to the 31.51 inch Color TFT-LCD Module T315XW02 VS. This LCD module has a TFT active matrix type liquid crystal panel 1366x768 pixels, and diagonal size of 31.51 inch. This module supports 1366x768 XGA-WIDE mode (Non-interlace).

Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot.

The T315XW02 VS has been designed to apply the 8-bit 1 channel LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important.

The T315XW02 VS model is RoHS verified which can be distinguished on panel label.

* General Information

Items	Specification	Unit	Note
Active Screen Size	31.51 inches		
Display Area	697.685 (H) x 392.256(V)	mm	
Outline Dimension	760.0(H) x 450.0(V) x 45(D)	mm	With Inverter
Driver Element	a-Si TFT active matrix		
Display Colors	16.7M	Colors	
Number of Pixels	1366 x 768	Pixel	
Pixel Pitch	0.51075	mm	
Pixel Arrangement	RGB vertical stripe		
Display Mode	Normally Black		
Surface Treatment	Anti-Glare, 3H		Haze =11%

2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause permanent damage to the unit.

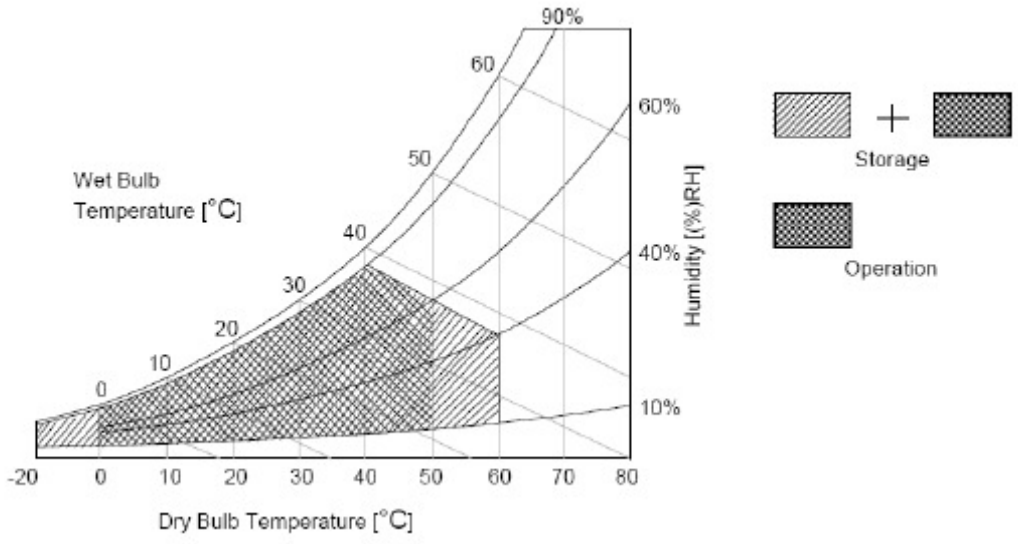
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vcc	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	Vin	-0.3	3.6	[Volt]	Note 1
BLU Input Voltage	VDDB	-0.3	28	[Volt]	Note 1
BLU Brightness Control Voltage	Vdim	-0.3	7.0	[Volt]	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3

Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39℃ and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

Note 3 : Surface temperature is measured at 50℃ Dry condition



3. Electrical Specification

The T315XW02 VS requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input power for the BLU, is to power inverter..

3-1 Electrical Characteristics

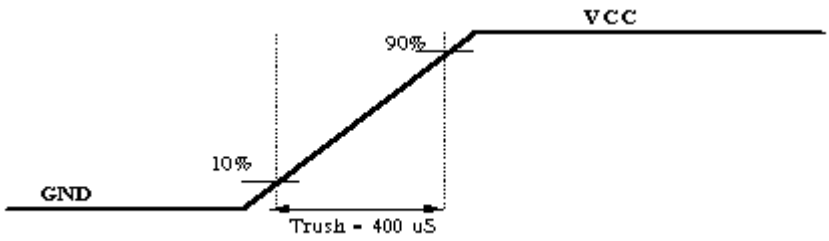
Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
LCD:							
Power Supply Input Voltage		Vcc	10.8	12	13.2	Vdc	1
Power Supply Input Current		Icc	-	0.45	0.55	A	2
Power Consumption		Pc	-	5.4	7.26	Watt	2
Inrush Current		I_{RUSH}	-	-	6	Apeak	3
LVDS Interface	Differential Input High Threshold Voltage	VTH	-	-	100	mV	4
	Differential Input Low Threshold Voltage	VTL	-100	-	-	mV	4
	Common Input Voltage	VCIM	1.10	1.25	1.40	V	4
CMOS Interface	Input High Threshold Voltage	VIH (High)	2.4		3.3	Vdc	
	Input Low Threshold Voltage	VIL (Low)	0		0.7	Vdc	
Life Time			50,000			Hours	5,6,7,8

Note :

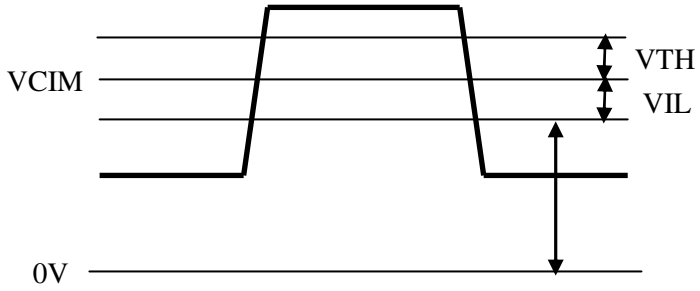
1. The ripple voltage should be controlled under 10% of V_{CC}

2. Vcc=12.0V, f_v =60Hz, fCLK=81.5Mhz , 25℃, Test Pattern : White Pattern

3. Measurement condition :



4. VCIM = 1.2V



5. The performance of the Lamp in LCD panel, for example life time or brightness, is extremely influenced by the characteristics of the DC-AC Inverter. So all the parameters of an inverter should be carefully designed as not to produce too much leakage current from high-voltage output of the inverter. When you design or order the inverter, please make sure unwanted lighting caused by the mismatch of the lamp and the inverter (no lighting, flicker, etc) never occurs. After confirmation, the LCD panel should be operated in the same condition as installed in your instrument.

6. Do not attach a conducting tape to lamp connecting wire. If the lamp wire attach to conducting tape, TFT-LCD Module have a low luminance and the inverter has abnormal action because leakage current occurs between lamp wire and conducting tape.

7. The relative humidity must not exceed 80% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃. When operate at low temperatures, the brightness of CCFL will drop and the life time of CCFL will be reduced.

8. Specified values are for a single lamp only which is aligned horizontally. The lifetime is defined as the time which luminance of the lamp is 50% compared to its original value.
[Operating condition: Continuous operating at Ta = 25±2℃]

3-2 Interface Connections

- Connector on Panel: **093G30-B0001A-1** (Manufactured by Starconn)

Pin No	Symbol	Description	Default
1	VCC	+12V, DC, Regulated	
2	VCC	+12V, DC, Regulated	
3	VCC	+12V, DC, Regulated	
4	VCC	+12V, DC, Regulated	
5	GND	Ground and Signal Return	
6	GND	Ground and Signal Return	
7	GND	Ground and Signal Return	
8	GND	Ground and Signal Return	
9	LVDS Option	Low/Open for Normal (NS), High for JEIDA	NS mode
10	Reserved	Open	AUO internal test
11	GND	Ground and Signal Return for LVDS	
12	RIN0-	LVDS Channel 0 negative	
13	RIN0+	LVDS Channel 0 positive	
14	GND	Ground and Signal Return for LVDS	
15	RIN1-	LVDS Channel 1 negative	
16	RIN1+	LVDS Channel 1 positive	
17	GND	Ground and Signal Return for LVDS	
18	RIN2-	LVDS Channel 2 negative	
19	RIN2+	LVDS Channel 2 positive	
20	GND	Ground and Signal Return for LVDS	
21	RCLK-	LVDS Clock negative	
22	RCLK+	LVDS Clock positive	
23	GND	Ground and Signal Return for LVDS	
24	RIN3-	LVDS Channel 3 negative	
25	RIN3+	LVDS Channel 3 positive	
26	GND	Ground and Signal Return for LVDS	
27	Reserved	Open or High	AUO internal test
28	Reserved	Open or High	AUO internal test
29	GND	Ground and Signal Return	
30	GND	Ground and Signal Return	

Note:

1. All GND (ground) pins should be connected together and should also be connected to the LCD's metal frame. All Vcc (power input) pins should be connected together.
2. For Pin 10, 27 and 28, panel will not damage if negligently connect these pins to high or low

BACKLIGHT CONNECTOR PIN CONFIGURATION

1. Electrical specification

Item	Symb.		Condition	Spec			Unit	Note
				Min	Typ	Max		
Input Voltage	VDDB		---	21.6	24.0	26.4	VDC	
Input Current (Turn on Condition)	IDDB		VDDB=24V	--	--	--	ADC	
Input Power (Turn on Condition)	PDDB		VDDB=24V	--	--	--	W	
Input Current (Stable on Condition)	IDDB		VDDB=24V	2.04	2.29	2.54	ADC	
Input Power (Stable on Condition)	PDDB		VDDB=24V	49.0	55.0	61.0	W	
Inrush Current	IRUSH		VDDB=24V	---	---	6.0	ADC	1
On/Off Control Voltage	VBLON	ON	VDDB=24V	2.0	---	5.0	VDC	
		OFF	VDDB=24V	0.0	---	0.8		
On/Off Control Current	IBLON		VDDB=24V	0.0	---	1.5	mADC	
Dimming Control Voltage	VDIM	MAX	VDDB=24V	---	3.3	---	VDC	2
		MIN	VDDB=24V	---	0.0	---		
Dimming Control Current	I_DIM	MIN	VDDB=24V	---	---	1.5	mADC	
PWM Function	V_PWM	MAX	---	2.0	---	5.0	VDC	
		MIN	---	0.0	---	0.8		
External PWM Control Current	I_EPWM		---	---	---	1.5	mADC	
External PWM Duty Ratio	D_EPWM		---	10	---	100	%	3
External PWM Frequency	F_EPWM		---	120	180	240	Hz	

Note 1 : Measurement condition Rising time = 20 ms (VDDB : 10%~90%);

Note 2 : VDIM= 3.3V (MAX, 100% brightness), VDIM= 0V (MIN, 10% brightness) （Ta=25±5℃, Turn on for 45minutes）

Note 3 : (a) Uniformity and flicker does not guarantee under 20% dimming control.
(b) 10% dimming function okay and no backlight shut down

2. Input specification

CN1: CI0114M1HRL-LF (Manufactured by Civilux)

Pin No	Symbol	Description
1	VDDB (Main Power)	DV input 24.0 VDC
2	VDDB (Main Power)	DV input 24.0 VDC
3	VDDB (Main Power)	DV input 24.0 VDC
4	VDDB (Main Power)	DV input 24.0 VDC
5	VDDB (Main Power)	DV input 24.0 VDC
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	DET Function	Panel status detect (Normal=0~ 0.8V, Abnormal=Open collector)
12	VBLON (Enable Pin)	BL On/Off control signal High/Open: On, Low: Off (Low=0~ 0.8V, High=2.0~5.0V)
13	VDIM	Internal PWM (3.3V,100% duty)for 100% < NC ; when External PWM >
14	PDIM	External PWM input (AC 0~3.3V, Duty: 10%~100%) < NC ; when Internal PWM >

3-3 Signal Timing Specifications

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications for it's proper operation.

* Timing Table

DE only Mode

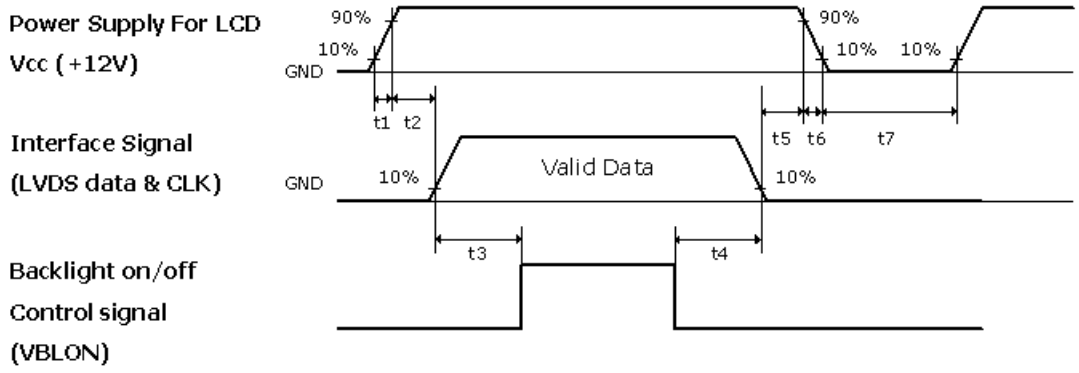
Vertical Frequency:

Signal	Item	Symbol	Min	Type	Max	Unit
Vertical Section	Period	Tv	776	810	1015	Th
	Active	Tdisp (v)		768		Th
	Blanking	Tblk (v)	8	42	247	Th
Horizontal Section	Period	Th	1414	1648	2000	Tclk
	Active	Tdisp (h)		1366		Tclk
	Blanking	Tblk (h)	48	282	634	Tclk
LVDS Clock	Frequency	1/Tclk	50	80	86	MHz
Vertical Frequency	Frequency	Freq	47	60	63	Hz
Horizontal Frequency	Frequency	Freq	43	48	53	KHz

Notes:
1.) Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.
Vertical display position is specified by the rise of DE after a "Low" level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise the of 1st DE is displayed at the top line of screen.
2.) If a period of DE "High" is less than 1366 DCLK or less than 768 lines, the rest of the screen displays black.
3.) The display position does not fit to the screen if a period of DE "High" and the effective data period do not synchronize with each other.

3-6 Power Sequence for LCD Module

3.6.1 Power Sequence for LCD



Parameter	Values			Units
	Min.	Typ.	Max.	
t1	0.4	-	30	ms
t2	0.1	-	50	ms
t3	200	-	-	ms
t4	10	-	-	ms
t5	0.1	-	50	ms
t6		-	300	ms
t7	500	-	-	ms

Note:

The timing controller will not be damaged in case of TV set AC input power suddenly shut down.

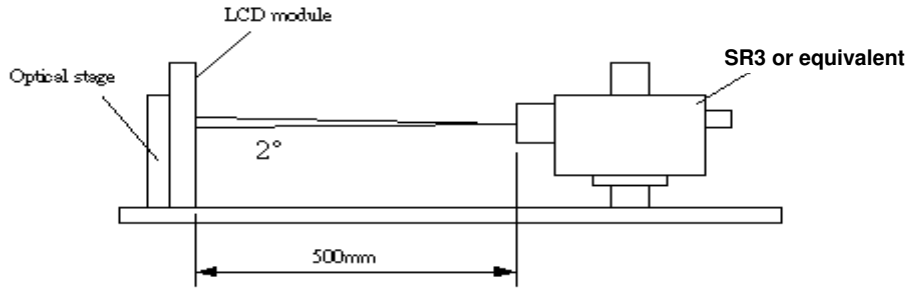
Once power reset, it should follow power sequence as spec. definition.

(1) Apply the lamp voltage within the LCD operation range. When the back-light turns on before the LCD operation or the LCD turns off before the back-light turns off, the display may momentarily become abnormal screen.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θequal to 0°.

Fig.1 1 presents additional information concerning the measurement equipment and method.



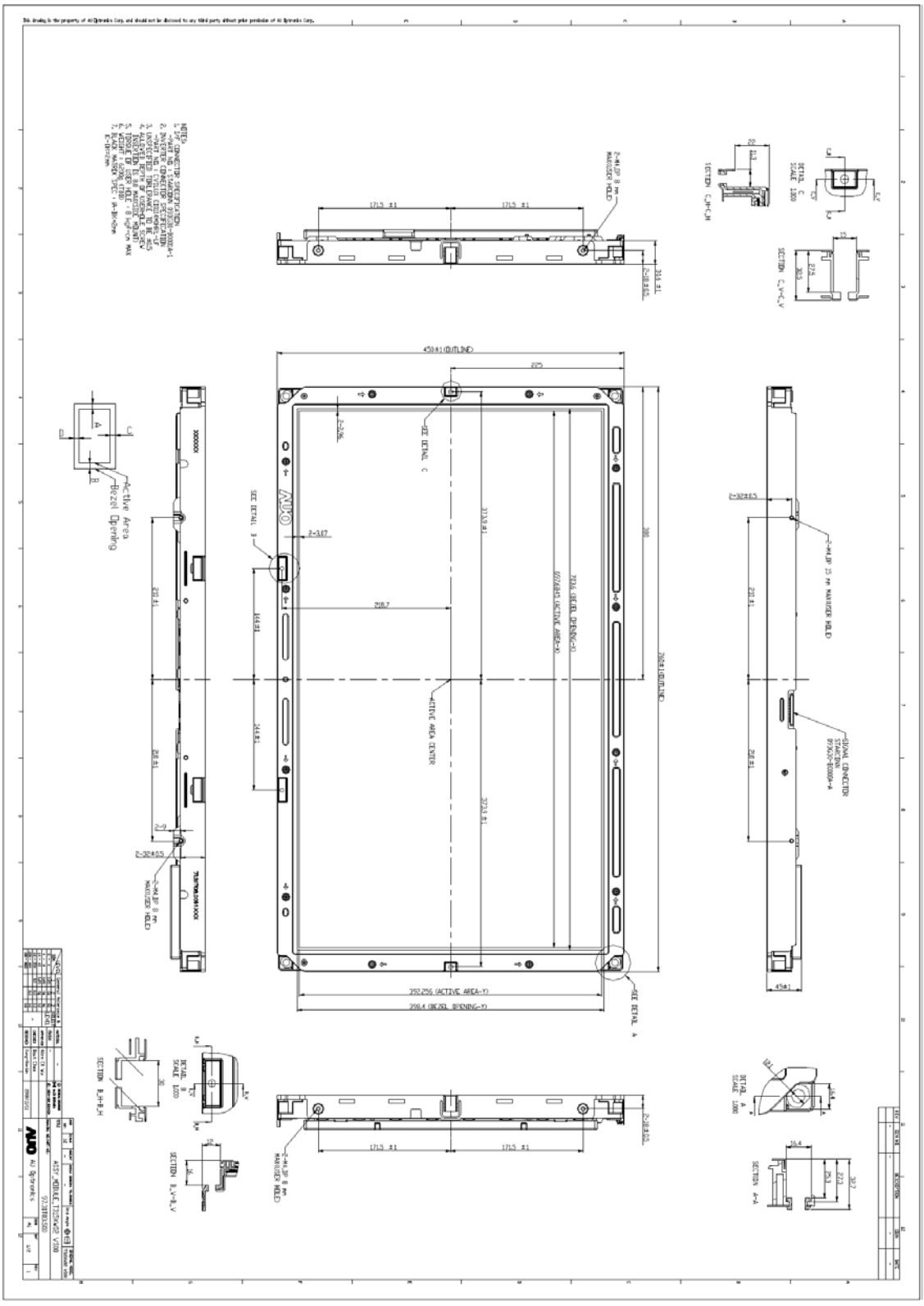
Parameter		Symbol	Values			Units	Notes
			Min.	Typ.	Max.		
Contrast Ratio		CR	2400	3000			1
Surface Luminance, white		LWH	360	450		cd/㎡	2
Luminance Variation		δ_{WHITE} 9 p			1.30		3
G to G Response time		Tγ		6.5		ms	4
Color Gamut		NTSC		72		%	
Color Coordinates							
	RED	R_X	Typ.-0.03	0.64	Typ.+0.03		
		R_Y		0.33			
	GREEN	G_X		0.28			
		G_Y		0.60			
	BLUE	B_X		0.15			
		B_Y		0.05			
	WHITE	W_X		0.28			
		W_Y		0.29			
Viewing Angle							
x axis, right(φ=0°)		θ_r		89		Degree	6
x axis, left(φ=180°)		θ_l		89			
y axis, up(φ=90°)		θ_u		89			
y axis, down (φ=0°)		θ_d		89			

5. Mechanical Characteristics

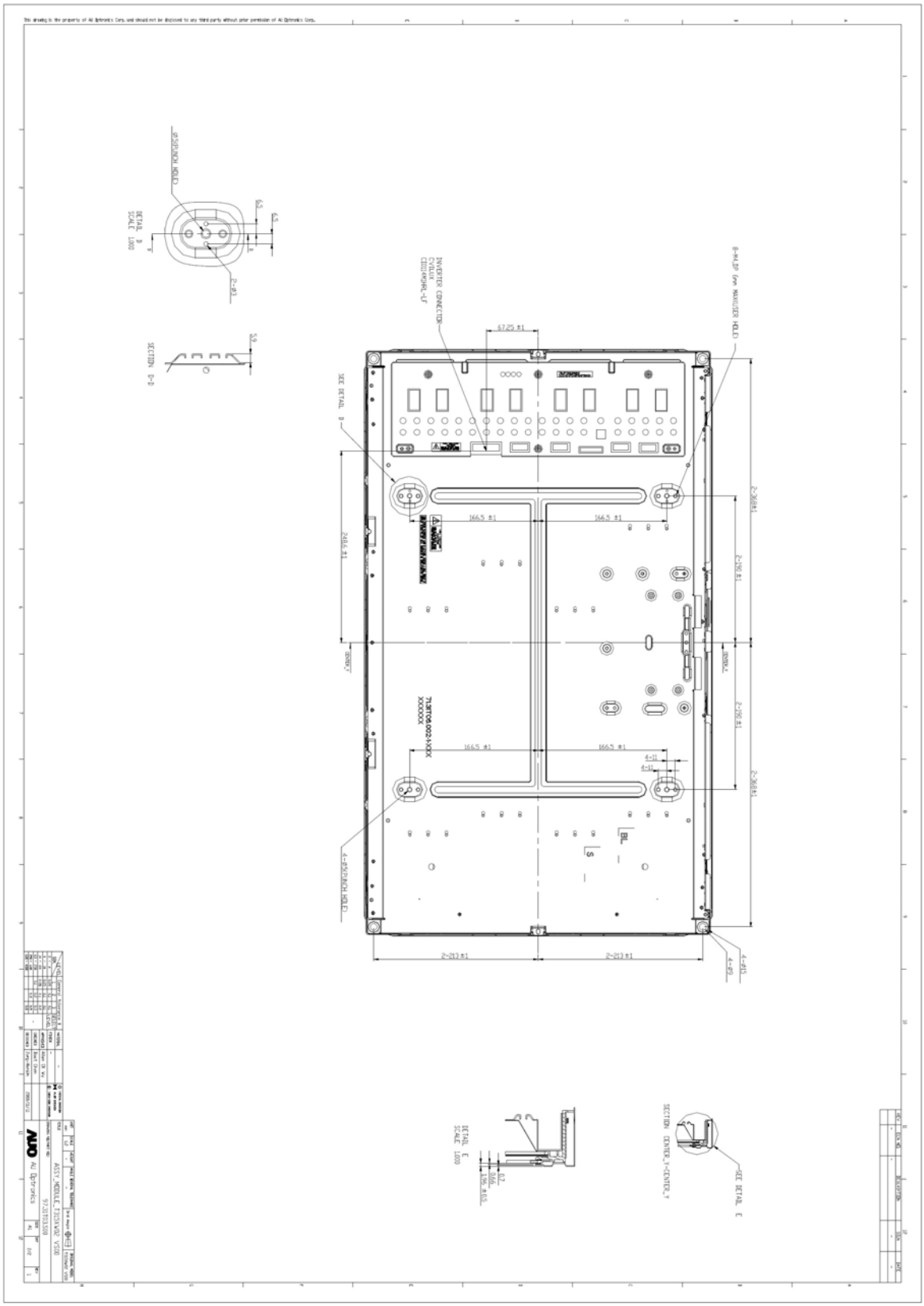
The contents provide general mechanical characteristics for the model T315XW02 VS. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	760.0mm
	Vertical	450.0mm
	Depth	45mm
Bezel Opening	Horizontal	703.6mm
	Vertical	398.3mm
Active Display Area	Horizontal	697.685mm
	Vertical	392.256mm
Weight	6000g Typ.	
Surface Treatment	AG, 3H	

Front:



Back:



1. General Description

This specification applies to the 42 inch Color TFT-LCD Module T420HW04 V2. This LCD module has a TFT active matrix type liquid crystal panel 1920x1080 pixels, and diagonal size of 42 inch. This module supports 1920x1080 Full-HD mode (Non-interlace).

Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot.

The T420HW04 V2 has been designed to apply the 8-bit 2 channel LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth.

* General Information

Items	Specification	Unit	Note
Active Screen Size	42.02	inches	
Display Area	930.24(H) x 523.26(V)	mm	
Outline Dimension	983.0(H) x 576.0(V) x 52.5(D)	mm	With inverter
Driver Element	a-Si TFT active matrix		
Display Colors	16.7M	Colors	
Number of Pixels	1920 x 1080	Pixel	
Pixel Pitch	0.4845	mm	
Pixel Arrangement	RGB vertical stripe		
Display Mode	Normally Black		
Lamp quantity, type	16pcs, Straight type	pcs	
Surface Treatment	Anti-Glare coating (Haze 11%) Hard coating (3H)		

2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Item	Symbol	Min	Max	Unit	Note
Power Supply Input Voltage	VDD	-0.3	14	[Volt]	1
Logic Input Voltage	Vin	-0.3	3.6	[Volt]	1
BLU Input Voltage	VDDB	-0.3	26.4	[Volt]	1
BLU Brightness Control Voltage	BLON	-0.3	3.6	[Volt]	1
Ambient Operating Temperature	TOP	0	+50	[°C]	2
Ambient Operating Humidity	HOP	10	80	[%RH]	2
Storage Temperature	TST	-10	+60	[°C]	2
Storage Humidity	HST	10	80	[%RH]	2
Shock (non-operation)		-	50	G	3
Vibration (non-operation)		-	1.5	G	4
Thermal shock		-20	60	C	5

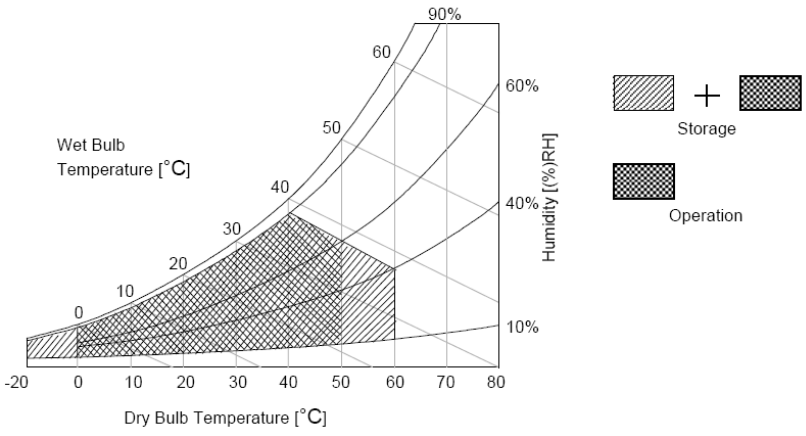
Note 1 : Duration = 50msec

Note 2 : Maximum Wet-Bulb should be 50℃ and No condensation.

Note 3 : Half sine wave, shock level : 50G(11ms), direction : ±x, ±y, ±z (one time each direction)

Note 4 : Wave form : Random, vibration level : 1.5G RMS, Bandwidth : 10~500Hz
Duration : X,Y,Z 30min (one time each direction)

Note 5 : -20C/1hr ~ 60C/1hr, 100 cycles



3. Electrical Specification

The T420HW04 requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input, which powers the CCFL, is typically generated by an inverter.

3-1 Electrical Characteristics

Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
LCD:							
Power Supply Input Voltage		Vdd	10.8	12	13.2	Vdc	
Power Supply Input Current		Idd	-	1		A	1
Power Consumption		Pc	-	12		Watt	1
Inrush Current		I_{RUSH}	-	-	4	A	5
LVDS Interface	Differential Input High Threshold Voltage	V_{TH}			+100	mV	4
	Differential Input Low Threshold Voltage	V_{TL}	-100			mV	4
	Common Input Voltage	V_{CIM}	0.6	1.2	1.8	V	
CMOS Interface	Input High Threshold Voltage	V_{IH} (High)	2.0		3.3	Vdc	
	Input Low Threshold Voltage	V_{IL} (Low)	0		0.8	Vdc	
Backlight Power Consumption						Watt	2
Life Time			50000			Hours	3

The performance of the Lamp in LCM, for example life time or brightness, is extremely influenced by the characteristics of the DC-AC Inverter. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter. When you design or order the inverter, please make sure unwanted lighting caused by the mismatch of the lamp and the inverter (no lighting, flicker, etc) never occurs. When you confirm it, the LCD Assembly should be operated in the same condition as installed in your instrument.

Do not attach a conducting tape to lamp connecting wire. If the lamp wire attach to conducting tape, TFT-LCD Module have a low luminance and the inverter has abnormal action because leakage current occurs between lamp wire and conducting tape.

The relative humidity must not exceed 80% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃. When operate at low temperatures, the brightness of CCFL will drop and the lifetime of CCFL will be reduced.

Note :

1. Vdd=12.0V, fv=60Hz, f_{CLK}=80 Mhz , 25℃, Vdd Duration time= 470 μs , Test pattern : white pattern
2. The Backlight power consumption shown above does include loss of external inverter at 25℃. The used lamp current is the lamp typical current
3. The life is determined as the time at which luminance of the lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operating at 25±2℃.
4. VCIM = 1.2V

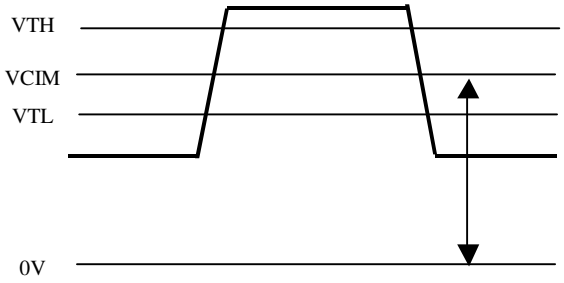
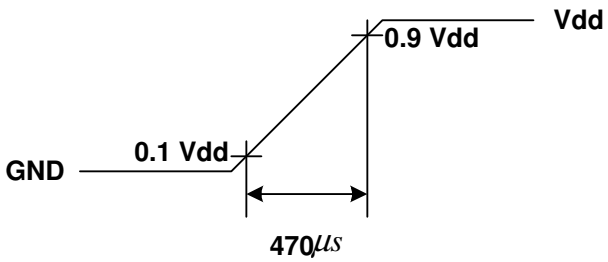


Figure : LVDS Differential Voltage

5. Measurement Condition: Rising time = 470 μ s



3-2 Interface Connections

- LCD connector: P-TWO 187059-5122 which is compatible FI-RE51S-HF (JAE)

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	27	GND	Ground
2	NC	No connection	28	RE0N	SECOND CHANNEL 0-
3	NC	No connection	29	RE0P	SECOND CHANNEL 0+
4	NC	No connection	30	RE1N	SECOND CHANNEL 1-
5	NC	No connection	31	RE1P	SECOND CHANNEL 1+
6	Reserved		32	RE 2N	SECOND CHANNEL 2-
7	LVDS SEL	LVDS order	33	RE 2P	SECOND CHANNEL 2+
8	NC	No connection	34	GND	Ground
9	Reserved		35	RECLKN	SECOND CLOCK CHANNEL C-
10	Reserved		36	RECLKP	SECOND CLOCK CHANNEL C+
11	GND	Ground	37	GND	Ground
12	RO 0N	FIRST CHANNEL 0-	38	RE3N	SECOND CHANNEL 3-
13	RO 0P	FIRST CHANNEL 0+	39	RE3P	SECOND CHANNEL 3+
14	RO 1N	FIRST CHANNEL 1-	40	NC	No connection
15	RO 1P	FIRST CHANNEL 1+	41	NC	No connection
16	RO 2N	FIRST CHANNEL 2-	42	GND	Ground
17	RO 2P	FIRST CHANNEL 2+	43	GND	Ground
18	GND	Ground	44	GND	Ground
19	ROCLKN	FIRST CLOCK CHANNEL C-	45	GND	Ground
20	ROCLKP	FIRST CLOCK CHANNEL C+	46	GND	Ground
21	GND	Ground	47	NC	No connection
22	RO 3N	FIRST CHANNEL 3-	48	VLCD	Power Supply +12V
23	RO 3P	FIRST CHANNEL 3+	49	VLCD	Power Supply +12V
24	NC	No connection	50	VLCD	Power Supply +12V
25	NC	No connection	51	VLCD	Power Supply +12V
26	GND	Ground	-	-	-

Note: 1. All GND (ground) pin should be connected together to the LCD module's metal frame.

2. All V_{LCD} (power input) pins should be connected.

Backlight Connector Pin Configuration

1. Electrical specification

No	ITEM	SYMBOL		CONDITION	MIN	TYP	MAX	UNIT	Note
1	Input Voltage	V_{DDB}		---	21.6	24.0	26.4	V_{DC}	
2	Input Current	I_{DDB}		V_{DDB}=24V 100% Brightness	6.94	7.3	7.66	A_{DC}	
3	Input Power	P_{DDB}		V_{DDB}=24V 100% Brightness		175		W	
4	Input inrush current	I_{RUSH}		V_{DDB}=24V 100% Brightness		---	9.9	A_{DC}	
5	Output Frequency	F_{BL}		V_{DDB}=24V		44		kHz	
6	ON/OFF Control Voltage	V_{BLON}	ON	V_{DDB}=24V	2.0	---	5.0	V_{DC}	
			OFF	V_{DDB}=24V	0.0	---	0.8	V_{DC}	
7	ON/OFF Control Current	I_{BLON}		V_{DDB}=24V	0	---	2	mA_{DC}	
8	Internal PWM Control Voltage	IV_{PWM}		V_{DDB}=24V	0	---	3.3	V_{DC}	

（Ta=25±5℃, Turn on for 45minutes）

*** Note : At < 20% dimming ratio, AUO would not guarantee display performance & start at High and Low Temperature condition.**

2. Input specification

Connector 1: S14B-PH-SM3-TB(JST) or equivalent

Symbol	Description
VDDB (Main Power)	DV input 24.0 VDC
VDDB (Main Power)	DV input 24.0 VDC
VDDB (Main Power)	DV input 24.0 VDC
VDDB (Main Power)	DV input 24.0 VDC
VDDB (Main Power)	DV input 24.0 VDC
GND	Ground
GND	Ground
GND	Ground
GND	Ground
GND	Ground
Reserved	Please leave it open
VBLON (Enable Pin)	BL On/Off control signal High/Open: On, Low: Off (Low=0~ 0.8V, High=2.0~5.0V)
VDIM	Internal PWM (3.3V,100% duty)/open for 100% luminance, 0V : 10% duty
NC	

3-3 Signal Timing Specifications

This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications for it's proper operation.

Timing Table (DE only Mode)

Vertical Frequency Range A (60Hz)

Signal	Item	Symbol	Min	Type	Max	Unit
Vertical Section	Period	Tv	1090	1125	1480	Th
	Active	Tdisp (v)		1080		Th
	Blanking	Tblk (v)	10	45	400	Th
Horizontal Section	Period	Th	1030	1100	1325	Tclk
	Active	Tdisp (h)		960		Tclk
	Blanking	Tblk (h)	70	140	365	Tclk
Clock	Period	CLK	20	13.47	12.9	ns
	Frequency	Freq	50	74.25	82	MHz
Vertical Frequency	Frequency	Vs	47	60	63	Hz
Horizontal Frequency	Frequency	Hs	60	67.5	73	KHz

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 60 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0°.

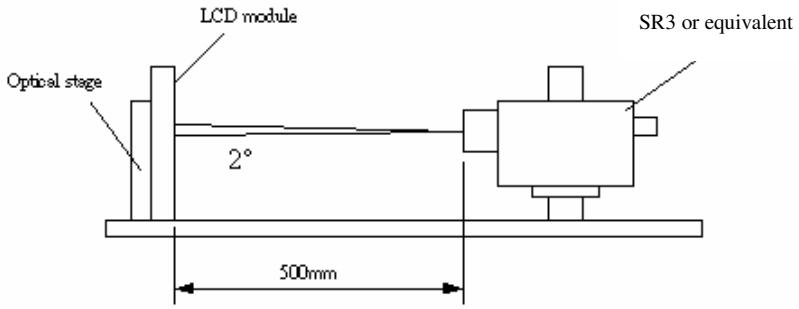


Fig.4-1 Optical measurement equipment and method

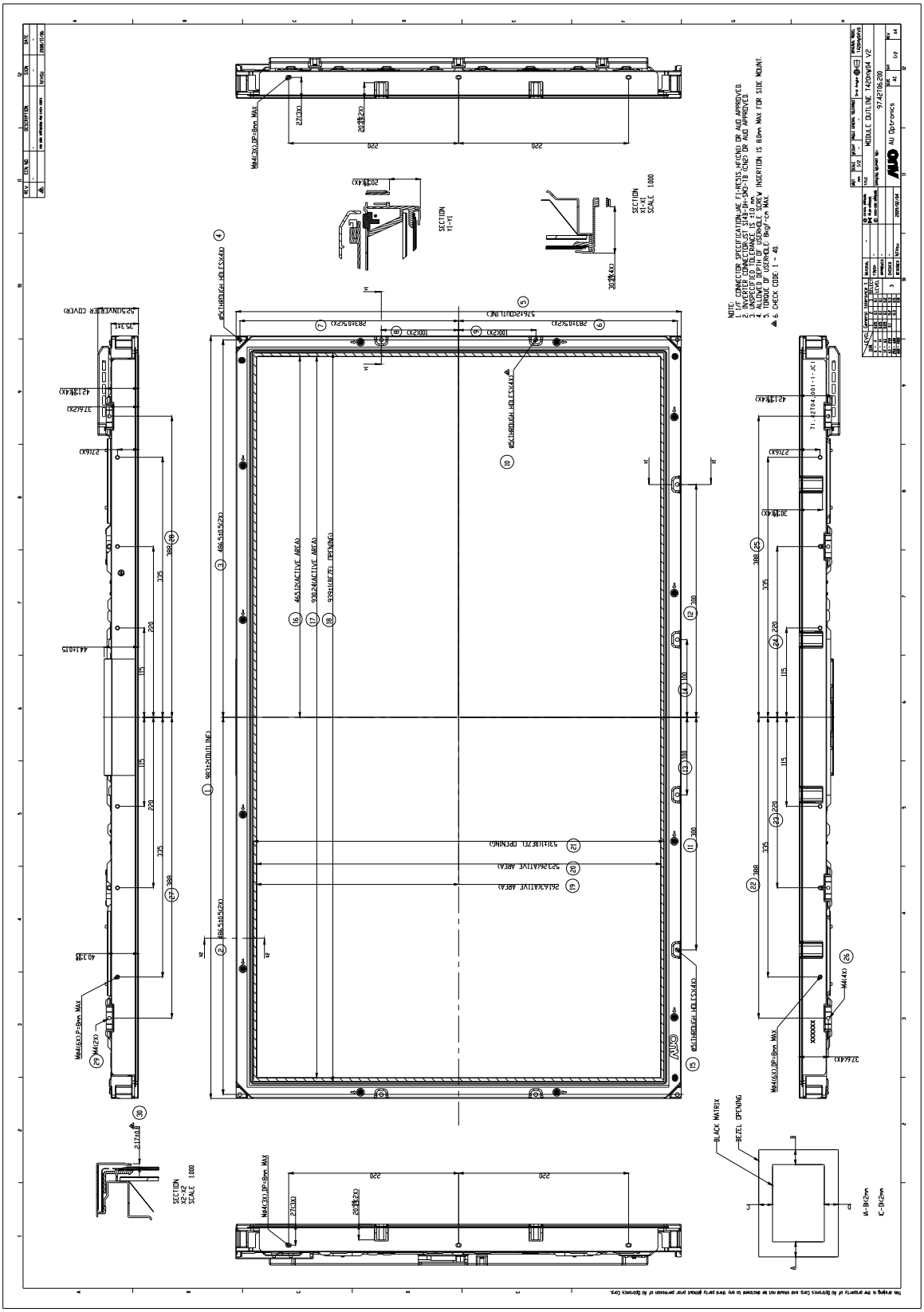
Parameter		Symbol	Values			Units	Notes
			Min.	Typ.	Max.		
Contrast Ratio		CR	4000	5000			1
Surface Luminance, white		LWH	400	500		cd/㎡	2
Luminance Variation		δ_{WHITE} 5p			1.3		3
Response Time (Average)		T γ		6.5		ms	4,5 (Gray to Gray)
Color Coordinates							
	RED	R_X	Typ.-0.03	0.640	Typ.+0.03		
		R_Y		0.330			
	GREEN	G_X		0.290			
		G_Y		0.600			
	BLUE	B_X		0.150			
		B_Y		0.060			
	WHITE	W_X		0.280			
		W_Y		0.290			
Viewing Angle							Contrast Ratio>10
	x axis, right(φ=0°)	θ_r		89		Degree	6
	x axis, left(φ=180°)	θ_l		89			
	y axis, up(φ=90°)	θ_u		89			
	y axis, down (φ=0°)	θ_d		89			

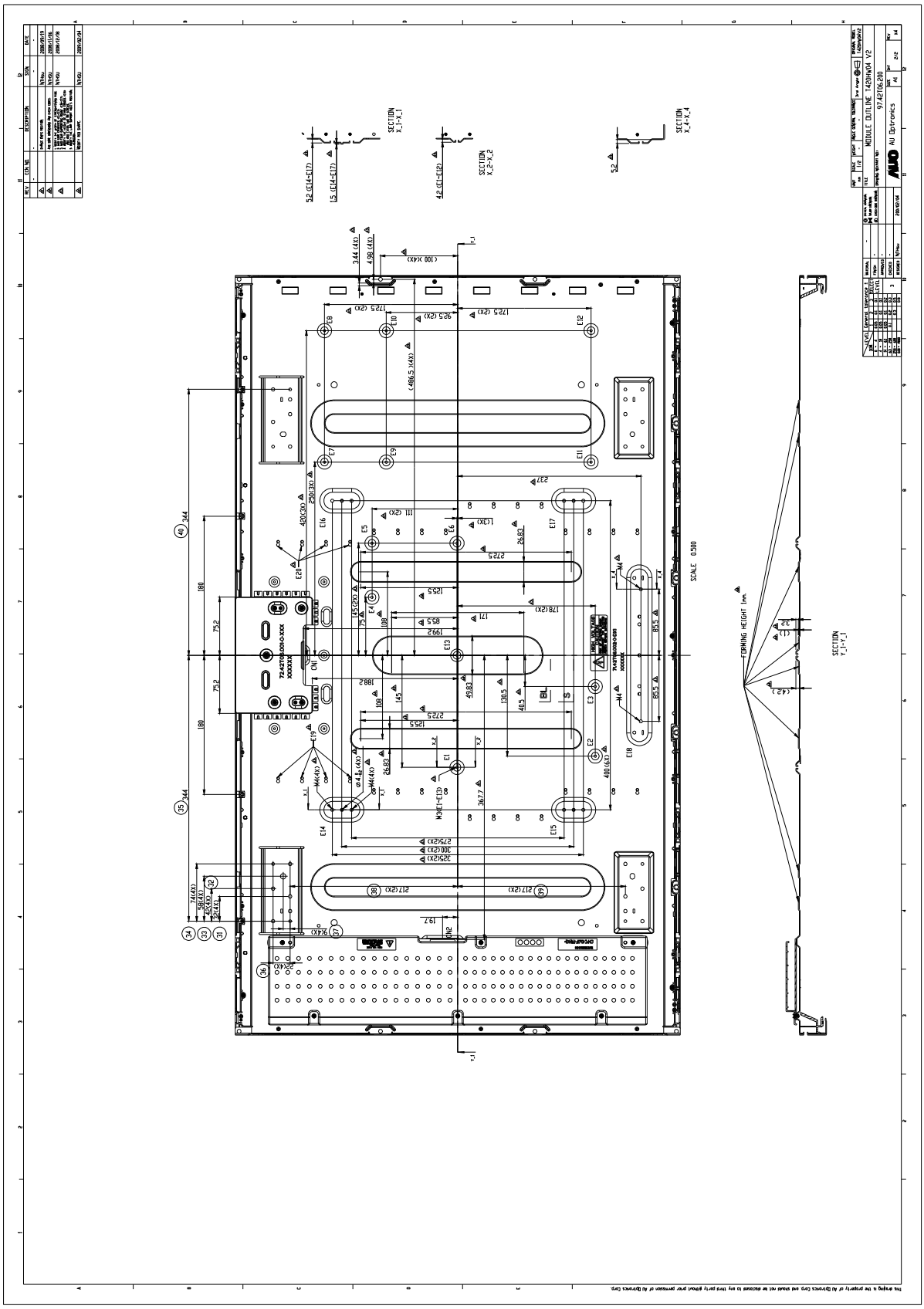
5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model T420HW04. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal (typ.)	983.0mm
	Vertical (typ.)	576.0mm
	Depth (typ.)	52.5mm (with inverter)
Bezel Area	Horizontal (typ.)	939.0mm
	Vertical (typ.)	531.0mm
Active Display Area	Horizontal	930.24mm
	Vertical	523.26mm
Weight	11100 (typ),	
Surface Treatment	Anti-Glare coating (Haze 11%) Hard coating (3H)	

2D drawing





MST6E16 SOFTWARE UPDATE STEP BY STEP

1. Take a normal USB disk

2. Plug USB disk into Pc

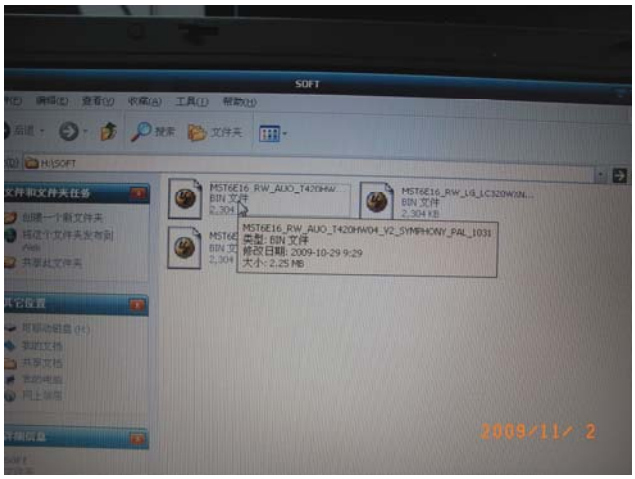
3. Open USB disk file.

4. See the update packet soft file

5. Exact the packet file to USB disk.

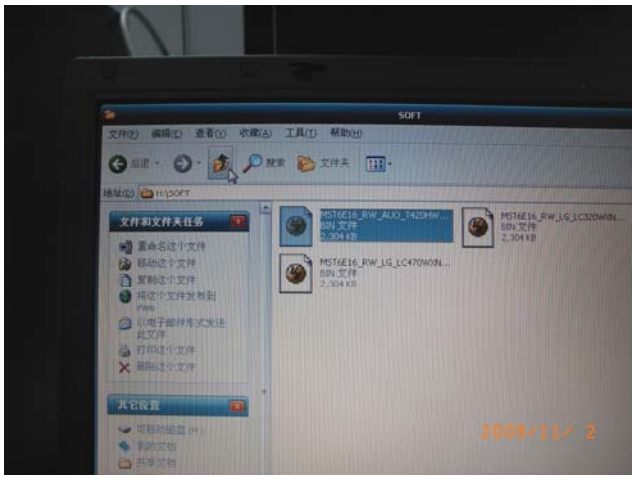
6. Exacting file.

7. The file is exact to SOFT file.



8. Go to the sub file and select the size software

9. Copy this software file



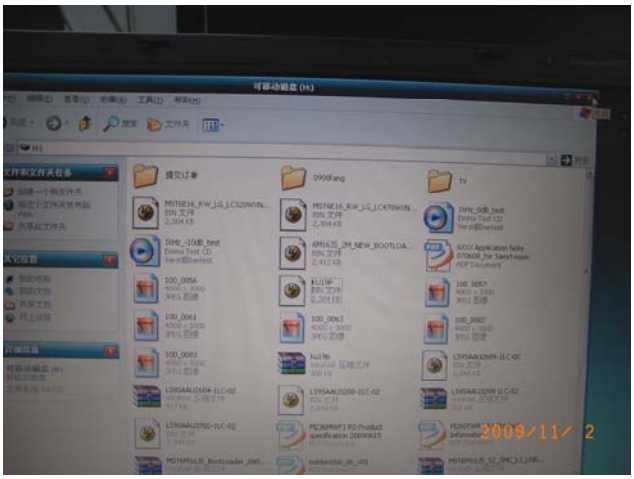
10. Go to USB boot list

11. Past this file to USB boot list.

12. The file is at USB list as H:\

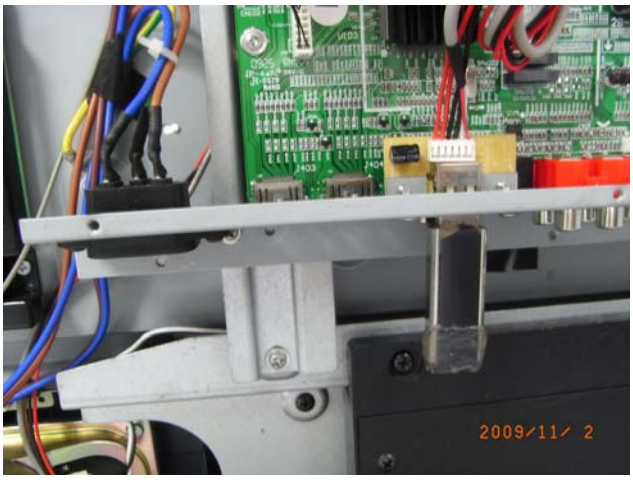
13. Rename this file to KU19P.

14. The file is KU19P, the format is .BIN

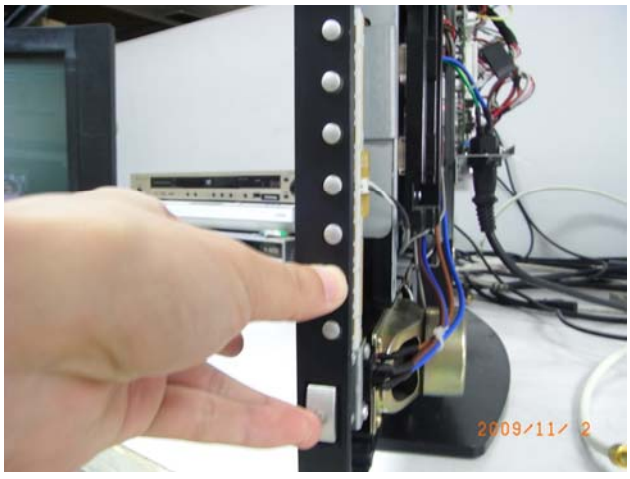


15. Close USB file.

16. Plug out the USB disk.



17. Plug this USB disk into TV USB terminal.



18. Push SOURCE key and Power on TV set.

19. After 10 sec. Led is flash slowly, display Chip erasing.

20. After 20 sec. Led is flash very fast. display Chip programming.

20. After 30 sec. Led flash slowly. Display Update finished.

21. Power off the TV set, and power on again. Wating for 10sec, standby on the TV.