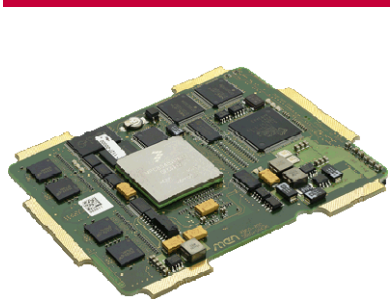
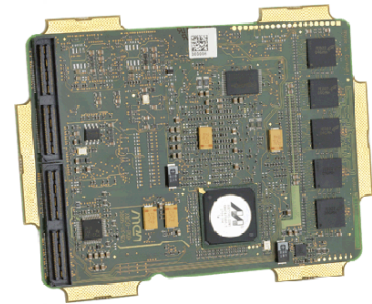
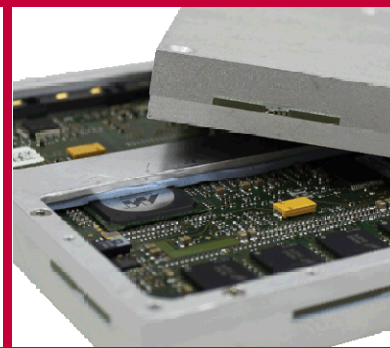


User Manual

XM50 – ESMexpress® COM with PowerPC® MPC8548



Module without cover and frame



XM50 – ESMexpress® COM with PowerPC® MPC8548

The XM50 is a computer-on-module of the ESMexpress® family controlled by an integrated PowerPC® MPC8548 or MPC8543 CPU processor (optionally with encryption unit) with clock frequencies between 800 MHz and 1.5 GHz. Together with an application-specific carrier board it forms a semi-custom solution for industrial, harsh, mobile and mission-critical environments.

The XM50 accommodates up to 2 GB of directly soldered ECC main memory and supports other memory like USB Flash on the carrier board. It also features industrial FRAM and SRAM.

Interfaces from the MPC8548 are all routed from the XM50 for availability on any ESMexpress® carrier board. Those interfaces include up to three Gigabit Ethernet channels, 8 PCI Express® lanes for one link (x4, x2 or x1, or x8 as an option), triple SATA, 6 USB host ports and one USB client realized using a UART-to-USB converter. Additional COM interfaces can be made available on the carrier board via USB to COM conversion.

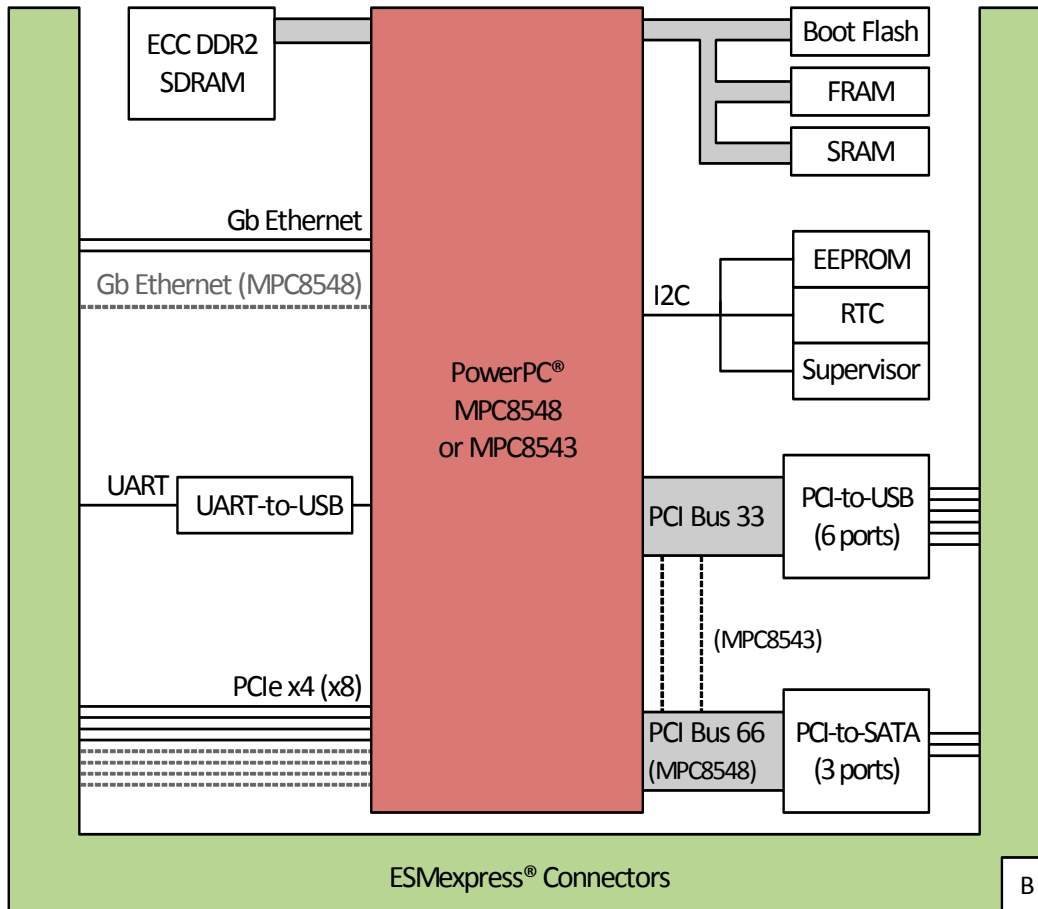
The XM50 comes with MENMON support. This firmware/BIOS can be used for bootstrapping operating systems (from disk, Flash or network), for hardware testing, or for debugging applications without running any operating system.

The XM50 is screened for operation in a -50°C to +85°C conduction or convection cooled environment. As all ESMexpress® modules it is embedded in a covered frame. This ensures EMC protection and allows efficient conductive cooling. Air cooling is also possible by applying a heat sink on top of the cover. Where operating temperatures are moderate, the module may even do without the frame and cover, with a suitable low-power processor and airflow. ESMexpress® modules are firmly screwed to a carrier board and come with rugged industry-proven connectors supporting high frequency and differential signals. Only soldered components are used to withstand shock and vibration, and the design is optimized for conformal coating. All ESMexpress® modules support a single 95x125mm form factor.

For evaluation and development purposes an ATX carrier board is available. The ESMexpress® module can be evaluated on a COM Express® carrier board via an adapter from ESMexpress® to COM Express®.

Diagram

Options B Onboard connector



Technical Data

CPU

- PowerPC® PowerQUICC™ III MPC8548, MPC8548E, MPC8543 or MPC8543E
 - 800 MHz up to 1.5 GHz
 - [Please see Standard Configurations for available standard versions.](#)
 - e500 PowerPC® core with MMU and double-precision embedded scalar and vector floating-point APU
 - Integrated Northbridge and Southbridge

Memory

- 2x 32 KB L1 data and instruction cache, 512 KB / 256 KB L2 cache integrated in MPC8548/MPC8543
- Up to 2 GB SDRAM system memory
 - Soldered
 - DDR2 with or without ECC
 - Up to 300 MHz memory bus frequency, depending on CPU
- 16 MB boot Flash
- 2 MB non-volatile SRAM
 - With GoldCap or battery backup on the carrier board
- 128 KB non-volatile FRAM
- Serial EEPROM 8 kbits for factory settings

Serial ATA (SATA)

- Three ports via ESMexpress® connector
- SATA Revision 1.x support
- Transfer rates up to 150 MB/s (1.5 Gbit/s)
- Via PCI-to-SATA bridge

USB

- Six USB 2.0 host ports via ESMexpress® connector
 - OHCI and EHCI implementation
 - Data rates up to 480 Mbit/s
- One USB client port via ESMexpress® connector
 - Via UART-to-USB converter
 - Data rates up to 115.2 kbit/s
 - 16-byte transmit/receive buffer
 - Handshake lines: none

Ethernet

- Three 10/100/1000Base-T Ethernet channels with MPC8548/E
- Two 10/100/1000Base-T Ethernet channels with MPC8543/E
- Two LED signals per channel for LAN link and activity status and connection speed
- Accessible via ESMexpress® connector

PCI Express®

- One x1 or one x2 or one x4 link via ESMexpress® connector
- PCIe® 1.x support
- Data rate 250 MB/s in each direction (2.5 Gbit/s per lane)

GPIO

- 1 line from board controller via ESMexpress® connector
- Usable for LED

Miscellaneous

- Real-time clock (with GoldCap or battery backup on the carrier board)
- Temperature sensor, power supervision and watchdog

Electrical Specifications

- Supply voltage/power consumption:
 - +12V (9..16 V), 12 W approx.

Mechanical Specifications

- Dimensions: 95 mm x 125 mm (conforming to ESMexpress® specification)
- ESMexpress® PCB mounted between a frame and a cover
- Weight: 250 g (incl. cover and frame)

Environmental Specifications

- Temperature range (operation): -50..+85°C Tcase (ESMexpress® cover/frame) (screened)
- Temperature range (storage): -50..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300 m to +3,000 m
- Shock: 15 g, 11 ms (EN 60068-2-27)
- Bump: 10 g, 16 ms (EN 60068-2-29)
- Vibration (sinusoidal): 1 g, 10 Hz – 150 Hz (EN 60068-2-6)
- Conformal coating on request

MTBF

- 209,732h @ 40°C according to IEC/TR 62380 (RDF 2000)

Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers


EMC

- EMC behavior depends on the system and housing surrounding the ESMexpress® module.
- MEN has performed general, successful EMC tests for ESMexpress® using the XC1 evaluation carrier according to:
 - EN 55022 (radio disturbance)
 - IEC 61000-4-2 (ESD)
 - IEC 61000-4-3 (electromagnetic field immunity)
 - IEC 61000-4-4 (burst)
 - IEC 61000-4-5 (surge)
 - IEC 61000-4-6 (conducted disturbances)

BIOS

- MENMON

Software Support

- Linux
- VxWorks®
- QNX® (on request; support of the FPU is currently not provided by QNX®)
- INTEGRITY® (Green Hills® Software) support available. Please contact Green Hills® for further information.
- OS-9® (on request)
-  For more information on supported operating system versions and drivers see [online data sheet](#).

Configuration Options

CPU

- Several PowerQUICC™ III types with different clock frequencies
- MPC8548 or MPC8548E
 - 1 GHz, 1.2 GHz, 1.33 GHz or 1.5 GHz
- MPC8543 or MPC8543E
 - 800 MHz or 1 GHz

Memory

- System RAM
 - 512 MB, 1 GB or 2 GB
 - With or without ECC
- SRAM
 - 0 MB or 2 MB
- FRAM
 - 0 KB or 128 KB

I/O

- Ethernet
 - Only two channels instead of three with MPC8543
- PCI Express® links: one x8 link
 - Reduces operation temperature range because of higher DDR SDRAM clock

Software Support

- QNX® (on request; support of the FPU is currently not provided by QNX®)
- OS-9® (on request)

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.



For available standard configurations see [online data sheet](#).

Product Safety



Electrostatic Discharge (ESD)

Computer boards and components contain electrostatic sensitive devices. Electrostatic discharge (ESD) can damage components. To protect the board and other components against damage from static electricity, you should follow some precautions whenever you work on your computer.

- Power down and unplug your computer system when working on the inside.
- Hold components by the edges and try not to touch the IC chips, leads, or circuitry.
- Use a grounded wrist strap before handling computer components.
- Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
- Store the board only in its original ESD-protected packaging. Retain the original packaging in case you need to return the board to MEN for repair.

About this Document

This user manual is intended only for system developers and integrators, it is not intended for end users.

It describes the hardware functions of the board, connection of peripheral devices and integration into a system. It also provides additional information for special applications and configurations of the board.

The manual does not include detailed information on individual components (data sheets etc.). A list of literature is given in the appendix.

History

Issue	Comments	Date
E1	First edition	2008-07-10
E2	Corrected USB device number and IDs in PCI device table; corrected SMB device table; added MTBF value	2008-11-27
E3	General update, minor errors corrected	2011-07-28
E4	Clarified technical data and options, added <i>Table 31. PCIe IRQ line mapping</i> , general improvements, minor errors corrected	2012-02-01
E5	Removed all ANSI-VITA 59 references, minor errors corrected	2014-02-25

Conventions



This sign marks important notes or warnings concerning the use of voltages which can lead to serious damage to your health and also cause damage or destruction of the component.



This sign marks important notes or warnings concerning proper functionality of the product described in this document. You should read them in any case.

italics

Folder, file and function names are printed in *italics*.

bold

Bold type is used for emphasis.

monospace

A monospaced font type is used for hexadecimal numbers, listings, C function descriptions or wherever appropriate. Hexadecimal numbers are preceded by "0x".

comment

Comments embedded into coding examples are shown in green color.

hyperlink

Hyperlinks are printed in blue color.



The globe will show you where [hyperlinks](#) lead directly to the Internet, so you can look for the latest information online.

IRQ#
/IRQ

Signal names followed by "#" or preceded by a slash ("/") indicate that this signal is either active low or that it becomes active at a falling edge.

in/out

Signal directions in signal mnemonics tables generally refer to the corresponding board or component, "in" meaning "to the board or component", "out" meaning "coming from it".



Vertical lines on the outer margin signal technical changes to the previous issue of the document.

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Since July 1, 2006 all MEN standard products comply with RoHS legislation.

Since January 2005 the SMD and manual soldering processes at MEN have already been completely lead-free. Between June 2004 and June 30, 2006 MEN's selected component suppliers have changed delivery to RoHS-compliant parts. During this period any change and status was traceable through the MEN ERP system and the boards gradually became RoHS-compliant.



WEEE Application

The WEEE directive does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company which puts the product on the market, as defined in the directive; components and sub-assemblies are not subject to product compliance.

In other words: Since MEN does not deliver ready-made products to end users, the WEEE directive is not applicable for MEN. Users are nevertheless recommended to properly recycle all electronic boards which have passed their life cycle.

Nevertheless, MEN is registered as a manufacturer in Germany. The registration number can be provided on request.

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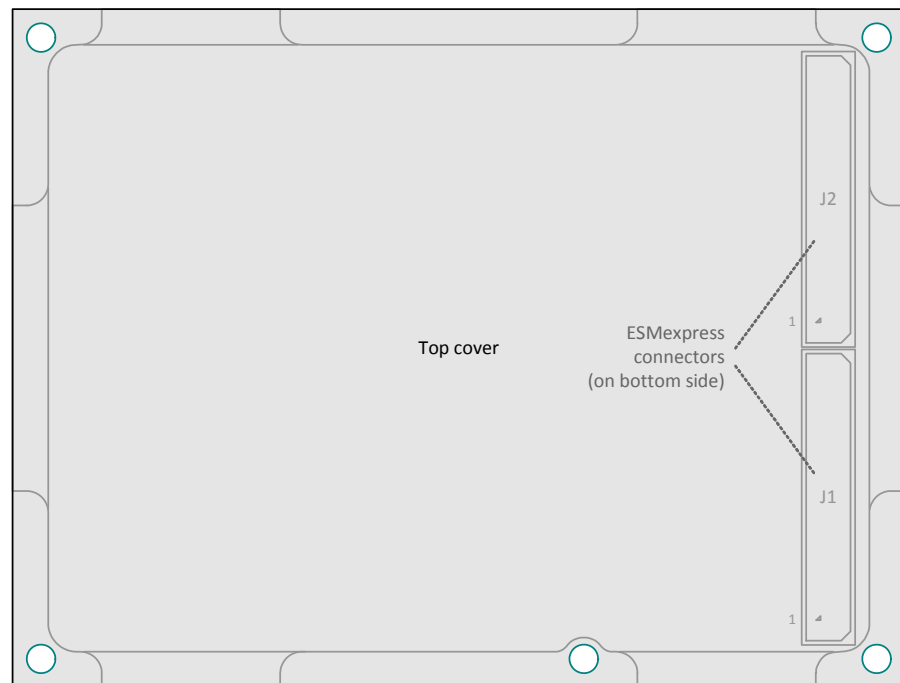
1 Getting Started

This chapter gives an overview of the board and some hints for first installation in a system.

1.1 Map of the Board

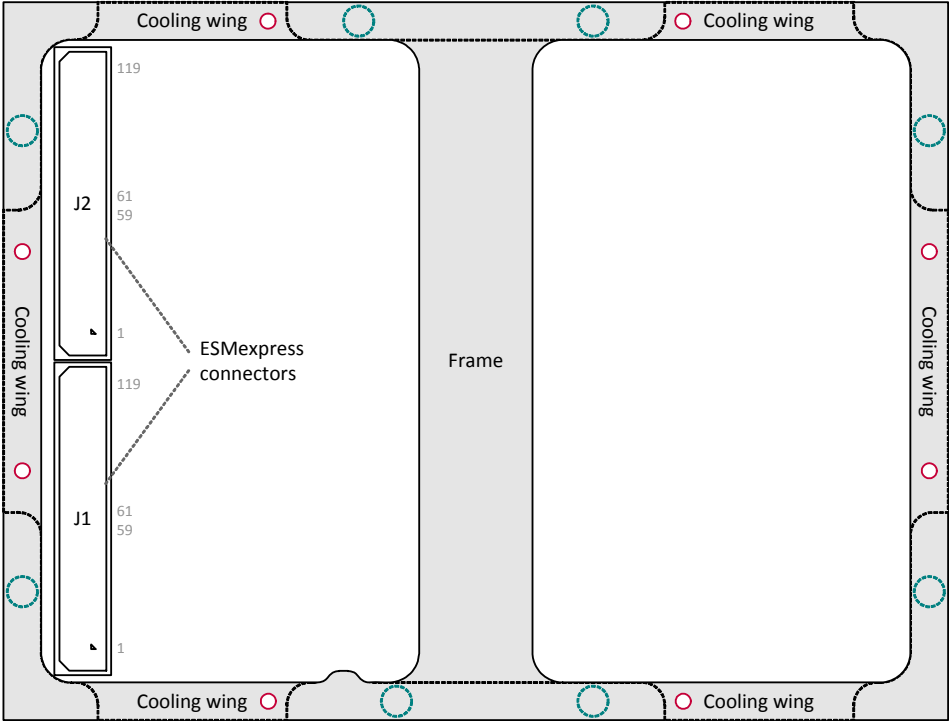
The following board map shows the board assembly from its cover side (top) and connector side (bottom). The cover includes holes for mounting the ESMexpress module onto a COM Express carrier.

Figure 1. Map of the board – cover side



○ Screw holes to install ESMexpress module on a COM Express carrier

Figure 2. Map of the board – connector side



- Holes for mounting screws on carrier board
- Screws connecting the frame and cover. Don't remove!

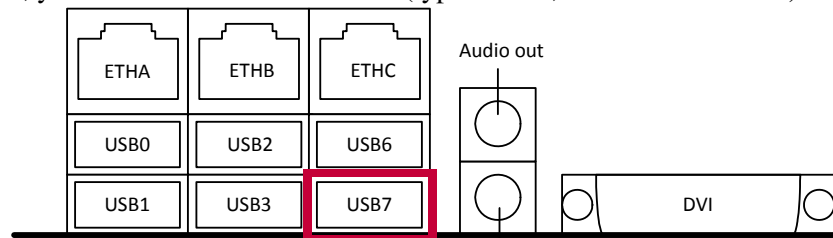
1.2 First Operation

You can use the following check list when installing the board for the first time and with minimum configuration using a Windows host PC.

- Power-down the system.
- Install the XM50 on your ESMexpress carrier board, making sure that the ESMexpress connectors are properly aligned.

To provide a better example, we assume that you are using MEN's standard evaluation carrier, XC1, which provides the necessary connections, for a Windows host PC. You can find more information on the XC1 in the XC1 User Manual, which is available for download on MEN's [website](#).

- Install a USB-to-UART driver on your host PC.
You can use a [driver provided by MEN](#) (article number 13T005-70, third-party) or go to the FTDI web site (www.ftdichip.com/FTDrivers.htm) and download a driver there.
- Connect a Windows PC to USB port 7 of XC1 (UART-to-USB COM interface). To do this, you need a suitable USB cable (type A to A, included with XC1).



- Power-up the system.
- Start up a terminal program on your Windows PC, e.g., HyperTerm, and open a terminal connection.
- Set your terminal connection to the following protocol:
 - 9600 baud data transmission rate
 - 8 data bits
 - 1 stop bit
 - No parity
- When the terminal connection is made, press Enter. Now you can use the MENMON BIOS/firmware (see detailed description in [Chapter 3 MENMON on page 39](#)).

If you enter command "LOGO" on the MENMON prompt, the terminal displays a message similar to the following:

```

Secondary MENMON for MEN MPC8548 Family (XM50) Beta1.5work2
-----
(c) 2007 - 2008 MEN Mikro Elektronik GmbH Nuremberg
MENMON 2nd Edition, Created Jun 12 2008 10:45:08
-----
CPU Board: XM50-00 | CPU: MPC8548
Serial Number: 4 | CPU/MEM C1k: 1386 / 198 MHz
HW Revision: 00.00.00 | CCB/LBC C1k: 396 / 50 MHz
-----
PCI1/PCI2: 32Bit 66MHz/32Bit 33MHz | PCIe: x4
DDR2 SDRAM: 512 MB ECC on 3.0/3/8 | FRAM/SRAM: 128 /2048 kB
Produced: | FLASH: 16 MB
Last repair: | Reset Cause: Power On
-----
Carrier Board: XC01-00, Rev 00.01.00, Serial 3
\

```

Note: Don't power off the XM50 now, otherwise the USB-to-UART interface on the host PC will be disconnected.

- Observe the installation instructions for the respective software.

1.3 Installing Operating System Software

The board supports Linux, VxWorks, INTEGRITY, QNX and OS-9.



By standard, no operating system is installed on the board. Please refer to the operating system installation documentation on how to install the software!



You can find any software available on MEN's [website](#).

2 Functional Description

The following describes the individual functions of the board and their configuration on the board. There is no detailed description of the individual controller chips and the CPU. They can be obtained from the data sheets or data books of the semiconductor manufacturer concerned ([Chapter 5.1 Literature and Web Resources on page 65](#)).

2.1 Power Supply

The XM50 board is supplied with +12V (9 to 16V) only via ESMexpress connectors J1/J2.

All other required voltages are generated on the board.

2.2 Board Supervision

The board features a temperature sensor and voltage monitor.

A voltage monitor supervises all used voltages and holds the CPU in reset condition until all supply voltages are within their nominal values.

In addition the board contains a PLD watchdog that must be triggered. After configuration the CPU serves the PLD watchdog. The watchdog timeout is automatically set to 1.12 s after the first trigger pulse by the CPU.

The watchdog can be enabled or disabled through MENMON and can be triggered by a software application. This function is normally supported by the board support package (see BSP documentation).

2.3 Real-Time Clock

The board includes an RA8581 real-time clock. Interrupt generation of the RTC is not supported. For data retention during power off the RTC must be supplied with 3V via J1 pin *Vbatt* (J1-55) using an external GoldCap or battery device mounted on the carrier board.

A control flag indicates a back-up power fail condition. In this case the contents of the RTC cannot be expected to be valid. A message will be displayed on the MENMON console in this case.

2.4 Processor Core

The board is equipped with the MPC8548 or MPC8543 processor, which includes a 32-bit PowerPC e500 core, the integrated host-to-PCI bridge, Ethernet controllers and UARTs.

2.4.1 General

The MPC8548/3 family of processors integrates an e500v2 processor core built on Power Architecture technology with system logic required for networking, telecommunications, and wireless infrastructure applications. The MPC8548/3 is a member of the PowerQUICC III family of devices that combine system-level support for industry-standard interfaces with processors that implement the embedded category of the Power Architecture technology.

The MPC8548/3 offers a double-precision floating-point auxiliary processing unit (APU), up to 512 KB of level-2 cache, up to four integrated 10/100/1Gbits/s enhanced three-speed Ethernet controllers with TCP/IP acceleration and classification capabilities, a DDR/DDR2 SDRAM memory controller, a programmable interrupt controller, two I²C controllers, a four-channel DMA controller, a general-purpose I/O port, and dual universal asynchronous receiver/transmitters (DUART).

The MPC8548/3 is available with (MPC8548/3E) or without an integrated security engine with XOR acceleration.

Table 1. Processor core options on XM50

Processor Type	Core Frequency	L2 Cache	Encryption Unit	Ethernet Ports
MPC8548	1 GHz, 1.2 GHz, 1.33 GHz or 1.5 GHz	512 KB	No	3
MPC8548E	1 GHz, 1.2 GHz, 1.33 GHz or 1.5 GHz	512 KB	Yes	3
MPC8543	800 MHz or 1 GHz	256 KB	No	2
MPC8543E	800 MHz or 1 GHz	256 KB	Yes	2

2.4.2 Thermal Considerations

The XM50 generates around 12 W of power dissipation when operated at 1.33 GHz.

The ESMexpress module is enclosed inside a cover and frame and therefore provides a flexible thermal interface that can be used as needed to fulfill the thermal needs of the application. Typically you should use it for conduction cooling or convection cooling. It depends on the system configuration and airflow if an additional heat sink is needed or not. In any case you should check your thermal conditions and implement appropriate cooling.

See also [Chapter 2.11.2 Thermal Concept on page 27](#).



Please note that if you do not use the cover and frame supplied by MEN and/or no heat sink, warranty on functionality and reliability of the XM50 may cease. If you have any questions or problems regarding thermal behavior, please contact MEN.

2.5 Bus Structure

2.5.1 Host-to-PCI Bridge

The integrated host-to-PCI bridge is used as host bridge and memory controller for the PowerPC processor. All transactions of the PowerPC to the PCI bus are controlled by the host bridge. The FRAM, SRAM and boot Flash are connected to the local memory bus of the integrated host-to-PCI bridge.

The PCI interface is PCI bus Rev. 2.2 compliant and supports all bus commands and transactions. Master and target operations are possible. Only big-endian operation is supported.

2.5.2 Local PCI Buses

Two local PCI buses are controlled by the integrated host-to-PCI bridge. One is connected to the PCI-to-USB bridge and runs at 33 MHz. The other connects the PCI-to-SATA bridge and operates at 66 MHz. Board versions with the MPC8543 processor only have one local PCI bus operating at 33 MHz.

The I/O voltage is fixed to 3.3V. The data width is 32 bits.

2.6 Memory and Mass Storage

2.6.1 DRAM System Memory

The board provides up to 2 GB onboard, soldered DDR2 (double data rate) SDRAM on nine memory components (incl. ECC). The memory bus is 72 bits wide and operates at up to 300 MHz (physical), depending on the processor type.

Depending on the board version the SDRAM may have ECC (error-correcting code). ECC memory provides greater data accuracy and system uptime by protecting against soft errors in computer memory.

2.6.2 FRAM

The board has up to 128 KB non-volatile FRAM memory connected to the local bus of the CPU.

The FRAM does not need a back-up voltage for data retention.

2.6.3 SRAM

The board has up to 2 MB non-volatile SRAM memory connected to the local bus of the CPU.

For data retention during power off the SRAM must be supplied with a back-up voltage of 3.3 V via J1 pin *Vbatt* (J1-55) using an external GoldCap or battery device mounted on the carrier board.

2.6.4 Boot Flash

The board has 16 MB of onboard Flash. It is controlled by the CPU.

Flash memory contains the boot software for the MENMON/operating system bootstrapper and application software. The MENMON sectors are software-protected against illegal write transactions through a password in the serial download function of MENMON (cf. [Chapter 3.5.1 Update via the Serial Console using SERDL on page 44](#)).

2.6.5 EEPROM

The board has an 8-kbit serial EEPROM for factory data.

2.6.6 Serial ATA (SATA)

The XM50 provides three serial ATA channels through a PCI-to-SATA converter that is connected to the PowerPC processor via a dedicated 66-MHz PCI bus. (On board versions with the MPC8543 processor PCI-to-SATA shares one 33-MHz PCI bus with PCI-to-USB.) The SATA channels are led to the ESMexpress connector.

The SATA interfaces supports transfer rates up to 1.5 Gbits/s.

You can find the pinout for the SATA signals in [Table 3, Pin assignment of ESMexpress connector J1, pins 61..120 on page 30](#).

2.7 USB Interfaces

The XM50 provides six USB 2.0 host ports with OHCI/EHCI implementation and one USB client port at the ESMexpress connector.

The six host ports are controlled via PCI-to-USB bridges from the PowerPC processor, while the client port is driven by a UART-to-USB converter.

The UART-to-USB interface supports data rates up to 115.2 kbits/s. It has no handshake lines. In connection with USB-to-UART driver software it can be used as a COM interface and is supported by MENMON as a console device.

You can find the pinout for the USB signals in [Table 3, Pin assignment of ESMexpress connector J1, pins 61..120 on page 30](#) and [Table 4, Pin assignment of ESMexpress connector J1, pins 1..60 on page 31](#).

2.8 Ethernet Interfaces

The XM50 has up to three Ethernet interfaces controlled by the CPU. All channels support up to 1000 Mbits/s and full-duplex operation.



Please note that ETHC is **not available** on board versions with the MPC8543 processor.

You can find the pinout for the Ethernet signals in [Table 4, Pin assignment of ESMexpress connector J1, pins 1..60 on page 31](#).



The unique MAC address is set at the factory and should not be changed. Any attempt to change this address may create node or bus contention and thereby render the board inoperable. The MAC addresses on XM50 are:

- ETHA: 0x 00 C0 3A 87 xx xx
- ETHB: 0x 00 C0 3A 88 xx xx
- ETHC: 0x 00 C0 3A 89 xx xx

where "00 C0 3A" is the MEN vendor code, "87", "88" and "89" are the MEN product codes, and "xx xx" is the hexadecimal serial number of the product, which depends on your board, e. g. "... 00 2A" for serial number "000042". (See [Chapter 5.2 Finding out the Board's Article Number, Revision and Serial Number on page 66](#).)

2.9 GPIO

The XM50 provides one GPIO pin driven by the board controller for user-defined options or for a board status LED. This LED can be made available on the carrier board.

You can find the GPIO pin in [Table 4, Pin assignment of ESMexpress connector J1, pins 1..60 on page 31](#).

2.10 PCI Express Interface

The PowerPC processor supports four PCI Express lanes which can be used as one x1 or one x2 or one x4 link. Any link supports a data rate of 250 MB/s in each direction with a bandwidth of 2.5 Gbits/s per lane. One x8 link is also possible on request, but this reduces the XM50's extended operation temperature range.

The following table shows which lanes must be used for each link type.

Table 2. Possible PCI Express link configurations

PCIe Lane	PCIe Link Configuration			
PCIE_B7				x8
PCIE_B6				
PCIE_B5				
PCIE_B4				
PCIE_B3			x4	
PCIE_B2				
PCIE_B1				
PCIE_B0	x1	x2		

Note: PCIE_B0..3 are standard, PCIE_B4..7 are an additional option.

The interface can be accessed on the ESMexpress connector.

You can find the pinout for the PCI Express signals in [Table 3, Pin assignment of ESMexpress connector J1, pins 61..120 on page 30](#), [Table 5, Pin assignment of ESMexpress connector J2, pins 61..120 on page 32](#) and [Table 6, Pin assignment of ESMexpress connector J2, pins 1..60 on page 33](#).

2.11 ESMexpress

ESMexpress is a Computer-On-Module (COM/SOM) standard that is especially ruggedized and provides a high-performance, low-power architecture for harsh environments.

The ESMexpress concept has been developed for applications that require highly robust electronics to ensure safe and reliable operation even in severe environments, e.g., in railways and avionics, industrial automation and medical engineering or mobile applications in general.

Together with an application-specific carrier board, it forms a semi-custom solution for industrial, harsh, mobile and mission-critical environments.

2.11.1 Mechanical Concept

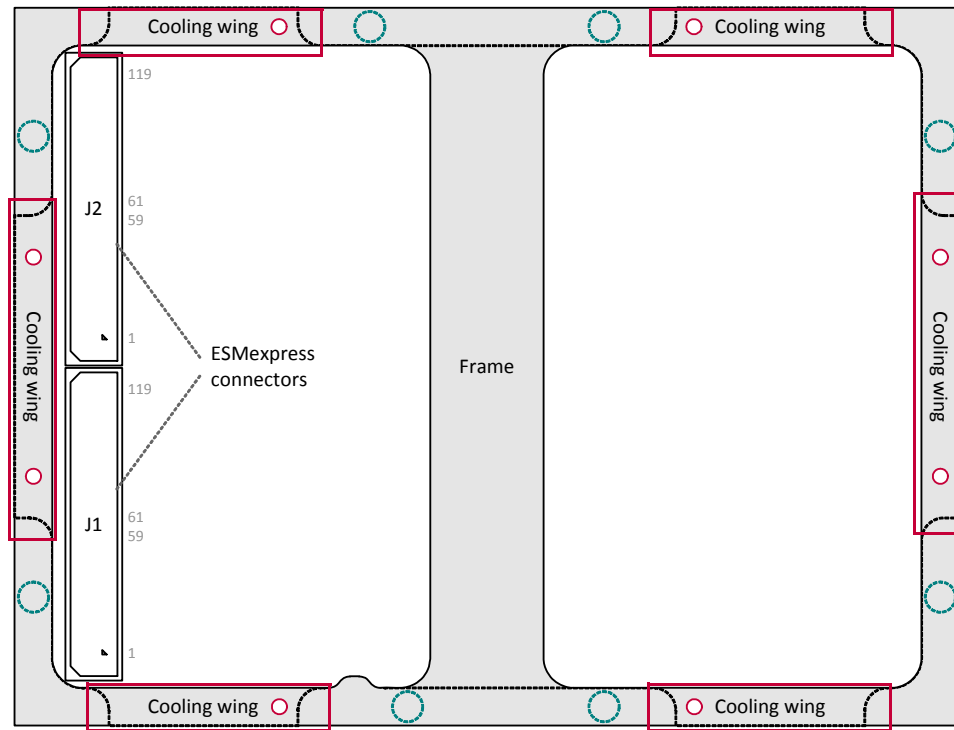
ESMexpress modules are embedded in a frame and a cover, and are firmly screwed to a carrier board. The frame and the cover ensure 100% EMC protection. Only soldered components are used to withstand shock and vibration, and the design is optimized for conformal coating. All ESMexpress modules support a single 95 x 125 mm form factor.

2.11.2 Thermal Concept

ESMexpress modules are equipped with eight cooling wings for conductive cooling. The heat generated on the board is transported to the frame and the cover via the cooling wings. The frame and the cover, however, are only part of the thermal solution for a module. They only provide a common interface between the ESMexpress module and implementation-specific thermal solutions.

The module can e.g. be cooled via conductive cooling, where the heat is transported to a housing or a heat sink built on top of the cover. Where operating temperatures are moderate, the module may even do without the frame and cover, with a suitable low-power processor and airflow.

Figure 3. ESMexpress thermal concept: cooling wings between frame and cover



- Holes for mounting screws on carrier board
- Screws connecting the frame and cover. Don't remove!

Please [contact MEN's sales team](#) for further information.

2.11.3 ESMexpress Connectors

The XM50 is connected to the carrier board via two 120-pin connectors.

Connector types:

- 2-row, 120-pin high-speed receptacle, 0.5mm pitch, e.g. Samtec QSH-060-01-L-D-A-K
- Mating connector:
2-row, 120-pin high-speed plug connector, 0.5mm pitch



Note: In the following pinout tables the ESMexpress connectors are shown as if seen **through** the cover side and PCB, i.e. the pin layout (position of pin 1) will be the same on a carrier board.

Cf. Figure 1, Map of the board – cover side (page 17) and Figure 2, Map of the board – connector side (page 18).

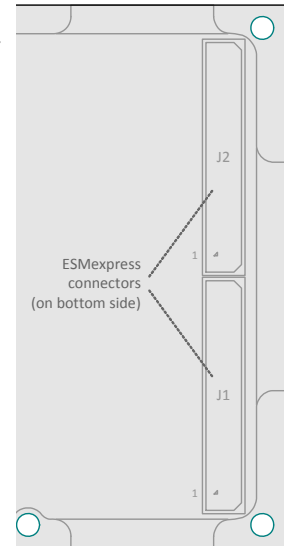


Table 3. Pin assignment of ESMexpress connector J1, pins 61..120

	119	PCIE_A0_TX+	GND	120	PCIE_A0_RX+
	117	PCIE_A0_TX-		118	PCIE_A0_RX-
	115	GND		116	GND
	113	PCIE_CLK_A0_REF+		114	-
	111	PCIE_CLK_A0_REF-		112	-
	109	GND		110	GND
	107	-		108	-
	105	-		106	-
	103	-		104	-
	101	-		102	-
	99	-		100	-
	97	GND		98	GND
	95	SATA0_TX+		96	SATA0_RX+
	93	SATA0_TX-		94	SATA0_RX-
	91	GND		92	GND
	89	SATA1_TX+		90	SATA1_RX+
	87	SATA1_TX-		88	SATA1_RX-
	85	GND		86	GND
	83	SATA2_TX+		84	SATA2_RX+
	81	SATA2_TX-		82	SATA2_RX-
	79	GND		80	GND
	77	USB0+		78	USB1+
	75	USB0-		76	USB1-
	73	USB_OC_0_1#		74	USB_OC_2_3#
	71	USB2+		72	USB3+
	69	USB2-		70	USB3-
	67	GND		68	GND
	65	USB4+		66	USB5+
63	USB4-	64	USB5-		
61	USB_OC_4_5#	62	-		

The PCI Express pins shown in grey color are available on request for a x1 link, e.g., for special XM50 versions without a J2 connector.

Table 4. Pin assignment of ESMexpress connector J1, pins 1..60

	59	-	60	UART-to-USB+
	57	-	58	UART-to-USB-
	55	Vbatt	56	-
	53	PWR_OK	54	PS_ON#
	51	SMB_DATA	52	RESET_IN#
	49	SMB_CLK	50	RESET_OUT#
	47	-	48	-
	45	GPOUT/LED#	46	-
	43	-	44	-
	41	-	42	-
	39	-	40	-
	37	-	38	-
	35	ETH_C_LED_LINK#	36	ETH_C_LED_ACT#
	33	ETH_C0+	34	ETH_C1+
	31	ETH_C0-	32	ETH_C1-
	29	ETH_C2+	30	ETH_C3+
	27	ETH_C2-	28	ETH_C3-
	25	ETH_C_REF	26	GND
	23	ETH_B_LED_LINK#	24	ETH_B_LED_ACT#
	21	ETH_B0+	22	ETH_B1+
	19	ETH_B0-	20	ETH_B1-
	17	ETH_B2+	18	ETH_B3+
	15	ETH_B2-	16	ETH_B3-
	13	ETH_B_REF	14	GND
	11	ETH_A_LED_LINK#	12	ETH_A_LED_ACT#
	9	ETH_A0+	10	ETH_A1+
	7	ETH_A0-	8	ETH_A1-
	5	ETH_A2+	6	ETH_A3+
	3	ETH_A2-	4	ETH_A3-
	1	ETH_A_REF	2	GND

Table 5. Pin assignment of ESMexpress connector J2, pins 61..120

	119	PCIE_B0_TX+	GND	120	PCIE_B0_RX+
	117	PCIE_B0_TX-		118	PCIE_B0_RX-
	115	GND		116	GND
	113	PCIE_B1_TX+		114	PCIE_B1_RX+
	111	PCIE_B1_TX-		112	PCIE_B1_RX-
	109	GND		110	GND
	107	PCIE_B2_TX+		108	PCIE_B2_RX+
	105	PCIE_B2_TX-		106	PCIE_B2_RX-
	103	GND		104	GND
	101	PCIE_B3_TX+		102	PCIE_B3_RX+
	99	PCIE_B3_TX-		100	PCIE_B3_RX-
	97	GND		98	GND
	95	PCIE_B4_TX+		96	PCIE_B4_RX+
	93	PCIE_B4_TX-		94	PCIE_B4_RX-
	91	GND		92	GND
	89	PCIE_B5_TX+		90	PCIE_B5_RX+
	87	PCIE_B5_TX-		88	PCIE_B5_RX-
	85	GND		86	GND
	83	PCIE_B6_TX+		84	PCIE_B6_RX+
	81	PCIE_B6_TX-		82	PCIE_B6_RX-
	79	GND		80	GND
	77	PCIE_B7_TX+		78	PCIE_B7_RX+
	75	PCIE_B7_TX-		76	PCIE_B7_RX-
	73	GND		74	GND
	71	-		72	-
	69	-		70	-
	67	GND		68	GND
	65	-		66	-
63	-	64	-		
61	-	62	-		

The PCI Express pins shown in grey color are available as an option for a x8 link.

Table 6. Pin assignment of ESMexpress connector J2, pins 1..60

	59	-		60	-
	57	-		58	-
	55	-		56	-
	53	GND		54	GND
	51	-		52	-
	49	-		50	-
	47	GND		48	GND
	45	-		46	-
	43	-		44	-
	41	GND		42	GND
	39	-		40	-
	37	-		38	-
	35	GND		36	GND
	33	-		34	-
	31	-		32	-
	29	GND	GND	30	GND
	27	-		28	-
	25	-		26	-
	23	GND		24	GND
	21	-		22	PCIE_CLK_B_REF+
	19	-		20	PCIE_CLK_B_REF-
	17	GND		18	GND
	15	-		16	-
	13	-		14	-
	11	GND		12	GND
	9	-		10	-
	7	-		8	-
	5	GND		6	GND
	3	-		4	-
	1	-		2	-

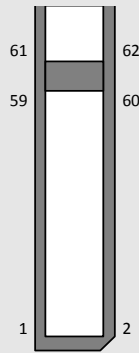


Table 7. Signal mnemonics of 120-pin ESMexpress connectors

	Signal	Direction	Function
Power	GND	-	Ground
	Vbatt		3V battery voltage
Power Management	PS_ON#	out	Enable signal for external power supply
	PWR_OK	in	Power OK signal from external power supply
	RESET_IN#	in	Reset signal from carrier board
	RESET_OUT#	out	Reset signal from CPU board
PCI Express	PCIE_CLK_A0_REF+, PCIE_CLK_A0_REF-	out	Reference clock A0 100 MHz (option for x1 link on J1)
	PCIE_CLK_B_REF+, PCIE_CLK_B_REF-	out	Reference clock B 100 MHz
	PCIE_B[3:0]_RX+, PCIE_B[3:0]_RX-	in	Differential PCIe receive lines, lanes 0 to 3
	PCIE_B[3:0]_TX+, PCIE_B[3:0]_TX-	out	Differential PCIe transmit lines, lanes 0 to 3
	PCIE_B[7:4]_RX+, PCIE_B[7:4]_RX-	in	Differential PCIe receive lines, lanes 4 to 7 (option for x8 link)
	PCIE_B[7:4]_TX+, PCIE_B[7:4]_TX-	out	Differential PCIe transmit lines, lanes 4 to 7 (option for x8 link)
SATA	SATA0_RX+, SATA0_RX-	in	Differential SATA receive lines, port 0
	SATA0_TX+, SATA0_TX-	out	Differential SATA transmit lines, port 0
	SATA1_RX+, SATA1_RX-	in	Differential SATA receive lines, port 1
	SATA1_TX+, SATA1_TX-	out	Differential SATA transmit lines, port 1
	SATA2_RX+, SATA2_RX-	in	Differential SATA receive lines, port 2
	SATA2_TX+, SATA2_TX-	out	Differential SATA transmit lines, port 2
USB	USB0+, USB0-	in/out	Differential USB lines, port 0
	USB1+, USB1-	in/out	Differential USB lines, port 1
	USB2+, USB2-	in/out	Differential USB lines, port 2
	USB3+, USB3-	in/out	Differential USB lines, port 3
	USB4+, USB4-	in/out	Differential USB lines, port 4
	USB5+, USB5-	in/out	Differential USB lines, port 5
	UART-to-USB+, UART-to-USB-	in/out	Differential UART-to-USB lines (USB port 7)
	USB_OC_0_1#	in	USB overcurrent, ports 0 and 1
	USB_OC_2_3#	in	USB overcurrent, ports 2 and 3
	USB_OC_4_5#	in	USB overcurrent, ports 4 and 5
	USB_OC_6_7#	in	USB overcurrent, ports 6 and 7

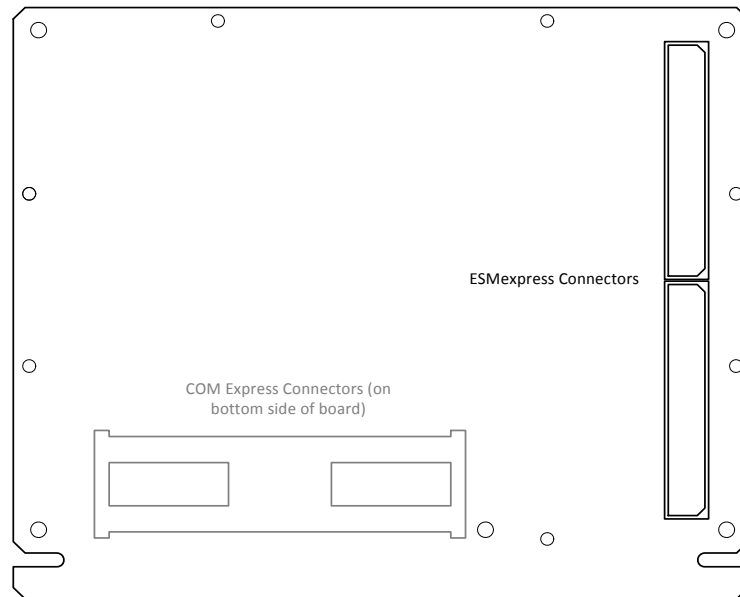
	Signal	Direction	Function
Ethernet	ETH_A_LED_ACT#	out	Signal for activity status LED, port A
	ETH_A_LED_LINK#	out	Signal for link status LED, port A
	ETH_A0+, ETH_A0-	in/out	Media Dependent Interface [0] data, differential pair, port A
	ETH_A1+, ETH_A1-	in/out	Media Dependent Interface [1] data, differential pair, port A
	ETH_A2+, ETH_A2-	in/out	Media Dependent Interface [2] data, differential pair, port A
	ETH_A3+, ETH_A3-	in/out	Media Dependent Interface [3] data, differential pair, port A
	ETH_A_REF	out	Port A reference voltage
	ETH_B_LED_ACT#	out	Signal for activity status LED, port B
	ETH_B_LED_LINK#	out	Signal for link status LED, port B
	ETH_B0+, ETH_B0-	in/out	Media Dependent Interface [0] data, differential pair, port B
	ETH_B1+, ETH_B1-	in/out	Media Dependent Interface [1] data, differential pair, port B
	ETH_B2+, ETH_B2-	in/out	Media Dependent Interface [2] data, differential pair, port B
	ETH_B3+, ETH_B3-	in/out	Media Dependent Interface [3] data, differential pair, port B
	ETH_B_REF	out	Port B reference voltage
	ETH_C_LED_ACT#	out	Signal for activity status LED, port C
	ETH_C_LED_LINK#	out	Signal for link status LED, port C
	ETH_C0+, ETH_C0-	in/out	Media Dependent Interface [0] data, differential pair, port C
	ETH_C1+, ETH_C1-	in/out	Media Dependent Interface [1] data, differential pair, port C
	ETH_C2+, ETH_C2-	in/out	Media Dependent Interface [2] data, differential pair, port C
	ETH_C3+, ETH_C3-	in/out	Media Dependent Interface [3] data, differential pair, port C
	ETH_C_REF	out	Port C reference voltage
Other	SMB_CLK	in/out	SMBus clock
	SMB_DATA	in/out	SMBus data
	GPOUT/LED#	in/out	User-defined general-purpose output (GPOUT30 of MPC854x)

2.11.4 Using an ESMexpress Module on a COM Express Carrier Board

The AE12 adapter card offers the possibility to evaluate an ESMexpress module on a COM Express carrier board. It complies with the COM Express Type 2 basic form factor.

On its top side the AE12 has ESMexpress connectors for connecting the ESMexpress module. On the bottom side the AE12 card is equipped with standard COM Express connectors for plugging it onto the COM Express carrier.

Figure 4. AE12 COM Express adapter board – Map of the board



The pin assignment of the COM Express connectors is compliant to the COM Express standard.

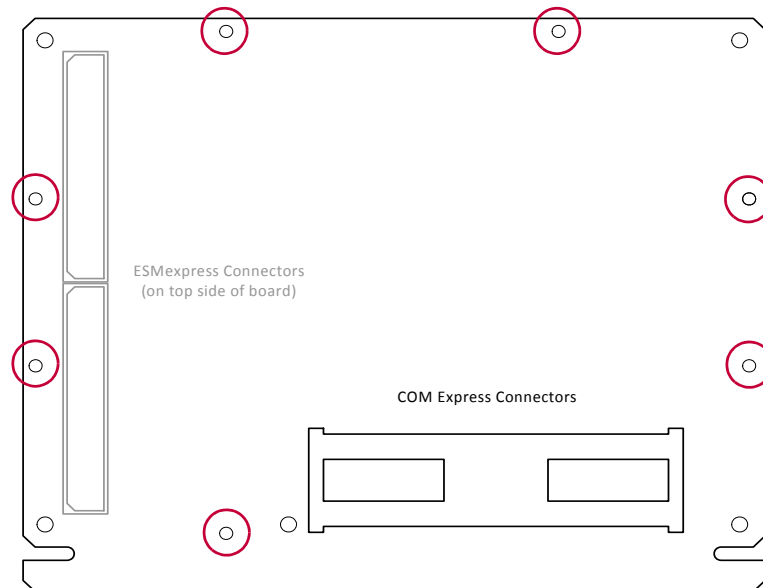
The pin assignment of the ESMexpress connectors is compliant to the ESMexpress standard.

Installing the ESMexpress Module on a COM Express Carrier

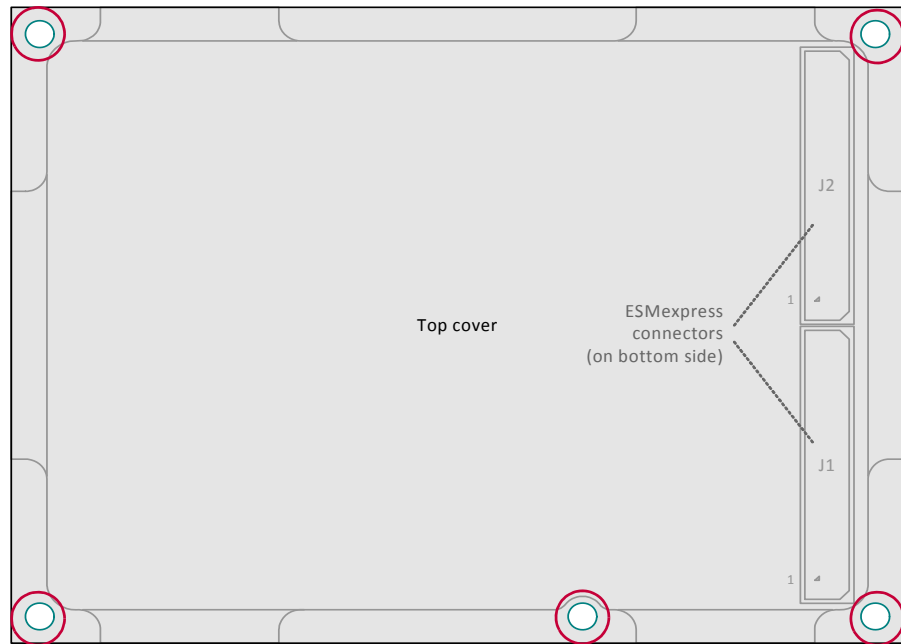
- ☑ Align the ESMexpress connectors and the mounting holes of the adapter and the module and plug the AE12 adapter firmly onto the ESMexpress module.



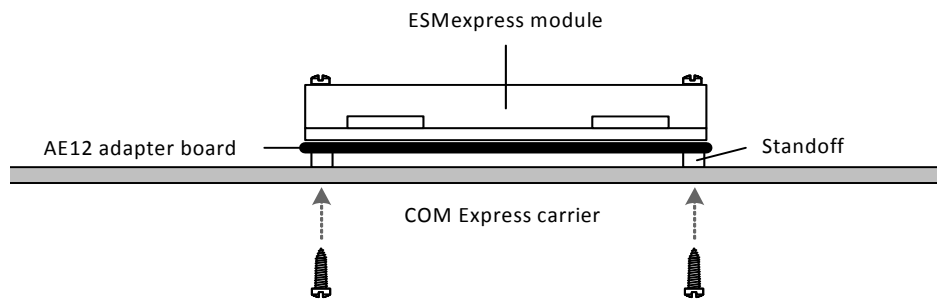
- ☑ Install the ESMexpress module on the adapter using the following mounting holes and the seven M2x4 cross-recess pan-head screws included in the delivery of the adapter:



- ☑ Turn the module around and insert five 2.5x18 cross-recess countersink-head screws (also included in the delivery) into the five COM Express mounting holes on the top of the ESMexpress module.



- ☑ Install the five 2.5x5 standoffs on the bottom of the adapter.
- ☑ Plug the ESMexpress module/AE12 assembly onto the COM Express carrier board.
- ☑ Screw the adapter onto the COM Express carrier board using five M2.5x4 screws.



3 MENMON

3.1 General

MENMON is the CPU board firmware that is invoked when the system is powered on.

The basic tasks of MENMON are:

- Initialize the CPU and its peripherals.
- PCI/PCIe auto configuration.
- Perform self-test.
- Provide debug/diagnostic features on MENMON command line.
- Interaction with the user via touch panel/TFT display (if supported by ESMexpress carrier).
- Boot operating system.
- Update firmware or operating system.



The following description only includes board-specific features. For a general description and in-depth details on MENMON, please refer to the [MENMON 2nd Edition User Manual](#).

3.1.1 State Diagram

Figure 5. MENMON – State diagram, Degraded Mode/Full Mode

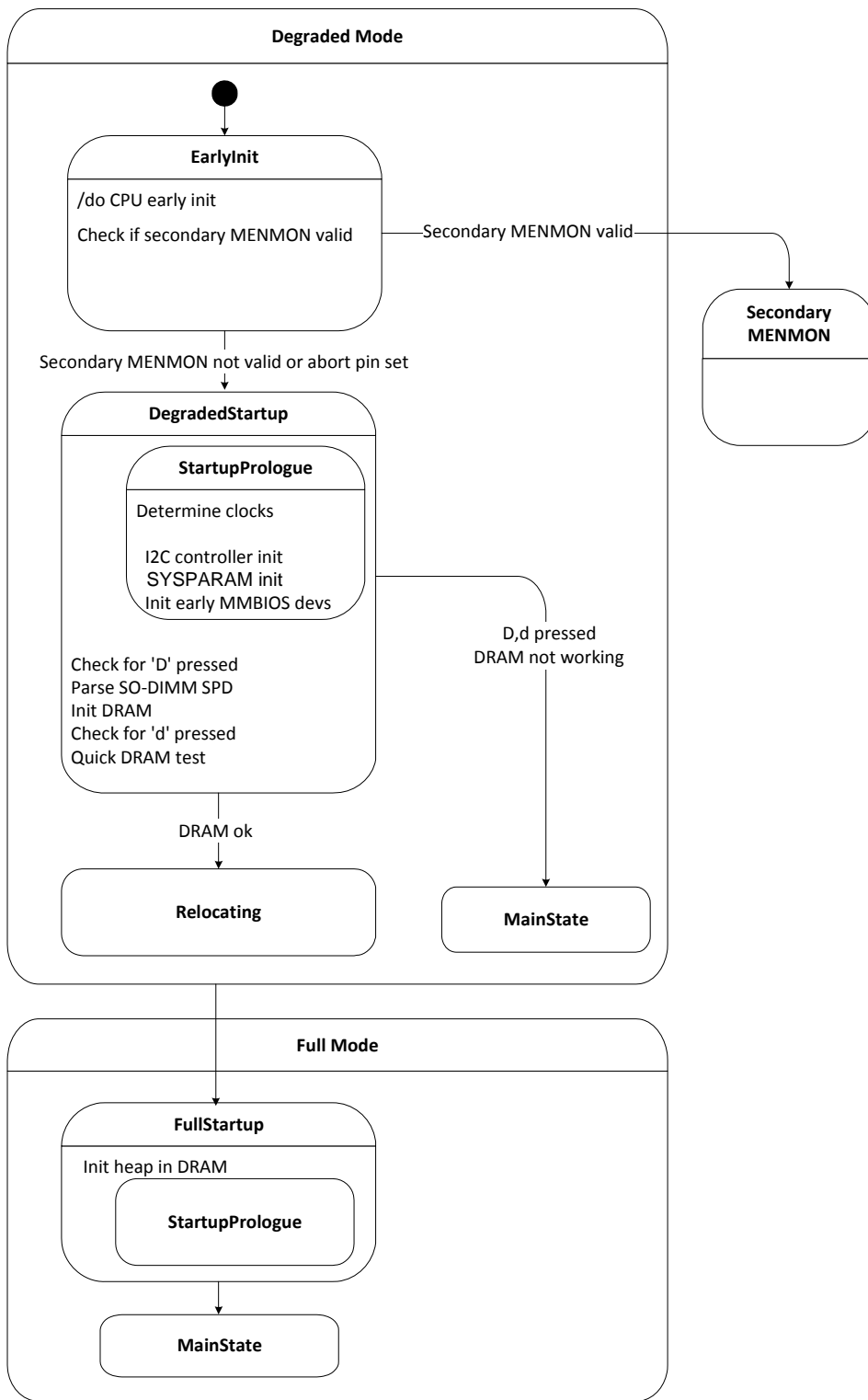
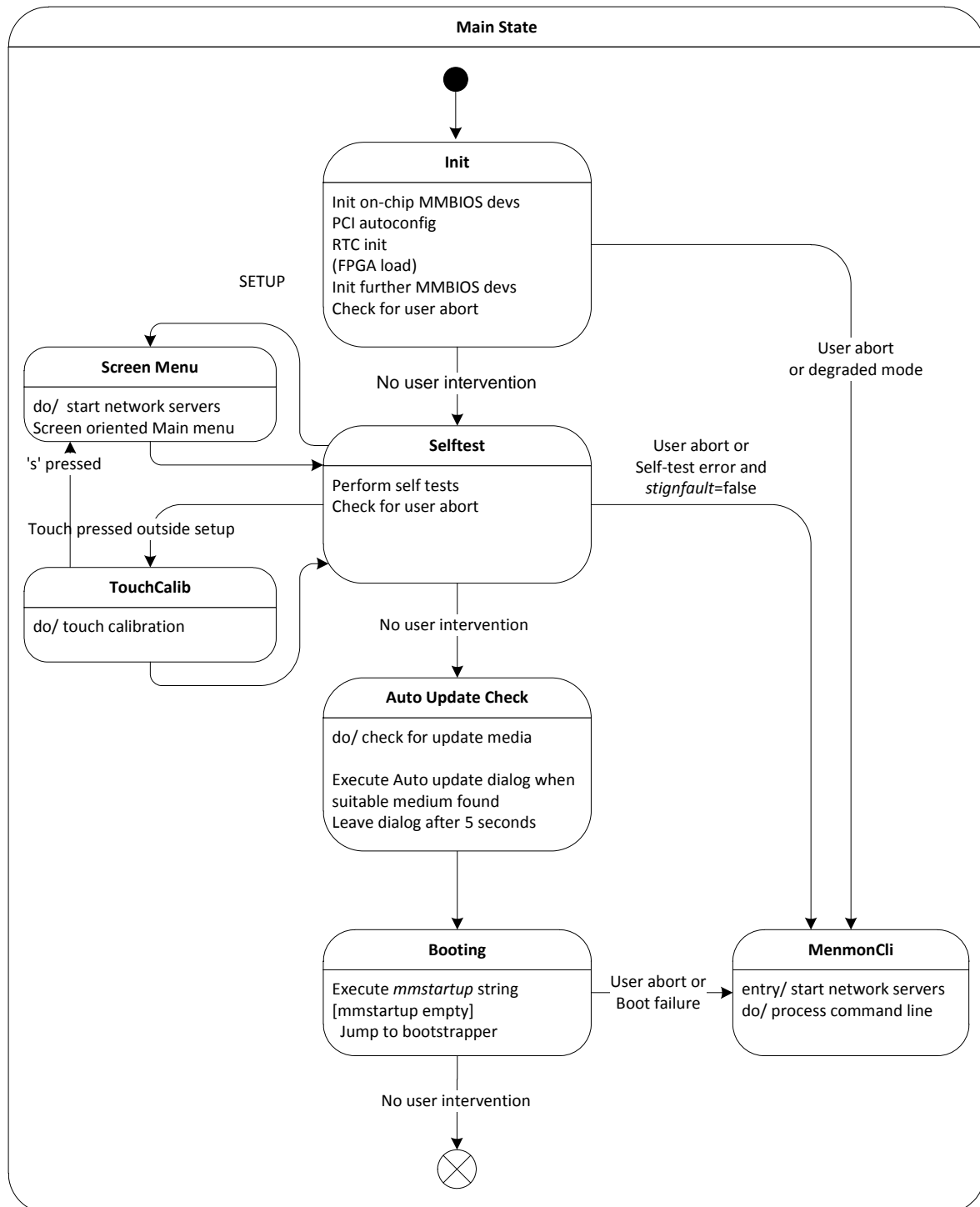


Figure 6. MENMON – State diagram, main state



3.2 Interacting with MENMON

To interact with MENMON, you can use the following consoles:

- UART-to-USB COM (via UART-to-USB interface)
- Touch panel / TFT interface (if present)
- Telnet via network connection
- HTTP */monpage* via network connection

The default setting of the COM ports is 9600 baud, 8 data bits, no parity, and one stop bit.

3.2.1 Entering the Setup Menu/Command Line

During normal boot, you can abort the booting process in different ways during the self-test, depending on your console:

- With a touch panel press the "Setup" button to enter the Setup Menu.
- With a text console press the "s" key to enter the Setup Menu.
- With a text console press "ESC" to enter the command line.

By default, the self-test is not left until 3 seconds have elapsed (measured from the beginning of the self-test), even if the actual test has finished earlier, to give the user a chance to abort booting and enter the Setup Menu.

You can modify the self-test wait time through MENMON system parameter *stwait* (see [page 57](#)).

3.3 Configuring MENMON for Automatic Boot

You can configure how MENMON boots the operating system either through the Setup Menu or through the command line.

In the Basic Setup Menu you can select the boot sequence for the bootable devices on the XM50. The selected sequence is stored in system parameter *mmstartup* as a string of MENMON commands. For example, if the user selects: "Int. CF, Ether, (None)", the *mmstartup* string will be set to "DBOOT 0; NBOOT TFTP".

You can view and modify this string directly, using the Expert Setup Menu, option *Startup string*, or through the command-line command *EE-MMSTARTUP*.



(See also [MENMON 2nd Edition User Manual](#) for further details.)

3.4 Calibrating the Touch Screen

You can enter the touch-panel calibration function through the Setup Main Menu.

This function is also entered automatically during the self-test, if you hit the touch screen at any position outside the "Setup" button. You may have missed the "Setup" button because the touch panel was incorrectly calibrated.

Follow the instructions on the screen to complete calibration.



(See also [MENMON 2nd Edition User Manual](#) for further details.)

3.5 Updating Boot Flash

3.5.1 Update via the Serial Console using *SERDL*

You can use command *SERDL* to update program data using the serial console.

The following table shows the XM50 locations:

Table 8. MENMON – Program update files and locations

File Name Extension	Typical File Name	Password for <i>SERDL</i>	Location
.SMM	14XM50-00_01_02.SMM	MENMON	Secondary MENMON
.Fxxx	MYFILE.F000	-	Starting at sector xxx in boot Flash
.Exx	MYFILE.E00	-	Starting at byte xx in EEPROM

3.5.2 Update from Network using *NDL*

You can use the network download command *NDL* to download the update files from a TFTP server in network. The file name extensions, locations and passwords are the same as for the *SERDL* command.

3.5.3 Update via Program Update Menu

MENMON scans an external medium connected to the first USB port (USB0) for files named *14XM50*.SMM*. The Program Update Menu will then give a list of all files on this medium conforming with this name pattern for selection.

3.5.4 Automatic Update Check

MENMON's automatic update check looks for some special files on an external medium connected to the first USB port (USB0). However, the XM50 implementation does not support program update here but can boot from the external medium.

The file that is searched for has a name stored in system parameter *bf* or *bootfile*, or – if this is empty – *BOOTFILE*. If this file is found, it is assumed that the external medium is supposed to be booted from.

To allow MENMON to locate this file, it must be in the root directory of a DOS FS. This works on unpartitioned media or on drives with one partition.

MENMON does not automatically start the boot but presents the following menu to the user:

```
Detected an update capable external medium

>Ignore, continue boot

Boot from external medium
```

If there is no user input for 5 seconds after the menu appears, booting continues.

3.5.5 Updating MENMON Code



Updates of MENMON are available for download from MEN's [website](#). MENMON's integrated Flash update functions allow you to do updates yourself. However, you need to take care and follow the instructions given here. Otherwise, you may make your board inoperable!



In any case, read the following instructions carefully!

Please be aware that you do MENMON updates at your own risk. After an incorrect update your CPU board may not be able to boot.

WARNING: After a MENMON update, the hardware revision displayed by MENMON will most probably be different from the actual hardware revision of your CPU board, because MENMON follows MEN's hardware revision updates.

Do the following to update MENMON:

- Unzip the downloaded file, e.g. *14xm50-00_01_02.zip*, into a temporary directory.
- Power on your XM50.
- Connect a terminal emulation program with the UART-to-USB port of your XM50 and set the terminal emulation program to 9600 baud, 8 data bits, 1 stop bit, no parity, no handshaking (if you haven't changed the target baud rate on your own).¹
- Reset the XM50 by pressing the reset button on the carrier board, or through software (e.g. reboot command under VxWorks).
- Press "ESC" immediately after resetting the XM50.
- In your terminal emulation program, you should see the "MenMon>" prompt.
- Enter "SERDL MENMON" to update the secondary MENMON. You should now see a "C" character appear every 3 seconds.
- In your terminal emulation program, start a "YModem" download of file *14xm50-00_01_02.smm* (for example, with Windows Hyperterm, select *Transfer > Send File* with protocol "YModem").
- When the download is completed, reset the XM50.

¹ You can change the baud rate at runtime using command *cons-baud*. See [Table 26, MENMON – Command reference \(page 60\)](#). If you want to accelerate file transfer you can select a higher baud rate in MENMON and then set the terminal emulation program accordingly.

3.6 Diagnostic Tests

3.6.1 Ethernet

Table 9. MENMON – Diagnostic tests: Ethernet

Test Name	Description	Availability
<i>ETHER0</i> <i>ETHER1</i> <i>ETHER2</i>	Ethernet 0/1/2 (ETHA/B/C) internal loopback test Groups: POST AUTO	Always (except ETHER2 with an MPC8543 processor)
<i>ETHER0_X</i> <i>ETHER1_X</i> <i>ETHER2_X</i>	Ethernet 0/1/2 (ETHA/B/C) external loopback test Groups: NONAUTO ENDLESS	Always (except ETHER2 with an MPC8543 processor)

3.6.1.1 Ethernet Internal Loopback Test

The test

- configures the network interface for loopback mode (on PHY)
- verifies that the interface's ROM has a good checksum
- verifies that the MAC address is valid (not 0xFFFFFFFF...)
- sends 10 frames with 0x400 bytes payload each
- verifies that frames are correctly received on the same interface.

If the network interface to test is the currently activated interface for the MENMON network stack, the interface is detached from the network stack during test and reactivated after test.

Checks:

- Connection between CPU and LAN controller
- Connection between LAN controller and PHY

Does not check:

- Connection between PHY and physical connector
- Interrupt line
- All LAN speeds

3.6.1.2 Ethernet External Loopback Test

This test is the same as the Ethernet Internal Loopback Test, but requires an external loopback connector. Before sending frames, the link state is monitored. If it is not ok within 2 seconds, the test fails.

Note: A loopback connector makes a connection between the following pins of the 8-pin Ethernet connector: 1-3, 2-6, 4-7, 5-8.

Checks:

- Connection between CPU and LAN controller
- Connection between LAN controller and PHY
- Connection between PHY and physical connector

Does not check:

- Interrupt line
- All LAN speeds

3.6.2 SDRAM, SRAM and FRAM

Table 10. MENMON – Diagnostic tests: SDRAM, SRAM and FRAM

Test Name	Description	Availability
<i>SDRAM</i>	Quick SDRAM connection test Groups: POST AUTO	Always
<i>SDRAM_X</i>	Full SDRAM test Groups: NONAUTO ENDLESS	Always
<i>SRAM</i>	Quick SRAM test Groups: POST AUTO	XM50 is known to have SRAM
<i>SRAM_X</i>	Full SRAM test Groups: NONAUTO ENDLESS	
<i>FRAM</i>	Quick FRAM test Groups: POST AUTO	XM50 is known to have FRAM
<i>FRAM_X</i>	Full FRAM test Groups: NONAUTO ENDLESS	

3.6.2.1 Quick RAM Test

This quick test checks most of the connections to the RAM chips but does not test all RAM cells. It executes very quickly (within milliseconds).

This test is non-destructive (saves/restores original RAM content).

Checks:

- All address lines
- All data lines
- Byte enable signals
- Indirectly, checks clock and other control signals

Does not check:

- SDRAM cells
- Burst mode

3.6.2.2 Extended RAM Test

This full-featured memory test allows to test all RAM cells. Depending on the size of the SDRAM, this test can take up to one minute.

It tests 8-, 16- or 32-bit access, each with random pattern, and single and burst access.

On each pass, this test first fills the entire memory (starting with the lowest address) with the selected pattern, using the selected access mode, and then verifies the entire block.

This test is destructive.

Checks:

- All address lines
- All data lines
- All control signals
- All SDRAM cells

3.6.3 EEPROM

Table 11. MENMON – Diagnostic tests: EEPROM

Test Name	Description	Availability
EEPROM	I2C access/Magic nibble check Groups: POST AUTO ENDLESS	Always

This test reads the first EEPROM cell over SMB and checks if bits 3..0 of this cell contain the magic nibble 0xE.

3.6.4 USB

Table 12. MENMON – Diagnostic tests: USB

Test Name	Description	Availability
USB0..USB5	USB device access / sector 0 access Groups: NONAUTO ENDLESS	Always

The test performs a sector 0 read from the Flash disk without verifying the content of the sector.

Checks:

- USB control lines (Data - / Data+)
- Basic USB transfer

Does not check:

- IRQ signals
- Partition table or file system on disk

3.6.5 Hardware Monitor Test

Table 13. MENMON – Diagnostic tests: hardware monitor

Test Name	Description	Availability
LM81	LM81 basic access test Groups: POST AUTO	Always

3.6.6 Touch

Table 14. MENMON – Diagnostic tests: touch

Test Name	Description	Availability
TOUCH	Touch controller communication test Groups: POST AUTO ENDLESS	Carrier board is known to have a touch controller

This test tries to communicate over the SPI bus with the touch controller on the carrier board by sending an Identify command to the controller.

Checks:

- SPI connection to touch controller

Does not check:

- Connection between touch controller and touch panel

3.6.7 RTC

Table 15. MENMON – Diagnostic tests: RTC

Test Name	Description	Availability
<i>RTC</i>	Quick presence test of RTC Groups: POST AUTO	Always
<i>RTC_X</i>	Extended test of RTC Groups: NONAUTO ENDLESS	Always

3.6.7.1 RTC Test

This is a quick presence test of the real-time clock (RTC) and is executed on POST.

Checks:

- Presence of RTC (I2C access)

Does not check:

- If RTC is running
- RTC backup voltage

3.6.7.2 Extended RTC Test

Checks:

- Presence (e.g. I2C access)
- RTC is running

Does not check:

- RTC backup voltage

3.7 MENMON Configuration and Organization

3.7.1 Consoles

You can select the active consoles by means of system parameters *con0..con3* and configure the console through parameters *ecl*, *gcon*, *hdp* and *tdp*. MENMON commands *CONS(-xxx)* also give access to the console settings (see [Chapter 3.8 MENMON Commands \(page 60\)](#)).

Table 16. MENMON – System parameters for console selection and configuration

Parameter (alias)	Description	Default	User Access
<i>cbr (baud)</i>	Baud rate of all UART consoles (decimal) (default: 9600 baud, 8n1)	9600	Read/write
<i>con0..con3</i>	CLUN of console 0..3 CLUN=0x00: disable CLUN=0xFF: Autoselect next available console <i>con0</i> is implicitly the debug console	<i>con0</i> : 08 (UART-to-USB COM) <i>con1</i> : 00 (none) <i>con2</i> : 00 (none) <i>con3</i> : 00 (none)	Read/write
<i>ecl</i>	CLUN of attached network interface (hex) CLUN=0x00: none CLUN=0xFF: first available Ethernet	0xFF	Read/write
<i>gcon</i>	CLUN of graphics device to display boot logo CLUN=0x00: disable CLUN=0xFF: Autoselect first available graphics console	0xFF (AUTO)	Read/write
<i>hdp</i>	HTTP server TCP port (decimal) 0: don't start telnet server -1: use default port 23 else: TCP port for telnet server	-1	Read/write
<i>tdp</i>	Telnet server TCP port (decimal) 0: don't start HTTP server -1: use default port 80 else: TCP port for HTTP server	-1	Read/write

3.7.2 Abort Pin

Since the XM50 has no real "abort" button, it is simulated by connecting pin 1 to pin 2 on the debug connector (TDI pin of debugger with GND).

If the abort pin is detected asserted, the secondary MENMON is not invoked and MENMON uses default parameters (such as baud rate, console port). This is useful if a secondary MENMON has been programmed that does not work or if you have misconfigured a system parameter.

Note that when a JTAG debugger is connected, the abort pin is always read as active.

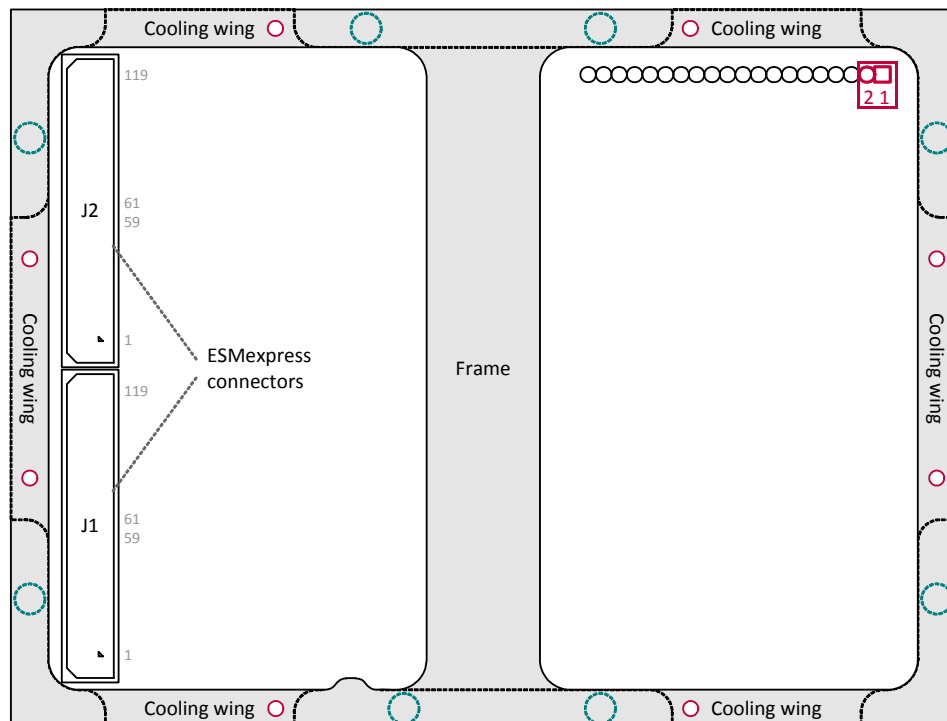


Note: The test connector is not assembled in standard versions of XM50. However, it is possible to connect the two pins. You should do so only if you are absolutely sure about what you are doing.

In any case, power off the system before you connect the abort pins!

The test connector pins are accessible at the bottom side of the PCB.

Figure 7. MENMON – Position of abort pins on test connector (bottom side)



3.7.3 MENMON Memory Map

3.7.3.1 MENMON Memory Address Mapping

Table 17. MENMON – Address map (full-featured mode)

Address Space	Size	Description
0x 0000 0000 .. 0000 1400	5 KB	Exception vectors
0x 0000 3000 .. 0000 3FFF	4 KB	MENMON parameter string
0x 0000 4200 .. 0000 42FF	256 bytes	VxWorks bootline
0x 0000 4300 .. 00FF FFFF	Nearly 16 MB	Free
0x 01D0 0000 .. 01DF FFFF	2 MB	Heap2
0x 01E0 0000 .. 01EF FFFF	1 MB	Text + Reloc
0x 01F0 0000 .. 01F1 FFFF	128 KB	Stack
0x 01F2 0000 .. 01F4 FFFF	128 KB	Stack for user programs and operating system boot
0x 01F5 0000 .. 01FE FFFF	640 KB	Heap
0x 01FF 0000 .. 01FF FFFF	64 KB	Not touched for OS post mortem buffer i.e. VxWorks WindView or MDIS debugs (requires ECC to be turned off!)
0x 0200 0000 .. End of RAM		Free or download area

3.7.3.2 Boot Flash Memory Map

Table 18. MENMON – Boot Flash memory map

Flash Offset	CPU Address	Size	Description
0x 00 0000	0x FF00 0000	14 MB (- 128 KB)	Available to user
0x DE 0000	0x FFDE 0000	128 KB	System parameter section in boot Flash (if <i>useflpar</i> system parameter is set to 1)
0x E0 0000	0x FFE0 0000	1 MB	Secondary MENMON
0x F0 0000	0x FFF0 0000	1 MB	Primary MENMON

3.7.4 MENMON BIOS Logical Units

The following table shows fixed assigned CLUNs. All other CLUNs are used dynamically.

Table 19. MENMON – Controller Logical Units (CLUNs)

CLUN	MENMON BIOS Name	Description
0x02	ETHER0	Ethernet #0 (ETHA)
0x03	ETHER1	Ethernet #1 (ETHB)
0x04	ETHER2	Ethernet #2 (ETHC)
0x06	USB	USB controller
0x08	UART-to-USB COM	MPC854X DUART channel #0
0x0A	TOUCH	Touch console (if present)
0x10	SATA0	SATA port 0
0x11	SATA1	SATA port 1
0x12	SATA2	SATA port 2
0x20		All other devices dynamically detected on PCI or FPGA devices
0x40		Telnet console
0x41		HTTP monitor console

Table 20. MENMON – Device Logical Units (DLUNs)

CLUN/DLUN	MENMON BIOS Name	Description
0x06/0x00	USB	USB controller ¹
0x10/0x00	SATA0	Disk at SATA port 0
0x11/0x00	SATA1	Disk at SATA port 1
0x12/0x00	SATA2	Disk at SATA port 2

¹ The actual disks can be selected through command USBDP, see also [page 61](#).

3.7.5 System Parameters

System parameters are parameters stored in EEPROM. Some parameters are automatically detected by MENMON (such as CPU type and frequency). The parameters can be modified through the *EE-xxx* command via the command line.

3.7.5.1 Physical Storage of Parameters

Most parameters are stored in the 1024-byte serial EEPROM on the XM50.

If required, you can configure MENMON to store some strings in boot Flash rather than in EEPROM.

3.7.5.2 Start-up with Faulty EEPROM

If a faulty EEPROM is detected (i.e. the checksum of the EEPROM section is wrong), the system parameters will use defaults. The behavior is the same if the EEPROM is blank. The default baud rate is 9600.

3.7.5.3 XM50 System Parameters

Note: Parameters marked by "Yes" in section "Parameter String" are part of the MENMON parameter string.

Table 21. MENMON – XM50 system parameters – Autodetected parameters

Parameter (alias)	Description	Standard Default	Parameter String	User Access
<i>ccbclkhz</i>	CCB clock frequency (decimal, Hz)		Yes	Read-only
<i>clun</i>	MENMON controller unit number that MENMON used as the boot device (hexadecimal)		Yes	Read-only
<i>cons</i>	Selected console. Set to name of first selected console		Yes	Read-only
<i>cpu</i>	CPU type as ASCII string (e.g. "MPC8548E")		Yes	Read-only
<i>cpuclkhz</i>	CPU core clock frequency (decimal, Hz)		Yes	Read-only
<i>dlun</i>	MENMON device unit number that MENMON used as the boot device (hexadecimal)		Yes	Read-only
<i>flash0</i>	Flash size (decimal, kilobytes)		Yes	Read-only
<i>fram0</i>	FRAM size (decimal, kilobytes)		Yes	Read-only
<i>immr</i>	Physical address of CCSR register block		Yes	Read-only
<i>mem0</i>	RAM size (decimal, kilobytes)		Yes	Read-only
<i>mem1</i>	Size of SRAM ¹ (decimal, kilobytes)		Yes	Read-only
<i>memclkhz</i>	Memory clock frequency (decimal, Hz)		Yes	Read-only

Parameter (alias)	Description	Standard Default	Parameter String	User Access
<i>mm</i>	Info whether primary or secondary MENMON has been used for booting, either "smm" or "pmm"		Yes	Read-only
<i>mmst</i>	Status of diagnostic tests, as a string		Yes	Read-only
<i>nmac0/1/2</i>	MAC address of Ethernet interface x (0..n). Format e.g. "00112233445566". Set automatically according to serial number of the board		Yes	Read-only
<i>pciclk</i>	PCI bus clock frequency = system input clock (decimal, Hz)		Yes	Read-only
<i>rststat</i>	Reset status code as a string, see Chapter 3.7.5.4 Reset Cause – Parameter rststat on page 59		Yes	Read-only
<i>usbdp</i>	USB boot device path in format "bus>1st_port_no>...>last_port_no" (e.g. "00>02>01" for USB bus = 0, port no. 1 = 2, port no. 2 = 1)		Yes	Read-only

¹ If implemented.

Table 22. MENMON – XM50 system parameters – Production data

Parameter (alias)	Description	Standard Default	Parameter String	User Access
<i>brd</i>	Board name	-	Yes	Read-only
<i>brdmod</i>	Board model "mm"	-	Yes	Read-only
<i>brdrev</i>	Board revision "xx.yy.zz"	-	Yes	Read-only
<i>prodat</i>	Board production date MM/DD/YYYY	-	Yes	Read-only
<i>repdat</i>	Board last repair date MM/DD/YYYY	-	Yes	Read-only
<i>sernbr</i>	Board serial number	-	Yes	Read-only

Table 23. MENMON – XM50 system parameters – MENMON persistent parameters

Parameter (alias)	Description	Standard Default	Parameter String	User Access
<i>bsadr (bs)</i>	Bootstrapper address. Used when BO command was called without arguments. (hexadecimal, 32 bits)	0	No	Read/write
<i>cbr (baud)</i>	Baudrate of all UART consoles (dec)	9600	Yes	Read/write
<i>con0..con3</i>	CLUN of console 0..3. (hex) (see Chapter 3.7.1 Consoles on page 51)	0xFF = auto	No	Read/write
<i>eccsth</i>	ECC single-bit error threshold	32	No	Read/write
<i>ecl</i>	CLUN of attached network interface (hex)	0xFF	No	Read/write
<i>gcon</i>	CLUN of graphics screen (hex) (see Chapter 3.7.1 Consoles on page 51)	0xFF = auto	No	Read/write
<i>hdp</i>	HTTP server TCP port (decimal)	-1	No	Read/write
<i>kerpar</i>	Linux Kernel Parameters (399 chars max). Part of VxWorks bootline if <i>useflpar=0</i> . (400 chars max if <i>useflpar=1</i>)	Empty string	No	Read/write
<i>ldlogodis</i>	Disable load of boot logo (bool)	0	No	Read/write
<i>mmstartup (startup)</i>	Start-up string 256 chars max if <i>useflpar=0</i> 512 chars max if <i>useflpar=1</i>	Empty string	No	Read/write
<i>nobanner</i>	Disable ASCII banner on start-up	0	No	Read/write
<i>noecc</i>	Do not use ECC even if board supports it (bool)	0	No	Read/write
<i>nspeed0/1/3</i>	Speed setting for Ethernet interface 0..3. Possible values: <i>AUTO</i> , <i>10HD</i> , <i>10FD</i> , <i>100HD</i> , <i>100FD</i> , <i>1000</i>	AUTO	Yes	Read/write
<i>stdis</i>	Disable POST (bool)	0	No	Read/write
<i>stdis_XXX</i>	Disable POST test with name XXX (bool) <i>stdis_ether</i> – Internal ETHER0/1/2 loopback <i>stdis_fram</i> – FRAM test ¹ <i>stdis_sram</i> – SRAM test ² <i>stdis_touch</i> – Touch controller test	0	No	Read/write
<i>stignfault</i>	Ignore POST failure, continue boot (bool)	1	No	Read/write
<i>stwait</i>	Time in 1/10 seconds to stay at least in SELFTEST state (decimal) 0 = Continue as soon as POST has finished	30	No	Read/write

Parameter (alias)	Description	Standard Default	Parameter String	User Access
<i>tdp</i>	Telnet server TCP port (decimal)	-1	No	Read/write
<i>tries</i>	Number of network tries	20	No	Read/write
<i>tto</i>	Minimum timeout between network retries (decimal, in seconds)	0	No	Read/write
<i>u00..u15</i>	User parameters (hex, 16 bits)	0x0000	No	Read/write
<i>updcdis</i>	Disable auto update check (bool)	0	No	Read/write
<i>useflpar</i>	Store <i>kerpar</i> and <i>mmstartup</i> parameters in boot Flash rather than in EEPROM (bool)	0	No	Read/write
<i>vmode</i>	Vesa Video Mode for graphics console (hex)	0x0101	No	Read/write
<i>wdt</i>	Time after which watchdog timer shall reset the system after MENMON has passed control to operating system (decimal, in 1/10 s) If 0, MENMON disables the watchdog timer before starting the operating system. Note: The XM50 watchdog supports only the following values: 0: Disable watchdog timer 11: Short time-out (1.12 seconds) 260: Long time-out (26.0 seconds)	0 (disabled)	No	Read/write

¹ If FRAM is implemented.

² If SRAM is implemented.

Table 24. MENMON – XM50 system parameters – VxWorks bootline parameters

Parameter (alias)	Description	Standard Default	Parameter String	User Access
<i>bf (bootfile)</i>	Boot file name (127 chars max)	Empty string	No	Read/write
<i>bootdev</i>	VxWorks boot device name	Empty string	No	Read/write
<i>e (netip)</i>	IP address, subnet mask, e.g. 192.1.1.28:ffff00	Empty string	No	Read/write
<i>g (netgw)</i>	IP address of default gateway	Empty string	No	Read/write
<i>h (nethost)</i>	Host IP address (used when booting over <i>NBOOT TFTP</i>)	Empty string	No	Read/write
<i>hostname</i>	VxWorks name of boot host	Empty string	No	Read/write
<i>netaddr</i>	Access the IP address part of <i>netip</i> parameter		No	Read/write
<i>netsm</i>	Access the subnet mask part of <i>netip</i> parameter		No	Read/write
<i>procnum</i>	VxWorks processor number (decimal)	0	No	Read/write
<i>s</i>	VxWorks start-up script	Empty string	No	Read/write
<i>tn (netname)</i>	Host name of this machine	Empty string	No	Read/write
<i>unitnum</i>	VxWorks boot device unit number (decimal)	0	No	Read/write

3.7.5.4 Reset Cause – Parameter *rststat*

The following *rststat* values are possible:

When MENMON starts up, it determines the reset cause and sets system parameter *rststat* accordingly:

Table 25. MENMON – Reset causes through system parameter *rststat*

<i>rststat</i> Value	Description
<i>cbrst</i>	Board was reset by carrier board
<i>pwon</i>	Power On
<i>swrst</i>	Board was reset by software (by means of the board's reset controller).
<i>wdog</i>	Board was reset by watchdog timer unit

3.8 MENMON Commands

The following table gives all MENMON commands that can be entered on the XM50 MENMON prompt. You can call this list also using the *H* command.

Table 26. MENMON – Command reference

Command	Description
.[<reg>] [<val>]	Display/modify registers in debugger model
ACT [<addr>] [<size>]	Execute a HWACT script
ARP	Dump network stack ARP table
B[DC<no>] [<addr>]	Set/display/clear breakpoints
BIOS_DBG <mask> [net] cons <clun>	Set MENMON BIOS or network debug level, set debug console
BO [<addr>] [<opts>]	Call OS bootstrapper
BOOTP [<opts>]	Obtain IP config via BOOTP
C[BWLLNAX#] <addr> [<val> ...]	Change memory
CHAM [<clun>]	Dump FPGA Chameleon table
CONS	Show active consoles
CONS-ACT <clun1> [<clun2>] ...	Test console configuration
CONS-BAUD <baud>	Change baud rate instantly without storing
CONS-GX <clun>	Test graphics console
D [<addr>] [<cnt>]	Dump memory
DBOOT [<clun>] [<dlun>] [<opts>]	Boot from disk
DCACHE OFF ON	Enable/disable data cache
DIAG [<which>] [VTF]	Run diagnostic tests
DSKRD <args>	Read blocks from RAW disk
DSKWR <args>	Write blocks to RAW disk
EE[-xxx] [<arg>]	Persistent system parameter commands
EER[-xxx] [<arg>]	Raw serial EEPROM commands
ERASE <D> [<O>] [<S>]	Erase Flash sectors
FI <from> <to> <val>	Fill memory (byte)
GO [<addr>]	Jump to user program
H HELP	Print help
I [<D>]	List board information
ICACHE OFF ON	Enable/disable instruction cache
IOI	Scan for BIOS devices
LM81	Show current voltage and temperature values
LOGO	Display MENMON start-up text screen
LS <clun> <dlun> [<opts>]	List files/partitions on device

Command	Description
MC <addr1> <addr2> <cnt>	Compare memory
MII <clun> [<reg>] [<val>]	Ethernet MII register command
MO <from> <to> <cnt>	Move (copy) memory
MS <from> <to> <val>	Search pattern in memory
MT [<opts>] <start> <end> [<runs>]	Memory test
NBOOT [<opts>]	Boot from network
NDL [<opts>]	Update Flash from network
NETSTAT	Show current state of networking parameters
PCI	PCI probe
PCIC <dev> <addr> [<bus>] [<func>] [<val>]	PCI config register change
PCID[+] <dev> [<bus>] [<func>]	PCI config register dump
PCIR	List PCI resources
PCI-VPD[-] <devNo> [<busNo>] [<capId>]	PCI Vital Product Data dump
PFLASH <D> <O> <S> [<A>]	Program Flash
PGM-XXX <args>	Media copy tool
PING <host> [<opts>]	Network connectivity test
RELOC	Relocate MM to RAM
RST	Cause an instant system reset
RTC[-xxx] [<arg>]	Real time clock commands
S [<addr>]	Single step user program
SERDL [<passwd>]	Update Flash using YModem protocol
SETUP	Open interactive Setup menu
UNZIP src size [<opt>] [<dest>] [<size>]	Unzip memory zipped by <i>gzip</i>
USB [<bus>]	Init USB controller and devices on a USB bus
USBT [<bus> <p1>.. <p5>]< td=""> <td>Shows the USB device tree</td> </p5>]<>	Shows the USB device tree
USBDP [<bus p1..p5>] [-d<x>]	Display/modify USB device path

4 Organization of the Board

To install software on the board or to develop low-level software it is essential to be familiar with the board's address and interrupt organization.

4.1 Memory Mappings

Table 27. Memory map – processor view

CPU Address Range	Size	Description
0x 0000 0000 .. End of RAM	512/1024/ 2048 MB	SDRAM
0x 8000 0000 .. DFFF FFFF	1536 MB	PCIe Memory Space
0x E000 0000 .. E7FF FFFF	128 MB	PCI1 Memory Space
0x E800 0000 .. EFFF FFFF	128 MB	PCI2 Memory Space
0x F000 0000 .. F00F 0000	128 MB	CCSR
0x F200 0000 .. F200 3FFF		Config PLD
0x F300 0000 .. F301 FFFF		FRAM (opt.)
0x F400 0000 .. F41F FFFF		SRAM (opt.)
0x FB00 0000 .. FBFF FFFF	16 MB	PCIe I/O / ISA Space
0x FC00 0000 .. FC00 7FFF	32 KB	PCI1 I/O Space
0x FF00 0000 .. FFFF FFFF	16 MB	Flash

Table 28. Address mapping for PCI

CPU Address Range	Interface	Mapped to PCI Space	Description
0x 8000 0000 .. 9FFF FFFF	PCIe	0x 8000 0000 .. 9FFF FFFF (MEM)	PCIe memory space (prefetchable BARs)
0x A000 0000 .. DFFF FFFF	PCIe	0x A000 0000 .. DFFF FFFF (MEM)	PCIe memory space (non-prefetchable BARs)
0x E000 0000 .. E7FF FFFF	PCI1	0x E000 0000 .. E7FF FFFF (MEM)	PCI1 memory space
0x E700 0000 .. EFFF FFFF	PCI2 ¹	0x E700 0000 .. EFFF FFFF (MEM)	PCI2 memory space
0x FB00 0000 .. FBFE FFFF	PCIe	0x 0000 0000 .. 00FE FFFF (ISA)	PCIe ISA memory
0x FBFF 8000 .. FBFF FFFF	PCIe	0x 0000 .. 7FFF (I/O)	PCIe I/O space
0x FC00 0000 .. FC00 7FFF	PCI1	0x 8000 .. FFFF (I/O)	PCI1 I/O space

¹ PCI2 not available for MPC8543.

4.2 Interrupt Handling

Interrupt handling is done via the 12 external interrupt lines of the CPU (IRQ[11:0]). While IRQ lines 8 to 10 are used as PCI interrupt lines and lines 0 to 3 for PCIe (see tables below), the Ethernet function unit interrupt is routed to a dedicated interrupt line. The mapping is as follows:

Table 29. Dedicated interrupt line assignment

MPC854X External Interrupt Line	Function
IRQ0	Ethernet

Table 30. PCI IRQ line mapping

MPC854X IRQ Input	PCI Interrupt Line	Function	Assigned Number (MENMON)
IRQ8	INTA	SATA	0x8
IRQ9	INTB	1st USB Controller (USB0/1/2)	0x9
IRQ10	INTC	2nd USB Controller (USB3/4/5)	0xA

Table 31. PCIe IRQ line mapping

MPC854X IRQ Input	PCI Interrupt Line (PCIe Interface)	Assigned Number (MENMON)
IRQ0	INTA	0xF0
IRQ1	INTB	0xF1
IRQ2	INTC	0xF2
IRQ3	INTD	0xF3

4.3 SMB Devices

Table 32. SMB devices

I ² C Bus	Address	Function
0x0	0x5E	LM81 hardware monitor
	0xA2	Real-time clock
	0xA8	CPU EEPROM
	0xD2	Clock generator
0x1	0xAC	Reserved for carrier board EEPROM

4.4 Onboard PCI Devices

Table 33. *Onboard PCI devices*

Interface	Device Number	Vendor ID	Device ID	Function	Interrupt
PCI1	0x00	0x1057	0x0013	PCI host bridge in MPC854X	-
	0x10	0x1095	0x3114	SATA	INTA
PCI2	0x00	0x1057	0x0013	PCI host bridge in MPC854X	-
	0x11	0x1033	0x0035/ 0x00E0	1st USB Controller (USB0/1/2)	INTB
	0x12	0x1033	0x0035/ 0x00E0	2nd USB Controller (USB3/4/5)	INTC
PCIe	0x00	0x1957	0x0013	PCIe bridge in MPC854X	-

5 Appendix



5.1 Literature and Web Resources

- XM50 data sheet with up-to-date information and documentation:
www.men.de/products/15XM50-.html
- XC1 data sheet with up-to-date information and documentation:
www.men.de/products/08XC01-.html

5.1.1 PowerPC

- MPC8548:
MPC8548E PowerQUICC™ III Integrated Processor Family Reference Manual
MPC8548ERM; 2007; Freescale Semiconductor, Inc.
www.freescale.com

5.1.2 SATA

- Serial ATA International Organization (SATA-IO)
www.serialata.org

5.1.3 USB

- USB Implementers Forum, Inc.
www.usb.org

5.1.4 Ethernet

- ANSI/IEEE 802.3-1996, Information Technology - Telecommunications and Information Exchange between Systems - Local and Metropolitan Area Networks - Specific Requirements - Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications; 1996; IEEE
www.ieee.org
- Charles Spurgeon's Ethernet Web Site
Extensive information about Ethernet (IEEE 802.3) local area network (LAN) technology.
www.ethermanage.com/ethernet/
- InterOperability Laboratory, University of New Hampshire
This page covers general Ethernet technology.
www.iol.unh.edu/services/testing/ethernet/training/

5.1.5 PCI Express

- PCI Special Interest Group
www.pcisig.com

5.2 Finding out the Board's Article Number, Revision and Serial Number

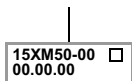
MEN user documentation may describe several different models and/or hardware revisions of the XM50. You can find information on the article number, the board revision and the serial number on two labels attached to the board.

- **Article number:** Gives the board's family and model. This is also MEN's ordering number. To be complete it must have 9 characters.
- **Revision number:** Gives the hardware revision of the board.
- **Serial number:** Unique identification assigned during production.

If you need support, you should communicate these numbers to MEN.

Figure 8. Labels giving the board's article number, revision and serial number

Complete article number



Revision number



Serial number