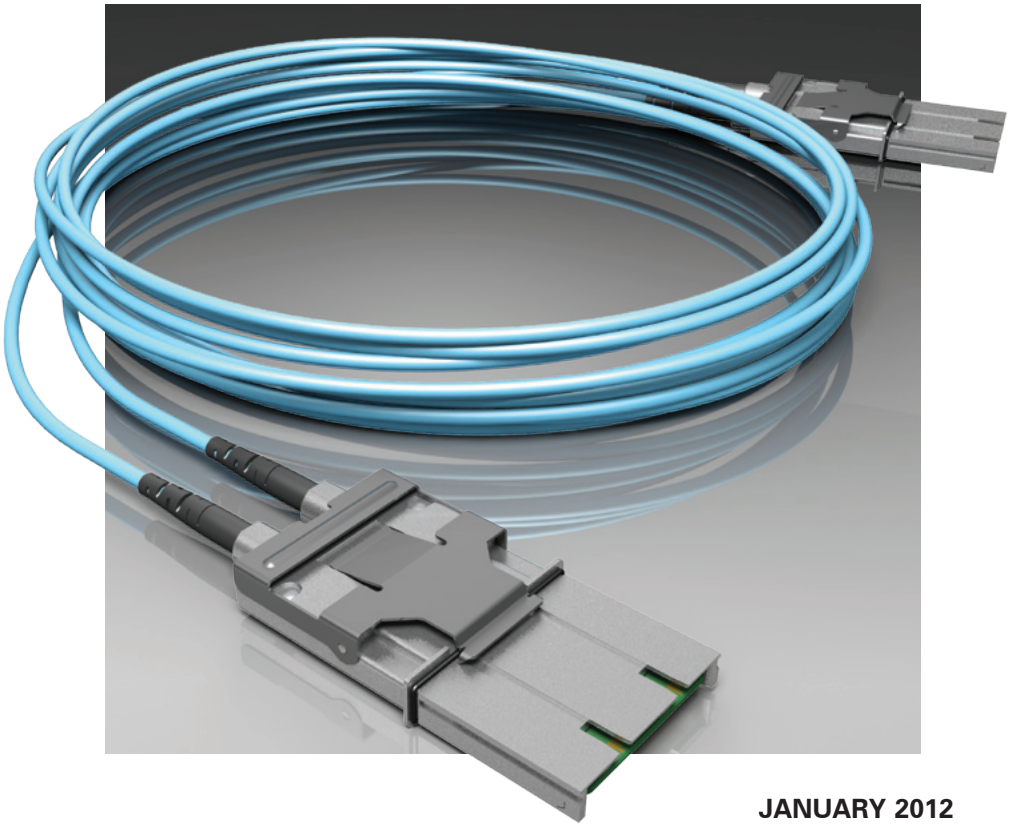
PCIe® x8
Active Optical Cable Assembly
User Manual



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Covering:

PCIE0 SERIES

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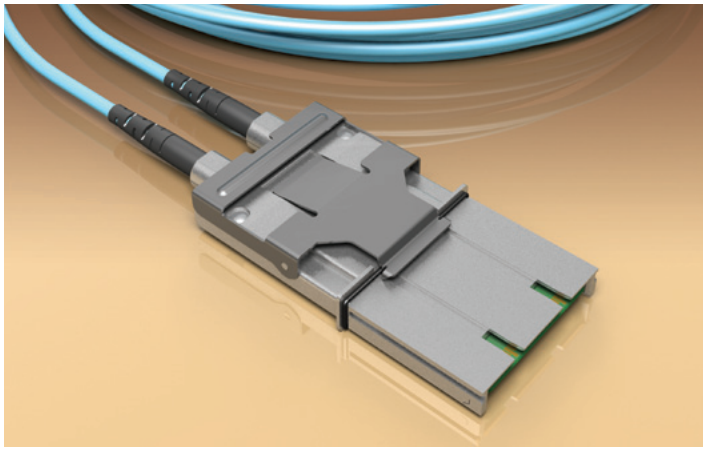
DESCRIPTION

PCIe® x8 Active Optical Cable Assembly is an 8 lane full duplex external cable assembly that is a direct replacement for copper or active copper cable assemblies. Each lane is capable of transmitting PCIe® signaling at Gen 1 (2.5 GT/s), Gen 2 (5 GT/s), and Gen 3 (8 GT/s). The cable can drive Gen 1 or Gen 2 signaling up to a distance of 300m and is also capable of supporting the emerging Gen 3 data rate at 100m distances. The electrical to optical conversion circuitry is fully integrated into the connector housing at each end of the assembly and the optical signal is transmitted over a small diameter optical fiber. The cable auxiliary signals (CPWRON, CPERST, CPRSNT and CWAKE) are also transmitted over the optical link.



Fiber Cable used in the PCIe® x8 AOC is a nonconductive plenum rated cable with a 3mm cable diameter and 30mm bend radius.

Cable Connector attached at each end of the fiber cable is a metalized housing that contains the electrical to optical components and mates to a standard x8 PCIe® electrical port.

Note: Unlike traditional copper cable, active optical PCIe® cables are directional. One end must be connected to the host system (upstream direction), and the other to the target system (downstream direction). The ends of the cable are labeled with Host and Target direction, and are not interchangeable.

SYSTEM REQUIREMENTS

Power

The PCIe® x8 AOC requires the host and target systems to provide 3.3 volts to connector pins B14, B15, and B16 at both ends of the cable assembly as described in the PCIe® cabling specification (optional feature). See the Connector Pin Assignment on page 10.

Note: The PCIe® cabling specification specifies power as an "option," and therefore, not all PCIe® systems provide power to the connector ports. Active Optical Cable Assemblies cannot be used with systems that do not provide power to the cable ports.

In systems that use the sideband signal "CWAKE," both ends of the Active Optical Cable Assembly must be powered at all times and, therefore, they must be powered by Vaux. In systems that do not use CWAKE, the cable ends may be powered by Vmain.

Clock

Constant Clock (CC): Active Optical Cables require the use of a constant clocking scheme. The PCIe® Active Optical Cable Assembly uses a constant clock frequency of 100 MHz as specified in PCIe® standard. If a clock frequency other than 100 MHz is required it must be specified at the time of purchasing the assembly.

Spread Spectrum Clock (SSC) is used in many systems running PCIe®. However, due to signaling technology limitations, the PCIe® standard cannot support SSC beyond 7m of link length. As noted in "Clock Constant" above, Active Optical Cables require the use of a constant clocking scheme. In order to use a PCIe® Active Optical Cable Assembly in a system that uses SSC clocking, the SSC must be completely disabled at the host. If disabling the SSC is not possible then a clock isolation adapter card will be required to isolate the SSC clock.

Note: Some motherboards allow SSC to be disabled; however, in some cases the disable function has a delay that allows the SSC to run for a period of time. Motherboards that delay the SSC disable function cannot be used with optical cable assemblies. Ensure that the motherboard you are using completely disables SSC or uses a clock isolation adapter card.

SYSTEM REQUIREMENTS

Adapter Cards

A Host adapter card and a Target adapter card that are compatible with Active Optical Cables should be installed at each end of the link. Adapter cards that have been qualified with the PCIe® x8 AOC are listed in Table 1 below.

Table 1: Compatible Adapter Cards

				Compatible with systems using:	
Vendor	**Part Number**	**Host / Target**	**Clock Isolation**	**SSC[1]**	**CC[2]**
Samtec Optical	PCIEA-H-8G2-01	Host	Yes	Yes	Yes
	PCIEA-T-8G2-01	Target	Yes	Yes	Yes
One Stop Systems	OSS-PCIe-HIB25-x8-H	Host	No	No	Yes
	OSS-PCIe-HIB25-x8-T	Target	No	No	Yes
Dolphin	IXH610 x8	Host	Yes	Yes	Yes
	IXH610 x8	Target	Yes	Yes	Yes

[1] Spread Spectrum Clocking
[2] Constant Clocking

Auxiliary (Sideband)

Signals (CPWRON, CPERST, CPRSNT and CWAKE) are also transmitted over the optical link. The link will be properly established if OSS or Samtec adapter cards are installed. If custom adapter cards are used, the PCI Express® External Cabling Specification 2.0 should be followed.

Note: Auxiliary sideband signal usage and implementation over copper cable varies widely between systems. For Active Optical Cable Assemblies sideband signals should preferably be implemented following the PCIe® 2.0 standard. At a minimum, the sideband signals CPERST and CPRSNT need to be connected, and their final state must conform to Table 2 below for the link to exchange data. CPWRON and CWAKE do not need to be connected, but if they are, their final state must be HIGH. If sidebands are to be ignored entirely, a special "no-sideband" cable can be purchased. Table 2 below summarizes the minimum sideband implementation requirements.

Table 2: Minimum Sideband Implementation Requirements

Sideband Signal	Driving End	Function	Required	End State
CPERST	Host	Reset	Yes[1]	High
CPRSNT	Target	Cable Present	Yes[1]	Low
CPWRON	Host	Power On	No	High
CWAKE	Target	Host Wakeup	No	High

[1] A "no-sideband" cable is available as an option for applications where sidebands are ignored.

INSTALLATION

Connecting AOC

Power to either the adapter card or motherboard should be in the **off** state prior to installing the cable assembly. Refer to the label on the connector ends to identify the host end of the cable assembly and the target end of the assembly. Insert the host end of the assembly into the host card and the target end into the target card ensuring the connector is fully seated and the latching mechanism is fully engaged with host connector. Apply power after the cable has been installed.

Power Sequence

PCIe® Active Optical Cables do not require a special powering sequence. But whether using an Active Optical Cable or a passive copper cable, it is critical that the target be powered prior to the PCIe® controller on the motherboard enumerates (searches and detects) all the PCIe® devices. There is a short delay from when the host is powered and then starts to enumerate, but to ensure that the target is powered prior to the host beginning its search it is good practice to apply power to the target side and then to the host side.

TECHNICAL INFORMATION

Equivalent Sideband IO Circuit

The sideband input signals are pulled high using an internal pull-up resistor (Rpu) of 20-50 kohms as shown in the equivalent IO circuit diagram below, Figure 1. Refer to Table 3 to determine which sideband signals are inputs to the host end of the cable and which signals are inputs to the target end of the link.

Figure 1: Equivalent Sideband IO Circuit

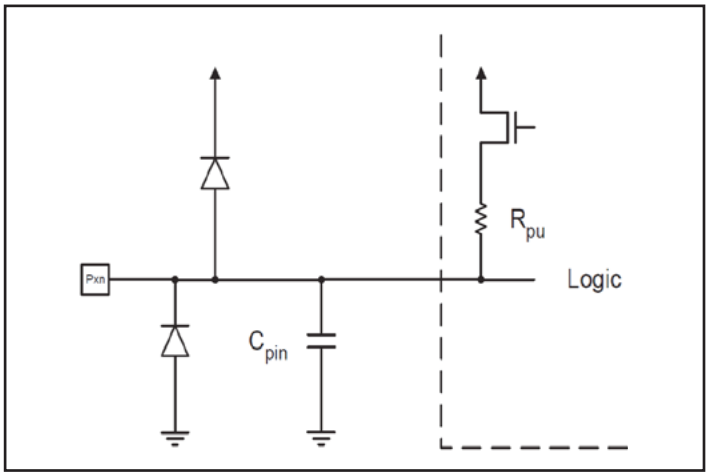


Table 3: Sideband Signal Input / Output Reference

SIDEBAND SIGNAL	Host Side	Pull-up	Target Side	Pull-up
CPWRON	Input	Yes	Output	N/A
CPERST	Input	No	Output	N/A
CPRSNT	Output	N/A	Input	Yes
CWAKE	Output	N/A	Input	Yes

Specifications

General Characteristics

SPECIFICATIONS	SYMBOL	UNIT	MIN	TYP.	MAX	NOTES
Operating Case Temperature	T_{CASE}	ºC	0		70	Case Temperature
Operating Humidity		%RH	5		90	Noncondensing
Storage Temperature Range	T_{STO}	ºC	-40		85	
Link Distance	m		0.5		300	(100m max at Gen 3 rate)

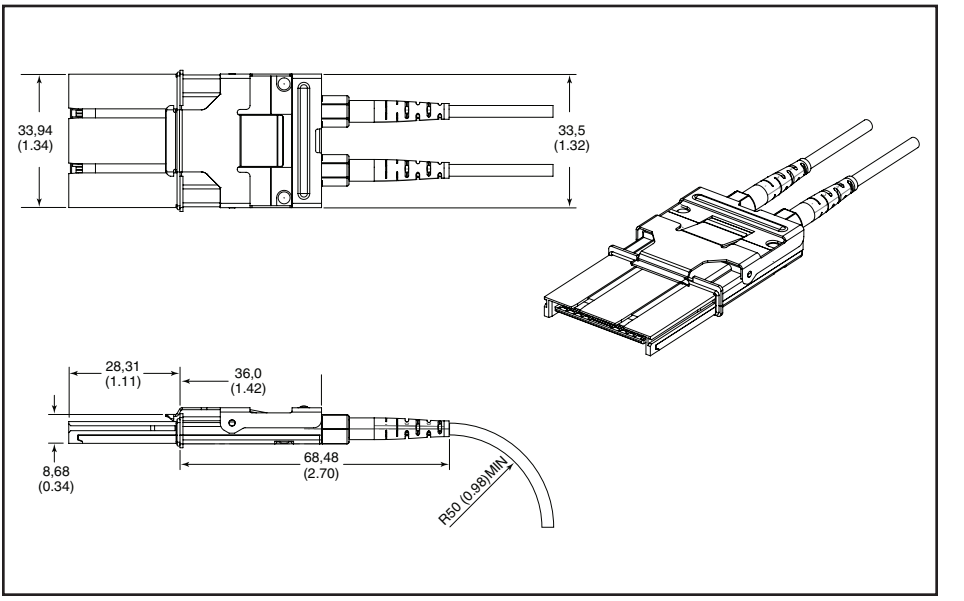
TECHNICAL INFORMATION

Electrical Characteristics

SPECIFICATIONS	SYMBOL	UNIT	MIN	TYP.	MAX	NOTES
Data Rate (channel)		GT/s	1	2.5/5.0/8.0	8.0	Gen 1 / Gen 2 / Gen 3
Differential Input Amplitude	V_{DI}	mV	300		1200	Peak to peak differential
Differential Output Amplitude	V_{DO}	mV		700		Peak to peak differential
Power Supply Voltage	V_{CC1}	V	3.15	3.3	3.45	Supplied through pins B14 and B15
Power Supply Current	I_{CC1}	mA		460		Per connector end
Power Consumption	P_{DISS}	W		1.5 [1]	2.0 [2]	Per connector end
Bit Error Rate	BER				10^{-15}	

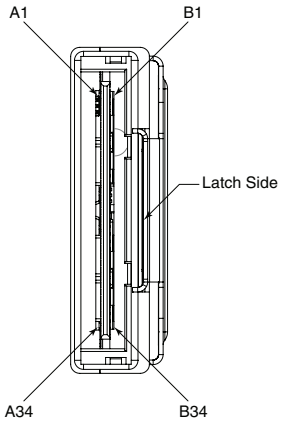
[1]Nominal supply voltage, room temperature.
[2]Maximum supply voltage, 75°C.

Mechanical Dimensions



TECHNICAL INFORMATION

Connector Pin Assignment



PIN#	Signal	Description	Notes
A1, A4, A7, A10, A13, A16, A22, A25, A28, A31, A34	GND	Ground reference for PCI Express® transmitter Lanes	
A2	PETp0	Differential PCI Express® transmitter Lane 0	
A3	PETn0	Differential PCI Express® transmitter Lane 0	
A5	PETp1	Differential PCI Express® transmitter Lane 1	
A6	PETn1	Differential PCI Express® transmitter Lane 1	
A8	PETp2	Differential PCI Express® transmitter Lane 2	
A9	PETn2	Differential PCI Express® transmitter Lane 2	
A11	PETp3	Differential PCI Express® transmitter Lane 3	
A12	PETn3	Differential PCI Express® transmitter Lane 3	
A14	CREFCLK+	Differential 100 MHz cable reference clock	1, 2
A15	CREFCLK-	Differential 100 MHz cable reference clock	1, 2
A17	NC		
A18	NC		
A19	SB_RTN	Signal return for single ended sideband signals	
A20	CPRSNT#	Used for detection of whether a cable is installed and the downstream subsystem is powered	1
A21	CPWRON	Turns power on / off to slave-type downstream subsystems	1
A23	PETp4	Differential PCI Express® transmitter Lane 4	
A24	PETn4	Differential PCI Express® transmitter Lane 4	
A26	PETp5	Differential PCI Express® transmitter Lane 5	
A27	PETn5	Differential PCI Express® transmitter Lane 5	
A29	PETp6	Differential PCI Express® transmitter Lane 6	
A30	PETn6	Differential PCI Express® transmitter Lane 6	
A32	PETp7	Differential PCI Express® transmitter Lane 7	
A33	PETn7	Differential PCI Express® transmitter Lane 7	

[1] Cable propagation of these signals is directional. Connect Host side to upstream system, Target side to downstream system.
[2] Constant 100 MHz Clocking only. For Spread Spectrum Clocking (SSC) support use our clock isolation adapter card (Available Q1, 2012).
[3] Must be connected to 3.3V (+/-5%) Vaux or Vmain
[4] Must be connected to Power Ground

TECHNICAL INFORMATION

PIN#	Signal	Description	Notes
B1, B4, B7, B10, B13, B22, B25, B28, B31, B34	GND	Ground reference for PCI Express® receiver Lanes	
B2	PERp0	Differential PCI Express® receiver Lane 0	
B3	PERn0	Differential PCI Express® receiver Lane 0	
B5	PERp1	Differential PCI Express® receiver Lane 1	
B6	PERn1	Differential PCI Express® receiver Lane 1	
B8	PERp2	Differential PCI Express® receiver Lane 2	
B9	PERn2	Differential PCI Express® receiver Lane 2	
B11	PERp3	Differential PCI Express® receiver Lane 3	
B12	PERn3	Differential PCI Express® receiver Lane 3	
B14	PWR	3.3V Cable power	3
B15	PWR	3.3V Cable power	3
B16	PWR	3.3V Cable power	3
B17	PWR RTN	Cable power return	4
B18	PWR RTN	Cable power return	4
B19	PWR RTN	Cable power return	4
B20	CWAKE#	Power management signal for wakeup events	1
B21	CPERST#	Cable PERST#	1
B23	PERp4	Differential PCI Express® receiver Lane 4	
B24	PERn4	Differential PCI Express® receiver Lane 4	
B26	PERp5	Differential PCI Express® receiver Lane 5	
B27	PERn5	Differential PCI Express® receiver Lane 5	
B29	PERp6	Differential PCI Express® receiver Lane 6	
B30	PERn6	Differential PCI Express® receiver Lane 6	
B32	PERp7	Differential PCI Express® receiver Lane 7	
B33	PERn7	Differential PCI Express® receiver Lane 7	

[1] Cable propagation of these signals is directional. Connect Host side to upstream system, Target side to downstream system.
[2] Constant 100 MHz Clocking only. For Spread Spectrum Clocking (SSC) support use our clock isolation adapter card (Available Q1, 2012).
[3] Must be connected to 3.3V (+/-5%) Vaux or Vmain
[4] Must be connected to Power Ground

PCIe® CABLE ASSEMBLY PART NUMBERING

PCIe® Active Optical Cable

PCIEO - 4G2 - 005.0 - 001

Product Category

Speed

x4 Gen2	4G2
x8 Gen2	8G2

Fiber Length

5m	005.0
10m	010.0
100m	100.0

Specific Product Variant

	Clock Frequency	Sideband
001	100	standard
002	100	Forced RF
003	100.3	standard
004	100.3	Forced RF
005	No CK	standard
006	No CK	Forced RF

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