2030 Computer Manual

Revision 1.4

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System Overview

Control of the 2030 Series systems is based on the Motorola MC68010 microprocessor running Microware Systems OS9 multitasking, multiple user operating system. This combination provides the ideal hardware and software foundation for the real-time control and computing requirements of the 2030 systems. The back plane used to communicate to the individual boards within the computer system is the Gespac G96 bus.

The standard computer system hardware configuration includes the MC68010 computer card, up to 8 M bytes of SRAM memory, a SASI/SCSI interface, a 40 M byte hard disk, cartridge streamer tape drive, floppy disk drive, and I/O controller card. The I/O controller card provides 4 serial ports, a printer port, and operator keypad port. Optional cards for the computer system include a IEEE-488 controller and local area network interface.

Digital test system emulator modules are interfaced to the computer system through the EMBus controller board. The EMBus controller supports up to 6 emulator modules.

The TBus controller board provides the interface to the analog Testhead. The TBus controller maps a section of the MC68010 memory for use by the boards of the Testhead. This is accomplished by extending the data and address buses of the G96 bus through optically coupled buffers to the analog Testhead.

Start	End	Description
$000000	$01FFFF	RAM, overlaid by ROM after reset (128 K bytes)
$020000	$FBE8FF	Available for RAM
$FBE900	$FBE9FF	2030 analog Testhead
$FBEA00	$FCFFFF	Available for RAM
$FD0000	$FD01FF	peripheral block 0 (512 bytes)
$FD0200	$FD03FF	peripheral block 1 (512 bytes)
$FD0400	$FD05FF	peripheral block 2 (512 bytes)
$FD0600	$FD07FF	peripheral block 3 (512 bytes)
$FD8000	$FD81FF	X2212P 4 bit EEPROM (odd addresses only)
$FD8200	$FD822F	MK68901 peripheral (odd addresses only)
$FD8240	$FD825F	MM58274 calendar (odd addresses only)
$FD8261		write "1" to remove ROM from low RAM area
$FD8281		SMC8136 baud rate generator
$FD82C2	$FD82C6	NS16081 floating point coprocessor option
$FE0000	$FFFFFF	ROM

Table 1 - 2030 Memory Map

Board	IRQ	Vector	Address	Device	I/O Mode	Vector Register
Testhead Controller	7 (NMI)	31	$FBE900	/AMSint	N/A (memory)	No (autovector)
MPU14A	6	74	$FD8201	/term (read)	Async.	Yes
		76	$FD8201	/term (write)	Async.	Yes
		70	$FD8201	abort button	Async.	Yes
		71	$FD8241	real time clock	Async.	Yes
		77	$FD8201	tick timer	Async.	Yes
Dual Serial Port Card	5	29	$FD07F1	/t5	Sync.	Yes (async mode)

Board	IRQ	Vector	Address	Device	I/O Mode	Vector Register
		29	$FD07F5	/t6	Sync.	Yes (async mode)
I/O Controller	4	80	$FD0001	/t1	Async.	Yes
		80	$FD0011	/t2	Async.	Yes
		81	$FD0021	/t3	Async.	Yes
		81	$FD0031	/t4	Async.	Yes
		82	$FD0041	/p	Async.	Yes
		82	$FD0041	/opif	Async.	Yes
		82	$FD0041	/kp	Async.	Yes
GPIB Controller	4	83	$FD0101	/g	Async.	Yes
EVLAN-11	3	65	$FD0400	/ev0	Async.	Yes
GESCNX	3	67	$FD04C0	/kbd	Async.	Yes
GESVIG	?	??	$FD0440	/crt	Async.	Yes
GESHDI	1	25	$FD0681	/s0 - /s3	Sync.	No (autovector)
GESFDC-2B	1	25	$FD0631	/f?	Sync.	No (autovector)
EMBus Controller	Unused		$FB8000		N/A (memory)	No (autovector)

Table 2 - G96 Interrupt Map

Notes for G96 Interrupt Map:
1. The polarity of IACK is active HIGH which follows the G64 convention.
2. Synchronous devices are autovectored.

IRQ Number	Mode
1	Autovectored
2	Undefined
3	Vectored
4	Vectored
5	Autovectored
6	Vectored (only used by the MPU14A board)
7	Autovectored

Table 3 - Interrupt Modes

Address Range	Mode
$FD0000-$FD01FF	Asynchronous
$FD0200-$FD03FF	Asynchronous
$FD0400-$FD05FF	Asynchronous
$FD0600-$FD07FF	Synchronous

Table 4 - Peripheral Addressing Modes

INSTALLATION

This section contains information regarding the shipment, inspection, installation and self test of the Series 2030 CPU. The Series 2030 CPU is shipped essentially ready for use when received. However, the following sections should be covered before attempting to operate the system.

RECEIVING INSPECTION

A close visual inspection should be performed promptly after the system has been received. Any evidence of rough handling should be reported to the shipper and to Digalog Systems.

Look for broken switches, scratched or dented panel surfaces, and for any other damage to the exterior of the unit. Also check the Terminal and cables for possible mishandling. If damages of any kind are found, refer to the procedures outlined in the warranty at the beginning of this manual.

The Emulator is shipped fully operational apart from the systems connections which must be made in accordance with Section 3.13. However, a careful inspection should be performed to ensure functionality.

POWER REQUIREMENTS

The Series 2030 CPU requires 115 VAC. A standard power cord is included. Care must be taken to ensure that the unit is grounded properly. If grounding outlets are not available, adapters with grounding connections must be used.

ENVIRONMENTAL OPERATING CONDITIONS

The Series 2030 CPU is designed for use between 10 and 40 degrees Celsius. A cooling fan is mounted on the front panel of the unit to provide cooling for the system's electronics. Care must be taken to ensure that fan openings remain uncovered for proper air flow.

DAMAGE may occur if the filters are not periodically cleaned.

EXTERNAL CABLES AND CONNECTIONS

Depending on the system configuration, cable connections will need to be made between some or all of the following devices: Computer, Terminal, Printer, Keypad, Testhead, Emulator and GPIB Instruments.
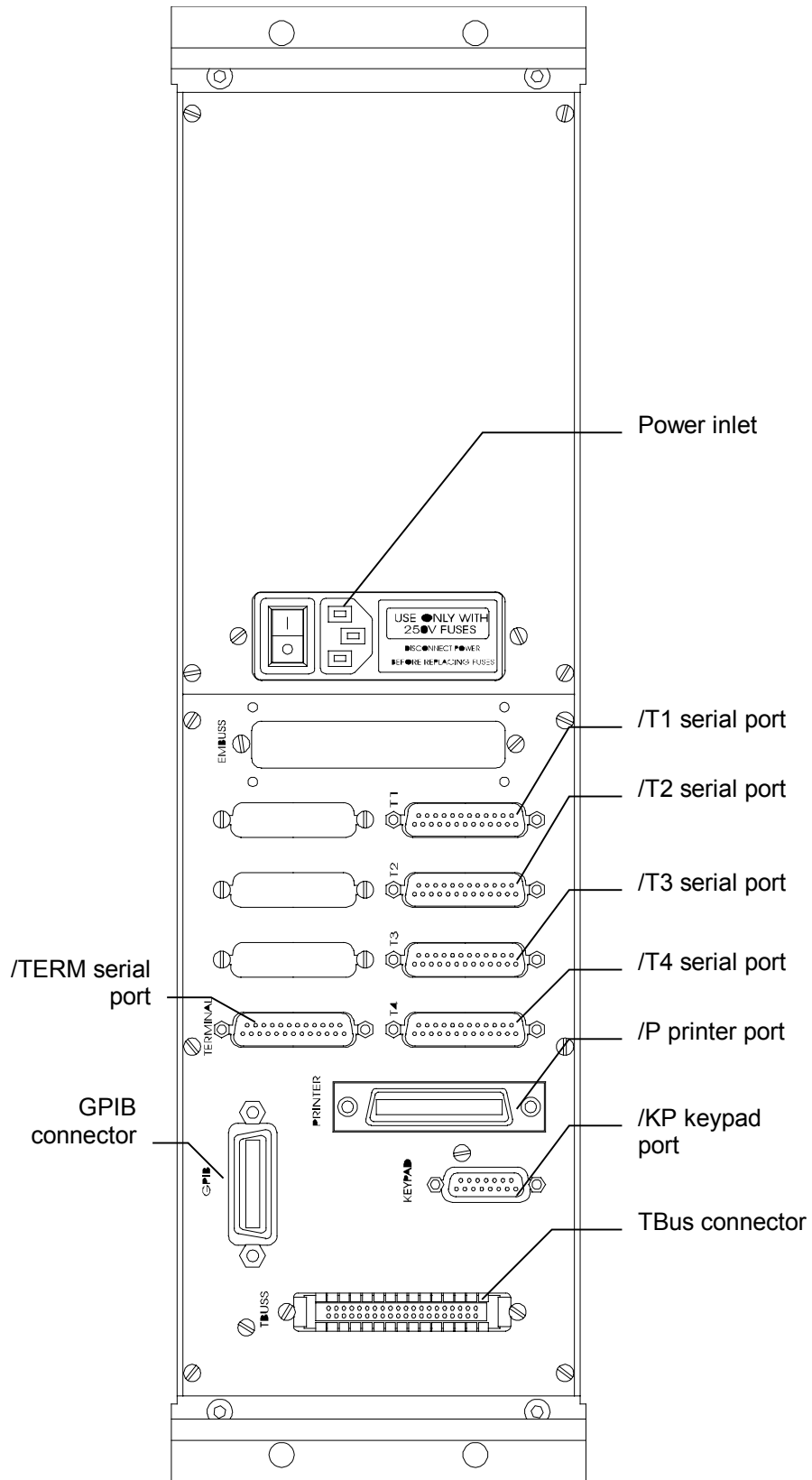
Power inlet

/T1 serial port

/T2 serial port

/T3 serial port

/TERM serial port

/T4 serial port

/P printer port

GPIB connector

/KP keypad port

TBus connector

Figure 1 - 2030 Computer Back Panel

STARTUP

Ordinarily, when power is applied or the reset button is released, the loader program will bring up the OS9/68000 operating system from the hard disk, and the system will begin accepting commands from the console keyboard (or will request a user to log in). It may be instructive to see exactly what happens during this complicated process to help users diagnose (and avoid) problems and make the most of the many opportunities to fine-tune the operating system to their personal requirements.

The loader is located in EPROM on the CPU board at $FE0000-$FFFFFF. When the RESET line is asserted by the power-on reset circuit, reset push-button, or reset instruction, the memory map is switched to overlay the EPROMs at $000000-$01FFFF. The microprocessor enters supervisor state, loads its stack pointer from locations 0-3, and loads its program counter from locations 4-7. The loader is executed and immediately clears a latch to restore RAM access at $0000000-$01FFFF.

The loader then begins to initialize RAM. All of the 68010 exception vectors at $000C- $03FF (all vectors except reset and bus error, which are handled in the EPROMs) are assigned values starting at $00000040A and incremented by 10. In turn, between $040A and $0DEB, a 10-byte routine is installed for each vector. These short routines consist of the instructions PEA #xxxx, JMP yyyyyyyy. (The reason for having the original vectors essentially point to jump instructions is to allow implementing OS9 on hardware which does not permit the original vectors to be in RAM. The jump instructions provide a second level of vectors which will always be in RAM and thus dynamically configurable by the operating system.) The loader does not need to initialize the jump addresses. That is done later by the OS9 kernel using its own F$IRQ service request. The PEA arguments start at $000C and increment by 4 and thus are equal to the original vector offsets. (The 68010 automatically stacks the vector offset, but OS9 was designed for the 68000, which did not.)

The loader then determines the amount of RAM in the system and creates a linked list of RAM blocks. OS9 was designed to work with noncontiguous memory blocks, but our loader only recognizes the contiguous block starting at location 0, so the linked list is trivial.

This is when the message, "DIGALOG SYSTEMS, INC." is displayed. The loader requests the SASI interface to read logical sector number zero of logical unit number zero (the hard disk). OS9 disks contain the boot file location in bytes $15-$17 of this sector and the boot file size in bytes $18-$19. If the size word is nonzero, a seek is performed to the indicated sector and the file is loaded into RAM starting at $2400. The loader then transfers control to the module at $2400 (which should be the OS9 kernel). At this point, the loader is finished.

The loader may not be able to find the boot file on logical unit zero. This always occurs on the first few attempts after a cold start while the hard disk is not yet up to speed. The loader would then try unit one (floppy disk) starting over from where the DIGALOG SYSTEMS message is displayed. As long as a boot file cannot be located on either unit, the loader will alternate between units trying to locate one.

The loader can be directed to get the boot file from the hard disk by removing the floppy disk before powering up the computer or resetting the CPU. The loader can be forced to get the boot file from a floppy disk by turning off the power briefly, thus causing the hard disk to lose enough speed whereby the floppy drive is accessed first. In either case, the desired unit must contain a valid boot file. Boot files are installed with the utility program OS9GEN, which makes the file contiguous and installs the size and location in sector zero as mentioned above. The boot file (OS9Boot) is made up of modules; some are mandatory and others, optional. KERNEL must be the first module. The others may be in any order. INIT is mandatory; it is a data module containing system configuration parameters (see the OS9/68000 technical manual for a description of the INIT module).

RBF is required for any disk I/O; GESHDI is required to operate the SASI controller and S0 & RB5400 are needed for the hard disk and floppy disk units. SYSGO is required; it is a simple endless loop, which is actually the mainline program of the entire operating system. The boot file is limited to 64K bytes, which requires some of the necessary modules to be located in the boot loader EEPROM. When the KERNEL starts,

it will search memory for modules and add any it finds to the module directory. The following modules are located in the boot loader EEPROM: SHELL, which is the command line interpreter; CLOCK and TK68901, which implement the real time clock; and MK68901, which is the console serial port driver. The descriptor TERM, which is for the console serial port, is located in the boot file to allow its characteristics (such as baud rate) to be changed. Any other modules that are desired may be loaded later. When control is passed to the kernel, it initializes the operating system tables and data structures and then transfers control to SYSGO. In turn, this transfers control to the command line interpreter, SHELL. This is more complicated than absolutely necessary, but it makes OS9 adaptable to a wider variety of applications.

The shell is capable of reading command lines from the disk as well as from the terminal. The file /S0/STARTUP is passed by SYSGO to the shell as its first set of commands. This is where most system customization takes place. The clock is set (from the battery powered calendar), additional I/O modules are loaded, terminal port parameters are adjusted, time sharing consoles are activated, the message of the day is displayed, etc. In short, any command can be given to or any program can be run by STARTUP. If and when these commands have all been executed, the shell then takes input from the console. Time-sharing consoles e.g., /T1, may be activated by the command:

SHELL </T1 >/Tl >>/T1&

which will not require a login password. However, if the user leaves the shell by typing control-Z, no additional login sessions are possible. Usually, these consoles are activated with the command:

TSMON /T1 &

which uses CMDS/LOGIN and SYS/PASSWORD to request the user's ID. If the user leaves the shell, future login sessions are still possible.
References: OS9/68000 user manual sections. 1, 2, 3.3, 5; OS9GEN, TSMON commands; technical manual sections 1.1, 2, 5.1. For creating text files, such as Startup, see BUILD and EDT commands or SCRED screen editor user's manual.

OPERATION

Microware'sOS9/68000 operating system is an advanced multitasking operating system designed for high performance in real-time system applications. It combines significant new operating system concepts with the overall architecture of Unix; yet OS9/68000 is by far smaller and more efficient than Unix. OS9/68000 supports modular programming techniques that multiply programmer efficiency and dramatically improve software maintainability. Its tree-structured directory system and memory module format allow dynamic linking of standard library or custom modules together to form an overall application program.

Microware's BASIC combines all the standard BASIC statements with advanced features, such as PASCAL-type loop constructs and data structures. It is procedure oriented, supports modular programming, and is totally integrated into the OS9 modular software environment. Procedures may call each other (or themselves)even using automatic parameter passing. External procedures written in Basic09, C, or assembly language can be mixed freely and interchangeably.

Most of the system utilities that are available through the Shell (console command interpreter) are described in the Microware OS9/68000 User's Guide. This manual also describes the Shell itself and the OS9 file system.

Many of the same language or equivalent utilities are accessible in assembly language through system service requests (using a trap instruction). These calls are described in the OS9/68000 Technical Manual. This manual is also useful to advanced Basic09 programmers who need detailed knowledge of the I/O system, memory management, and process scheduling.

Microware BASIC has its own manual. The section describing external procedure calls (the RUN statement) is of interest not only to users who write their own assembly language procedures, but also to anyone desiring more insight into the nature of the Digalog extensions to Basic09 which interface with the test system

hardware. Finally, the Relocating Macro Assembler (R68/L68) and screen editor (UMacs) are described in their own separate manuals (a lower performance text editor, Edt, is described as a utility in the user's manual). Although Microwave BASIC has its own interactive source text editor, it is possible to write source programs using UMacs. UMacs can also used to write and maintain the Startup file (and any other user command files), Sys/Password file (used by Login), assembly language source files, etc.
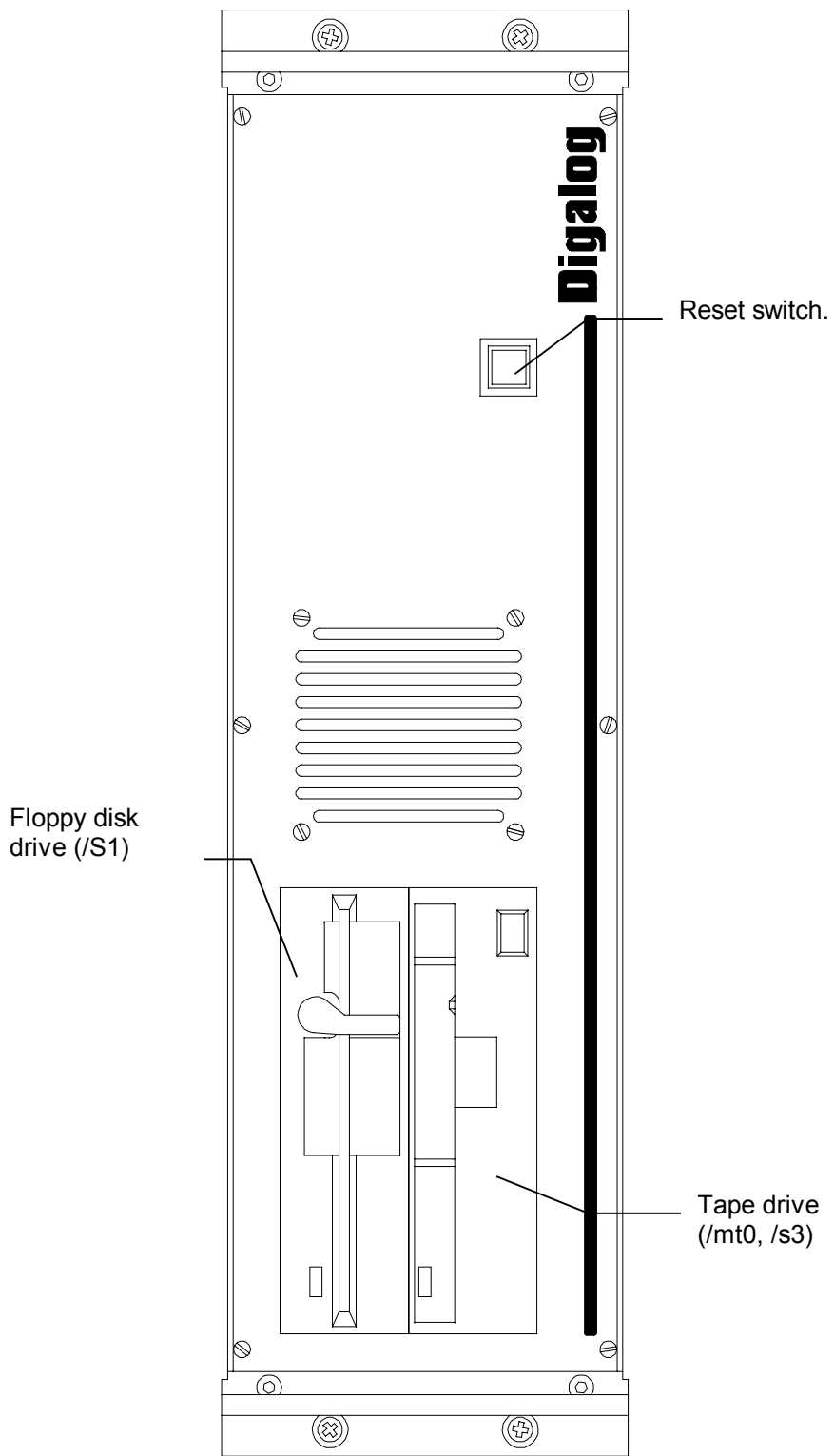
Figure 2 - 2030 Computer Front View

Reset switch.

Floppy disk
drive (/S1)

Tape drive
(/mt0, /s3)

Digalog

CHARACTER I/O DEVICES

The standard character I/O devices are of four types: asynchronous bit-serial ports for terminals and modems, a parallel Centronix type port for printers, a parallel IEEE-488 (GPIB) port for instruments, and a port for the small 24-key pad.

Serial port /TERM is physically located on the CPU board and serves the main (or only) user console.

Serial port /T1, /T2, /T3 and /T4 are located on the I/O controller board and are for additional user terminals or any other purpose such as serial printers, data networks, bar-code readers, etc.

All ports /TERM and /T1-/T4 conform to EIA-RS232 pinout and signal levels. Baud rate, character format, and other operating characteristics are determined by the XMODE utility program.

The parallel port /P implements a subset of the Centronix interface (8 data, strobe, and acknowledge) and is compatible with most printers. The XMODE utility may be used to set a time limit for acknowledge.

The IEEE-488 port, /G, is described in a separate section (4.11).

The keypad may be used two ways. As a standard OS9 I/O device (/KP), it provides a subset of the ASCII character set including the digits 0-9, symbols +.-/*&$ etc., letters a- h and A-H, delete, cancel, and carriage return. Alternatively, the procedure KPscan(N) reads the instantaneous state of the keypad as a key number 0-23 (24 for no key). This permits the keypad to be polled at any time for the duration of a keystroke to be determined as well as its identity.

MASS STORAGE PERIPHERALS

Four devices are used for file storage and backup: the hard disk (/S0), floppy (/S1), streaming back-up tape (/S3) and incremental tape backup (/mt0). A SASI interface controller is used.

The standard hard disk is a four-surface plated media design with a formatted capacity of 40 Mb (1 Mb = 1048576 bytes). However, other drives of similar capacity may be substituted as availability changes.

The floppy disk format is double sided, double bit density, double track density (96 TPI, 80 tracks) for a formatted capacity of 655360 bytes.

The back-up (streaming) tape uses the QIC-02 format with a high-capacity cassette style cartridge. The hard disk may be backed up and restored as a whole disk image for emergency use. The back-up tape may be used as a (very slow) read only device for recovery of individual files by treating the tape drive as a disk. The file descriptor used for this is s3. For individual file or directory backup, the user may execute the Fsave and Frestore commands. The descriptor used for doing this is /mt0. Follow the Fsave/Frestore instructions found in the Microware manual sets. Because of the way Fsave writes files to the tape, incremental restoration of files is much faster than trying to restore them from a streamed (bit image) tape.

The floppy disk cannot be backed up to or used as a hard disk back-up per se other than that individual files may be read or written in the usual manner. In particular, the OS9 BACKUP command is not used with this system. The DSAVE command may be used in conjunction with the COPY command to copy all files on a device or in a subdirectory. DSAVE produces a shell procedure file which may be viewed and edited before execution to copy a particular list of files to a target device for backup purposes.

For backing up the hard disk, the command BSTREAM may be used. This will display the tape ID block (if the tape has been used previously) and prompt for an R (restore) or B (back-up) command. Bstream is limited to backing up 40Mb (or less) hard disks as it does not support multiple volume backups. An alternative way of backing up the system's hard disk is to use the Fsave command. This program does a file-by-file backup of the hard disk structure and files and supports multiple volumes (tapes) if a hard drive larger than 40 MB needs to be backed up. Fsave uses the descriptor /mt0. Other tape operations may be accessed through the tape utility

provided by Microware. They include erasing, rewinding, reading and writing tapes. Please refer to the Microware manual set for more information on the tape utility.

When the equipment is to be moved, stored, or transported, it is recommended to park the hard disk heads on a reserved landing zone of the disk surface. The command BPARK is used for this purpose.

Before a new hard disk or floppy can be used, it must be formatted, which provides it with sector address marks and a blank directory structure. In addition, if a device is to be used as the source of the boot file (see this manual section 3.14), the OS9GEN command must be used to properly initialize it.

References: OS9/68000 user manual ATTR, COPY, DEL, DELDIR, DIR, DSAVE, FORMAT, FREE, MAKDIR, OS9GEN and RENAME commands; chapter 4 (the OS9 file system).

G-96 Mother board Assembly

The G-96 bus offers 8 and 16 bit data bus capability, synchronous and asynchronous data transfers, single Euro board mechanical standard and a high reliability DIN 41612 connector. Twenty-four address lines and a signal named PAGE* allow a 32M word (64M bytes) address space. The GESMPU14-A computer card (Digalog P.N. 2025-1020) can access up to 16M bytes.

The interrupt structure includes 6 interrupt lines, 1 interrupt acknowledge, and a daisy chain implementation that allows both vectored and non-vectored interrupts to be used at the same time.

The G96 bus must be terminated at one end with 3 volt@132 ohm resistor networks. These networks are included on the EMBus controller card (Digalog P.N. 0000-2211). If the system is an analog test system, the termination is provided by a terminator card (Digalog P.N. 0000-2007). Terminators are located in the far right hand slot. Only the power lines and interrupt daisy chain lines are without terminators.

VPA* (valid peripheral address) is the address strobe for the peripheral area. VMA* is used for all other address validation. VPA*, VMA* and IACK* are mutually exclusive.

Address lines A0-A23 refer to word addresses with UDS* and LDS* selecting even or odd byte addresses. Thus, A1 on the MC68010 is connected to A0 on the G-96 bus, A2 to A1, A3 to A2, etc. A23 of the G96 bus is driven low and is unused by the GESMPU14-A board.

For further information, refer to the "G-64 Bus Specifications Manual," Revision 3.0, June 1988.

Pin Number	Power Supply
1	-12V
2	+5V STANDBY
3	+12V
4	+5V
5	+5V
6	GND
7	GND

Table 5 - G96 Mother board Power Suppy Connector Pin Out

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
C1	GND	B1	GND	A1	GND
C2	A16	B2	A8	A2	A0
C3	A17	B3	A9	A3	A1
C4	A18	B4	A10	A4	A2
C5	A19	B5	A11	A5	A3
C6	A20	B6	A12	A6	A4
C7	A21	B7	A13	A7	A5
C8	A22	B8	A14	A8	A6
C9	A23	B9	A15	A9	A7
C10		B10	BRQ*	A10	BGRT*
C11		B11	UDS*	A11	LDS*
C12		B12	BGACK*	A12	HALT*
C13	GND	B13	E	A13	SYCLK (8 MHz)
C14		B14	RESET*	A14	VPA*
C15		B15	NMI*	A15	DTACK*
C16	IRQ3*	B16	IRQ1*	A16	VMA*
C17	IRQ5*	B17	IRQ2*	A17	R/W*
C18	VED* (NC)	B18	IACK*	A18	IRQ4*
C19	GND	B19	D12*	A19	D8*
C20	P5* (NC)	B20	D13*	A20	D9*
C21	P4* (NC)	B21	D14*	A21	D10*
C22	P3* (NC)	B22	D15*	A22	D11*
C23	P2* (NC)	B23	D4*	A23	D0*
C24	P1* (NC)	B24	D5*	A24	D1*
C25	P0* (NC)	B25	D6*	A25	D2*
C26		B26	D7*	A26	D3*
C27	SYSFAIL* (NC)	B27	BERR*	A27	PAGE*
C28	ARBCLK (16 MHz)	B28	CHAIN IN	A28	CHAIN OUT
C29		B29	+5 STANDBY	A29	PWF*
C30		B30	-12V	A30	+12V
C31	+5V	B31	+5V	A31	+5V
C32	GND	B32	GND	A32	GND

Table 6 - G-96 Bus Connector Pin Out
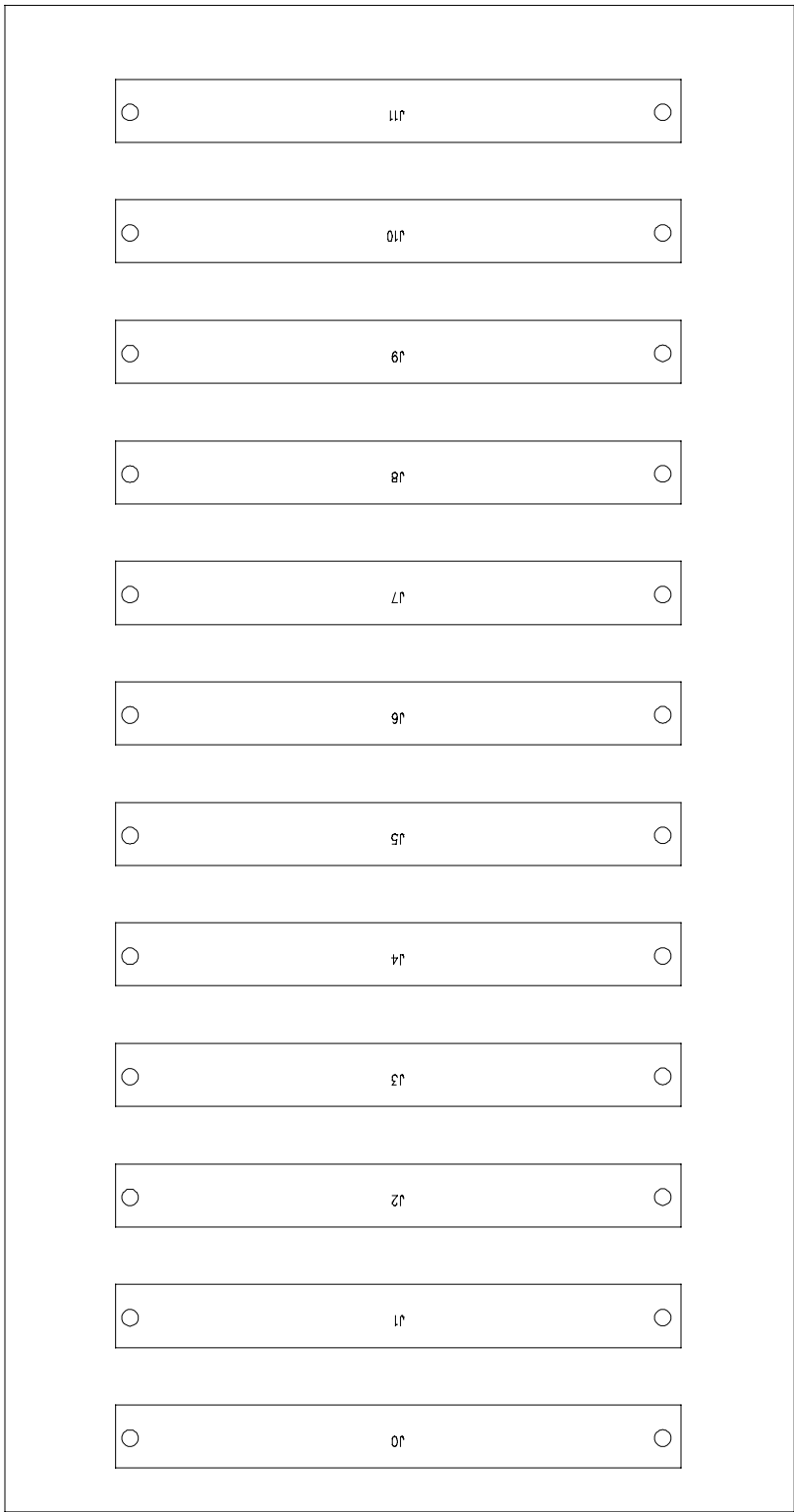
Figure 3 - 0000-2230 G96 Mother Board

Computer Power Supply System

The 2030 computer chassis is powered from one power supply with multiple outputs. This power supply provides +5 volts, -12 volts and 2 separate +12 volt supplies. 115V AC power (50/60 Hz) is provided to the supply via a combination power entry module, fuse holder and line filter.   The entry fuse is a 3 amp slow blow fuse.
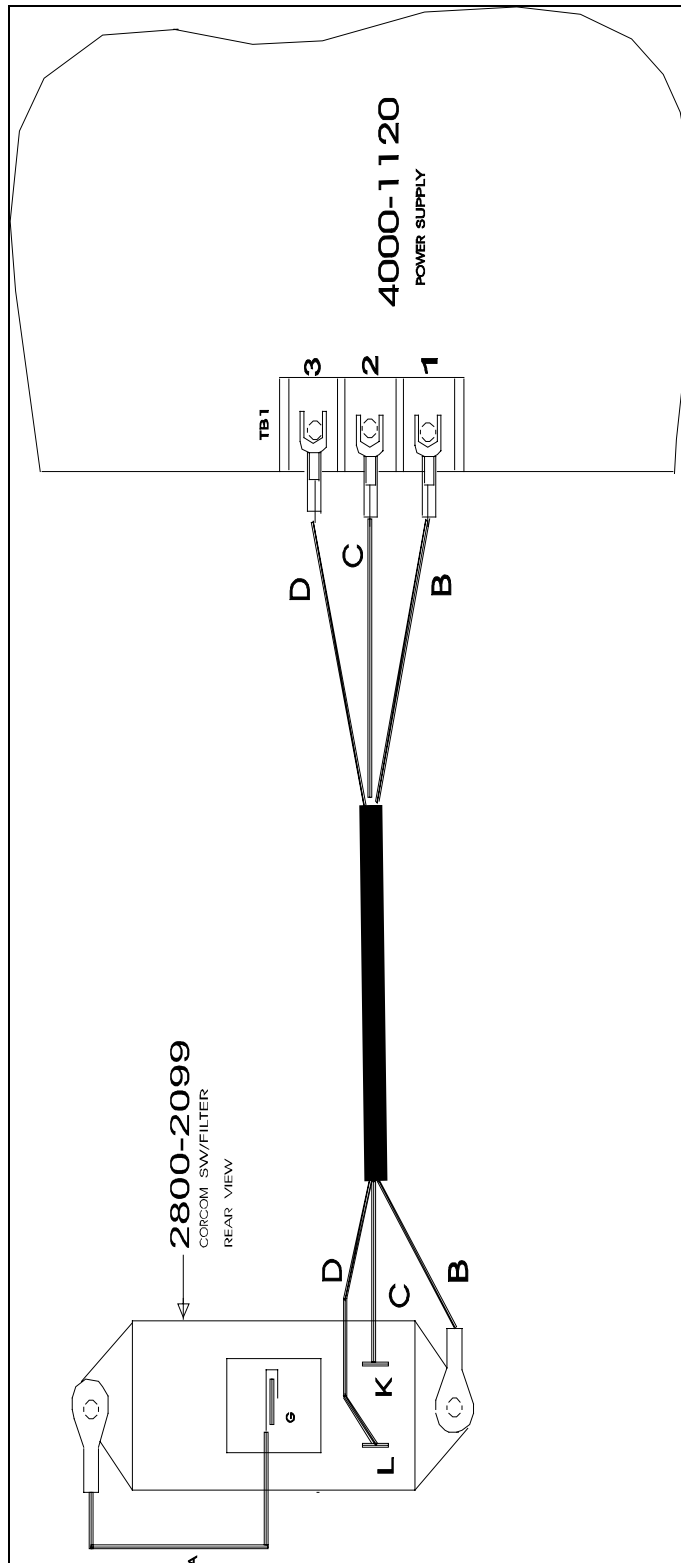
Figure 4 - 0000-2067 AC Power Supply Harness Installation

Power Supply Pin Number	Signal Description	G-96 Mother board Pin Number	Hard disk Pin Number
1	+5 volts	4,5	
2	+5 volts		4
3	GND	6,7	
4	GND		3
5	+12 volts		1
6	GND		2
7	+12 volts	3	
8	-12 volts	1	
9	Unused		
+S	+5 volt sense line	4	
-S	GND sense line	6	

Table 7 - DC Power Supply Harness Connections

Note: Below is pictured a hard disk connector on the DC harness.
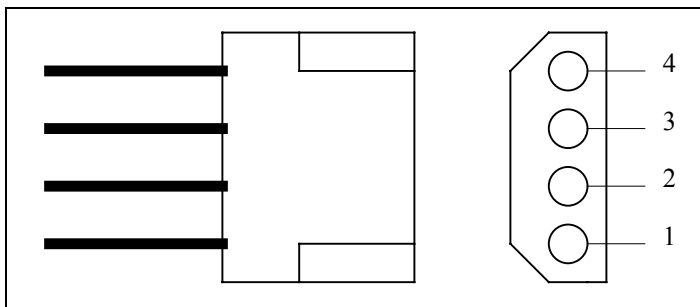
GESMPU14-A MC68010 Microprocessor Module

The GESMPU14-A is a high performance computer board based on the MC68010 32 bit microprocessor. It includes a battery powered calendar/clock, asynchronous serial port, sockets for up to 128K bytes of PROM, a small EEPROM with 256 4 bit words, and a socket for an optional NS16081 arithmetic co-processor.

The MK68901 multifunction peripheral provides the serial port, four user programmable timers, and interrupt vectoring for the other on board functions.

The EPROMs provide boot strap software that loads the OS-9 operating system from the SASI disk controller. They also contain a monitor for bus error and abort push-button exceptions.

The MC68010 microprocessor requires a DTACK* signal (data transfer acknowledge) to complete each address cycle. On this board, an 8 microsecond timer will generate a bus error if the DTACK* signal does not occur within this time. The faulted cycle will be rerun up to 8 times automatically by on board logic before the MC68010 is allowed to fetch the bus error vector and initiate an exception. Each retry is preceded by a 100 millisecond delay making the systems very robust in surviving power transients. Once the bus error exception is initiated, the system will enter the bus error monitor. It is advised that the user write down the information displayed on the screen so that the information is available later while debugging the system. A hardware reset is usually the only method that can be used to recover from this error condition.

The system clock rate is 8 MHz. A machine cycle requires at least 4 clock cycles (8 states). With static RAM, the CPU can maintain 16 bit memory transfers at 2 MHz.

INT1* through INT5* are assigned hardware interrupt levels 1-5, which may be vectored or autovectored. Level 6 is always vectored by the MK68901, which handles the serial port, abort button, and PWF* (power fail) interrupts. NMI* (nonmaskable interrupt) is connected at level 7 and is always autovectored.

On board logic decodes a 2K byte block of addresses for peripherals. Address locations in this area use the address qualifier VPA*. Within this 2K byte block, 4 blocks of 512 bytes may be individually jumpered for either asynchronous transfer using DTACK* or synchronous transfer using the 1 MHz E clock.

When the computer board is reset, the on board EPROM will overlay the lowest block of memory addresses (including the vector table) as well as appear at the EPROM addresses. During system initialization, the software will set an on board latch to remove the EPROM from the low addresses and permit access to RAM instead.

There are three LEDs on the front edge of the board. The red indicates the supervisory mode (from the MC68010 function code). The yellow indicates a bus error retry. The green indicates a microprocessor halt. Only a hardware reset will restart a halted microprocessor.

The yellow LED will also light during a synchronous data transfer. When the bus timer does time out and lights the LED, the MC68010 ignores the BERR* signal during the asynchronous transfer.

Start	End	Description
$000000	$01FFFF	RAM: overlaid by ROM after reset (128K bytes)
$020000	$FBE8FF	Available for RAM
$FBE900	$FBE9FF	2030 analog Testhead
$FBEA00	$FCFFFF	Available for RAM
$FD0000	$FD01FF	Peripheral Block 0 (512 bytes)
$FD0200	$FD03FF	Peripheral Block 1 (512 bytes)
$FD0400	$FD05FF	Peripheral Block 2 (512 bytes)
$FD0600	$FD07FF	Peripheral Block 3 (512 bytes)
$FD8000	$FD81FF	X2212P 4-bit EEPROM (odd addresses only)
$FD8200	$FD822F	MK68901 peripheral (odd addresses only)
$FD8240	$FD825F	MM58274 calendar (odd addresses only)
$FD8261		Write "1" to remove ROM from low RAM area
$FD8281		SMC8136 baud-rate generator
$FD82C2	$FD82C6	NS16081 floating-point coprocessor option
$FE0000	$FFFFFF	ROM

Table 8 - GESMPU14-A Memory Map

For pin assignments of the G-96 bus connector, please see the section titled "G-96 Mother board Assembly".

Connector - Pin	Signal
P2-1	Gate 0
P2-2	Output 0
P2-3	GND
P2-4	Gate 1
P2-5	Output 1
P2-6	GND
P2-7	Output 2
P2-8	GND
P2-9	Output 3
P2-10	GND

Table 9 - MK68901 Timer Interface Connection

Note: The above connector is normally not used as part of the 2030 tester configuration.

Connector - Pin	Signal	Connector - Pin	Signal
P4-1	Shield	P4-2	TxD
P4-3	RxD	P4-4	RTS
P4-5	CTS	P4-6	DSR
P4-7	GND	P4-8	DCD
P4-9		P4-10	
P4-11		P4-12	
P4-13		P4-14	
P4-15	TxClock	P4-16	
P4-17	RxClock	P4-18	
P4-19		P4-20	DTR

Table 10 - GESMPU14-A RS-232 Connector

Connector-Pin	Signal
P3-1	Reset switch
P3-2	GND
P3-3	Abort switch N.C.
P3-4	Abort switch N.O.
P3-5	+5 volts

Table 11 - Reset/Abort Switch Connector

Note: J1 jumper must be open for external use of the abort switch.

Note that when setting the jumpers on most Gespac cards, the jumper field is numbered like most integrated circuits i.e., in a U-shaped pattern.. For further reference, consult the GESMPU-14A data sheet.

Jumper Field	Function	Jumpers	Settings	Result
J1	Local/Remote abort selector	J1-1 to J1-2	Closed	Local abort switch
J2	Internal/External Tx and Rx clock selector	J2-1 to J2-10	Closed	Internal baud rate clock
		J2-2 to J2-3	Closed	
		J2-8 to J2-9	Closed	
		J2-4 to J2-7	Open	
		J2-5 to J2-6	Open	
J4	RS-232C modem/terminal selector	J4-1 to J4-18	Open	DCE (modem)
		J4-2 to J4-17	Open	
		J4-3 to J4-16	Closed	
		J4-4 to J4-15	Closed	
		J4-5 to J4-14	Closed	
		J4-6 to J4-13	Closed	
		J4-7 to J4-12	Closed	
		J4-8 to J4-11	Closed	
		J4-9 to J4-10	Closed	
J5	EPROM access time selector, bus system clock selector	J5-1 to J5-10	Open	450 ns access time, 8 MHz system clock
		J5-2 to J5-9	Open	
		J5-3 to J5-8	Closed	

Jumper Field	Function	Jumpers	Settings	Result
		J5-4 to J5-7	Closed	
		J5-5 to J5-6	Open	
J6	Real time clock power enable	J6-1 to J6-2	Closed	Battery connected
J7	Async/Sync VPA field mode, Autovectored/vectored interrupt selector	J7-1 to J7-18	Open	VPA field 0 async.
		J7-2 to J7-17	Open	VPA field 1 async.
		J7-3 to J7-16	Open	VPA field 2 async.
		J7-4 to J7-15	Closed	VPA field 3 sync.
		J7-5 to J7-14	Open	IRQ5 autovectored
		J7-6 to J7-13	Closed	IRQ4 vectored
		J7-7 to J7-12	Closed	IRQ3 vectored
		J7-8 to J7-11	Open	IRQ2 autovectored
		J7-9 to J7-10	Open	IRQ1 autovectored
J8	IACK sense selection	J8-1 to J8-2	Closed	IACK when high
		J8-2 to J8-3	Open	
J9	EPROM type selection	J9-1 to J9-2	Closed	27256
		J9-2 to J9-3	Open	
J10	EPROM type selection	J10-1 to J10-2	Open	27256
		J10-2 to J10-3	Closed	
		J10-4 to J10-5	Closed	
		J10-5 to J10-6	Open	
J11	SYCLK and Enable three state control, IACK three state control, power fail signal selector	J11-1 to J11-2	Open	IACK active during DMA
		J11-2 to J11-3	Closed	
		J11-4 to J11-5	Open	Enable, SYCLK free running during DMA
		J11-5 to J11-6	Closed	
		J11-7 to J11-8	Open	No power fail interrupt
Note	Jumper field J3 does not exist.			

Table 12 - GESMPU-14A Jumper Settings for OS9 Version 2.4

Figure 5 - 2025-1020 GESMPU-14A Computer Card

Memory Card

Three different memory cards are used in the 2030 computer systems. The first two use the same printed circuit board. The 256 kilobyte board uses 32 8 kilobyte SRAM chips and has the Digalog P.N. 0000-2203. The 1 megabyte board uses 32 kilo byte SRAM chips and has the Digalog P.N. 0000-2213. The only way to tell the two cards apart is to identify the type of chip on the board. The 1 megabyte configuration is the most popular.

The last memory card used in the 2030 computer is the 0000-2232 card. While this card may be configured up to 6 ways, only one has been used. This configuration is the 1 megabyte configuration.

0000-2203, 0000-2213

This is a no wait state static RAM board using 32 8 bit memory chips surface mounted on one side of the card. When equipped with 8 kilo byte chips the total capacity is 256 kilo bytes. When equipped with 32 kilo byte chips the capacity is 1 megabyte per board. In any system which contains both 256 kilobyte and 1 megabyte memory boards, the 1 megabyte boards must be addressed first, followed by the 256 kilobyte boards.

Jumper Field	Function	Jumpers	Settings	Result
JP8	Board capacity	A to B	Closed	256 kilo byte
		B to C	Open	
JP9	Board capacity	A to B	Closed	256 kilo byte
		B to C	Open	
JP10	Board capacity	A to B	Closed	256 kilo byte
		B to C	Open	
JP11	Board capacity	A to B	Closed	256 kilo byte
		B to C	Open	
JP13	Board capacity	1 to 2	Closed	256 kilo byte
JP14	Board capacity	1 to 2	Closed	256 kilo byte

Table 13 - 0000-2203 Jumper Settings, Capacity

Address Range	JP7	JP6	JP5	JP4	JP3	JP2	JP1
$00000000 - $0003FFFF	Closed	Closed	Closed	Closed	Closed	Closed	Closed
$00040000 - $0007FFFF	Closed	Closed	Closed	Closed	Closed	Closed	Open
$00080000 - $000BFFFF	Closed	Closed	Closed	Closed	Closed	Open	Closed
$000C0000 - $000FFFFF	Closed	Closed	Closed	Closed	Closed	Open	Open
$00100000 - $0013FFFF	Closed	Closed	Closed	Closed	Open	Closed	Closed
$00140000 - $0017FFFF	Closed	Closed	Closed	Closed	Open	Closed	Open
$00180000 - $001BFFFF	Closed	Closed	Closed	Closed	Open	Open	Closed
$001C0000 - $001FFFFF	Closed	Closed	Closed	Closed	Open	Open	Open

Table 14 - 0000-2203 Jumper Settings, Address Range, First Eight Settings

Jumper Field	Function	Jumpers	Settings	Result
JP8	Board capacity	A to B	Open	1 megabyte
		B to C	Closed	
JP9	Board capacity	A to B	Open	1 megabyte
		B to C	Closed	
JP10	Board capacity	A to B	Open	1 megabyte
		B to C	Closed	
JP11	Board capacity	A to B	Open	1 megabyte
		B to C	Closed	
JP13	Board capacity	1 to 2	Open	1 megabyte
JP14	Board capacity	1 to 2	Open	1 megabyte

Table 15 - 0000-2213 Jumper Settings, Capacity

Address Range	JP7	JP6	JP5	JP4	JP3	JP2	JP1
$00000000 - $000FFFFF	Closed	Closed	Closed	Closed	Closed	Open	Open
$00100000 - $001FFFFF	Closed	Closed	Closed	Closed	Open	Open	Open
$00200000 - $002FFFFF	Closed	Closed	Closed	Open	Closed	Open	Open
$00300000 - $003FFFFF	Closed	Closed	Closed	Open	Open	Open	Open
$00400000 - $004FFFFF	Closed	Closed	Open	Closed	Closed	Open	Open
$00500000 - $005FFFFF	Closed	Closed	Open	Closed	Open	Open	Open
$00600000 - $006FFFFF	Closed	Closed	Open	Open	Closed	Open	Open
$00700000 - $007FFFFF	Closed	Closed	Open	Open	Open	Open	Open

Table 16 - 0000-2213 Jumper Settings, Address Range, First Eight Settings

Figure 6 - 0000-2203/0000-2213 Memory Card

For pin assignments of the G-96 bus connector, please see the section titled "G-96 Mother board Assembly".

0000-2232

This G64/G96 form factor card allows the system to have 1, 2 or 4 megabytes of no wait state static RAM. It can also be configured for 1, 2 or 4 megabytes of PROM. The card accepts either 128 kilo byte SRAM or PROM chips, for the 1 megabyte mode, or 512 kilo byte SRAM or PROM chips for the 2 or 4 megabyte modes.

In the 2 megabyte mode the sockets for the SRAM/PROM are half populated. 512 kilo byte chips are placed in U1, U3, U5 and U7.

In any of the selected configurations the address lines are routed through a PLD such that no gaps appear in the memory map. When using the selection jumpers, the user selects a card number. To translate the card number into the base address, multiply the card number by the memory capacity of the card. When using the selection jumpers on the card it should be remembered that you are selecting the card number. To translate the card number to the base address multiply the card number times the memory capacity of the card. Examples:

Card number 0, 4 megabyte capacity: $000000 * $400000= $000000
Card number 1, 4 megabyte capacity: $000001 * $400000= $400000
Card number 3, 1 megabyte capacity: $000003 * $100000= $300000

When placing memory cards of mixed capacity in the same system the following practice is recommended. Place the largest capacity card (e.g. 4 megabyte) lowest in the memory map (i.e. $000000). Place the next largest capacity card in the memory map following the last address of the first card. Continue placing successively lower capacity cards in the system with addresses following the previous card. An example follows:

Card Number	Size	Address Range
0	4 megabyte	$000000 - $3FFFFF
2	2 megabyte	$400000 - $5FFFFF
6	1 megabyte	$600000 - $7FFFFF

Note that even though there are not six 1 megabyte cards in the system, the 1 megabyte card had to be selected as card number six to get base address $600000.

The physical location of the cards in the rack are irrelevant with the exception of the chain-in and chain-out jumper. This jumper is used to connect or separate cards on the same interrupt vector.

Jumpers	Function	Jumper	Setting	Result
JP1	Memory type, ROM or RAM	JP1	Open	Card selected for RAM
JP8	Chain-in Chain-out	JP8	Open	Chain-in not connected to chain-out

Table 17 - 0000-2232 Card Type Selection

Memory Size	JP2	JP3
Forbidden Condition	Closed	Closed
1 megabyte	Open	Closed
2 megabyte	Closed	Open
4 megabyte	Open	Open

Table 18 - 0000-2232 Memory Size Selection

Card Number	JP4	JP5	JP6	JP7
0	Closed	Closed	Closed	Closed
1	Open	Closed	Closed	Closed
2	Closed	Open	Closed	Closed
3	Open	Open	Closed	Closed
4	Closed	Closed	Open	Closed
5	Open	Closed	Open	Closed
6	Closed	Open	Open	Closed
7	Open	Open	Open	Closed
8	Closed	Closed	Closed	Open
9	Open	Closed	Closed	Open
A	Closed	Open	Closed	Open
B	Open	Open	Closed	Open
C	Closed	Closed	Open	Open
D	Open	Closed	Open	Open
E	Closed	Open	Open	Open
F	Open	Open	Open	Open

Table 19 - 0000-2232 1 Megabyte Card Number Selections

Card Number	JP5	JP6	JP7
0	Closed	Closed	Closed
1	Open	Closed	Closed
2	Closed	Open	Closed
3	Open	Open	Closed
4	Closed	Closed	Open
5	Open	Closed	Open
6	Closed	Open	Open
7	Open	Open	Open

Table 20 - 0000-2232 2 Megabyte Card Number Selection

Note: JP4 is unused. Leave the jumper open**.**

Card Number	JP6	JP7
0	Closed	Closed
1	Open	Closed
2	Closed	Open
3	Open	Open

Table 21 - 0000-2232 4 Megabyte Card Number Selection

Note: JP4 and JP5 are not used. Leave the jumpers open.
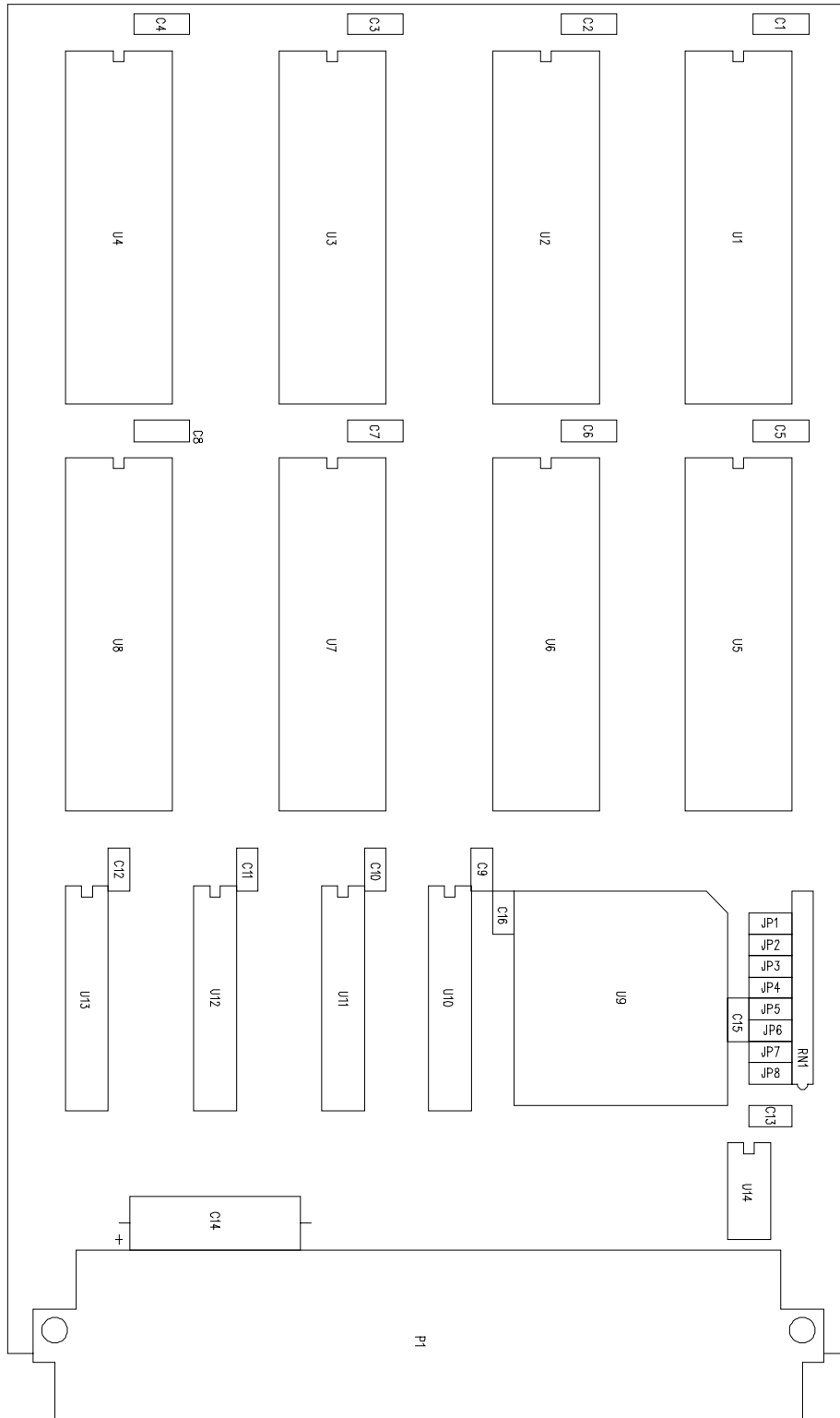
Figure 7 - 0000-2232 Memory Card

For pin assignments of the G-96 bus connector, please see the section titled "G-96 Mother board Assembly".

Dual Serial Port Card

The Dual Serial Port Card provides two serial communication channels on the G64/G96 bus. As configured for use in the Digalog Systems computer, the card offers asynchronous communication using the RS-232C protocol. Its baud rate is software programmable. RS-422 levels are also possible with this card. The TTY interface on the GESSIO cards is not supported by Digalog Systems.

The communication ports on this card are known to the operating system through the device descriptors "t5" and "t6." The settings of each device descriptor as shipped from Digalog are listed in the back of this manual. The device driver "sc6850" and the file manager "SCF" are used to control the card.

Four different Dual Serial Port Cards are in use on the 2030 computers. They are the GESSIO-1A and GESSIO-1B cards (Digalog P.N. 2000-3020) and Digalog's Dual Serial Port Card (P.N. 0000-3220 and 0000-3520). All cards except the GESSIO-1A are interchangeable without having to change the software. The GESSIO-1A card cannot be used with the Digalog implementation of the OS-9 operating system, version 2.4 and above.

2000-3020 GESSIO-1B Dual Serial Port Card

Connector - Pin	Signal	Connector - Pin	Signal
P2-1	Shield	P2-2	TxD
P2-3	RxD	P2-4	RTS
P2-5	CTS	P2-6	DSR
P2-7	GND	P2-8	DCD
P2-9		P2-10	
P2-11		P2-12	
P2-13		P2-14	TxDR (RS-422)*
P2-15	TxClock	P2-16	RxDR (RS-422)*
P2-17	RxClock	P2-18	TxCR (RS-422)*
P2-19	RxCR (RS-422)*	P2-20	DTR

Table 22 - GESSIO-1B Channel 1 (/t5) Connector Pin Out

Note: Signals with a * are not connected under normal operation.

Connector - Pin	Signal	Connector - Pin	Signal
P4-1	Shield	P4-2	TxD
P4-3	RxD	P4-4	RTS
P4-5	CTS	P4-6	DSR
P4-7	GND	P4-8	DCD
P4-9		P4-10	
P4-11		P4-12	
P4-13		P4-14	TxDR (RS-422)*
P4-15	TxClock	P4-16	RxDR (RS-422)*
P4-17	RxClock	P4-18	TxCR (RS-422)*
P4-19	RxCR (RS-422)*	P4-20	DTR

Table 23 - GESSIO-1B Channel 2 (/t6) Connector Pin Out

Note: Signals with a * are not connected under normal operation.

For pin assignments of the G-96 bus connector, please see the section titled "G-96 Mother board Assembly".

Note that when setting the jumpers on most Gespac cards, the jumper field is numbered like most integrated circuits i.e., in a U shaped pattern. For further reference, consult the GESSIO-1B data sheet.

Jumper Field	Function	Jumpers	Setting	Result
J1	TTY power supply, +12 volts	J1-1 to J1-2	Open	+12 volts supplied from external supply.
		J1-2 to J1-3	Closed	
J2	TTY power supply, ground	J2-1 to J2-2	Open	Ground supplied from external supply.
		J2-2 to J2-3	Closed	
J3	TTY mode selector, channel 2	J3-1 to J3-8	Closed	TTY mode for channel 2 is DCE.
		J3-2 to J3-7	Closed	
		J3-3 to J3-6	Closed	
		J3-4 to J3-5	Closed	
J4	TTY mode selector, channel 1	J4-1 to J4-8	Closed	TTY mode for channel 1 is DCE.
		J4-2 to J4-7	Closed	
		J4-3 to J4-6	Closed	
		J4-4 to J4-5	Closed	
J5	Protocol selector, channel 1	J5-1 to J5-10	Open	RS-232, DCE (modem)
		J5-2 to J5-9	Open	
		J5-3 to J5-8	Open	
		J5-4 to J5-7	Closed	
		J5-5 to J5-6	Closed	
J6	Protocol selector, channel 1	J6-1 to J6-10	Open	RS-232, DCE (modem)
		J6-2 to J6-9	Open	
		J6-3 to J6-8	Open	
		J6-4 to J6-7	Closed	
		J6-5 to J6-6	Closed	
J7	Protocol selector, channel 1	J7-1 to J7-10	Open	RS-232, DCE (modem)
		J7-2 to J7-9	Open	
		J7-3 to J7-8	Closed	
		J7-4 to J7-7	Closed	
		J7-5 to J7-6	Closed	
J8	Protocol selector, channel 2	J8-1 to J8-10	Open	RS-232, DCE (modem)
		J8-2 to J8-9	Open	
		J8-3 to J8-8	Open	
		J8-4 to J8-7	Closed	
		J8-5 to J8-6	Closed	
J9	Protocol selector, channel 2	J9-1 to J9-10	Open	RS-232, DCE (modem)
		J9-2 to J9-9	Open	
		J9-3 to J9-8	Open	
		J9-4 to J9-7	Closed	
		J9-5 to J9-6	Closed	
J10	Protocol selector, channel 2	J10-1 to J10-10	Open	RS-232, DCE (modem)
		J10-2 to J10-9	Open	
		J10-3 to J10-8	Closed	
		J10-4 to J10-7	Closed	
		J10-5 to J10-6	Closed	
J11	RS-422 terminator resistor, channel 1	J11-1 to J11-2	Open	No resistor
J12	RS-422 terminator resistor, channel 1	J12-1 to J12-2	Open	No resistor

Jumper Field	Function	Jumpers	Setting	Result
J13	RS-422 terminator resistor, channel 1	J13-1 to J13-2	Open	No resistor
J14	Protocol selector, channel 1	J14-1 to J14-2	Open	RS-232, DCE (modem)
J15	RS-422 terminator resistor, channel 1	J15-1 to J15-2	Closed	Resistor
J16	RS-422 terminator resistor, channel 1	J16-1 to J16-2	Open	No resistor
J17	RS-422 terminator resistor, channel 1	J17-1 to J17-2	Open	No resistor
J18	RS-422 terminator resistor, channel 1	J18-1 to J18-2	Open	No resistor
J19	RS-422 terminator resistor, channel 1	J19-1 to J19-2	Open	No resistor
J20	Protocol selector, channel 2	J20-1 to J20-2	Open	RS-232, DCE (modem)
J21	RS-422 terminator resistor, channel 2	J21-1 to J21-2	Open	No resistor
J22	RS-422 terminator resistor, channel 2	J22-1 to J22-2	Open	No resistor
J23	RS-422 terminator resistor, channel 2	J23-1 to J23-2	Closed	Resistor
J24	RS-422 terminator resistor, channel 2	J24-1 to J24-2	Open	No resistor
J25	RS-422 terminator resistor, channel 2	J25-1 to J25-2	Open	No resistor
J26	RS-422 terminator resistor, channel 2	J26-1 to J26-2	Open	No resistor
J27	RS-422 terminator resistor, channel 2	J27-1 to J27-2	Open	No resistor
J28	RS-422 terminator resistor, channel 2	J28-1 to J28-2	Open	No resistor
J29	TTY current loop power	J29-1 to J29-2	Open	External
		J29-3 to J29-4	Open	
J30	TTY current loop power	J30-1 to J30-2	Open	External
		J30-3 to J30-4	Open	
J31	TTY current loop power	J31-1 to J31-2	Open	External
		J31-3 to J31-4	Open	
J32	TTY current loop power	J32-1 to J32-2	Open	External
		J32-3 to J32-4	Open	
J33	RS-485 three state control, channel 1	J33-1 to J33-2	Open	No three state (RS-422)
		J33-2 to J33-3	Closed	
J34	TTY source polarity selector, channel 2	J34-1 to J34-2	Open	Parallel
		J34-2 to J34-3	Closed	
J35	TTY source polarity selector, channel 1	J35-1 to J35-2	Open	Parallel
		J35-2 to J35-3	Closed	
J36	RS-485 three state control, channel 2	J36-1 to J36-2	Open	No three state (RS-422)
		J36-2 to J36-3	Closed	
J37	Baud rate selector, channel 1	J37-1 to J37-18	Closed	Baud rate by software selection
		J37-2 to J37-	Open	

Jumper Field	Function	Jumpers	Setting	Result
		17		
		J37-3 to J37-16	Open	
		J37-4 to J37-15	Open	
		J37-5 to J37-14	Open	
		J37-6 to J37-13	Open	
		J37-7 to J37-12	Open	
		J37-8 to J37-11	Open	
		J37-9 to J37-10	Open	
J38	Baud rate selector, channel 2	J38-1 to J38-18	Closed	Baud rate by software selection
		J38-2 to J38-17	Open	
		J38-3 to J38-16	Open	
		J38-4 to J38-15	Open	
		J38-5 to J38-14	Open	
		J38-6 to J38-13	Open	
		J38-7 to J38-12	Open	
		J38-8 to J38-11	Open	
		J38-9 to J38-10	Open	
J39	Sync. full speed selector, channel 1	J39-1 to J39-2	Open	Normal baud rate output clock
		J39-2 to J39-3	Closed	
J40	Sync. full speed selector, channel 2	J40-1 to J40-2	Open	Normal baud rate output clock
		J40-2 to J40-3	Closed	
J41	Field address option	J41-1 to J41-2	Open	Standard GESSIO-1B mapping
		J41-2 to J41-3	Closed	
		J41-4 to J41-5	Closed	
		J41-5 to J41-6	Open	
J42	Address selection	J42-1 to J42-16	Closed	$7F0 - $7FF in the VPA field (odd bytes)
		J42-2 to J42-15	Open	
		J42-3 to J42-14	Open	
		J42-4 to J42-13	Open	
		J42-5 to J42-12	Open	

Jumper Field	Function	Jumpers	Setting	Result
		J42-6 to J42-11	Open	
		J42-7 to J42-10	Open	
		J42-8 to J42-9	Open	
J43	Interrupt level selector	J43-1 to J43-12	Open	Interrupt level 5
		J43-2 to J43-11	Open	
		J43-3 to J43-10	Open	
		J43-4 to J43-9	Open	
		J43-5 to J43-8	Open	
		J43-6 to J43-7	Closed	
J44	Interrupt operating mode	J44-1 to J44-2	Closed	with DTACK signal
J45	Interrupt mode selector	J45-1 to J45-10	Open	IACK Active high
		J45-2 to J45-9	Open	*
		J45-3 to J45-8	Closed	*
		J45-4 to J45-7	Open	*
		J45-5 to J45-6	Closed	* = used when board is vectored irq.

Table 24 - GESSIO-1B Jumper Selections, OS-9 Version 2.4

Figure 8 - 2000-3020 GESSIO-1B Dual Serial Port Card

0000-3220, 0000-3520 Dual Serial Port Cards

Connector - Pin	Signal	Connector - Pin	Signal
P3-1	Shield	P3-2	TxD
P3-3	RxD	P3-4	RTS
P3-5	CTS	P3-6	DSR
P3-7	GND	P3-8	DCD
P3-9		P3-10	
P3-11		P3-12	
P3-13		P3-14	
P3-15	TxClock	P3-16	
P3-17	RxClock	P3-18	
P3-19		P3-20	DTR

Table 25 - 0000-3220, 0000-3520 Channel 2 (/t6) Connector Pin Out

Connector - Pin	Signal	Connector - Pin	Signal
P2-1	Shield	P2-2	TxD
P2-3	RxD	P2-4	RTS
P2-5	CTS	P2-6	DSR
P2-7	GND	P2-8	DCD
P2-9		P2-10	
P2-11		P2-12	
P2-13		P2-14	
P2-15	TxClock	P2-16	
P2-17	RxClock	P2-18	
P2-19		P2-20	DTR

Table 26 - 0000-3220, 0000-3520 Channel 1 (/t5) Connector Pin Out

For pin assignments of the G-96 bus connector, please see the section titled "G-96 Mother board Assembly".

Jumpers	Function	Jumper	Setting	Result
JP7-13	Base Address Selectors			$7F0 - $7FF in the VPA address range
	Address line A3	JP7	Open	
	Address line A4	JP8	Open	
	Address line A5	JP9	Open	
	Address line A6	JP10	Open	
	Address line A7	JP11	Open	
	Address line A8	JP12	Open	
	Address line A9	JP13	Open	
JP14-18	Interrupt level selection			IRQ 5 selected
	IRQ 4	JP14	Open	
	IRQ 2	JP15	Open	
	IRQ 5	JP16	Closed	
	IRQ 3	JP17	Open	
	IRQ 1	JP18	Open	
JP1-2,4-6	RS232/422 mode select, channel 1			RS-232
		JP1	Open	
		JP2	Closed	

Jumpers	Function	Jumper	Setting	Result
		JP4	Open	
		JP5	Open	
		JP6	Open	
JP19-20,22-24	RS232/422 mode select, channel 2			RS-232
		JP19	Open	
		JP20	Closed	
		JP22	Open	
		JP23	Open	
		JP24	Open	
JP3	CTS,DCD pullup, channel 1	JP3	Closed	Pulled up
JP21	CTS,DCD pullup, channel 2	JP21	Closed	Pulled up

Table 27 - 0000-3220, 0000-3520 Jumper Settings for RS-232, OS9 Version 2.4

Jumpers	Function	Jumper	Setting	Result
JP7-13	Base Address Selectors			$7F0 - $7FF in the VPA address range
	Address line A3	JP7	Open	$010
	Address line A4	JP8	Open	$020
	Address line A5	JP9	Open	$040
	Address line A6	JP10	Open	$080
	Address line A7	JP11	Open	$100
	Address line A8	JP12	Open	$200
	Address line A9	JP13	Open	$400
JP14-18	Interrupt level selection			IRQ 5 selected
	IRQ 4	JP14	Open	
	IRQ 2	JP15	Open	
	IRQ 5	JP16	Closed	
	IRQ 3	JP17	Open	
	IRQ 1	JP18	Open	
JP1-2,4-6	RS232/422 mode select, channel 1			RS-422
		JP1	Closed	
		JP2	Open	
		JP4	Closed	
		JP5	Open	
		JP6	Closed	
JP19-20,22-24	RS232/422 mode select, channel 2			RS-422
		JP19	Closed	
		JP20	Open	
		JP22	Closed	
		JP23	Open	
		JP24	Closed	
JP3	CTS,DCD pullup, channel 1	JP3	Closed	Pulled up
JP21	CTS,DCD pullup, channel 2	JP21	Closed	Pulled up

Table 28 - 0000-3220, 0000-3520 Jumper Settings for RS-422, OS9 Version 2.4
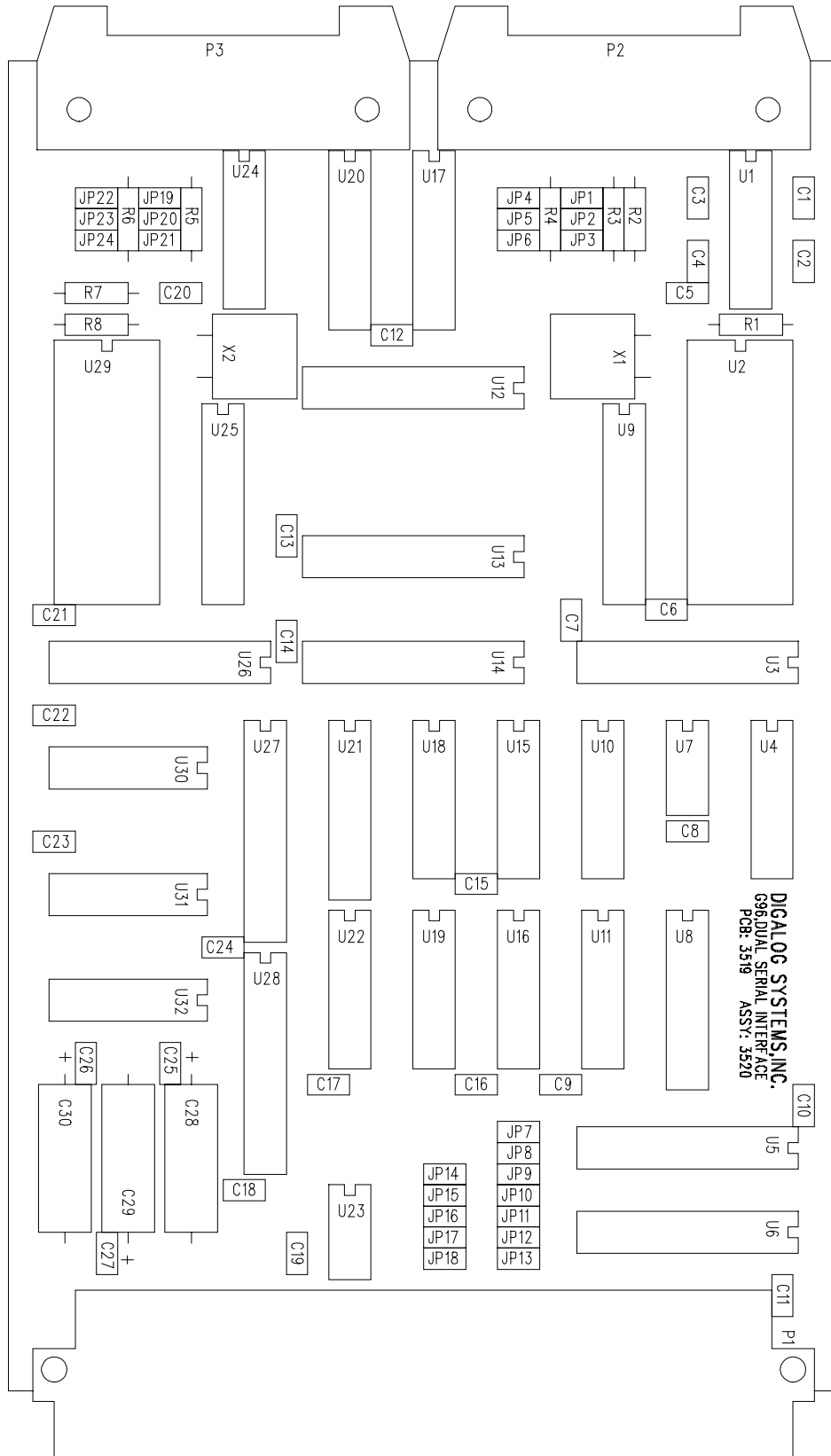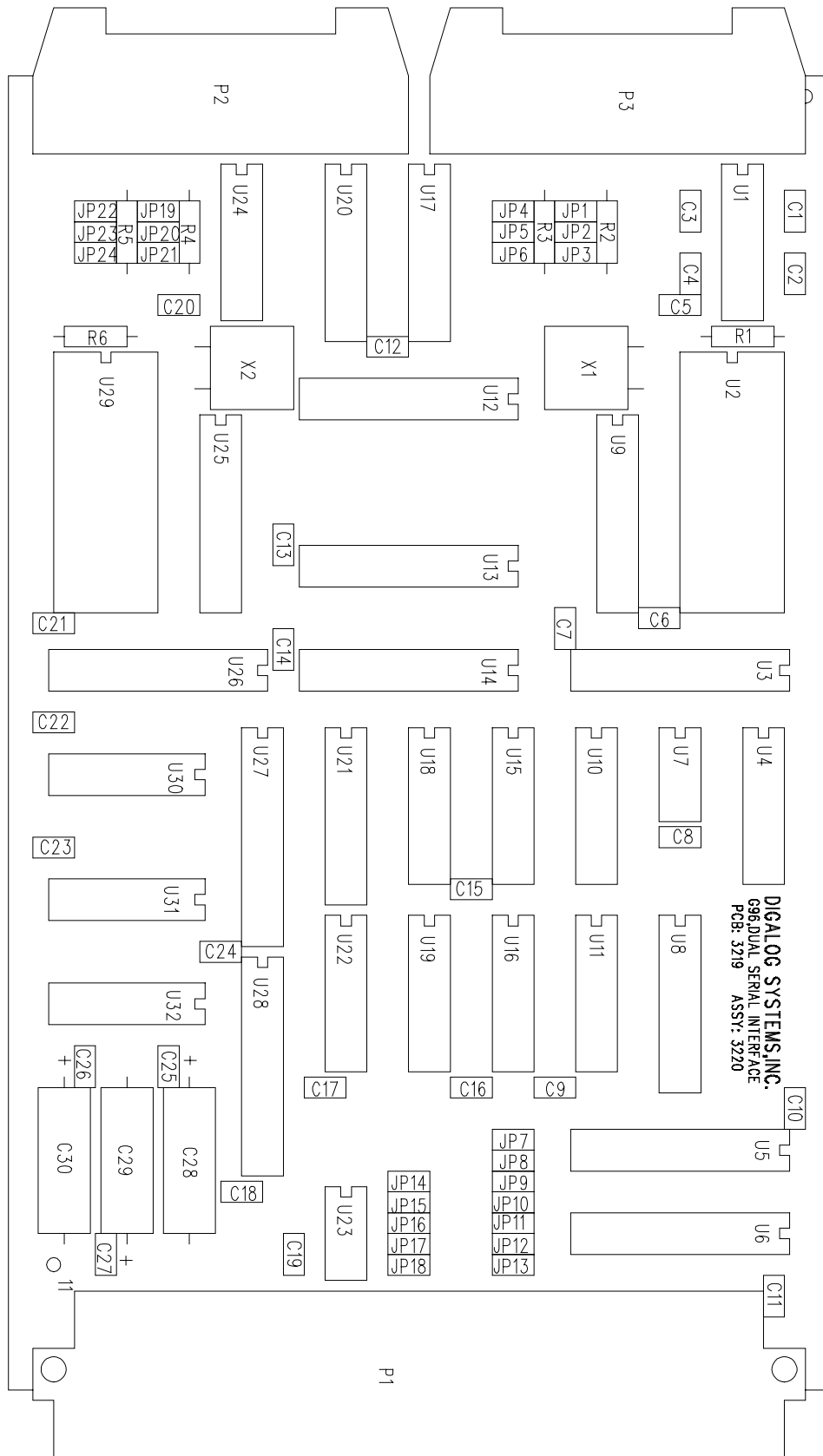
Figure 9 - 0000-3520 Dual Serial Port Card

Figure 10 - 0000-3220 Dual Serial Port Card

SCSI/SASI Host Adapter

The host adapter is a simple G96 card with two MC6821 PIAs to implement a SASI/SCSI bus. The bus is carried by a 50 wire ribbon to the disk controller. The disk controller is mounted on the hard drive.

Access to the card is permitted at odd addresses only. The base address is located in the VPA space of the computer system and is determined by on board jumpers.

Relative Address	Device	Register
1	PIA 0	DDRA/DRA
3	PIA 0	DDRB/DRB
5	PIA 0	CRA
7	PIA 0	CRB
9	PIA 1	DDRA/DRA
B	PIA 1	DDRB/DRB
D	PIA 1	CRA
F	PIA 1	CRB

Table 29 - 2000-3022, 0000-3422 SCSI/SASI Host Adapter Memory Map

For pin assignments of the G-96 bus connector, please see the section titled "G-96 Mother board Assembly".

Jumpers	Function	Jumper	Setting	Result
J3	Base Address Selectors			$681 - $68F in the VPA address range
	Address line A3	J3-A3	Closed	($010)
	Address line A4	J3-A4	Closed	($020)
	Address line A5	J3-A5	Closed	($040)
	Address line A6	J3-A6	Open	$080
	Address line A7	J3-A7	Closed	($100)
	Address line A8	J3-A8	Open	$200
	Address line A9	J3-A9	Open	$400
J2	Interrupt level selection			IRQ 1 selected
	Option code	J2-A	Open	
	Option code	J2-B	Open	
	Option code	J2-C	Open	
	Option code	J2-D	Open	
	PIA 0 interrupt A to IRQ 1	J2-PIA0-IA	Open	
	PIA 0 interrupt A to NMI	J2-PIA0-NA	Open	
	PIA 0 interrupt B to IRQ 1	J2-PIA0-IB	Closed	
	PIA 0 interrupt B to NMI	J2-PIA0-NB	Open	
	PIA 1 interrupt A to IRQ 1	J2-PIA1-IA	Open	
	PIA 1 interrupt A to NMI	J2-PIA1-NA	Open	
	PIA 1 interrupt B to IRQ 1	J2-PIA1-IB	Closed	
	PIA 1 interrupt B to NMI	J2-PIA1-NB	Open	
J1	SCSI/SASI bus parity			Odd parity
		J1-O	Closed	
		J1-E	Open	

Table 30 - 2000-3022 GESHDI-2A Jumper Settings for OS-9 Version 2.4
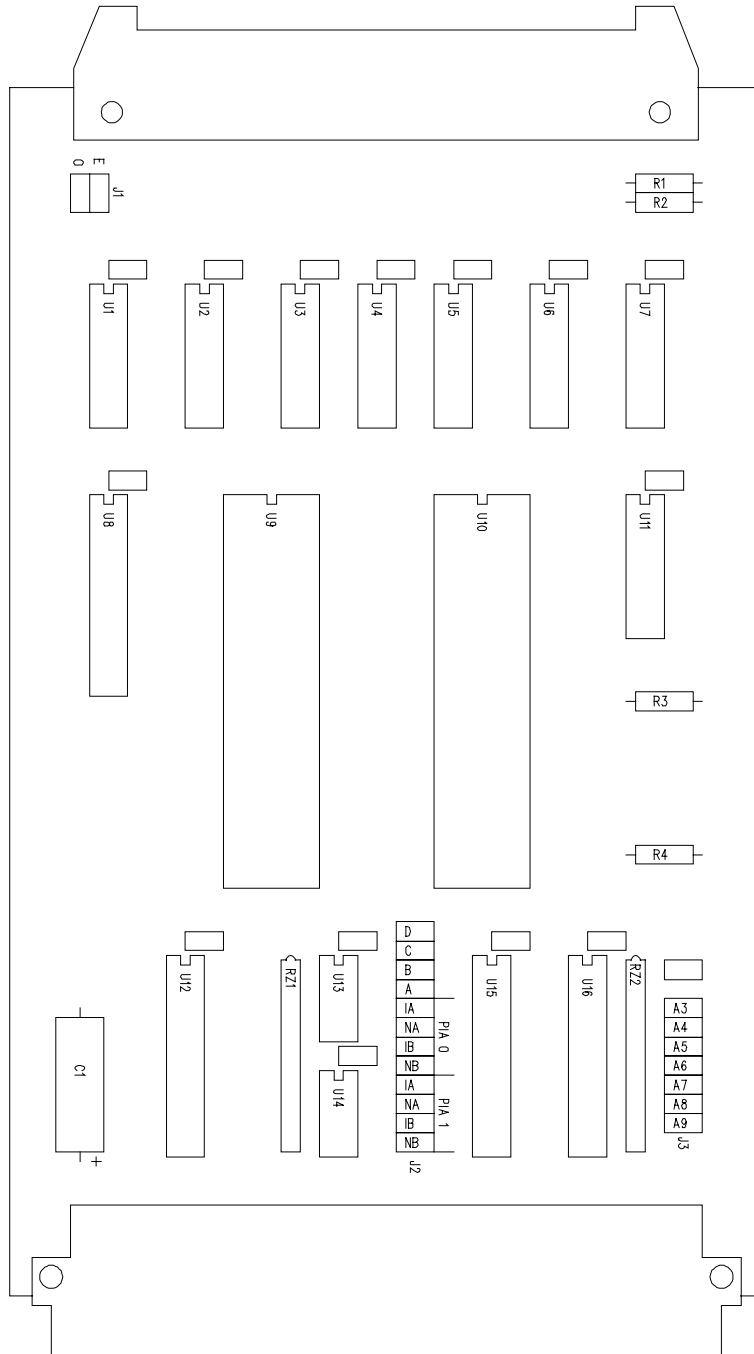
Figure 11 - 2000-3022 GESHDI -2A SCSI/SASI Host Adapter

Jumpers	Function	Jumper	Setting	Result
JP3-JP9	Base Address Selectors			$681 - $68F in the VPA address range
	Address line A3	JP3	Closed	($010)
	Address line A4	JP4	Closed	($020)
	Address line A5	JP5	Closed	($040)
	Address line A6	JP6	Open	$080
	Address line A7	JP7	Closed	($100)

Jumpers	Function	Jumper	Setting	Result
	Address line A8	JP8	Closed	$200
	Address line A9	JP9	Open	$400
JP10-21	Interrupt level selection			IRQ 1 selected
	Option code	JP10	Open	
	Option code	JP11	Open	
	Option code	JP12	Open	
	Option code	JP13	Open	
	PIA 0 interrupt A to IRQ 1	JP14	Open	
	PIA 0 interrupt A to NMI	JP15	Open	
	PIA 0 interrupt B to IRQ 1	JP16	Closed	
	PIA 0 interrupt B to NMI	JP17	Open	
	PIA 1 interrupt A to IRQ 1	JP18	Open	
	PIA 1 interrupt A to NMI	JP19	Open	
	PIA 1 interrupt B to IRQ 1	JP20	Closed	
	PIA 1 interrupt B to NMI	JP21	Open	
JP1-JP2	SCSI/SASI bus parity			Odd parity
		JP2	Closed	
		JP1	Open	

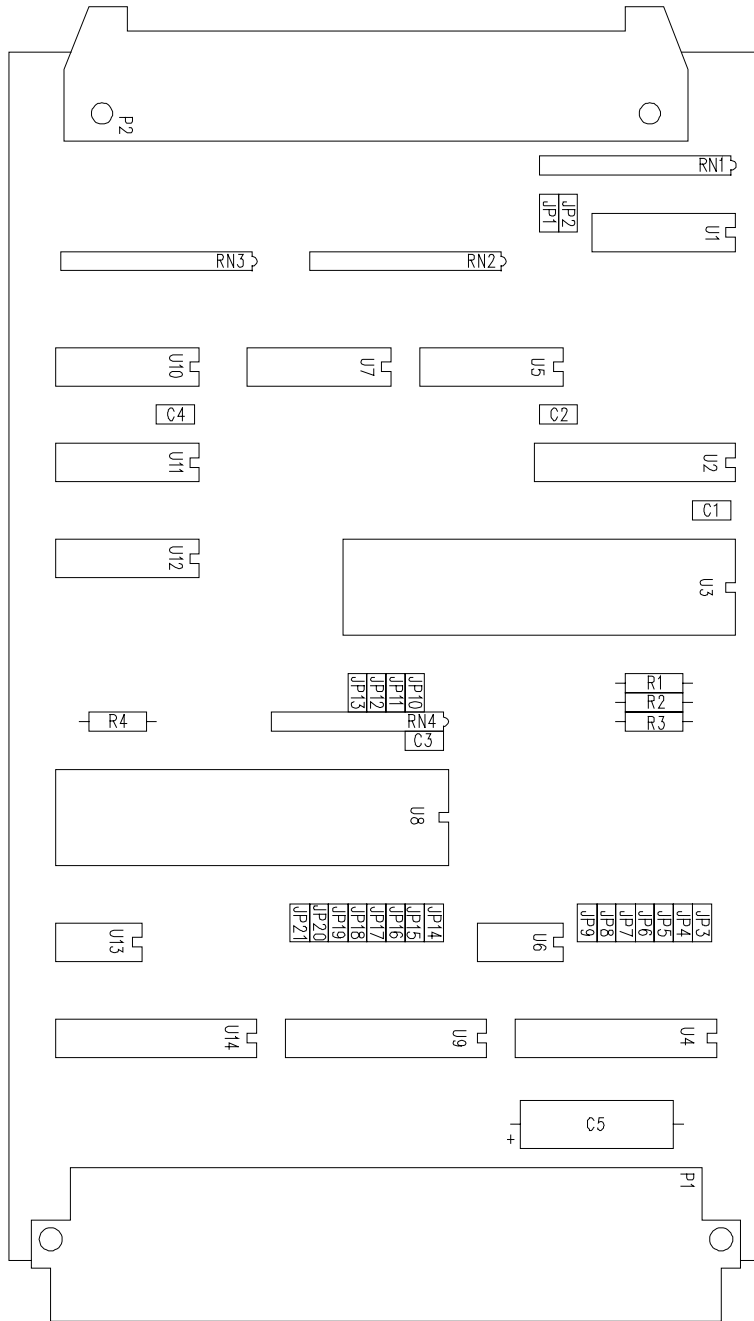**Table 31 - 0000-3422 Jumper Settings for OS-9 Version 2.4**

Figure 12 - 0000-3422 SCSI/SASI Host Adapter

Disk Controller OMTI-5400

The disk controller supports one QIC-02 streaming tape drive and up to three hard/floppy drives in any combination. The standard configuration is one 40 mega byte hard disk, one 720K floppy drive and a cassette cartridge tape drive.

Backup to the tape drive can be accomplished using one tape. The OS-9 utilities Fsave and Frestore are recommended for this procedure.

| Jumpers	Function	Jumper	Setting	Result
W0	SCSI Controller ID			SCSI ID = 0
		W0-0	Closed	0
		W0-1	Open	1
		W0-2	Open	2
		W0-3	Open	3
		W0-4	Open	4
		W0-5	Open	5
		W0-6	Open	6
		W0-7	Open	7
W1	Host parity	W1-1 to W1-2	Open	Parity disabled
		W1-2 to W1-3	Closed	
W2	QIC-02 parity	W2-1 to W2-2	Open	Parity disabled
		W2-2 to W2-3	Closed	
W3/W4	Hard disk sector size			512 bytes/sector
		W3/W4	Open/Open	128 bytes/sector
		W3/W4	Closed/Open	256 bytes/sector
		W3/W4	Open/Closed	512 bytes/sector
		W3/W4	Closed/Closed	1024 bytes/sector
W5	LUN 0 Type Hard or Floppy	W5	Open	Hard
W6	LUN 1 Type Hard or Floppy	W6	Closed	Floppy
W7	LUN 2 Type Hard or Floppy	W7	Open	Hard
W8	LUN 3 Type Tape or Floppy	W8	Open	Tape
W9	Not on board			
W10-W11	Reserved			
		W10	Open	
		W11	Open	
W12-W13	Not on board			
W14	Motor on override	W14	Open	Disabled
W15	Ready override	W15	Open	Disabled
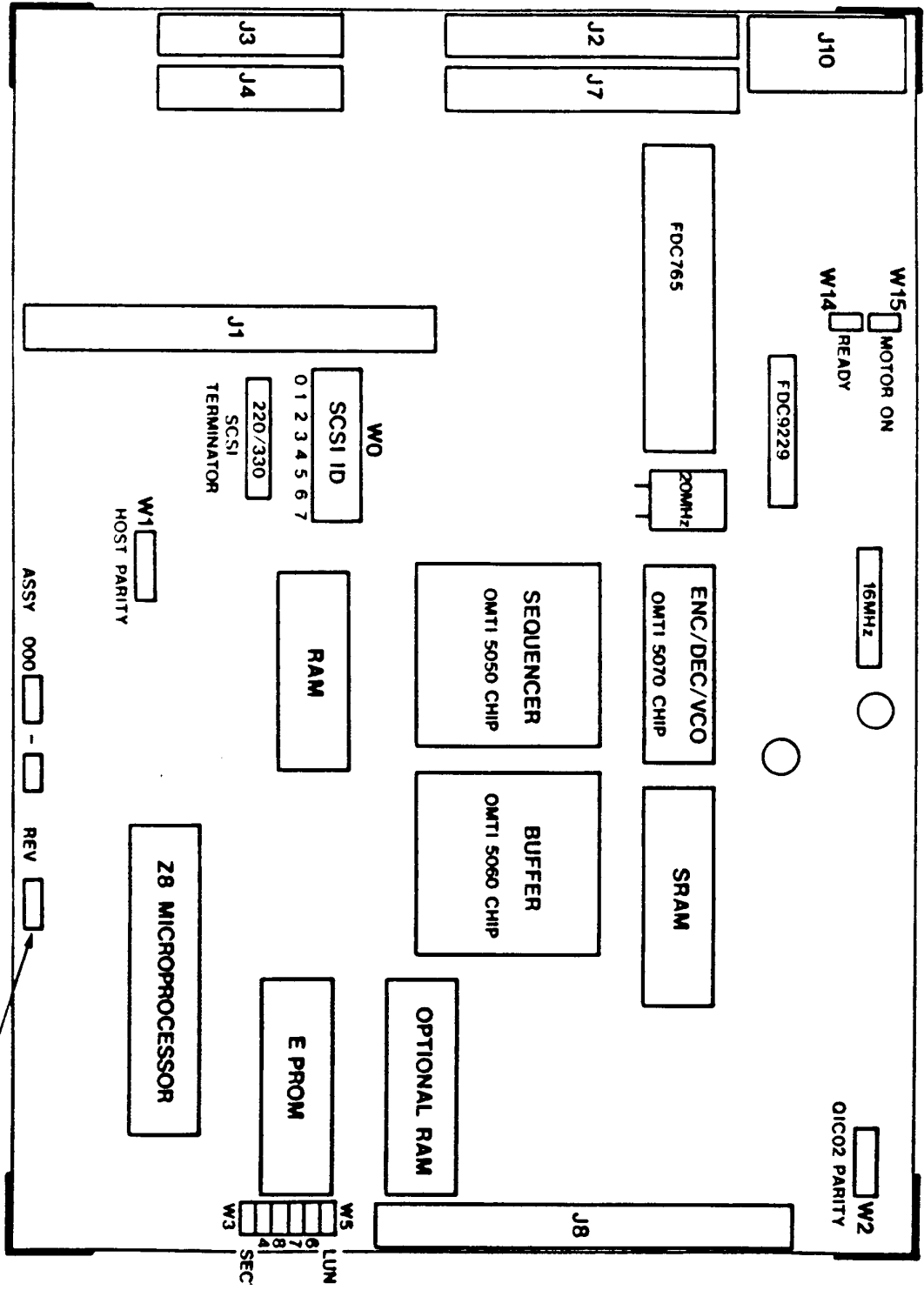
Figure 13 - 2000-3012 Disk Controller OMTI-5400

I/O Controller Assembly

The I/O Controller Assembly contains four serial ports, a printer port and a user keypad port. Two different assemblies are used in the 2030 computer system. The Digalog part numbers for the assemblies are 0000-1568 and 0000-2268.

Software used to set options of the I/O controller are the serial port descriptors t1, t2, t3 and t4 and the printer port descriptor p. An additional descriptor kp is used to control an optional keypad. Control of the board is through the device drivers sc68681 and

The base address and selection of hardware interrupt level is done via jumpers located on the board. The base address is located in the VPA space. Interrupts are from 1 to 5. If the interrupt level selected is vectored then acknowledge priority between boards is handled by the G-96 bus chain in and chain out signals. Interrupt priority on board is the /p VIA, the /t1-/t2 DUART and the /t3-/t4 DUART

Serial Ports

The serial ports are asynchronous format and are controlled by two MC68681 dual UART chips. Jumpers for each serial port select RS-232 (single ended, mark = -12 volts, space = +12 volts) or RS-422 (differential 5 volts) voltage levels.

Data is preceded by a mark to space transition for one bit time and transmitted LSB first, 8 bits, no parity. Software allows selection of 1, 1.5, or 2 stop bit times at mark level. Software selection also allows for selection of standard baud rates at 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 4800, 9600, and 19200. Selecting external baud rate will enable the internal timer but not program the frequency. The frequency may be set by writing to the counter register of the MC68681. The value written is N=115200/rate. The most significant byte of n is written to the chip address +12 and the least significant byte to address +14. Note that if both ports in one chip are set external then both will run at the same rate.

DTR handshake is not implemented. Instead, software provides for transmission to be stopped and started by receipt of the XOFF ($13) and XON ($11) characters.

Printer port

A Centronix type parallel port with active low STB and ACK is provided by a 6522 VIA. The other Centronix control signals are not implemented. Software allows for a timeout error to occur after a programmable delay if ACK does not occur. The VIA used for the printer port also provides an interface for a 24 key matrix encoded keypad.

Memory Map

Access to the card is permitted at odd addresses only. The base address is located in the VPA space of the computer system and is determined by on board jumpers.

Relative Address	Device	Device Descriptors
$01 - $1F	MC68681 #1	/T1, /T2
$21 - $3F	MC68681 #2	/T3, /T4
$41 - $5F	MC6522	/P, /KP
$61 -$7f	MC6522 Vector register	Repeated 64 times

Jumpers	Function	Jumper	Setting	Result
JP1-JP3	Base Address Selection			VPA+$000
		JP3	Closed	($0100)
		JP2	Closed	($0200)
		JP1	Closed	($0400)
JP7-JP11	Interrupt level selection			IRQ 4
		JP7	Open	
		JP8	Open	
		JP8	Open	
		JP10	Closed	
		JP11	Open	
JP4-JP6	Interrupt priority selection			4
		JP6	Closed	(1)
		JP5	Closed	(2)
		JP4	Open	4
JP12	Chain in, Chain out	JP12-A to JP12-B	Open	Chain out connected
		JP12-B to JP12-C	Closed	

Table 32 - 0000-1568 Jumper Settings for OS-9 V2.4

Note: The 0000-1568 I/O Controller Card shares an interrupt with the GPIB Controller Card, in the OS-9 V2.4 configuration. For this reason the I/O Controller Card must be installed adjacent to and to the right of the GPIB Controller Card.

Jumper	IRQ 1	IRQ 2	IRQ 3	IRQ 4	IRQ 5
JP7	Closed	Open	Open	Open	Open
JP8	Open	Closed	Open	Open	Open
JP9	Open	Open	Closed	Open	Open
JP10	Open	Open	Open	Closed	Open
JP11	Open	Open	Open	Open	Closed
JP6	Open	Closed	Open	Closed	Open
JP5	Closed	Open	Open	Closed	Closed
JP4	Closed	Closed	Closed	Open	Open

Table 33 - 0000-1568 Other Interrupt Possibilities

Jumpers	Function	Jumper	Setting	Result
JP23-JP25	Base Address Selection			VPA+$000
		JP25	Closed	($0100)
		JP24	Closed	($0200)

Jumpers	Function	Jumper	Setting	Result
		JP23	Closed	($0400)
JP27-JP31	Interrupt level selection			IRQ 4
		JP28	Open	
		JP29	Open	
		JP27	Open	
		JP31	Closed	
		JP30	Open	
	Interrupt priority selection			4
		JP26	Closed	(1)
		JP21	Closed	(2)
		JP22	Open	4
JP32	Chain out	JP32	Closed	Chain out connected
JP33	Chain in	JP33	Open	Chain in disconnected.

Table 34 - 0000-2268 Jumper Settings for OS-9 V2.4

Note: The 0000-2268 I/O Controller Card shares an interrupt with the GPIB Controller Card, in the OS-9 V2.4 configuration. For this reason the I/O Controller Card must be installed adjacent to and to the right of the GPIB Controller Card.

Jumper	RQ 1	RQ 2	RQ 3	RQ 4	RQ 5
JP28	Closed	Open	Open	Open	Open
JP29	Open	Closed	Open	Open	Open
JP27	Open	Open	Closed	Open	Open
JP31	Open	Open	Open	Closed	Open
JP30	Open	Open	Open	Open	Closed
JP26	Open	Closed	Open	Closed	Open
JP21	Closed	Open	Open	Closed	Closed
JP22	Closed	Closed	Closed	Open	Open

Table 35 - 0000-2268 Other Interrupt Possibilities

/t1	/t2	/t3	/t4	Setting
JP14	JP19	JP24	JP29	Closed
JP15	JP20	JP25	JP30	Open
JP16	JP21	JP26	JP31	Open
JP17	JP22	JP27	JP32	Open
JP18	JP23	JP28	JP33	Open

Table 36 - 0000-1568 Jumper settings for RS-232

/t1	/t2	/t3	/t4	Setting
JP14	JP19	JP24	JP29	Open
JP15	JP20	JP25	JP30	Closed
JP16	JP21	JP26	JP31	Closed
JP17	JP22	JP27	JP32	Closed
JP18	JP23	JP28	JP33	Open

Table 37 - 0000-1568 Jumper settings for RS-422

Note: It is a Delco Electronics standard that /t3 be set to RS-422 and all other ports to RS-232.

/t1	/t2	/t3	/t4	Setting
JP1	JP6	JP11	JP16	Closed
JP2	JP7	JP12	JP17	Open
JP3	JP8	JP13	JP18	Open
JP4	JP9	JP14	JP19	Open
JP5	JP10	JP15	JP20	Open

Table 38 - 0000-2268 Jumper Settings for RS-232

/t1	/t2	/t3	/t4	Setting
JP1	JP6	JP11	JP16	Open
JP2	JP7	JP12	JP17	Closed
JP3	JP8	JP13	JP18	Closed
JP4	JP9	JP14	JP19	Closed
JP5	JP10	JP15	JP20	Open

Table 39 - 0000-2268 Jumper Settings for RS-422

Note: It is a Delco Electronics standard that /t3 be set to RS-422 and all other ports to RS-232.

For pin assignments of the G-96 bus connector, please see the section titled "G-96 Mother board Assembly".

Connector-Pin	Signal	Connector-Pin	Signal
1	+12V	2	-5V
3	NC	4	+5V
5	NC	6	GND
7	PA0	8	PA1
9	PA2	10	PA3
11	PA4	12	PA5
13	PA6	14	PA7
15	CA1	16	CA2
17	ACK	18	DAT8
19	DAT7	20	DAT6
21	DAT5	22	DAT4
23	DAT3	24	DAT2
25	DAT1	26	STB
27	RDR4	28	TDR4
29	CTS4	30	RTS4
31	RD4	32	TD4
33	RDR3	34	TDR3
35	CTS3	36	RTS3
37	RD3	38	TD3
39	RDR2	40	TDR2
41	CTS2	42	RTS2
43	RD2	44	TD2
45	RDR1	46	TDR1
47	CTS1	48	RTS1
49	RD1	50	TD1

Table 40 - 0000-1568, 0000-2268 Output Connector Pin Out
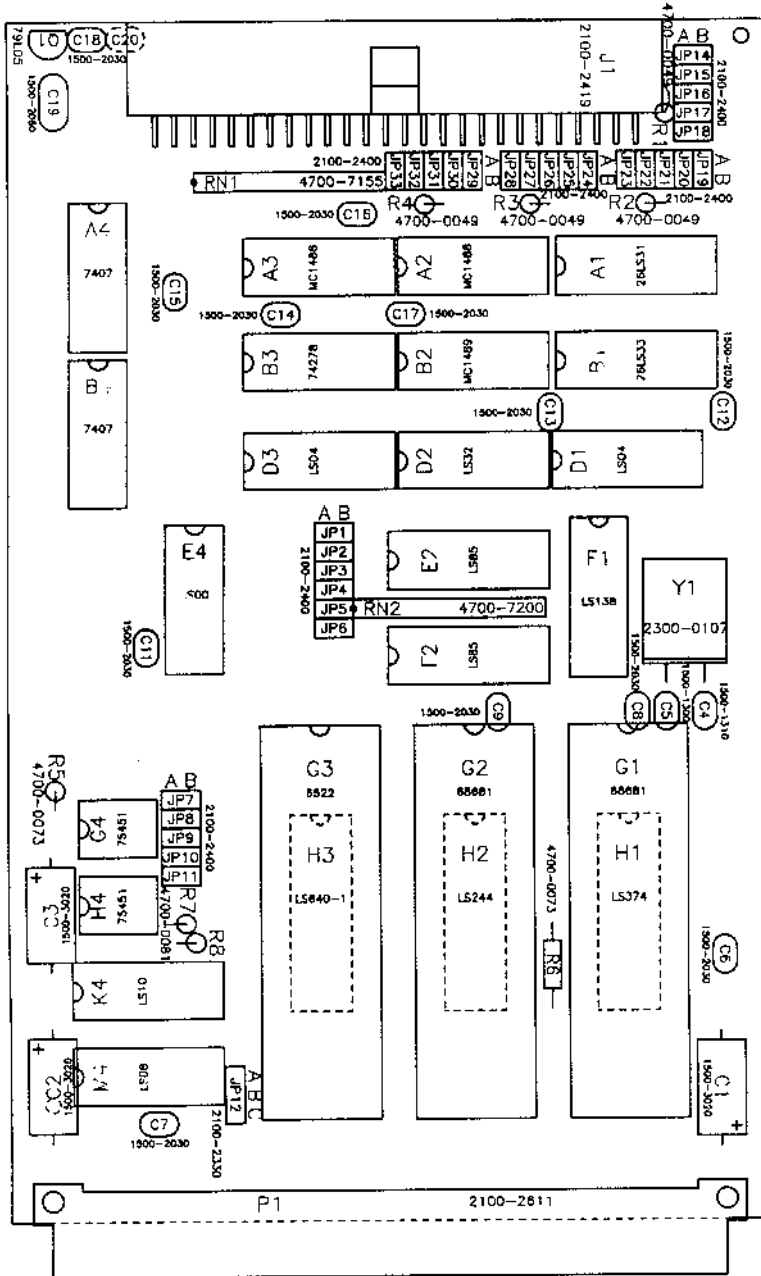
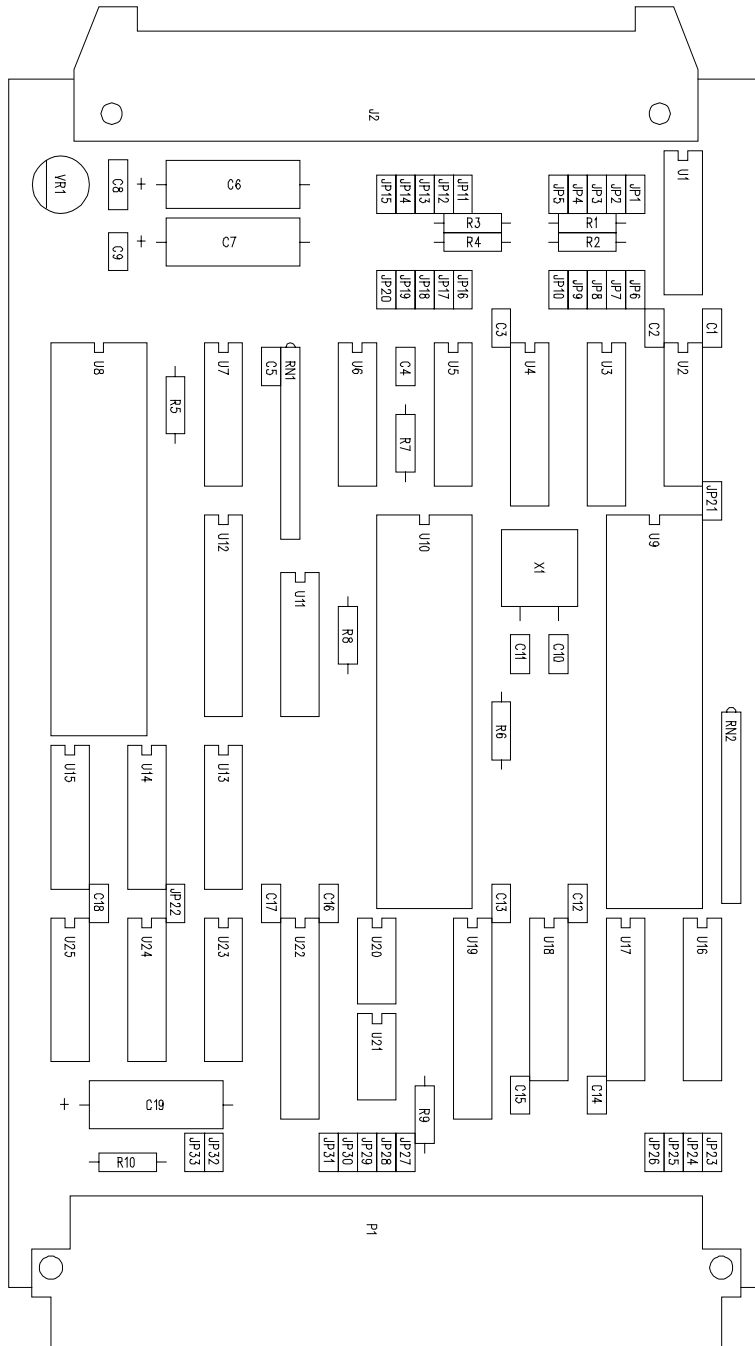**Figure 14 - 0000-1568 I/O Controller Assembly**

Figure 15 - 0000-2268 I/O Controller Assembly

I/O Interface Card

Mounted on a plate at the back of the computer is a circuit card that converts the signals from the I/O Controller assembly to connectors usable by the outside world. This card is called the I/O Interface card and accepts the other end of the 50 pin connector coming from the I/O Controller Assembly. This card contains 4 DB-25 connectors for RS-232/422 a Centronix 36 pin connector for a printer parallel port and a DB-15 connector that is used by a keypad or Operator Interface Panel. The pin out of the connectors are listed in the following tables.

The RS-232 ports located on the 4 DB-25 connectors are configured as DCE ports. This means that there is a driver connected to pins 3 and 5 and a receiver connected to pins 2 and 4. Remember that the signal name for the RS-232 port stays the same. Whether a device is driving or receiving on a particular line is dependent on if that device is DTE or DCE.

Connector-Pin	Signal	Connector-Pin	Signal
1	Frame Ground	2	TD
3	RD	4	RTS
5	CTS	6	DSR
7	GND	8	DCD
9		10	
11	TDR	12	
13		14	
15		16	
17		18	RDR
19		20	DTR
21		22	
23		24	
25			

Table 41 - /t1, /t2, /t3, /t4 Connector Pin Out

Connector-Pin	Signal	Connector-Pin	Signal
1	STB	19	GND
2	DAT1	20	GND
3	DAT2	21	GND
4	DAT3	22	GND
5	DAT4	23	GND
6	DAT5	24	GND
7	DAT6	25	GND
8	DAT7	26	GND
9	DAT8	27	GND
10	ACK	28	GND
11	Frame Ground	29	GND
12		30	GND
13		31	
14		32	
15		33	
16		34	
17		35	
18		36	

Table 42 - /p Connector Pin Out

Connector-Pin	Signal	Connector-Pin	Signal
1	CA2	2	CA1
3	PA7	4	PA6
5	PA5	6	PA4
7	PA3	8	PA2
9	PA1	10	PA0
11	Frame Ground	12	GND
13	GND	14	GND
15	GND		

Table 43 - /kp Connector Pin Out

Testhead Controller Assembly

The Testhead controller card consists of data and address buffers, address decoders and TBus optoisolator circuitry. The TBus isolator is connected via shielded ribbon cable to the Digital motherboard in the Testhead. The TBus provides address, data and timing signals to the cards located in the Testhead. The isolation provided prevents electrical noise from the computer system from interfering with analog measurements.

By using the Testhead Controller Assembly the Testhead is memory mapped into the MC68010 VMA space. The Testhead occupies 256 bytes within this space. Byte swapping is performed on the Testhead Controller Assembly such that the 8 bit TBus appears as contiguous bytes on the 16 bit G96 bus. Only byte write and read commands may be performed within the TBus memory space. Word write and read commands will generate bus errors.

The memory address that the Testhead Controller Assembly occupies is fixed at $FBE900 through $FBE9FF. Jumpers were placed on the board allow the user to select which interrupt the TBus interrupt will be routed to. Later engineering change orders hardwired the interrupt to the G96 bus. No jumpers should be installed on the jumper field.

For pin assignments of the G-96 bus connector, please see the section titled "G-96 Mother board Assembly".

Connector-Pin	Signal	Connector-Pin	Signal
1	TE*	2	TGND
3	TR/W*	4	TGND
5	TINT*	6	TGND
7	TEN*	8	TGND
9	TRESET*	10	TGND
11	TD0*	12	TGND
13	TD1*	14	TGND
15	TD2*	16	TGND
17	TD3*	18	TGND
19	TD4*	20	TGND
21	TD5*	22	+5T
23	TD6*	24	+5T
25	TD7*	26	+5T
27	TA0	28	+5T
29	TA1	30	+5T

Connector-Pin	Signal	Connector-Pin	Signal
31	TA2	32	+5T
33	TA3	34	+5T
35	TA4	36	+5T
37	TA5	38	+5T
39	TA6	40	TA7

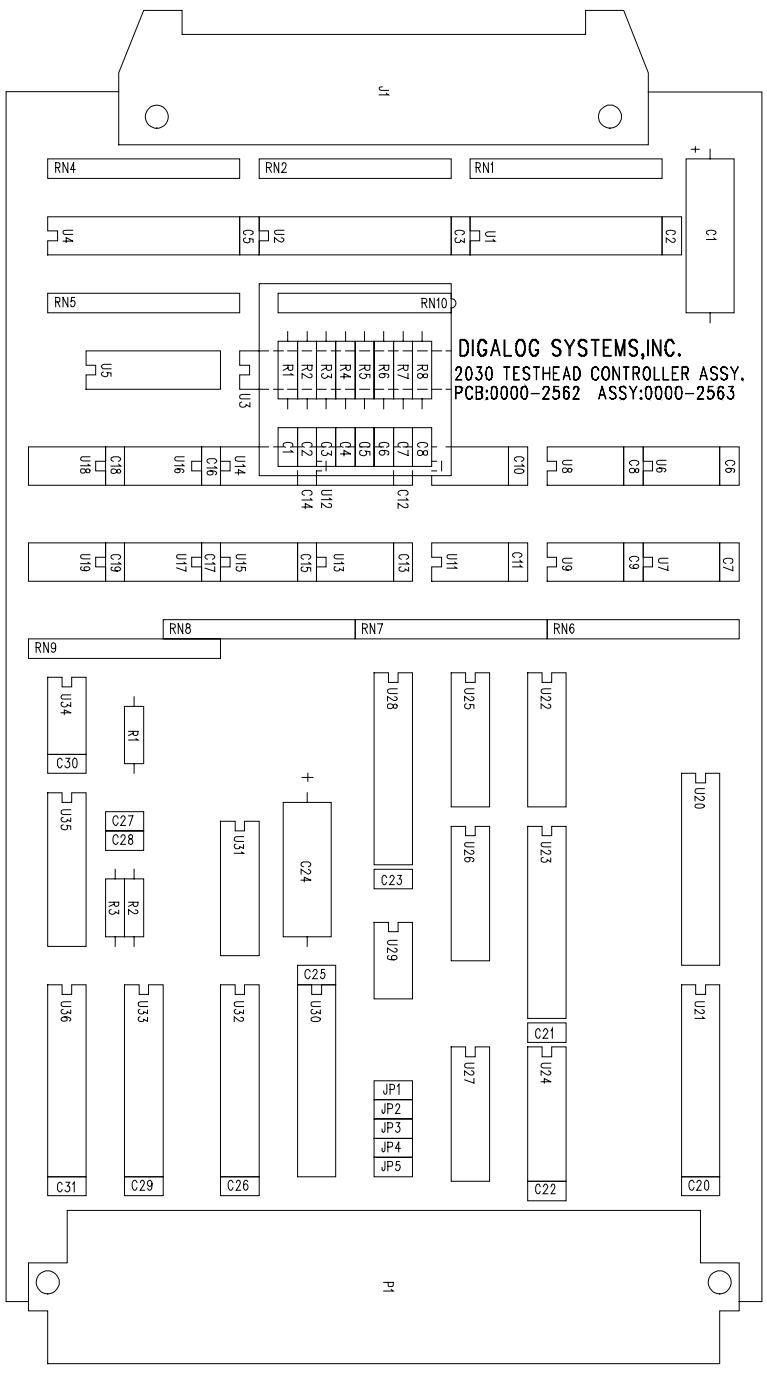**Table 44 - 0000-2563 Output Connector Pin Out**

Figure 16 - 0000-2563 Testhead Controller Assembly

GPIB Controller Assembly

Digalog System's GPIB Controller Assembly uses a TMS9914A chip set to implement the IEEE-488 instrument control bus. Included on the card are interrupt vector registers and daisy-chain IACK logic. The hardware implementation supports the IEEE-488 controller, talker and listener functions. The card is connected to a standard IEEE-488 connector through the Digalog P.N. 0000-2059 cable. Two part numbers have been used for GPIB Controller Assemblies, 0000-1570 and 0000-1970. They are completely interchangeable.

The device driver "gpib" and file manager "SCF" is used to control the functions on the board. System implementation parameters are stored in the device descriptor "g". A "no response" time out and device address parameters are also stored in the descriptor. As Microware had not envisioned using the SCF device drivers and descriptors with an addressable bus, the time out and address parameters are kept in the "tabs" and "tabc" entries of the device descriptor. The time out parameter is stored in "tabs" and GPIB address is stored in "tabc". Application programming of the GPIB Controller Assembly is described in the "Series2030 Analog Manual".

Access to the card is permitted at odd addresses only. The base address is located in the VPA space of the computer system and is determined by on board jumpers.

Relative Address	Device
1-15	TMS9914A Registers
17 - 31	Interrupt vector register (repeated 8 times)

Table 45 - GPIB Controller Address Map

Jumpers	Function	Jumper	Setting	Result
JP1-JP6	Base Address Selection			VPA+$0100
		JP1	Closed	($0020)
		JP2	Closed	($0040)
		JP3	Closed	($0080)
		JP4	Open	$0100
		JP5	Closed	($0200)
		JP6	Closed	($0400)
JP7-JP11	Interrupt level selection			IRQ 4
		JP7	Open	
		JP8	Open	
		JP9	Open	
		JP10	Closed	
		JP11	Open	
JP12-JP14	Interrupt priority selection			4
		JP12	Closed	(1)
		JP13	Closed	(2)
		JP14	Open	4

Table 46 - 0000-1570 Jumper Settings for OS-9 V2.4

Note: The 0000-1570 GPIB Controller Card shares an interrupt with the I/O Controller Assembly, in the OS-9 V2.4 configuration. For this reason the GPIB Controller Card must be installed adjacent to and to the left of the I/O Controller Card.

Jumper	IRQ 1	IRQ 2	IRQ 3	IRQ 4	IRQ 5
JP7	Closed	Open	Open	Open	Open
JP8	Open	Closed	Open	Open	Open
JP9	Open	Open	Closed	Open	Open
JP10	Open	Open	Open	Closed	Open
JP11	Open	Open	Open	Open	Closed
JP12	Open	Closed	Open	Closed	Open
JP13	Closed	Open	Open	Closed	Closed
JP14	Closed	Closed	Closed	Open	Open

Table 47 - 0000-1570 Other Interrupt Jumper Possibilities

Jumpers	Function	Jumper	Setting	Result
JP1-JP6	Base Address Selection			VPA+$0100
		JP9	Closed	($0020)
		JP8	Closed	($0040)
		JP7	Closed	($0080)
		JP6	Open	$0100
		JP5	Closed	($0200)
		JP4	Closed	($0400)
JP7-JP11	Interrupt level selection			IRQ 4
		JP10	Open	
		JP11	Open	
		JP12	Open	
		JP13	Closed	
		JP14	Open	
JP12-JP14	Interrupt priority selection			4
		JP3	Closed	(1)
		JP2	Closed	(2)
		JP1	Open	4

Table 48 - 0000-1970 Jumper Settings for OS-9 V2.4

Note: The 0000-1970 GPIB Controller Card shares an interrupt with the I/O Controller Assembly, in the OS-9 V2.4 configuration. For this reason the GPIB Controller Card must be installed adjacent to and to the left of the I/O Controller Card.

Jumper	IRQ 4	IRQ 2	IRQ 3	IRQ 4	IRQ 5
JP10	Closed	Open	Open	Open	Open
JP11	Open	Closed	Open	Open	Open
JP12	Open	Open	Closed	Open	Open
JP13	Open	Open	Open	Closed	Open
JP14	Open	Open	Open	Open	Closed
JP3	Open	Closed	Open	Closed	Open
JP2	Closed	Open	Open	Closed	Closed
JP1	Closed	Closed	Closed	Open	Open

Table 49 - 0000-1970 Other Interrupt Jumper Possibilities

Connector Pin	Signal	Connector Pin	Signal
J1-1	DIO 1	J1-11	ATN
J1-2	DIO 2	J1-12	GND
J1-3	DIO 3	J1-13	DIO 5

J1-4	DIO4	J1-14	DIO 6
J1-5	EOI	J1-15	DIO 7
J1-6	DAV	J1-16	DIO 8
J1-7	NRFD	J1-17	REN
J1-8	NDAC	J1-18	GND
J1-9	IFC	J1-19	N/C
J1-10	SRQ	J1-20	N/C

Table 50 - 0000-1570, 0000-1970 J1 Connector Pin Out

The connector J1 of the GPIB Controller Assembly does not have a normal pin numbering sequence. Pin 2 is to the right of pin 1 and pin 11 is below pin 1.

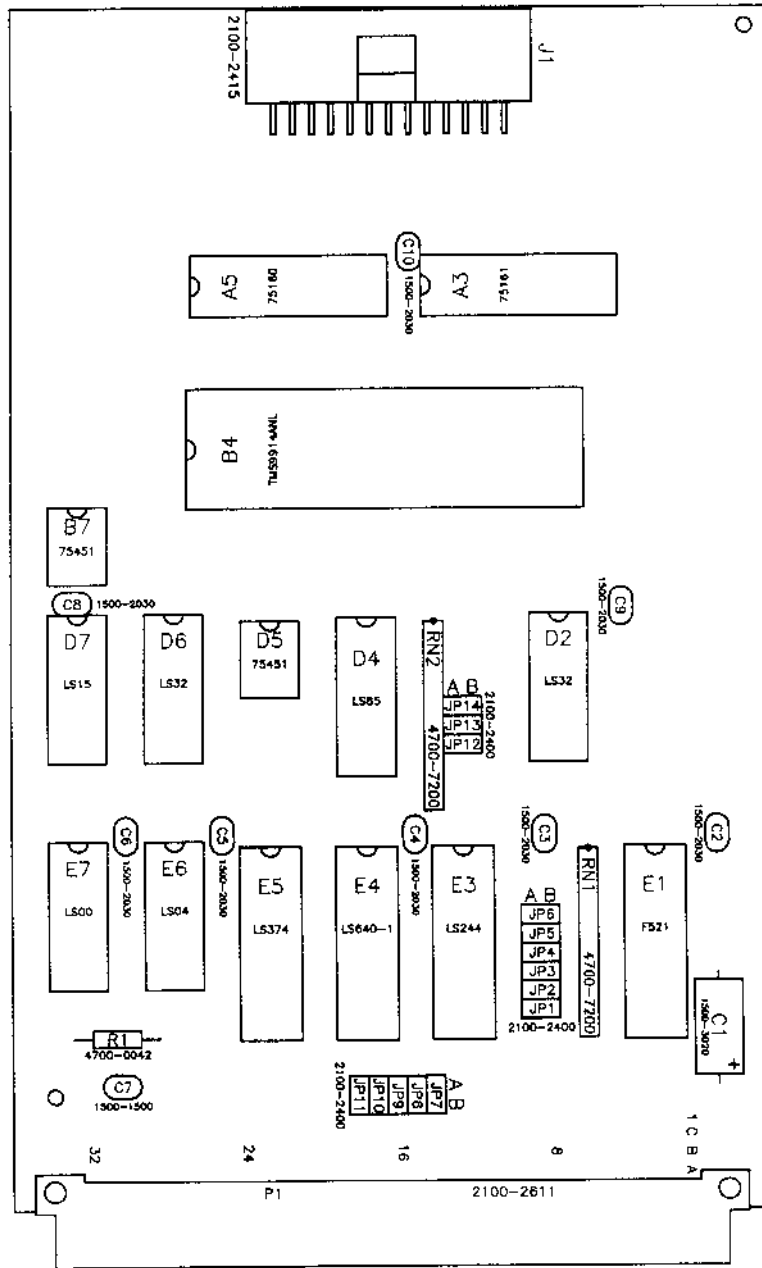*For pin assignments of the G-96 bus connector, please see the section titled "G-96 Mother board Assembly".*

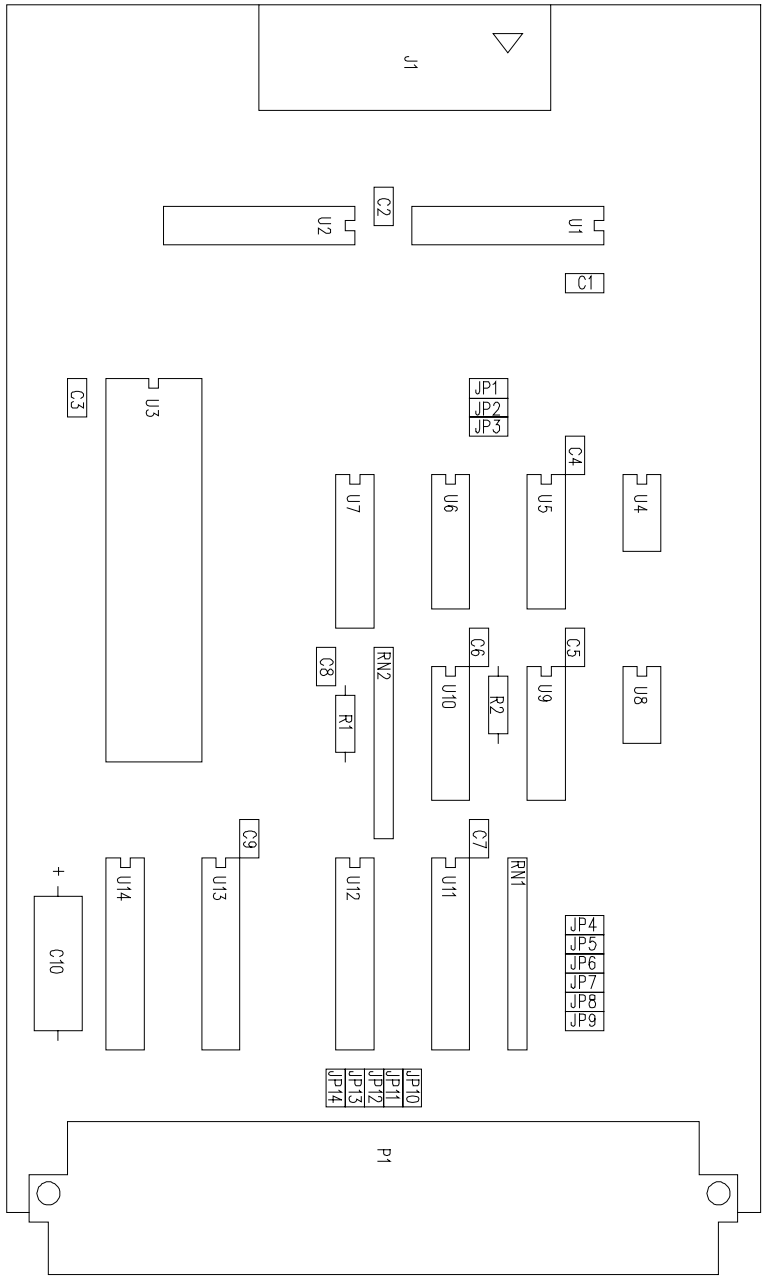**Figure 17 - 0000-1570 GPIB Controller Assembly**

Figure 18 - 0000-1970 GPIB Controller Assembly

Mass Storage Peripherals

Hard Drives

The hard drive used most in the 2030 Computer was either the NEC D5146H or the NEC D3142H. The two drives used have similar specifications. Earlier models used a Teac drive. The NEC drives have a storage capacity of 40 megabytes.

The first hard drive installed into the 2030 Computer must be addressed as unit number 1. The second hard drive must be addressed as unit number 3. Only two hard drives can be supported in the 2030 Computer.

Switch	Number	Position	Result
SW2	1	On	Address 1 selected
SW2	2	Off	Address 2 not selected
SW2	3	Off	Address 3 not selected
SW2	4	Off	Address 4 not selected

Table 51 - 2000-3017 Hard Drive Address Selection

The ST-412 bus used for the hard drives requires termination on the last drive on the cable. Digalog uses a "serial configuration" for multiple drives. This means for the last drive SW1-1 needs to be set to the off position and SW2 through SW-8 needs to be set to the on position. For all other drives SW1-1 through SW1-8 need to be set to the off position.

Floppy Drive

Most of the 2030 Computers use a Teac FD-55FR-511-U floppy disk drive. Some use a FD55GFR model. This floppy disk drive uses a 5.25" double sided double density (DSDD) floppy disk. Formatted storage capacity is about 644 kilobytes.

NOTE: Do NOT use double sided high density (DSHD) disks with this drive. While appearing to work, this floppy disk will not retain data reliably.

This floppy disk drive requires that terminator resistor pack RA1 be installed for proper operation.

Jumper Name	Position	Result
D0	Open	Address 1 not selected
D1	Closed	Address 2 selected
D2	Open	Address 3 not selected
D3	Open	Address 4 not selected
IL	Open	
U1	Closed	
U0	Open	
FG	Closed	
HS	Closed	
HL	Open	
IU	Open	
ML	Open	MOTOR ON input active
RY	Closed	

Table 52 - 2000-3016 Floppy Disk Drive Jumper Settings

For the FD55GFR Jumper settings please consult the factory.

MAINTENANCE

Procedure for installing 2nd hard disk

1.) Remove the 68000 computer rack from the system.

2.) Remove the right rear panel of the computer. This is the panel that contains the power switch. There is no need to disconnect the wires.

3.) The hard disk assembly should now be visible from the back of the computer. Remove the hard disk assembly according to the directions on page 25 of chapter 6 of the 2030 analog tester manual. Be sure to note the positions of all cables.

4.) The hard disk just taken out is known as "/S0." The one that is going to be installed will be known as "/S2." If **/SO** is a NEC D5146H or D3142H, check to see that S1-1 is in the "off" position.

5.) The jumpers for /S2 (NEC D3142H) are:

Switch	Position
S1-1	OFF
S1-2	OFF
S1-3	OFF
S1-4	OFF
S1-5	OFF
S1-6	OFF
S1-7	OFF
S1-8	OFF
S2-1	OFF
S2-2	OFF
S2-3	ON
S2-4	OFF

Table 53 - NEC D3142H /S2 Jumper Positions

The jumpers for /S2 (Toshiba M222XD2) are:

Jumper	Position
1 TO 2	OFF
3 TO 4	OFF
5 TO 6	ON
7 TO 8	OFF
9 TO 10	OFF
11 TO 12	ON
SW1-1	OPEN
SW1-2	OPEN
SW1-3	OPEN
SW1-4	OPEN
SW1-5	OPEN
SW1-6	OPEN
SW1-7	OPEN
SW1-8	OPEN

Table 54 - Toshiba M222XD2 /S2 Jumper Positions

/SO will have to be repositioned in the mounting plates in order to install /S2. Install /S2 immediately under and with the same orientation as /SO.

7.) Install cable 0000-2054 to J4 of the OMTI5400 board and J2 of /S2.

8.) Replace cable 0000-2051 with cable 0000-2045. The middle connector of this cable connects to /S2 (J1).

9.) Install cable 6000-2044 in the computer.

10.) Re-install the hard drive assembly into the computer.

11.) Check disk operation by using the OS-9 utility Dcheck.

12.) Re-install the computer rack back into the system.