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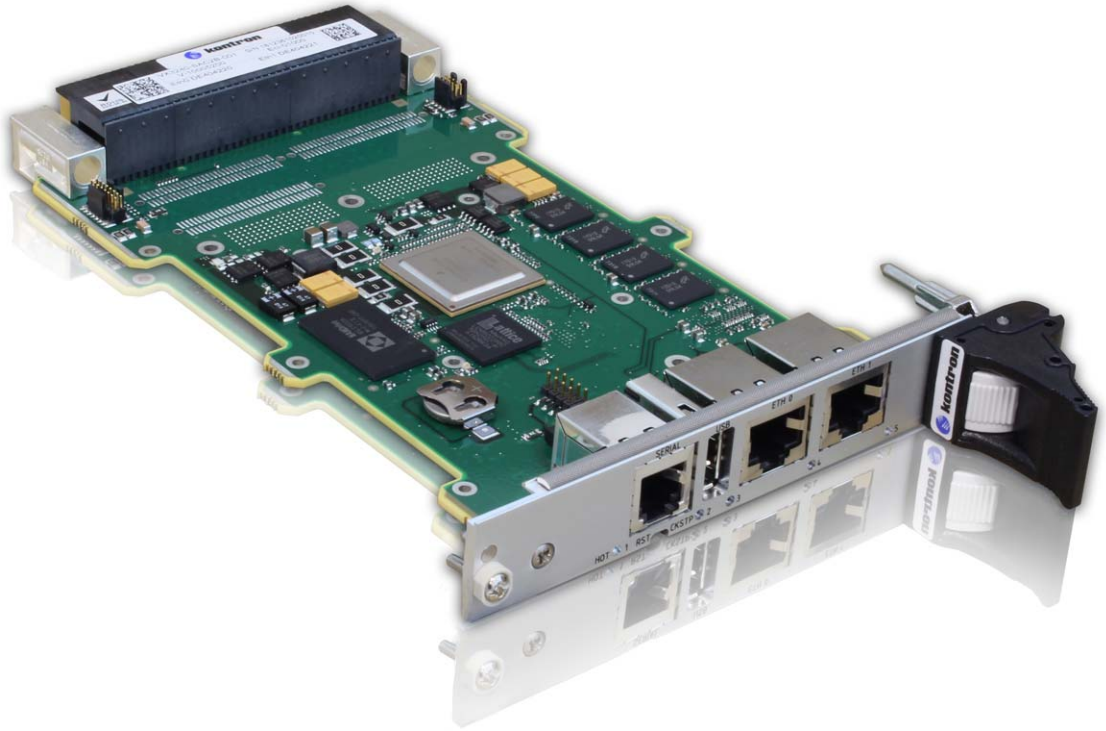
» VX3240 «



3U VPX Single Board Computer
User's Guide

CA.DT.B07-0e - July 2013

Revision History

Publication Title:	VX3240 User's Guide	
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- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1 - Introduction

VX3240 is a low-power 3U VPX SBC featuring a quad-core Freescale P2041 QorIQ™ device with quad PowerPC e500mc cores at 1.2 GHz. VX3240 supports up to 8 GB DDR-3 SDRAM and provides a wide range of I/Os including Gigabit Ethernet, GPIOs, PMC/XMC I/Os, USB, SATA and serial ports. With such a features set, the VX3240 is the ideal general purpose solution for SWaP-C constrained embedded applications. Coupled with Kontron Long Term Supply policy, VX3240 is the perfect migration path to a new 10+ year period of deployments for PowerPC-based applications in the Military, Aerospace and Transportation markets.

In this document, the term:

- **VX3240** refers to the 3U VPX board
  - VX3240-SA refers to the standard commercial version of the board.
- **VX3240-RTM** refers to the 3U VPX Rear Transition Module (RTM).

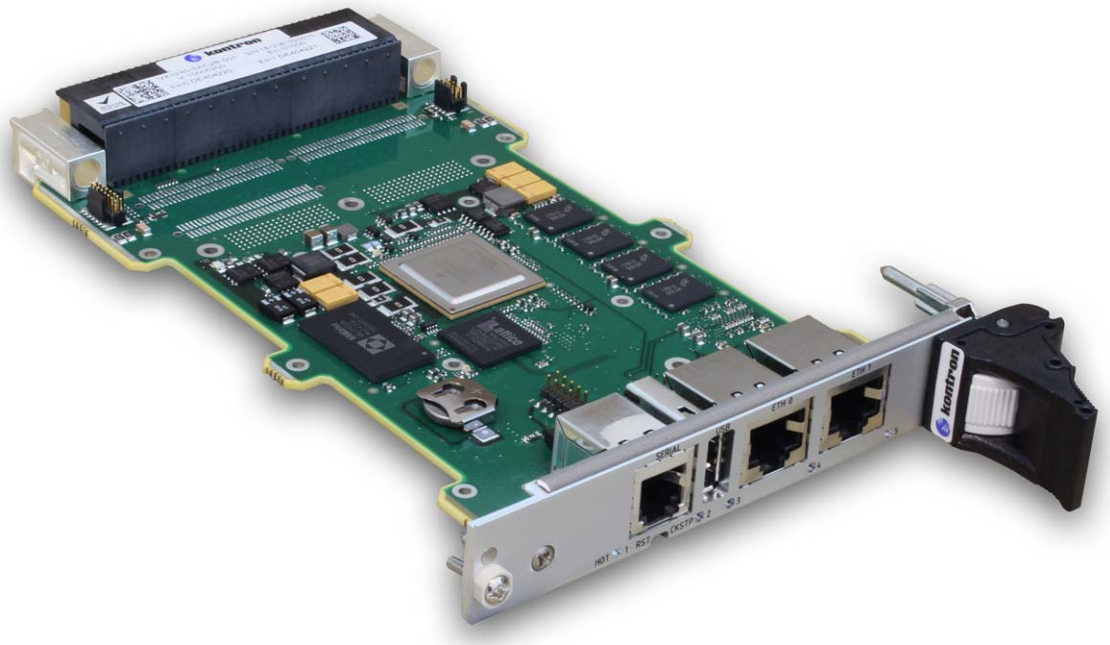


Figure 1: VX3240-SA Overview

1.1 Manual Overview

1.1.1 Objectives

This guide provides general information, hardware preparation and installation instructions, operating instructions and a functional description of the VX3240 board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.8 “Related Publications").

As the standard policy for all the Kontron, hardware technical documentation reflects the most recent version of our products. The “Hardware Release Notes" (see section 1.8 “Related Publications") is to help to keep track of various evolutions that have happened during the early steps of the VX3240 ramp-up or later in its lifetime.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2 Audience

This guide is written to cover, as far as possible, the range of people who will handle or use the VX3240, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, systems, cabling, grounding and communications.

1.1.3 Scope

This guide describes all variants of the VX3240 series. It does not cover any PMC modules which are described in specific guides (see section 1.8 “Related Publications").

1.1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Functional Description
- Chapter 3 - Physical I/O
- Chapter 4 - Installation
- Chapter 5 - Power Considerations
- Chapter 6 - VX3240-RTM Characteristics
- Chapter 7 - Backplane Suggestions

1.2 VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is a proposed ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

For further information regarding this standards and its use, visit the home page of the VITA - Open Standards, Open Markets.

1.3 Board Overview

1.3.1 Main Features

» Freescale QorIQ™ P2041 Architecture

The VX3240 3U VPX SBC is based on the Freescale QorIQ™ P2041 integrated host processor, clocked at 1.2 GHz.

The QorIQ™ P2041 combines four e500mc processor cores built on Power Architecture® technology with high-performance data path acceleration architecture (DPAA), CoreNet fabric infrastructure, as well as network and peripheral bus interfaces required for networking, Telecom/datacom, wireless infrastructure, and military/aerospace applications.

The QorIQ™ P2041 is a flexible device that can be configured to meet many system application needs. The P2041's e500mc cores can be combined as a fully-symmetric, multiprocessing, system-on-a-chip, or they can be operated with varying degrees of independence to perform asymmetric multiprocessing. Full processor independence, including the ability to independently boot and reset each core, is a defining characteristic of the QorIQ™ P2041. The ability of the cores to run different operating systems, or run OS-less, provides the user with significant flexibility in partitioning between control, datapath, and applications processing. It also simplifies consolidation of functions previously spread across multiple discrete processors onto a single device.

The QorIQ™ P2041 offers four high-performance 32-bit e500mc cores built on Power Architecture® technology. Like previous e500 cores, each e500mc is a superscalar dual issue processor, supporting out-of-order execution and in-order completion, which allows the e500mc core built on Power Architecture® technology to perform more instructions per clock than other RISC and CISC architectures.

» Soldered DDR3 Memories with the Support of ECC

The QorIQ™ P2041 accesses one memory-channel having a total size of 2, 4 or 8 GB. The DDR3 memory technology used operates at 1066 Gbits/s. The resulting peak memory bandwidth is 8.5 GB/s. An 8 bits ECC memory is implemented to detect and correct errors.

Numerous Storage Interface

The following storage features are available:

- An onboard or mezzanine SATA NAND Flash with 32 GB capacity (Multiple Levels Cell) or 8 GB capacity (Single Level Cell extended temperature).
- Dual redundant 128 MB NOR flash memory is used to store firmware code.
- Two serial 256 Kbits EEPROMs are dedicated to system and application data storage.
- A 1 Mbits ferroelectric, non-volatile random access memory allows the backup of critical data when the board is powered off. This 1 Mbits ferroelectric RAM is a user memory device.

One SATA gen1 and one USB 2.0 port available on the P1 backplane connector.

Backplane Switch

Available on P1 connector:

- Two compliant VITA 31.1 Gigabit Ethernet links,
- One 4x PCI Express gen 2 link without Non Transparent (NT) capability.

Extensive I/O Connectivity

The VX3240 provides two 10/100/1000BASE-TX Ethernet interfaces, two EIA-232 serial lines, two general purpose I/Os, two USB 2.0 links, two SATA interfaces and one 4x PCI-Express link.

Software

The VX3240 is delivered with the OpenSource U-Boot firmware.

The VX3240 supports the OpenSource YOCTO Project Poky Danny 1.3 release (http://git.yoctoproject.org/cgit/cgit.cgi/poky/refs/tags) used together with the Freescale PowerPC layer (http://git.yoctoproject.org/cgit/cgit.cgi/meta-fsl-ppc/) which generates a 3.0.48-r10 Linux kernel. Kontron has a meta-vx3240 layer which further refines this development kit specifically for the VX3240 board.

Harsh Environments

The VX3240 has been designed using the same PCB for both air and conduction-cooled boards. Builds variants span a complete range of temperature, shock and vibration requirements as specified in the VITA 47 standards.

Rear Transition Module

The VX3240 supports the PB-VX3-001, a 3U VPX Rear Transition Module compliant with the definition of the Rear Transistion Module on VPX standard - VITA 46.10.

It offers connectivity on the rear for:

- One USB 2.0 port
- Two Gigabit Ethernet ports without LED signals
- Two COM (Serial) ports
- One SATA gen 2 port
- Two GPIOs
- One Reset button
- One System Management Bus Connector
- One JTAG connector

1.3.2 Order Code Table

Available order codes are listed in table below:

Article	Order Code	Description
		3U VPX Air-Cooled Commercial Build SBC
VX3240-SA	VX3240-SAC2-00000	VX3240 Air-Cooled Commercial Build, QorIQ P2041 1.2 GHz, 2 GB DDR3-SDRAM, no Sata Flash (MLC) on board, no XMC/PMC slot, 1000BASE-T Ethernet interfaces
		Associated Products
VX3240-RTM	PB-VX3-001	VX3240 VPX Rear Transition Module (no PIM connector), 10/100/1000BASE-TX Ethernet interfaces
COP/JTAG Module	COP-PN3-B	COP JTAG Equipment
Serial Cable	KIT-RJ12DB9	Serial Cable Adapter

Table 1: Order Code

1.3.3 I/O Interfaces

Front Interfaces

FUNCTION	DESCRIPTION
Gigabit Ethernet	Two 1000BASE-T ports on RJ-45 connectors
Serial	One RJ-12 connector for EIA-232 simplified UART interface (with RTS/CTS)
USB	One USB 2.0 port on 4-pin standard USB connector
LEDs	Three LEDs reporting the board CPU health status and activity
Reset	Board Reset Button

Table 2: Front I/O Interfaces

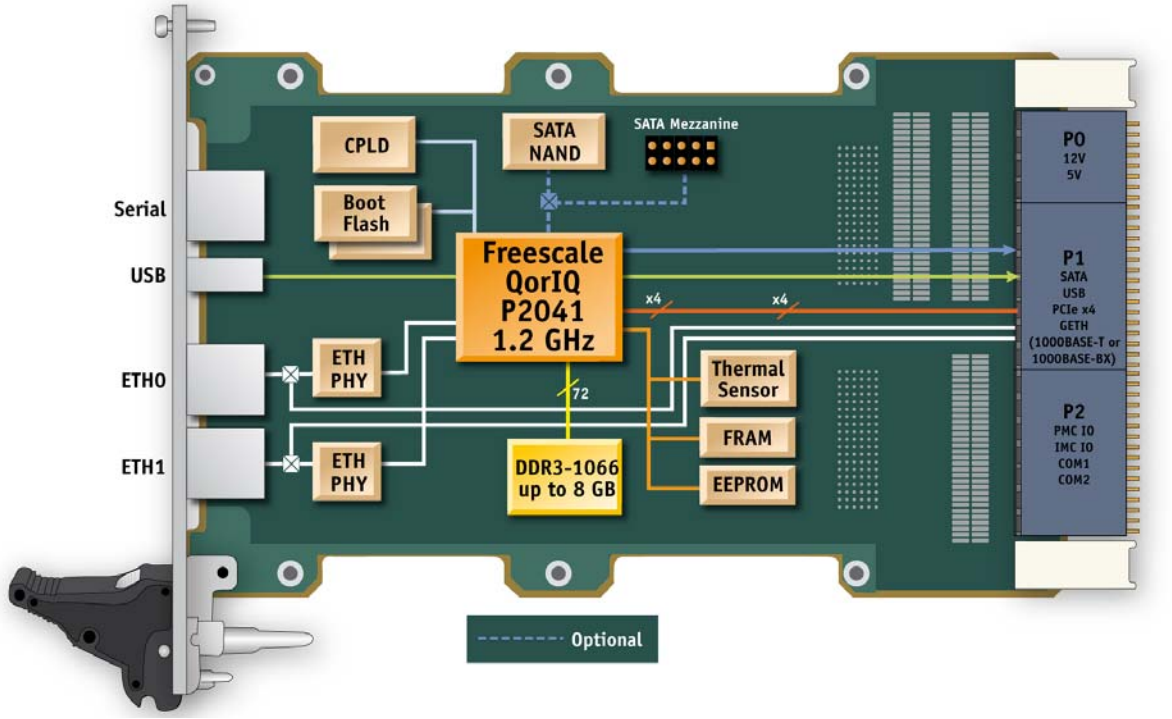
Rear Interfaces

FUNCTION	DESCRIPTION
VPX	VPX standard on P0/P1/P2
Gigabit Ethernet	Two Gigabit Ethernet ports on P1
PCI Express	PCI Express x4 on P1 (VITA 46.4)
Serial	Two simplified EIA-232 interfaces on P2 (with RTS/CTS)
USB	One USB 2.0 port on P1
SATA	One SATA II port on P1
Reset	Main reset input available on P0 connector
GPIOs	2 User GPIOs on P1 and 3 additional GPIOs on P0
SMB	2x System Management Bus on P0

Table 3: Rear I/O Interfaces

1.4 Functional Block Diagram

The following diagrams provide additional information concerning board functionalities and components layout.



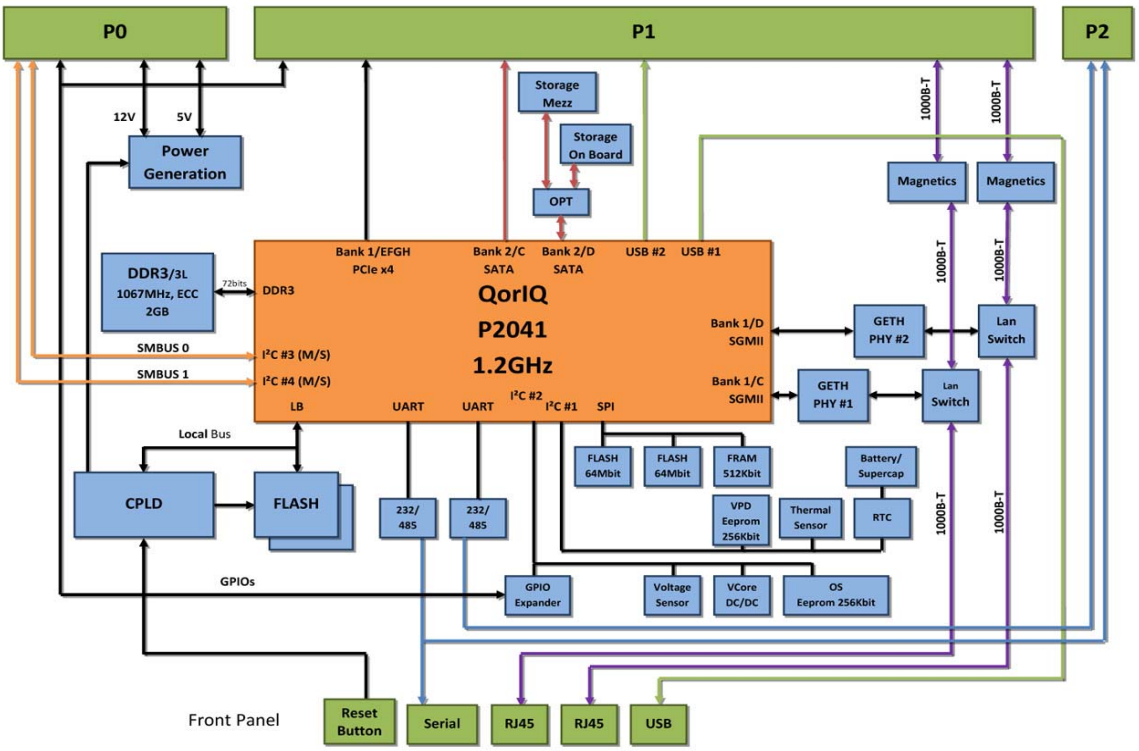


Figure 2: VX3240 Functional Block Diagrams

1.4.1 VX3240 Components Layout

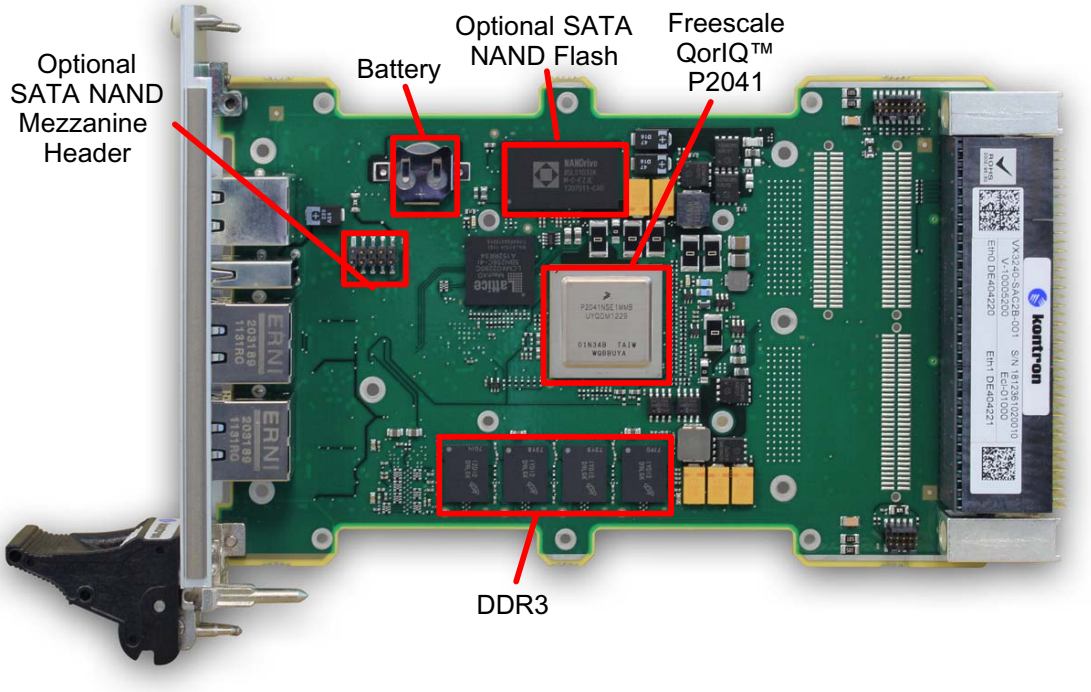


Figure 3: VX3240 Components Layout (Top View)

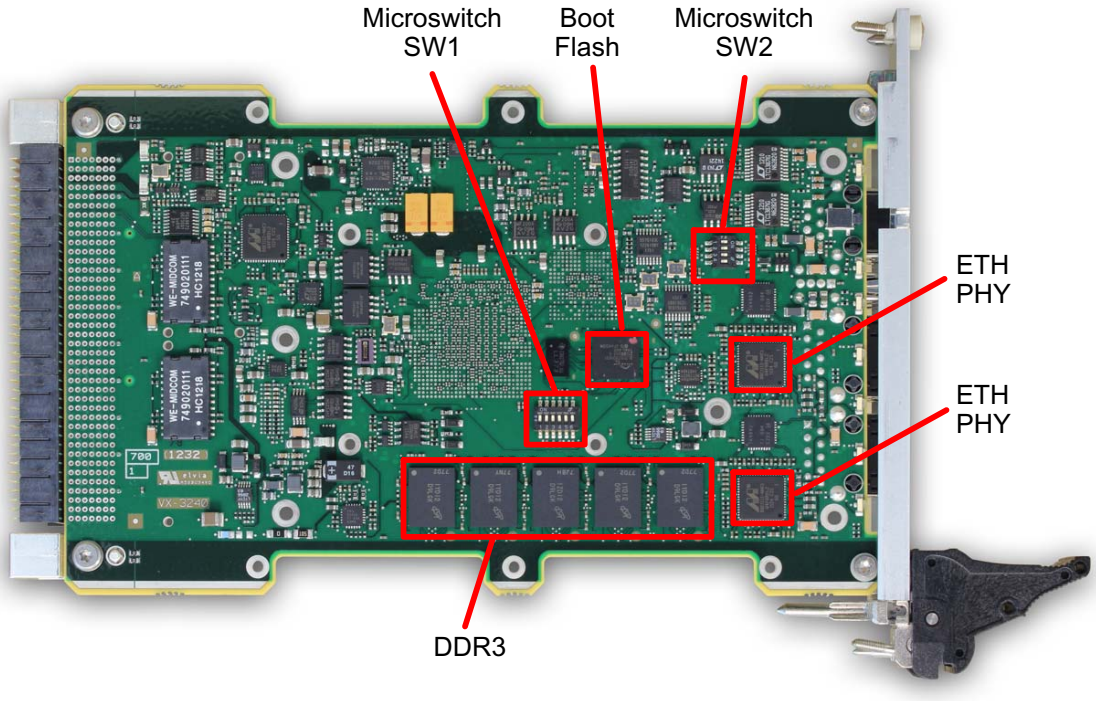


Figure 4: VX3240 Board Components Layout (Bottom View)

1.5 Technical Specification

VX3240	SPECIFICATIONS
Form Factor	
Form Factor	VPX 3U, single slot 0.8”
Processor and Chipset	
Processor	Freescale QorIQ™ P2041 (quad e500mc core) @ 1.2 GHz.
Cache Structure	L1 cache: 32 KB Data + 32 KB Instruction L2 cache:128 KB, CPCache: 1024KB
Gigabit Ethernet Controller	Three on-chip, triple-speed Ethernet controllers supporting 10 Mbps, 100 Mbps and 1 Gbps Ethernet/IEEE®802.3 networks with SGMII utilization.
Memory Controller	Integrated DDR3 memory controller with ECC support, up to 1200 MHz, 72-bit.
SATA	Up to 3 Gb/s integrated Serial ATA host controllers on up to 2 ports. One SATA link on VPX P1 and one for onboard SSD Disk.
USB	Two Enhanced Host Controllers Interface (EHCI) that allow data transfers up to 480 Mb/s. One USB link on front panel or rear panel P1 and one on rear panel P1 only.
UARTs	2 x UART, 16550-style, 4-wires.
PCI Express	One x4 Gen2 link (5Gbps)
Memory	
System Memory	One single bank 2 GB DDR3 SDRAM @1200 MHz, 64-bit wide + ECC, soldered.
Firmware Boot device	128 MB soldered NOR flash for U-Boot, redundant boot device (2 x 64 MB partition)
SSD SATA Disk	Up to 32 GB (MLC technology) SSD SATA disk SATA Nand Flash storage on socket (for SATA Nand Flash modules) or directly onboard.
FRAM	1 Mbit F-RAM on SPI (default) or I2C (spare option)
EEPROM	1 x serial 256 Kbit EEPROM dedicated to DDR data (spare EEPROM for SPD) 1 x serial 256 Kbit EEPROM dedicated to system data (VPD) 1 x serial 256 Kbit EEPROM dedicated to application data 1 x serial 256 Kbit EEPROM dedicated to firmware boot (spare EEPROM) 1 x serial 256 Kbit EEPROM dedicated for board date (spare EEPROM)
SPI	Two 64 Mbit flashes

VX3240	SPECIFICATIONS
Onboard Controllers	
Watchdog	No watchdog controller.
RTC	I²C Real Time Clock, RV-8564-C2 from Micro-Crystal Switzerland.
Gigabit Ethernet PHY	Three Marvell 88E1112 transceivers with SerDes and Copper media interface.
System cPLD	Board controller for power sequencing control, reset generation and distribution, monitoring, system clock configuration and flash booting bank selection. Also provides configuration/status registers on local bus processor interface.
Hardware Monitoring	Temperature (LM73) and Voltage (NCT7802Y) sensors.
GPIO Expander	I²C GPIO Expander PCA9672.
System Rear Intectonnection	
Gigabit Ethernet	Two 1000BASE-T on P1 switchable on front panel by microswitches (onboard LAN switch).
PCI Express	x4 Gen2 (5 Gbps) PCI Express on P1.
USB Port	One (default) or two high-speed USB Port on P1.
SATA Port	One SATA Port on P1.
Serial Ports	Two EIA-232 Serial Ports on P2.
GPIOs	Three GPIOs on P0. Two GPIOs on P1.
Front Interfaces	
Gigabit Ethernet	Two 1000BASE-T on RJ-45 connectors switchable on rear panel by microswitches (on board LAN switch).
Serial Port	One EIA-232 Serial Port on RJ-12 connector.
USB Port	One USB connector
Reset	Reset button
LEDs	5 bicolor LEDs.
Various Interfaces	
Debug Interface	JTAG/COP port for emulation probe connection.

VX3240	SPECIFICATIONS
MISC	
Battery	BR1225 on board socket.
Firmware	U-Boot
Backplane Power Supply	VS1 (+12V), VS3 (+5V) inputs fully protected by fuse. VS2 (+3V3) not used. +3V3 SB optional. +12V SB and -12V SB not used.
Operating temperature Range	0.8" SA: 0°C to +55ºC with passive module heat sink, forced system airflow (1.8 m/s to 3 m/s depending on the processor heatsink)
Humidity	0-90% non-condensing (SA), 95% Coated.
Board Weight	SA environment class: 250g with heatsink

Table 4: VX3240 Main Specifications

For a detailed description of the VX3240-RTM (Rear Transition Module), refer to the Technical Specifications table in Chapter 6 " VX3240-RTM Characteristics", section 6.2 "Technical Specifications" page 56.

1.5.1 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

VX3240-SAA1N-000

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)	IEC62380
	25°C	40°C	40°C	25°C	40°C	55°C	Typical Railway Mission Profile
VX3240/SA	318 426h	228 653h	31696h	51 971h	41 492h	8 237h	341 175h

Table 5: VX3240-SAA1N-000 MTBF Data

1.6 Software Support

Kontron is one of the few cPCI, VME and VPX vendors providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, customers possessing a maintenance agreement with Kontron can be guaranteed hotline software support and are supplied with regular software updates. A dedicated web site is also provided for online updates and release downloads.

The VX3240 can operate under the following operating system:

- Linux

Please contact Kontron for further information concerning other operating systems and software support.

1.7 Standard

This Kontron product complies with the requirements of the following standards.

TYPE	ASPECT	DESCRIPTION
CE	Emission	EN55022 EN61000-6-3
	Immission	EN55024 EN61000-6-2
	Electrical Safety	EN60950-1
Mechanical	Mechanical Dimensions	IEEE1101.10
Environmental	WEEE	Waste electrical and electronic equipment
	RoHS	Restriction of the use of certain hazardous substances in electrical and electronic equipment

Table 6: Standards

1.7.1 Environmental Specifications

	SA - Standard Commercial
Conformal Coating	Optional
Airflow	2 m/s
Temperature	VITA 47-Class AC1
Cooling Method	Convection
Operating	0°C to +55°C
Storage	-45°C to +85°C
Vibration Sine (Operating)	2g / 20-500 Hz acceleration / frequency range
Random	VITA 47-Class V1
Shock (Operating)	20g / 11 ms peak accel. / shock duration half sine
Altitude (Operating)	-1,640 to 60,000 ft
Relative Humidity	90% non-condensing (95% with coating option)

Table 7: Environmental Specifications

1.8 Related Publications

The following publications contain information relating to this product:

PRODUCT	PUBLICATION	
VX3240 Boards	VX3240 Hardware Release Notes VX3240 U-Boot User Manual	CA.DT.B10 (not yet available) SD.DT.xxx (not yet available)
EZ3-VX3240 Systems	EZ3-VX3240-00-L Quick Start EZ3-VX3240 Getting Started -	SD.DT.xxx (not yet available) SD.DT.xxx (not yet available)
Serial ATA	Serial ATA 2.0 Specification	
VITA 46.0	VPX Base Standard - ANSI/VITA 46.0-2007	
VITA 46.4	PCI Express® on VPX Fabric Connector - VITA Draft Standard	
VITA 46.6	Gigabit Ethernet Control Plane on VPX - VITA Draft Standard	
VITA 46.10	Rear Transition Module on VPX - ANSI-VITA 46.10-2009	

Table 8: Related Publications

Chapter 2 - Functional Description

2.1 Processor and System Memory

2.1.1 Processor

The QorIQ™ P2041 SoC includes the following functions and features:

- Four e500mc cores built on Power Architecture technology cache. P2041 also supports 128-Kbyte private backside cache for each of the cores.
  - Three levels of instructions: user, supervisor, and hypervisor
  - Independent boot and reset
  - Secure boot capability
- 1-Mbyte shared CoreNet platform cache (CPC)
  - Hierarchical interconnect fabric
  - CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet end-points
  - Queue manager fabric supporting packet-level queue management and quality of service scheduling
- One 64-bit DDR3/3L SDRAM memory controller with ECC and chip-select interleaving support
- Data path acceleration architecture incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution
  - Queue Management for scheduling, packet sequencing, and congestion management
  - Hardware Buffer Management for buffer allocation and de-allocation
  - Encryption/decryption (SEC 4.2)
  - RegEx Pattern Matching (PME 2.1)
  - RapidIO messaging manager (RMan)
- Ethernet interfaces
  - Five 1 Gbps or four 2.5 Gbps Ethernet controllers. P2041 also supports a 10 Gbps Ethernet (XAUI) Controller
- High speed peripheral interfaces
  - Three PCI Express 2.0 controllers/ports running at up to 5 Gbps
  - Two serial RapidIO controllers/ports version 1.3 with features of 2.1 running at up to 5 Gbps
  - RapidIO message manager (RMan) with Type 5-6 and Type 8-11 support
  - Dual SATA 2.0 interfaces supporting 1.5 and 3.0 Gbps operation
- Additional peripheral interfaces
  - Two USB 2.0 controllers with integrated PHY
  - SD/MMC controller (eSDHC)
  - Enhanced SPI controller
  - Four I2C controllers
  - Dual DUARTs

- Ten SerDes lanes to 5 GHz
- Enhanced local bus controller (eLBC)
- Multicore programmable interrupt controller (PIC)
- Two 4-channel DMA engines

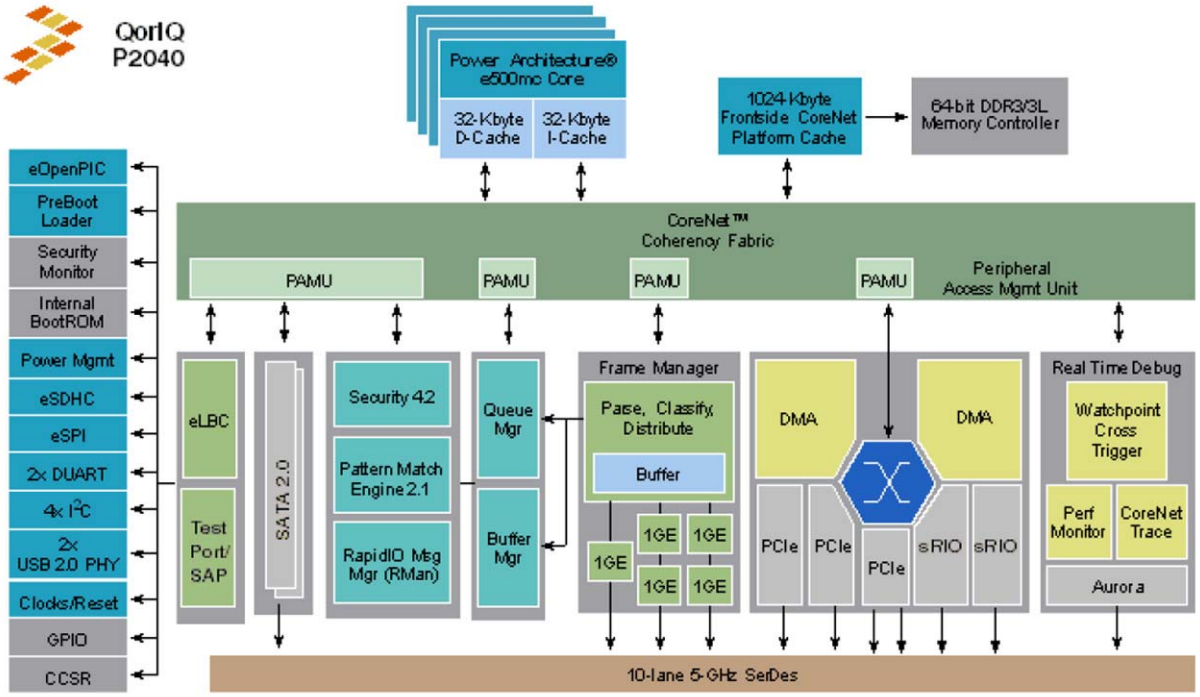


Figure 5: QorIQ™ P2041 Block Diagram

2.1.2 System Memory

The VX3240 supports a single-channel (72-bit), registered Double Data Rate (DDR3) memory with Error Checking and Correcting (ECC).

- The DDR3 interface operates at a rate up to 1066 Gbits/s resulting in a peak bandwidth of 8.5 GB/s.
- The available memory configurations are 2 GB, 4 GB or 8 GB..
- Using ECC, the P2041 detects and corrects all single-bit errors, and detects all double-bit errors and all errors within a nibble.

2.2 PCI Express Bus

The VX3240 provides one x4 PCI Express link directly routed to VPX P1.

The PCI Express bus interface operates up to 5 Gbps on each lane resulting in a peak bandwith of 500 MB/s per lane (500 MB/s on RX way and 500 MB/S on TX way). The resulting bandwidth for the x4 PCI Express link is 2 GB/s (4x 500 MB/s) per way.

The VX3240 does not support PCI Express Non Transparent (NT) mode for PCIe backplane links. The VX3240 should not be used as a Peripheral board.

2.3 Gigabit Ethernet interfaces

The QorIQ™ P2041 integrates two triple-speed Ethernet controllers which are associated on the VX3240 board with two external Marvell 88E1112 Ethernet PHY.

The Ethernet channels 0 and 1 can either be routed to:

- The front panel RJ-45 connectors,
- The VPX P1 connector, thanks to the use of Lan Switch.

2.4 USB Interfaces

The VX3240 provides two USB 2.0 ports.

- One USB port is available on the front panel.
- One USB port is available on VPX P1 connector.

Each port provides a +5V output to power external USB devices such as keyboards.

On the USB 2.0 Rear I/O ports, it is strongly recommended to use a cable below 3 meters in length for USB 2.0 devices.

The USB 2.0 ports are high-speed, full-speed, and low-speed capable. Hi-speed USB 2.0 allows data transfers of up to 480 Mb/s - 40 times faster than a full-speed USB (USB 1.1).

2.5 Serial Interfaces

The VX3240 integrates two serial communications ports, COM1 and COM2 in PC parlance.

COM1 and COM2 are available via the VPX P2 connector.

COM1 is also available via the front panel connector.

- COM1: EIA-232 (simplified RX/TX) port on RJ-12 front panel connector or on the rear P2 connector
- COM2: EIA-232 (simplified RX/TX) port on the rear P2 connector

Default serial mode is EIA-232, 115200 bauds.

2.6 Storage

2.6.1 Flash Memory

The VX3240 provides one 128 MB flash device.

This flash device (NOR flash) is organized in two partitions of 64 MB which operate as redundant boot devices. The selection of the active boot flash partitions is controlled by a DIP switch.

2.6.2 Serial EEPROMs

There are two 256-kbit onboard serial EEPROMS:

- One serial 256 Kbit EEPROM dedicated to system data.
- One serial 256 Kbit EEPROM dedicated to application data.

2.6.3 SPI EEPROM

There are two 64-Mbit onboard SPI Flashes.

2.6.4 F-RAM

A 1-Mbit SPI F-RAM (Ferroelectric Nonvolatile RAM) provides fast, non-volatile storage of mission state data not to be lost when power is removed.

F-RAM combines the nonvolatile data storage capability of ROM with the benefits of RAM, which includes a high number of read and write cycles (100 Trillion), high speed read and write cycles, and low power consumption.

2.6.5 Dual Serial ATA

The QorIQ™ P2041 provides two Serial ATA 2.0 (3 Gbps) interfaces.

- One SATA port is available on VPX P1 connector. Refer to section 3.3.1.2 “VPX Connector Description ”page 28 for more information on P1 wafer assignment.
- One SATA port is available either on optional SATA NAND Flash or optional SATA NAND Flash Mezzanine header

2.7 CPLD Features

The CPLD manages the following features:

- Power-on/off control
- Reset control
- Local environmental control/monitoring
- Local Bus interface to processor
- LEDs control
- Internal registers that allow system management

2.8 I2C Buses

2.8.1 Internal I2C Slaves

The I2C buses controller allows interfacing to a wide number of 2-wire serial standards based on the original I2C concepts. The controller has four multi-master I2C buses (Master and Slave). The master interface is used to drive commands on to the I2C and get responses from other devices. The slave section monitors the I2C and will accept commands that are addressed to it. The slave section can also be put in a monitoring mode, where it will report all activity on the bus but not respond.

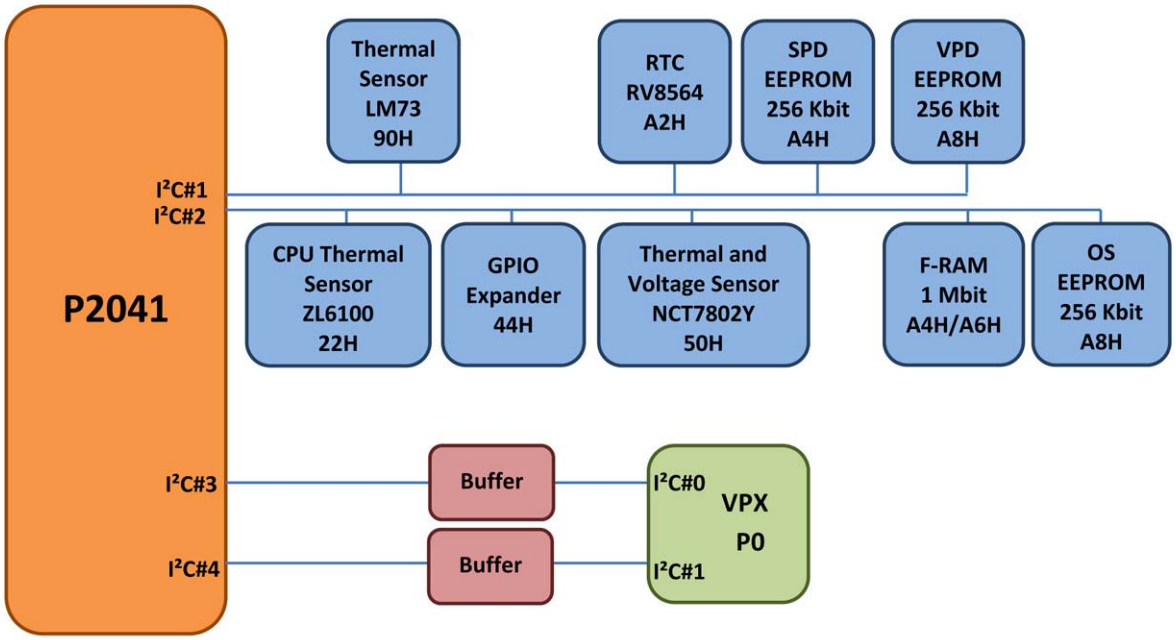


Figure 6: I2C Buses

2.8.2 RTC

The VX3240 RTC is based on the RV-8564-C2 CMOS real-time clock/calendar optimized for low power consumption (-40 °C / +85 °C). This RTC provides a programmable clock output, interrupt output and voltage low detector. An internal timer is also available. All address/data are transferred serially via the I2C bus, at a maximal spped of 400 Kbit/s. The built-in word address register is incremented automatically after each writing or read data byte.

The VX3240 RTC includes a built-in crystal oscillating at 32.768 MHz. Crystal accuracy across temperature: -160 ppm at -40 °C, 0 ppm at 25 °C, -140 ppm at +85 °C.

The RTC is connected to the first I2C controller inside the QorIQ™ P2041 at I2C hardware address A2H.

Nominal operating voltage 3V3. Minimal clock operating voltage 1.2V

A 3V RTC backup battery, BR1225 can be equipped in a keystone socket. This battery supports extended temperature range.

2.8.3 VPD EEPROM

One M24C256 eeprom (256 kb serial eeprom) contains Vital Product Data. This memory is organized as 8192x8 bits.

2.8.4 Thermal Sensors

To ensure optimal and long-term reliability of the VX3240, all onboard components must remain within the maximum temperature specifications. The most critical components on the VX3240 are the processor and the memory. Operating the VX3240 above the maximum operating limits will result in permanent damage to the board.

Three thermal sensors, located on the I2C bus, are available on the VX3240.

> **ZL6100 CPU sensor**: the CPU core temperature is monitored by a Intersil ZL6100ALAF device, at I2C hardware address 22H. This device uses remote sensing on CPU thermal diode and also indicates local board temperature. This sensor temperature is dedicated to junction processor temperature and checks only maximal Tj temperature.

  Key features:

  - Local temperature accuracy: +/- 3 °C
  - Remote temperature accuracy: +/- 0.75 °C
  - Operating temperature: -40°C / +125 °C

> **LM73 board sensor**: the board temperature on Top face is monitored by a LM73 device, at I2C hardware address 90H.

  Key features:

  - Local temperature accuracy: +/- 2 °C (-40 °C to +150 °C)
  - Operating temperature: -40 °C / +150 °C

> **NCT7802Y board sensor**: the board temperature on Bottom face is monitored by a Nuvoton NCT7802Y device, at I2C hardware address 50H.

  Key features:

  - Local temperature accuracy: +/- 2°C (25°C to +70°C)
  - Operating temperature: -40°C / +85°C

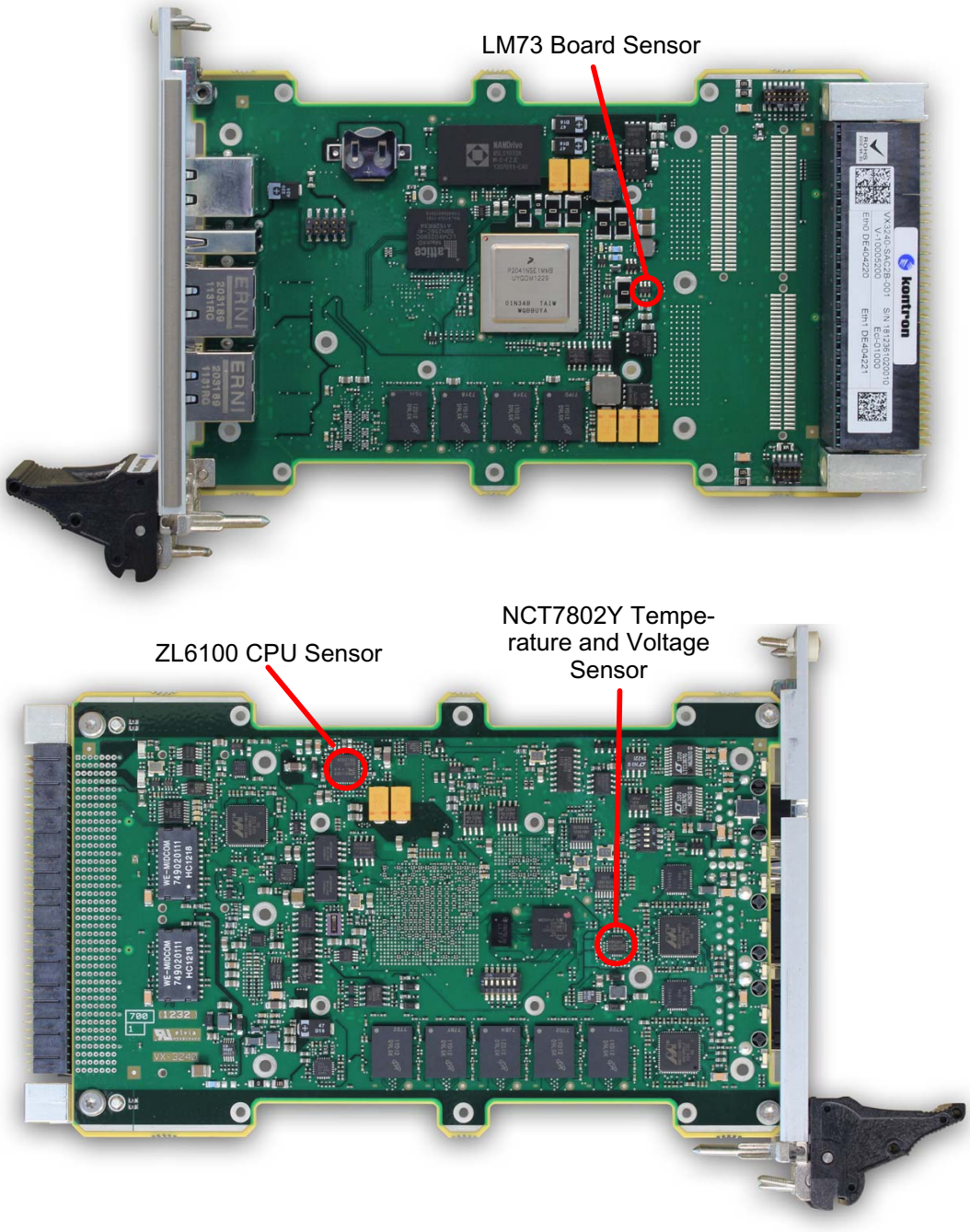


Figure 7: Location of Board and Processor Sensors

2.8.5 Voltage Sensors

The NCT7802Y, at I2C hardware address 50H, is a Nuvoton Hardware Monitor IC, wich can monitor power supply voltages and temperatures.

Key features:

- Voltage monitoring accuracy: +/- 10 mV
- Analog Input VSEN1: DDR Memory 1.5V
- Analog Input VSEN2: VPX VS1 12V
- Analog Input VSEN3: VPX VS3 5V
- Analog Input VCORE: CPU Core 1.05V

2.8.6 VX3240 VPX I2C interfaces

VX3240 implements two I2C buses connected to P0 VPX connector (refer to section 3.3.2 page 29 - P0 pin assignments)

- I2C0: CLK signal on pin P0/B5, DATA signal on pin P0/A5
- I2C1: CLK signal on pin P0/G4, DATA signal on pin P0/F4

2.8.7 GPIO Expander

The VX3240 implements a GPIO Expander NXP PCA9672PW, at I2C hardware address 44H, which drives GPIO1 to GPIO5 connected to P0 and P1 VPX connectors (refer to sections 3.3.2 page 29 and 3.3.3 page 30 – P0 and P1 pin assignments)

The PCA9672PW has a sinking current capability of 25 mA per GPIO. In applications requiring additional drive, two port pins may be connected together to sink up to 50 mA current. Both bits must then always be turned on or off together.

Chapter 3 - Physical I/O

3.1 Front Panel Connectors

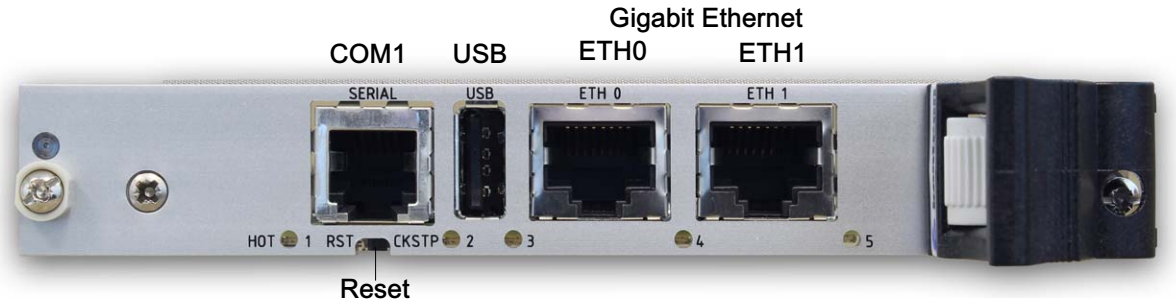


Figure 8: Front Panel Connectors Layout

3.1.1 Serial Connector COM

Pin Assignment

PIN	SIGNAL
1	RTS
2	Shell
3	TXD
4	RXD
5	GND
6	CTS

Table 9: Serial Connector Pin Assignment

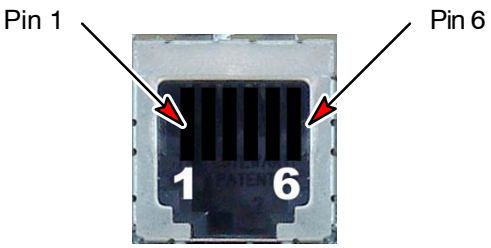


Figure 9: Serial Connector

MNEMONIC	DESCRIPTION
CTS	EIA-232 Clear-To-Send
RTS	EIA-232 Ready-To-Send
RXD	EIA-232Receive Data
TXD	EIA-232 Transmit Data
GND	Ground
Shell	Chassis Ground

Table 10: Serial Connector Signal Description

Serial Cable Designation

Serial cable is:

- RJ-14 (6 pin, 4 conductor) for a simple EIA-232 without handshake support.
- RJ-12 (6 pin, 6 conductor) for EIA-232 with handshaking.

A RJ-12 to DB9/DB25 male or DB9/DB25 female adapter is available from multiple sources, such as:
- Kontron Order Code KIT-RJ12DB9
- Triangle Cable http://www.trianglecables.com/db9m-rj12.html

Pin Connector DB9	Signal	Pin Connector RJ-12
1	RTS	1
2	TXD	3
3	RXD	4
4	CTS	6
5	GND	5

3.1.2 USB Connector

Pin Assignment

PIN	SIGNAL	FUNCTION	I/O
1	VCC (1)	VCC	--
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

Table 11: USB Connector Pin Assignment

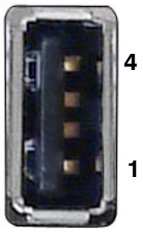


Figure 10: USB Connector

(1) +5V protected power up to 1A continuous, short circuit current limited (1A max.) with thermal shutdown, and automatic restart when short is removed.

3.1.3 Gigabit Ethernet Connectors

Pin Assignment

PIN	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-	-	I/O	BI_DC+
5	-	-	-	-	I/O	BI_DC-
6	I	TX-	I	RX-	I/O	BI_DB-
7	-	-	-	-	I/O	BI_DD+
8	-	-	-	-	I/O	BI_DD-
Shell	Chassis Ground					

Table 12: Gigabit Ethernet Connectors ETH0 and ETH1 Pin Assignment

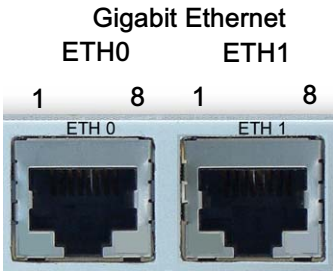


Figure 11: Dual Gigabit Ethernet Connector

The Ethernet transmission can operate effectively using a CAT5 cable with a maximum length of 100 m.

The Ethernet connectors are available as RJ-45 connectors with tab down. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

3.2 Front Panel Leds

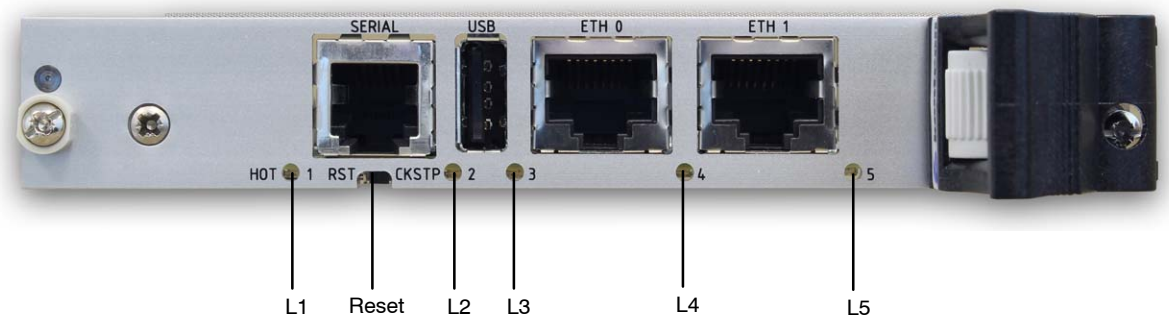


Figure 12: Front Panel LEDs

Status LEDs Default Settings

CPU LED	COLOR	DESCRIPTION
L1	RED	Thermal Alert
	GREEN	Card power OK, not in reset state
L2	RED	CPU Checkstop
	GREEN	Local Bus Activity
L3	RED	Reserved for future use
	GREEN	Reserved for future use
L4	RED	ETH0 - On: Link 10. Blink: Activity
	GREEN	ETH0 - On: Link 1000. Blink: Activity
	RED + GREEN	ETH0 - On: Link 100. Blink: Activity
L5	RED	ETH1 - On: Link 10. Blink: Activity
	GREEN	ETH1 - On: Link 1000. Blink: Activity
	RED + GREEN	ETH1 - On: Link 100. Blink: Activity

3.3 Onboard Connectors

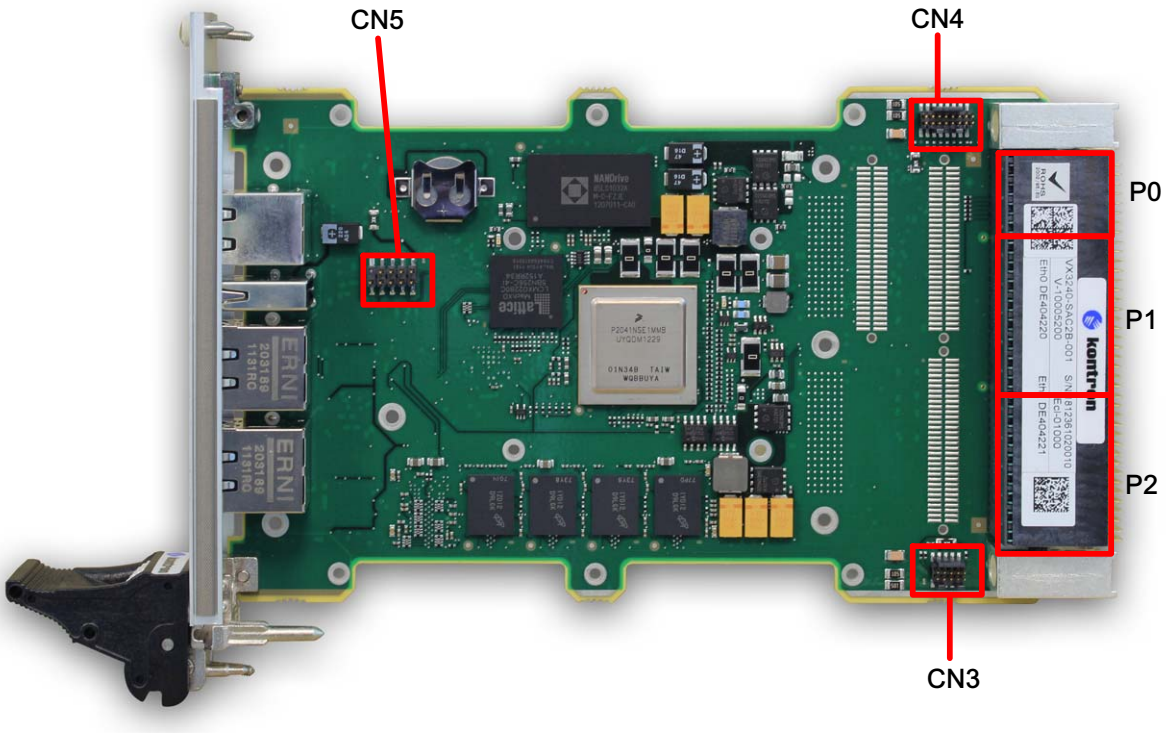


Figure 13: VX3240 Connectors Layout (top)

3.3.1 VPX Bus Interface

The complete VPX connector configuration comprises three connectors named P0, P1 and P2

- P0: one 8-wafer 7-row connector
- P1: one 16-wafer 7-row connector
- P2: one 16-wafer 7-row connector

The VX3240 is not hot-swappable but supports the addition or removal of other boards whilst in a powered-up state.

The VX3240 is designed for a VPX bus architecture.

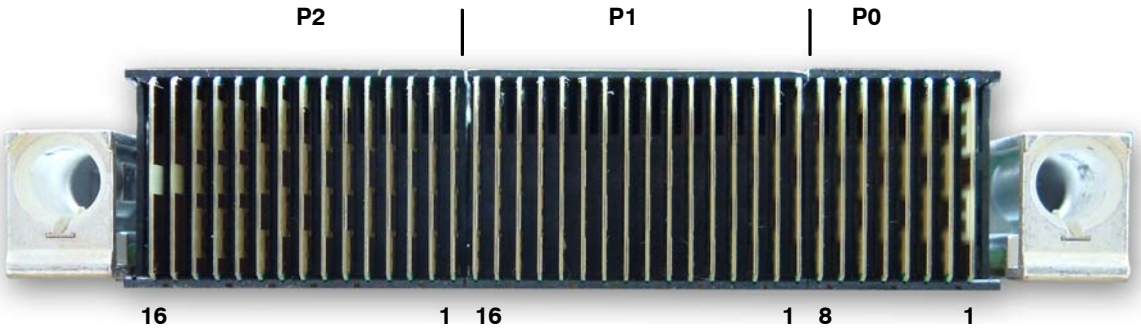


Figure 14: VPX Connectors

3.3.1.1 Board Connectors Identification

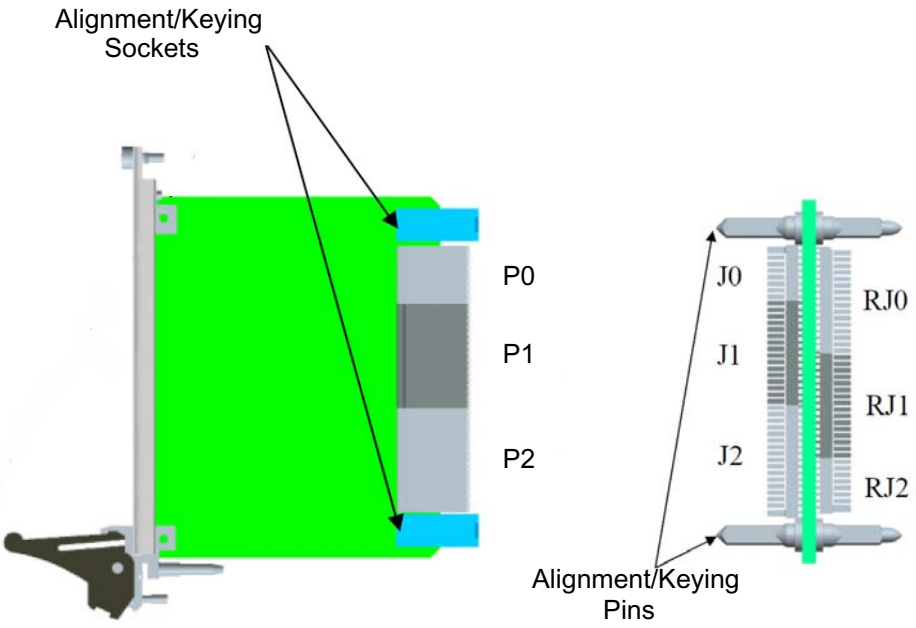


Figure 15: Connector Identification for 3U VPX Board

3.3.1.2 VPX Connectors Description

The VX3240 is provided with three VPX bus connectors, P0, P1 and P2

The VX3240 board provides Rear I/O connectivity for special compact systems.

When the Rear I/O module is used, the signals may be routed to the Rear I/O module interface. Thus the Rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

The VX3240 Rear I/O provides the following interfaces:

- Three GPIOs P0
- One USB 2.0 ports P1
- Two Gigabit Ethernet ports without LED signals P1
- One SATA ports P1
- Two GPIOs P1
- x4 or x1 PCI-Express P1
- Two EIA-232 COM ports P2

3.3.2 P0 Connector

P0 Wafer Assignment

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	VS1	VS1	VS1	N.C.	NC (VS2)	NC (VS2)	NC (VS2)
2	VS1	VS1	VS1	N.C.	NC (VS2)	NC (VS2)	NC (VS2)
3	VS3	VS3	VS3	N.C.	VS3	VS3	VS3
4	I2C1_CLK	I2C1_DAT	GND	NC (-12V_AUX)	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	I2C0_CLK	I2C0_DAT
6	GA3*	GA2*	GND	NC (+12V_AUX)	GND	GA1*	GA0*
7	GPIO5 (TCK)	GND	Reserved	Reserved	GND	GPIO3 (TMS)	GPIO4 (TRST*)
8	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
CASE	GND						

* signal active when low

Table 13: VPX Connector P0 Wafer Assignment

P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
3V3_AUX	+3.3 Volts auxiliary power
GA0* to GA4*	Geographical Address Inputs 0-4
GAP	Geographical Address Parity
GND	Ground
GPIOx	General purpose I/O
I2C0	I2C Bus 0
I2C1	I2C Bus 1
N.C.	Not Connected
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
SYSRESET*	System Reset. Input and open collector output.
VS1	+12 Volts DC power (VS1 VPX supply)
VS3	+5 Volts DC power (VS3 VPX supply)

Table 14: VPX Connector P0 Signal Definition

3.3.3 P1 Connector

P1 Wafer Assignment

➢ Legend for Table 15:

P1_VBAT	Battery Voltage	USB	USB
P1_SYS_CON*	System Controller	SATA	Serial ATA Port
PCIe L0-RX | L0-TX	x4 PCI-Express	ETHx	Gigabit Ethernet Port

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	Reserved	GND	PCIe L0-TX-	PCIe L0-TX+	GND	PCIe L0-RX-	PCIe L0-RX+
2	GND	PCIe L1-TX-	PCIe L1-TX+	GND	PCIe L1-RX-	PCIe L1-RX+	GND
3	VBAT	GND	PCIe L2-TX-	PCIe L2-TX+	GND	PCIe L2-RX-	PCIe L2-RX+
4	GND	PCIe L3-TX-	PCIe L3-TX+	GND	PCIe L3-RX-	PCIe L3-RX+	GND
5	SYS_CON*	GND	Reserved	Reserved	GND	Reserved	Reserved
6	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
7	Reserved	GND	Reserved	Reserved	GND	Reserved	Reserved
8	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
9	USB PWR	GND	SATA TX-	SATA TX+	GND	SATA RX-	SATA RX+
10	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
11	Reserved	GND	Reserved	Reserved	GND	Reserved	Reserved
12	GND	USB D-	USB D+	GND	Reserved	Reserved	GND
13	GPIO1	GND	ETH1 DB-	ETH1 DB+	GND	ETH1 DA-	ETH1 DA+
14	GND	ETH1 DD-	ETH1 DD+	GND	ETH1 DC-	ETH1 DC+	GND
15	GPIO2	GND	ETH0 DB-	ETH0 DB+	GND	ETH0 DA-	ETH0 DA+
16	GND	ETH0 DD-	ETH0 DD+	GND	ETH0 DC-	ETH0 DC+	GND
CASE	GND						

* signal active when low

Table 15: VPX Connector P1 Wafer Assignment

P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
ETH*x* DA+/-	10/100/1000BASE-TX Ethernet *x:* First pair of Transmit/Receive data.
ETH*x* DB+/-	10/100/1000BASE-TX Ethernet *x:* Second pair of Transmit/Receive data.
ETH*x* DC+/-	10/100/1000BASE-TX Ethernet *x:* Third pair of Transmit/Receive data.
ETH*x* DD+/-	10/100/1000BASE-TX Ethernet *x:* Fourth pair of Transmit/Receive data.
GND	Ground
GPIO*x*	General Purpose I/O *x*
PCIe L*x*-RX+/-	x4 PCI Express Link - Receive +/- Lane *x*
PCIe L*x*-TX+/-	x4 PCI Express Link - Transmit +/- Lane *x*
Reserved	Reserved
SATA RX+/-	Serial ATA Receive +/-
SATA TX+/-	Serial ATA Transmit +/-
SYS_CON*	System Controller Slot Indication
USB D+/-	Differential Data Pair of USB link
USB PWR	USB Power
VBAT	Battery Voltage Input, 3V. Optional alternated source for RTC backup voltage

Table 16: VPX Connector P1 Signal Definition

USB Interfaces

There are up to two independent USB interfaces available as described below:

USB PORT	CONNECTOR	USAGE
USB0	USB on the VX3240 (front panel)	External USB devices
USB1	USB on the VX3240-RTM (front panel)	External USB devices

Table 17: USB Port Features

All USB ports may be used at the same time. It is strongly recommended to use cables less than 3 meters in length for the Rear I/O interfaces.

> Ethernet Interfaces

Gigabit Ethernet signals are available on the Rear I/O interface (ETH0 and ETH1 in above Table).

Ethernet PORT	CONNECTOR
ETH0	ETH0 on the VX3240 (front panel) or CN12-R on the VX3240-RTM (front panel)
ETH1	ETH1 on the VX3240 (front panel) or CN13-R on the VX3240-RTM

Table 18: Ethernet Port Features

> SATA Interface

The VX3240 provides two SATA interfaces (SATA0 and SATA1 in above Table).

SATA0 can be used only on the Rear I/O interface, SATA1 is used for the onboard SATA NAND Flash module or mezzanine. All SATA ports can be used simultaneously.

SATA PORT	CONNECTOR	USAGE
SATA0	CN14-R on the VX3240-RTM	External SATA HDD drives, e.g. 2.5" or 3.5" SATA HDDs
SATA1	CN5 on the VX3240 (optional)	SATA Nand Flash Module

Table 19: SATA Port Features

3.3.4 P2 Connector

P2 Wafer Assignment

> Legend for Table 20:

COM*x* COM port

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	COM1 RTS	GND	Reserved	Reserved	GND	Reserved	Reserved
2	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
3	COM1 TXD	GND	Reserved	Reserved	GND	Reserved	Reserved
4	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
5	COM1 CTS	GND	Reserved	Reserved	GND	Reserved	Reserved
6	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
7	COM1 RXD	GND	Reserved	Reserved	GND	Reserved	Reserved
8	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
9	COM2 RTS	GND	Reserved	Reserved	GND	Reserved	Reserved
10	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
11	COM2 TXD	GND	Reserved	Reserved	GND	Reserved	Reserved
12	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
13	COM2 CTS	GND	Reserved	Reserved	GND	Reserved	Reserved
14	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
15	COM2 RXD	GND	Reserved	Reserved	GND	Reserved	Reserved
16	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
CASE	GND						

Table 20: VPX Connector P2 Wafer Assignment

P2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
COM*x* CTS	Channel EIA-232 *x* Clear To Send
COM*x* RTS	Channel EIA-232 *x* Ready To Send
COM*x* RXD	Channel EIA-232 *x* Receive Data
COM*x* TXD	Channel EIA-232 *x* Transmit Data
GND	Ground

Table 21: VPX Connector P2 Signal Definition

3.3.5 COP Header Connector

COP Header Signal Definition

The COP connector (Common On-chip Processor) can be utilized by external toolsets or testers to perform board-level validation, test and debug applications.

Pin	Mnemonic	Signal Definition
1	TDO	Test Data Out
2	N.C.	Not Connected
3	TDI	Test Data In
4	TRST*	Test Reset
5	N.C.	Not Connected
6	VCC	+3.3 Volts DC Probe Sense
7	TCK	Test Clock
8	CHKSTP_IN*	CPU Checkstop In
9	TMS	Test Mode Select
10	N.C.	Not Connected
11	SRESET*	COP Software Reset
12	N.C.	Not Connected
13	HRESET*	COP Hardware Reset
14	Key Pin	Not Connected
15	CHKSTP_OUT*	CPU Checkstop Out
16	GND	Ground

* Signals active when low.

Table 22: COP Header Pin Assignment

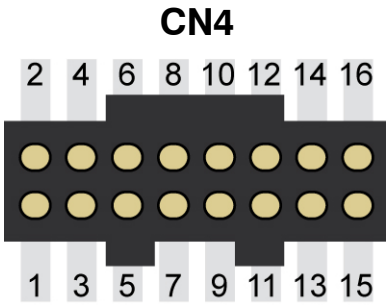


Figure 16: COP Header

3.3.6 JTAG Connector

JTAG Signal Definition

The CPLD is programmed via the JTAG (CN3) connector. The CPLD is the only device on the JTAG chain.

Pin	Mnemonic	Signal Definition
1	TCK	Test Clock
2	GND	Ground
3	TDO	Test Data Out
4	VCC	+3.3 Volts DC Probe Sense
5	TMS	Test Mode Select
6	N.C.	Not Connected
7	N.C.	Not Connected
8	N.C.	Not Connected
9	TDI	Test Data In
10	GND	Ground

Table 23: JTAG Connector Pin Assignment

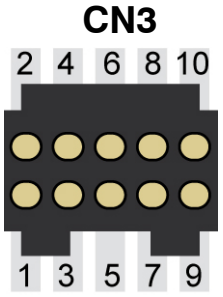


Figure 17: JTAG Connector

3.3.7 NAND Flash Connector

NAND Flash Signal Definition

Pin	Mnemonic	Signal Definition
1	PWR	+5 Volts DC Mezzanine Power Supply
2	SATA RX+	Serial ATA. Receive plus.
3	N.C.	Not Connected
4	SATA RX-	Serial ATA. Receive minus.
5	N.C.	Not Connected
6	GND	Ground
7	GND	Ground
8	SATA TX+	Serial ATA. Transmit plus.
9	N.C.	Not Connected
10	SATA TX-	Serial ATA. Transmit minus

Table 24: NAND Flash Connector Pin Assignment

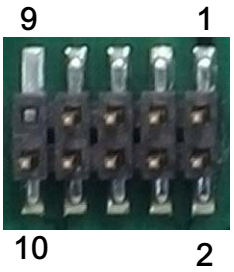


Figure 18: NAND Flash Connector

Chapter 4 - Installation

The VX3240 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

4.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VX3240. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.
In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

This board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

4.2 Board Identification

The VX3240 is identified by a label fitted on the top side of the board.

A Identification label: Order Code, Serial Number, Variant, E.C. level, Ethernet MAC addresses.

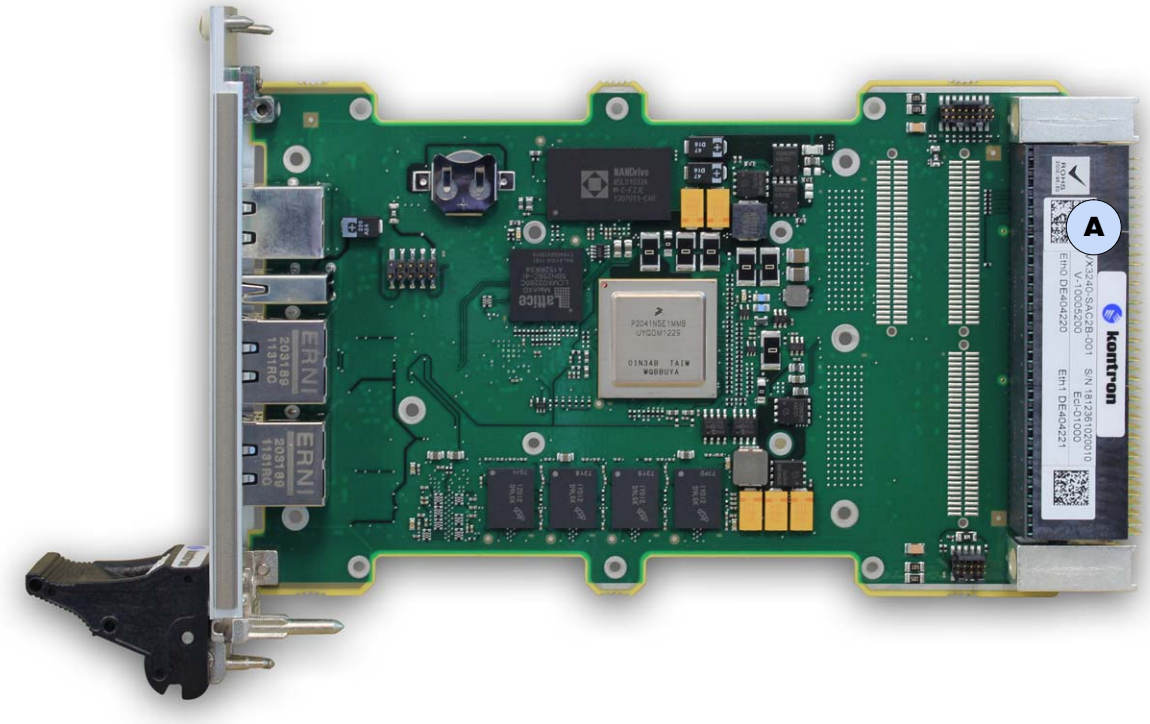


Figure 19: VX3240 Identification (Top Side)

4.3 Board Configuration - Microswitches

Two microswitches are available on the VX3240: SW1 and SW2.

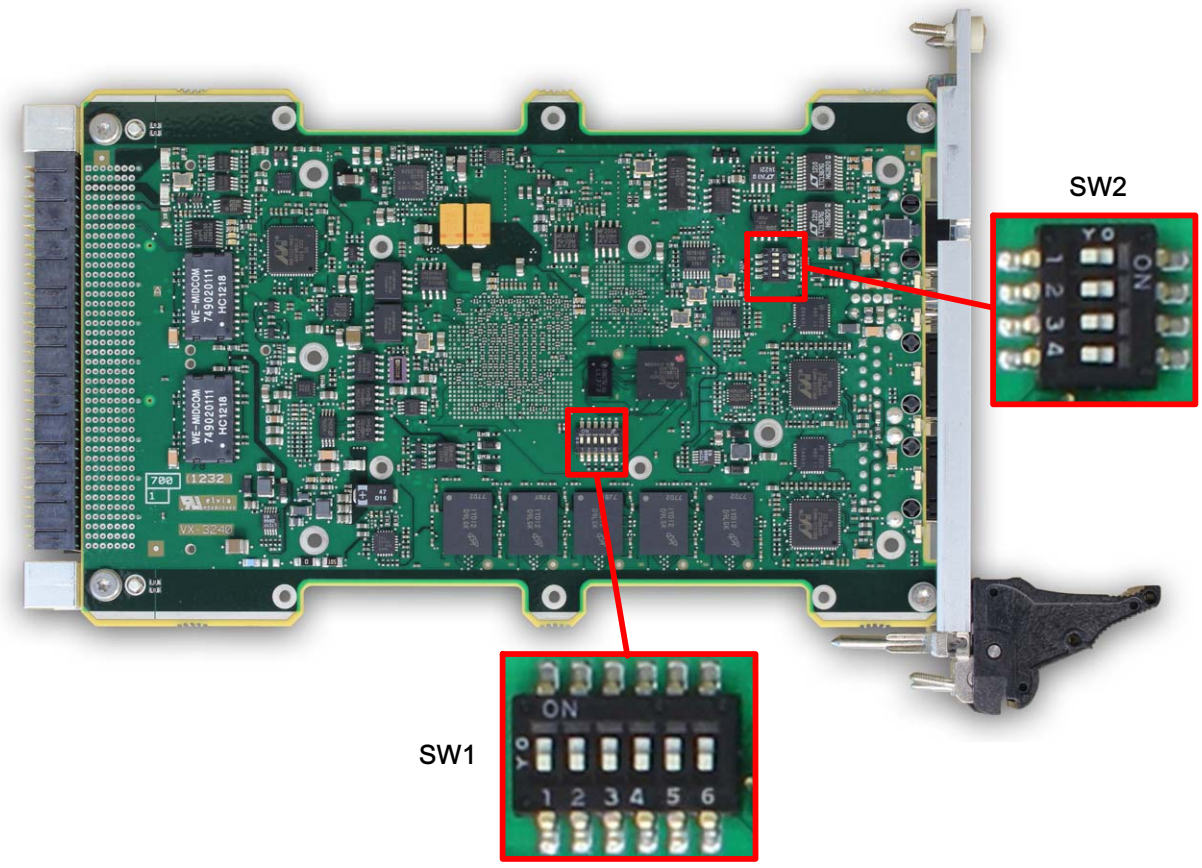


Figure 20: Board Configuration

4.3.1 DIP Switch SW1 Description

SW1	Function	Description
1	Reserved	Reserved
2	Reserved	Reserved
3	ETH1 Lan Switch	ON Ethernet Port 1 on rear panel OFF Ethernet Port 1 on front panel
4	ETH0 Lan Switch	ON Ethernet Port 0 on rear panel OFF Ethernet Port 0 on front panel
5	Reserved	Reserved
6	Rescue Boot Flash	ON CPU boots the firmware from its rescue flash. OFF Normal operation. CPU boots the firmware from its non rescue flash.

Table 25: SW1 Mircroswitch Description

4.3.2 DIP Switch SW2 Description

SW2	Function	Description
1	Reserved	Reserved
2	Reserved	Reserved
3	Reserved	Reserved
4	SPD Debug Mode	ON DDR3 SPD debug mode OFF Normal operation

Table 26: SW2 Mircroswitch Description

4.4 Package Content

The VX3240 is packaged with several components. The packing contents of the VX3240 Series may vary depending on customer requests.

- **CPU Module**
  - Order Code: refer to section 1.3.2 “Order Code Table” page 5
    - Processor specifications differ depending on Order Code
    - Heat sink assembled on the board
- **Rear Transition Module**
  - Order Code: refer to section 1.3.2 “Order Code Table” page 5
- **SATA Flash Disk Module**
  - Order Code: refer to section 1.3.2 “Order Code Table” page 5
- **CD-ROM Technical Documentation**

4.5 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX3240 in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of the VX3240 in a system proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed.

   
   Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX3240 refer to Chapter 4. For the installation of VX3240 specific peripheral devices and Rear I/O devices refer to the appropriate chapters in Chapter 3.

   
   Care must be taken when applying the procedures below to ensure that neither the VX3240 nor other system boards are physically damaged by the application of these procedures.

3. To install the VX3240 perform the following:

   1. Ensure that no power is applied to the system before proceeding.

      
      When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
   3. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
   4. Fasten the front panel retaining screws.
   5. Connect all external interfacing cables to the board as required.
   6. Ensure that the board and all required interfacing cables are properly secured.

The VX3240 is now ready for operation. For operation of the VX3240, refer to appropriate VX3240 specific software, application, and system documentation.

4.6 Standard Removal Procedure

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

   
   Care must be taken when applying the procedures below to ensure that neither the VX3240 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

   
   Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

4.7 Installation of Peripheral Devices

The VX3240 is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following sections provide information regarding installation and do not give detailed procedures.

4.7.1 SATA Nand Flash Mezzanine Installation

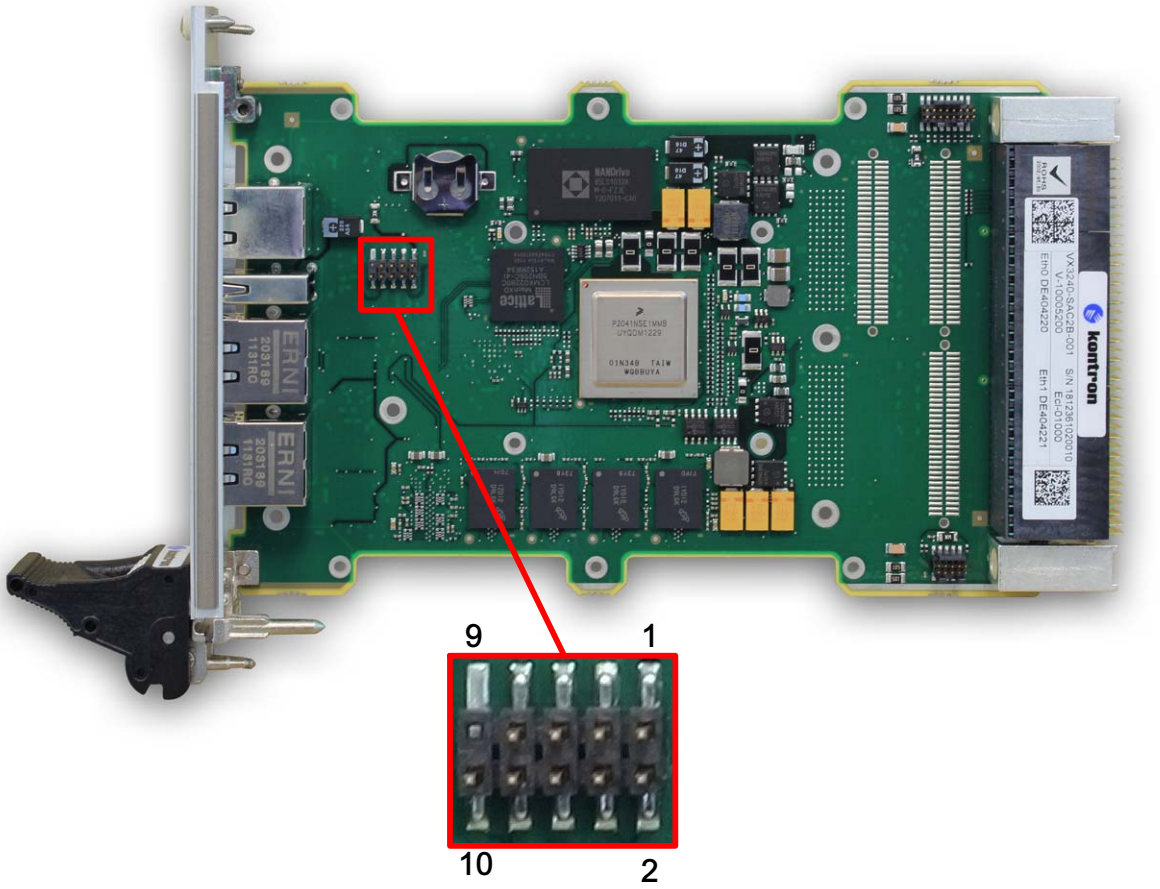


Figure 21: SATA Mezzanine Slot Location

The NAND Flash module is fixed to the board, by using on one side the connector, and on the other side, a nylon screw mounted on the VX3240 heatsink.

Make sure to use a nylon screw when installing the NAND Flash module, not to damage the VX3240 heatsink. Kontron Order Code: VIS-CLS-M3X6-NYLON. Radiospare Reference: 527-971.

Main Characteristics:

- Cheese head screw
- M3x6mm
- Nylon
- Operating range: -40°C - +158°C

Mounting of Flash Memory Modules (ref FDM-SATA-xxxx) :

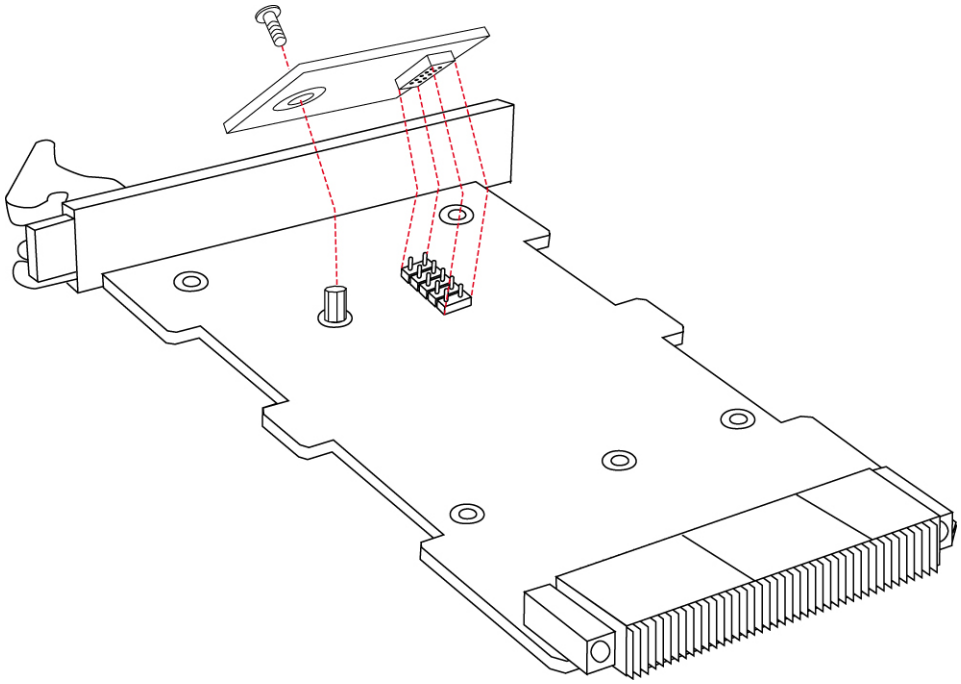


Figure 22: Flash Memory Module Installation

Order Code of the SATA NAND drive flash disk:

FDM-SATA-xGB-C0V

(x= up to 32 GB)

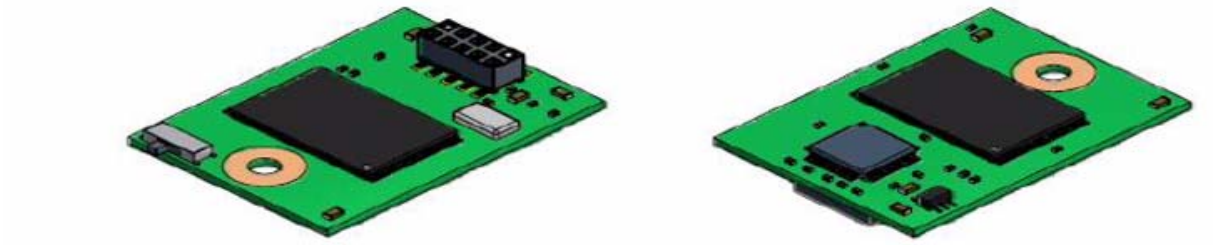


Figure 23: NAND Flash Disk Overview

4.7.2 Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. The battery is used to run a time of day clock during the absence of power. Operation without the battery is possible but the date and time will not be retained in the absence of power. Alternatively, the VPX VBAT signal on P0 can provide a 3.3V voltage from the backplane to retain the date and time.

Make sure not to remove the battery support, this could damage the heatsink.

To replace the battery, proceed as follows:

- Turn off power.
- Use a thin plastic tool to push the battery outside the safety cache. Push from the right or left top side of the safety cache.
- Remove the battery.
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

Care must be taken to ensure that the battery is correctly replaced.
The battery should be replaced only with an identical or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Reference of the battery used on the VX3240: RAYOVAC BR1225A
The design of an electronic circuit powered by a component class battery requires the designer to consider two interacting paths that determine a battery's life: consumption of active electrochemical components and thermal wear-out.

Battery Life

Figure 24 gives an estimate of years of service at various discharge currents for BR Lithium coin cells at room temperatures. The RTC circuit power consumption is specified at 500 nA, giving an expected duration of more than 10 years in the absence of external power.

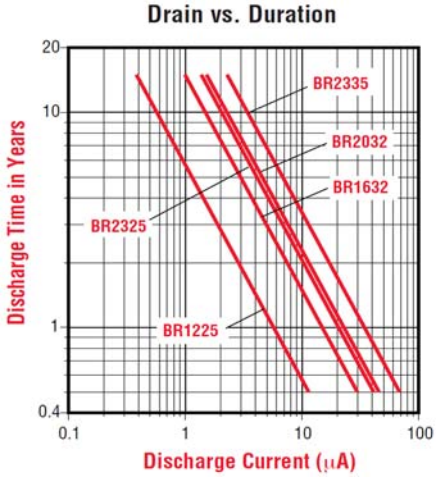


Figure 24: Battery Life

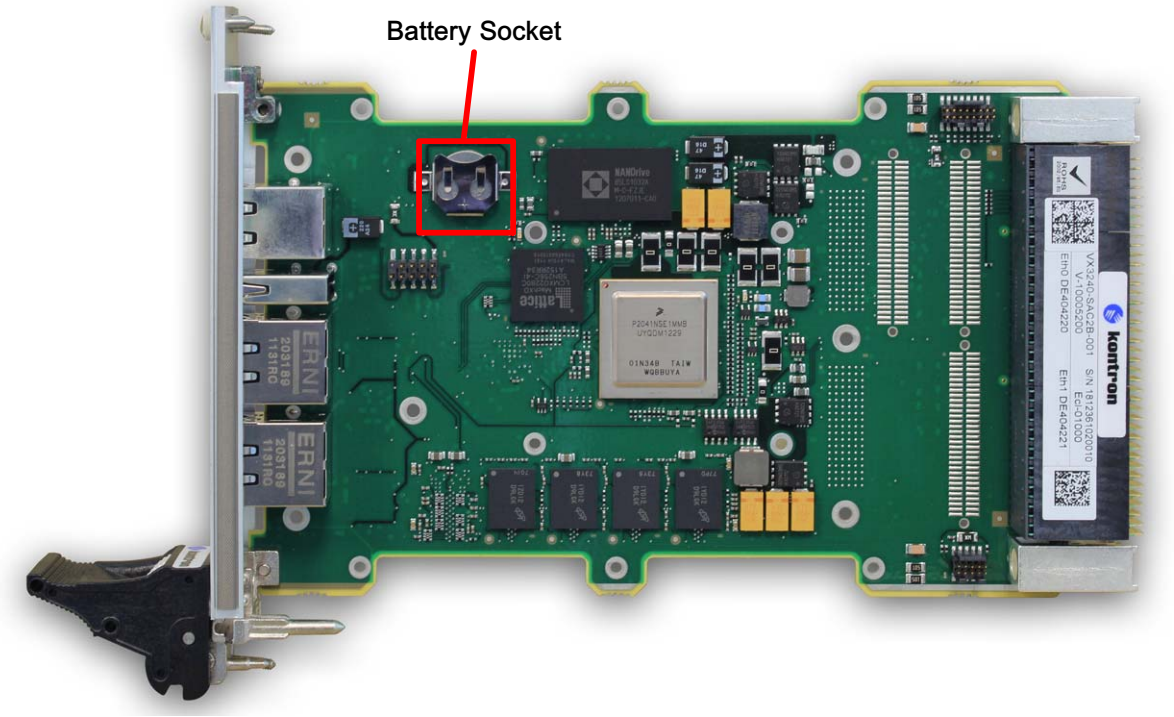


Figure 25: Battery Socket

4.8 Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The OS installation procedure is not addressed in this manual. Refer to appropriate OS software documentation for installation.

Chapter 5 - Power Considerations

5.1 System Power

The considerations presented in the ensuing chapters must be taken into account by system integrators when specifying the VX3240 system environment.

5.1.1 VX3240

The VX3240 has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The following table specifies the ranges for the different input power voltages within which the board is functional. The VX3240 is not guaranteed to function if the board is not operated within the prescribed limits.

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE
+3.3V	3.2V min. to 3.47V max.
+5V	4.85V min. to 5.25V max.
+12V	11.4V min. to 12.6V max.

Table 27: DC Operational Input Voltage Ranges

5.1.2 Backplane

Backplanes to be used with the VX3240 must be adequately specified. The backplane must provide optimal power distribution for the +3.3 V, +5 V and +12 V power inputs. It is recommended to use only backplanes which have at least two power planes for the +3.3 V and +5 V voltages.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided.

5.1.3 Power Supply Units

Power supplies for the VX3240 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the VX3240 has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

Non-industrial ATX PSUs may require a greater minimum load than a single VX3240 is capable of creating. When a PSU of this type is used, it will not power up correctly and the VX3240 may hangup. The solution is to use an industrial PSU or to add more load to the system.

The start-up behavior of VPX power supplies is critical for all new CPU boards. These boards require a defined power of sequence and start-up behavior of the power supply.

For information on the required behavior refer to the power supply specifications on the http://www.formfactors.org web site and to the VPX specification on the VITA web site (http://www.vita.com)

5.1.3.1 Start-Up Requirement

Power supplies must comply with the following guidelines, in order to be used with the VX3240.

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.
- Maximal power supplies needed during a system start-up:
  - +12 VDC: 3A max. during 1 millisecond.
  - + 5 VDC: 4.5A max. during 500 microseconds.

5.1.3.2 Power-Up Sequence

The time from +12 VDC until the output reaches its minimum in regulation level and from +5 VDC until the output reaches its minimum in regulation level must be < 20 ms.

5.1.3.3 Tolerance

The tolerance of the voltage lines is described in the VITA specification (VITA 46.0).The recommended measurement point for the voltage is the VPX connector on the CPU board.

The following table provides information regarding the required characteristics for each board input voltage.

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (P-P)
5V	+5.0 VDC	+5%/-2.5%	50 mV
3.3V	+3.3 VDC	+4.5%/-1.5%	50 mV
+12V	+12 VDC	+5%/-5%	50 mV
-12V	-12 VDC	+5%/-5%	50 mV
GND	Ground, not directly connected to potential earth (PE)		

Table 28: Input Voltage Characteristics

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

5.1.3.4 Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it goes under a certain level, the circuits may enter a latch-up state where even a hard RESET will have no effect. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.1.3.5 Rise Time Diagram

The following figure illustrates an example of the recommended start-up ramp of a VPX power supply for all Kontron boards delivered up to now.

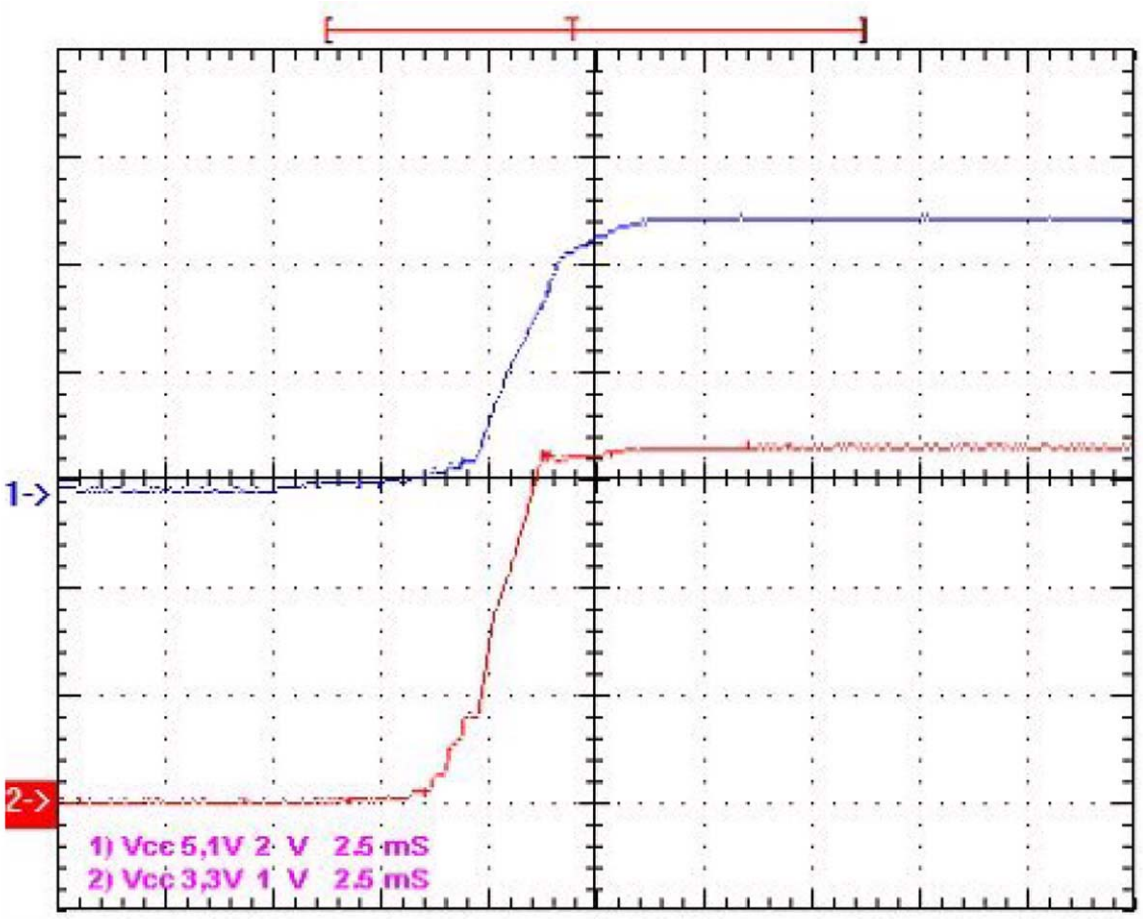


Figure 26: Start-Up Ramp of the CP3-SVE180 AC Power Supply

5.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the VX3240 and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption tables below list the voltage and power specifications for the VX3240 board. The values were measured using an 5-slot passive VPX backplane.

All measurements were conducted at a temperature of 25°C. The measured values varied, because the power consumption was dependent on processor activity.

5.2.1 VX3240 Thermal Power

The following data show total board consumption. These data help for thermal power analysis.

All power values in this table are measured in operational conditions.

VX3240 Thermal Power: Board Power based on Current Measurements

Board	Power Mode	Max. Total Power Consumption	Current Drawn	Test Condition
VX3240 VX3240-SAC2-00000 QorIQ™ P2041 1.2 GHz 2 GB DDR3 No SATA Flash No PMC/XMC 2x 1000BASE-T Ethernet	Linux 100% Proc. Load Measured at + 25°C	23W	1,3A (VS1) 1,4A (VS3)	Four memory test bench (100% Proc. load) Ethernet front panel linked up (no data transfer)
	Linux IDLE Mode Measured at + 25°C	16W	1A (VS1) 0,8A (VS3)	Interfaces not used
	Firmware Measured at + 25°C	19W	1,2 (VS1) 0,8A (VS3)	Interfaces not used
	Reset State (Measured at +25°C)	5W	0,07A (VS1) 0,8A (VS3)	Interfaces not used
	Standby mode	0.4W	100 mA (3V3_AUX)	If 3V3_AUX is present and main VS1 (+12V) and VS3 (+5V) power supplies not present. Board is in stand-by mode
Additional USB power consumption on 5V USB devices dependant (500mA max./port)		+5W	1A (VS3)	Note: this thermal power is not dissipated on board
Additional power consumption for optional SATA Nand Flash (on board or mezzanine)		+1.5W	300 mA (VS3)	Value for 32GB Nand Flash Note: this thermal power is dissipated on board or on daughter card

Table 29: Thermal Power

5.2.2 VX3240 Maximum Current

The following data provide maximum current values on VPX VS1 (+12V) and VS3 (+5V) power supplies. These maximum includes VS1/VS3 +5% tolerance and 5% margin to guarantee worst case part behavior.

VX3240 Maximum Current: based on maximum Current Measurements				
Board	**Current Draw**	**VS1 (+12V) Max. Current**	**VS3 (+5V) Max. Current**	**Test Condition**
VX3240 VX3240-SAC2-00000 QorIQ™ P2041 1.2 GHz 2 GB DDR3 32 GB SATA Flash No PMC/XMC 2x 1000BASE-T Ethernet	Maximum Current	1,3A	1,6A	Four memory test bench (100% Proc. load) Ethernet front panel linked up (no data transfer)
	Peak Current	3A	4,5A	Power Supplies Start-Up

Table 30: Maximum Current

Chapter 6 - VX3240-RTM Characteristics

6.1 Overview

The VX3240 provides optional Rear I/O connectivity for peripherals, a feature which may be particularly useful in specialized VPX systems. Some standard PC interfaces are implemented and assigned to the front panel and to the Rear I/O connector J2 on the VX3240.

When the VX3240-RTM is used, the signals of some of the main board/front panel connectors may be routed to the module interface. Thus, the VX3240 Rear Transition Module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

The VX3240-RTM provides the following functions:

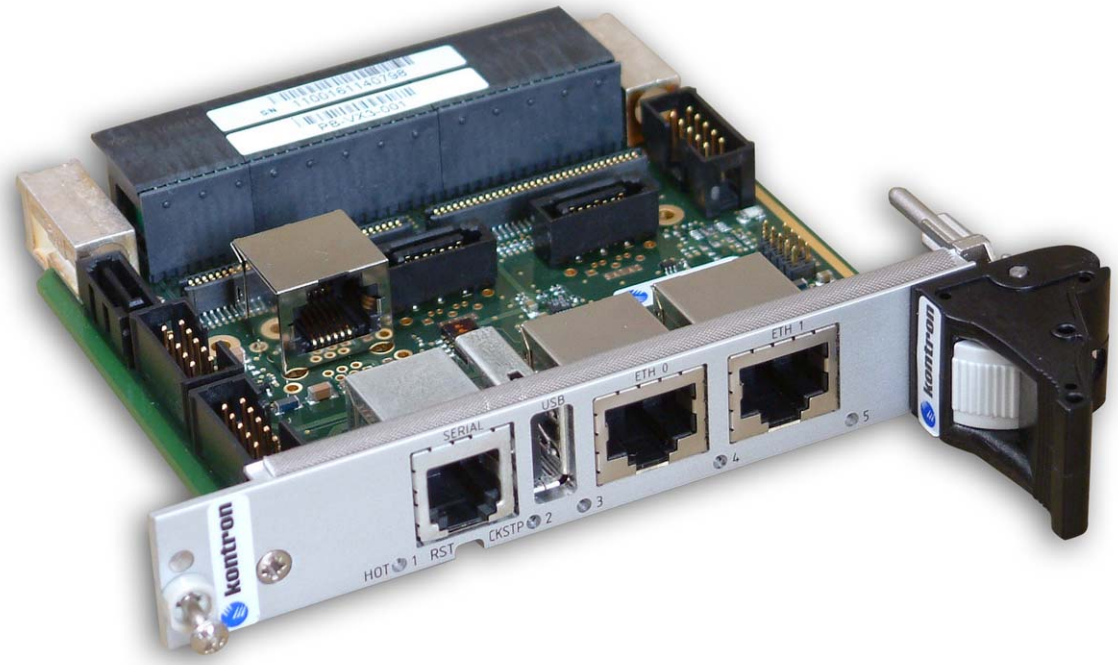
- VPX Rear I/O
- One USB 2.0 ports
- Two Gigabit Ethernet ports without LED signals
- Two COM (Serial) ports
- One SATA port
- Two GPIOs
- One Reset Button
- One System Management Bus connector
- One JTAG connector

Available order codes are listed in table below:

Article	Order Code	Description
VX3240-RTM	PB-VX3-001	VX3240 VPX Rear Transition Module, no PIM connector, 10/100/1000BASE-TX Ethernet interfaces

Table 31: Order Code

Ethernet interfaces manufacturing option: it is strongly recommended to use compatible RTM and SBC → ie same Ethernet manufacturing option.



VX3240-RTM-PB-VX3-001 (non PIM connector)

Figure 27: VX3240-RTM Overview

6.2 Technical Specifications

VX3240-RTM		SPECIFICATIONS
Front Panel Interfaces	USB	One USB 2.0 interface: 4-pin connector
	Ethernet	Up to two Gigabit Ethernet interfaces implemented as dual RJ-45 connector without LEDs
	COM	One serial port (COM1), RS-232 simplified, RJ-12 connector
	Reset	One Push Button
Onboard Interfaces	SATA	One SATA interface
	VPX	VPX connector for connecting Rear I/O to the backplane
	COM	One serial port (COM2) implemented as a RJ-12 onboard connector, RS-232 simplified
	GPIOs	Two General Purpose I/Os
	JTAG	
	I2C	
General	Temperature Range	Operational: 0°C to +55°C Storage: -55°C to +85°C
	Climatic Humidity	99% non-condensing
	Dimensions	Dimensions: 99.85 mm x 82.54 mm
	Board Weight	120g

Table 32: VX3240-RTM Main Specifications

6.3 RTM Configuration

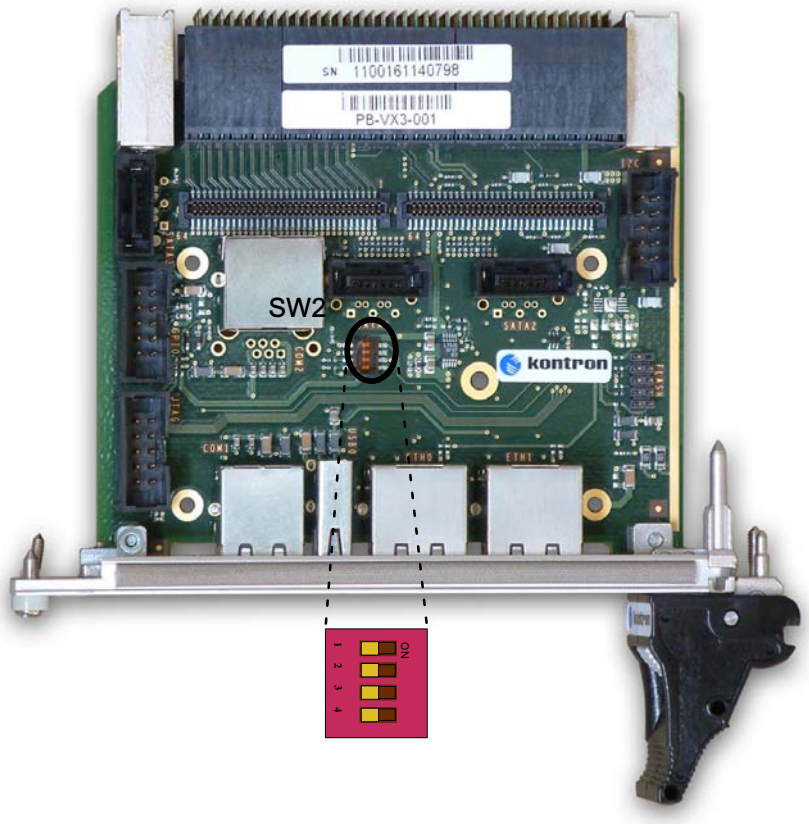


Figure 28: VX3240-RTM MicroSwitch Location

MicroSwitch SW2	FUNCTION	DESCRIPTION
1	NVMRO Non-Volatile Memory Read Only	ON (0) Set NVMRO VPX signal to Ground OFF (1) No action on NVMRO VPX signal **Default setting**
2	Reserved	Reserved
3	Reserved	Reserved
4	Reserved	Reserved

6.4 Connectors

6.4.1 RTM Connectors Identification

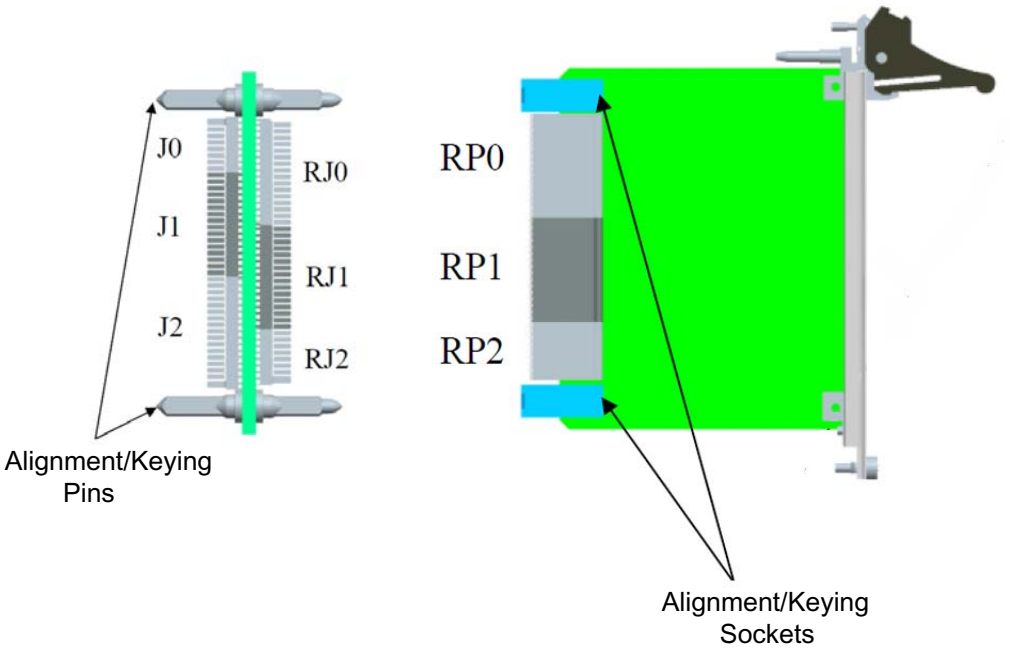


Figure 29: Connector Identification for 3U RTM

6.4.2 Front Panel Connectors

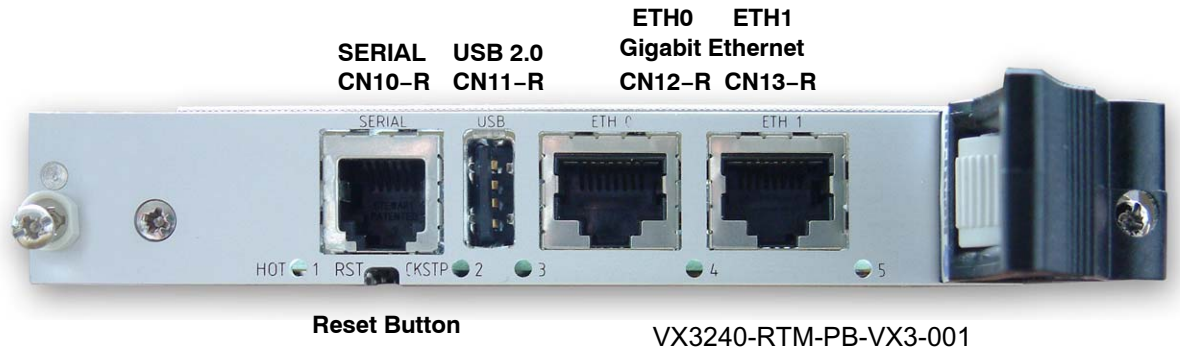
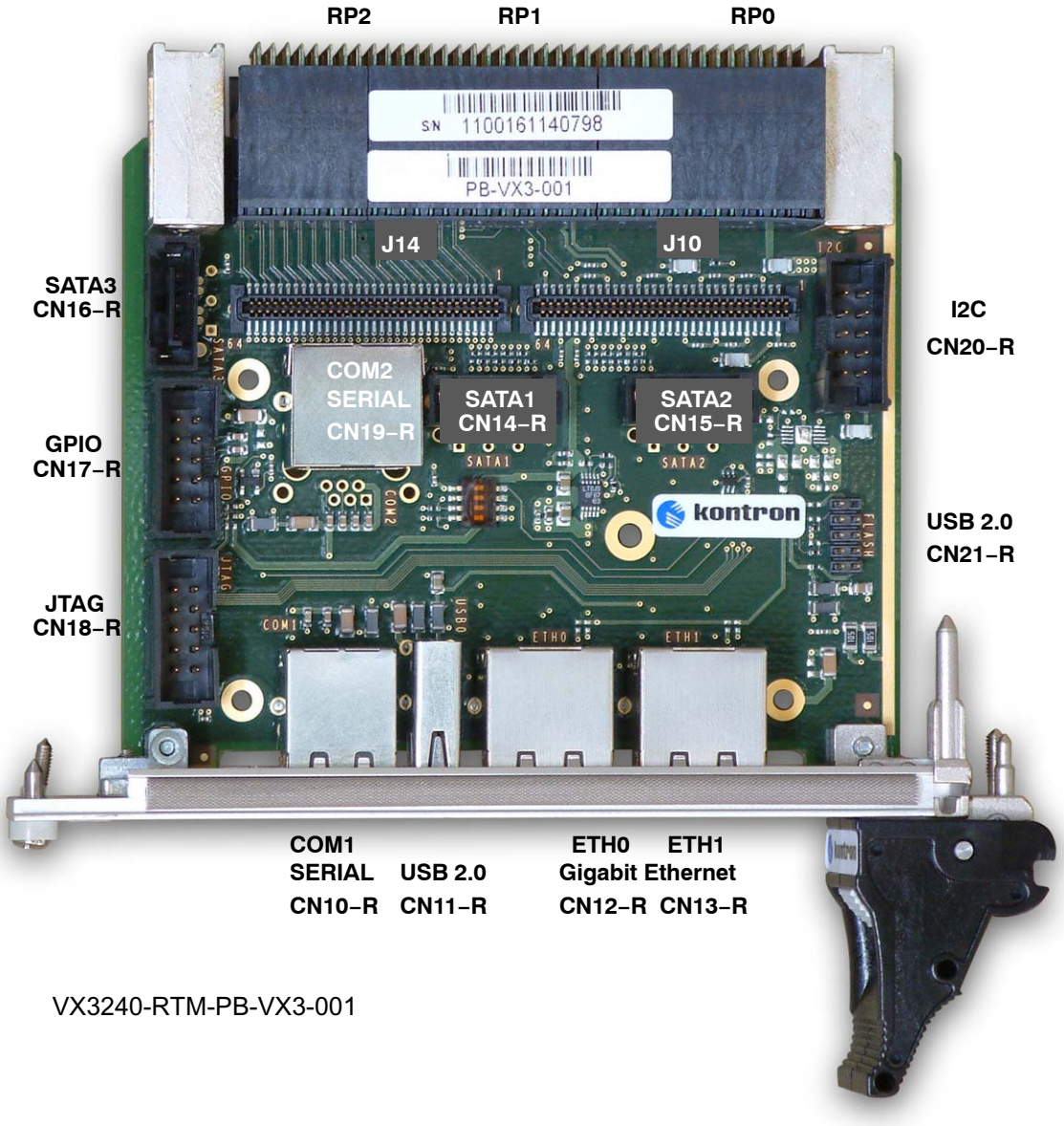


Figure 30: VX3240-RTM Front Panel Connectors

LED 1 to LED 5 are not connected.

6.4.3 Onboard Connectors



VX3240-RTM-PB-VX3-001

Figure 31: VX3240-RTM Onboard Connectors (PB-VX3-001)

USB 2.0 CN21-R, SATA2 CN15-R and SATA3 CN16-R are not used.

6.5 Modules Interfaces

6.5.1 COM Interfaces

The VX3240-RTM provides two COM (COM1 and COM2) ports for connecting devices to the VX3240-RTM.

COM1 serial port RJ-12 connector is located on the front panel of the RTM.

COM2 serial port RJ-12 connector is located onboard.

COM1 - EIA-232 Simplified

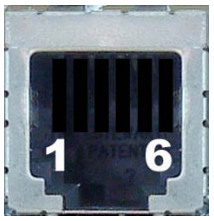
COM2 - EIA-232 Simplified

The following figure and table provide pinout information for:

- the 6-pin RJ-12 COM1 connector CN10-R located on the board front panel,
- the 6-pin RJ-12 COM2 connector CN19-R located onboard.

PIN	SIGNAL	FUNCTION
1	RTS	EIA-232 Ready-To-Send
2	Shell	Chassis Ground
3	TXD	EIA-232 Transmit Data
4	RXD	EIA-232Receive Data
5	GND	Ground
6	CTS	EIA-232 Clear-To-Send

Table 33: Serial Port Connector Pin Assignment



CN10–R
CN19–R

Figure 32: Serial Port Connector

6.5.2 USB Interfaces

There are two USB 2.0 ports available on the VX3240-RTM, each with a maximum transfer rate of 480 Mb/s provided for connecting USB devices.

- One interface is available on the VX3240-RTM front panel. One USB peripheral may be connected to this port. To connect more USB devices, an external hub is required.
- The second USB interface is onbard and used to connect a Flash disk.

USB Front Panel

The following figure and table provide pinout information for the CN11-R connector located on the front panel.

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND	--

Table 34: Front Panel USB Connector Pin Assignment

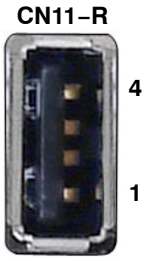


Figure 33: Front Panel USB Connector

The USB host interfaces on the VX3240-RTM can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

The Rear I/O interface supports the USB 1.1 and USB 2.0 standards. For USB 2.0 it is strongly recommended to use a cable length not exceeding 3 meters.

USB Onboard

The onboard USB device (CN21-R connector) is used to connect an USB flash disk module. The following figure and table provide pinout information for the onboard USB connector.

PIN	SIGNAL	FUNCTION	I/O
1	USB_PWR	VCC	--
2	N.C.	Not Connected	--
3	USB_D-	Differential USB-	I/O
4	N.C.	Not Connected	--
5	USB_D+	Differential USB+	I/O
6	N.C.	Not Connected	--
7	GND	GND	--
8	N.C.	Not Connected	--
9	N.C.	Not Connected	--
10	N.C.	Not Connected	--

Table 35: Onboard USB Connector Pin Assignment

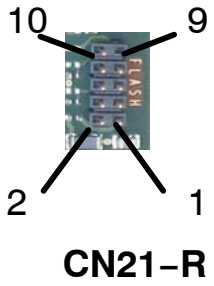


Figure 34: Onboard USB Connector

The USB Flash module is fixed to the board, by using on one side the CN21-R connector, and on the other side, a standoff screwed to the VX3240-RTM board and to the USB Flash module.

Figure 35: USB Flash Disk Overview

Order Code for the USB flash disk:

FDM-USB-*x*GB-2MM-IV: industrial version with conformal coating for use with rugged versions (*x* = 4 or 8 GB)

Note Contact Kontron for available capacity.

USB Flash Disk Layout:

- Maximum space reserved for USB flash disk is 36.9 mm x 26.6 mm (LxW)
- The distance between connector and screw hole is 27.3 mm~27.9mm
- Maximum allowable connector height is 3.68 mm

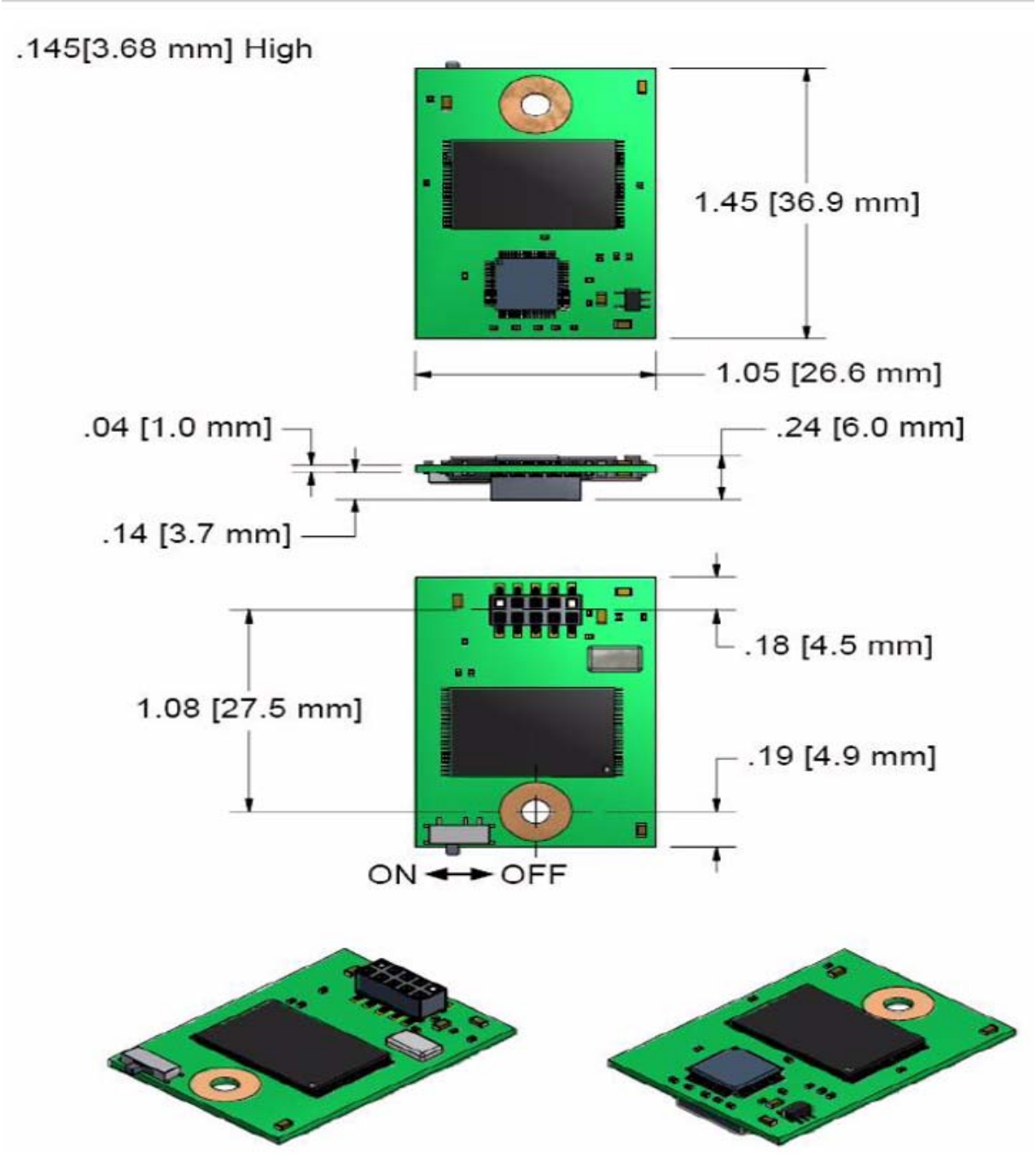


Figure 36: USB Flash Disk Layout

6.5.3 Gigabit Ethernet Interfaces

The Ethernet connectors are realized as RJ-45 connectors. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Ethernet interfaces manufacturing option: it is strongly recommended to use compatible RTM and SBC → ie Ethernet manufacturing option.

VX3240-RTM	SPECIFICATIONS	PB-VX3-001
Ethernet Front Panel Interfaces	Up to two Gigabit Ethernet interfaces implemented as dual RJ-45 connector without LEDs	Y (x2)

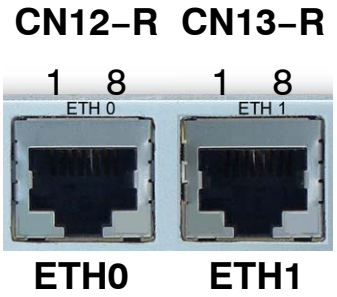


Figure 37: Gigabit Ethernet Connectors

The two RJ-45 ethernet ports have identical signals assigment. The Ethernet transmission can operate effectively using a CAT5 cable or higher specifications.

MDI/STANDARD ETHERNET CABLE						PIN	MDIX/CROSSED ETHERNET CABLE					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	TX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

Table 36: Gigabit Ethernet Connectors Pin Assignment

6.5.4 Serial ATA Interfaces

The onboard Serial ATA connectors CN14-R, CN15-R and CN16-R allow the connection of standard HDDs and other Serial ATA devices to the VX3240 Rear Transition Module.

The following figure and table provide pinout information for the SATA connectors CN14-R, CN15-R and CN16-R.

PIN	SIGNAL	FUNCTION	I/O
1	GND	Ground signal	--
2	SATA_TX+	Differential Transmit +	O
3	SATA_TX-	Differential Transmit -	O
4	GND	Ground signal	--
5	SATA_RX-	Differential Receive -	I
6	SATA_RX+	Differential Receive +	I
7	GND	Groudn Signal	--

Table 37: Onboard SATA Connectors Pin Assignment

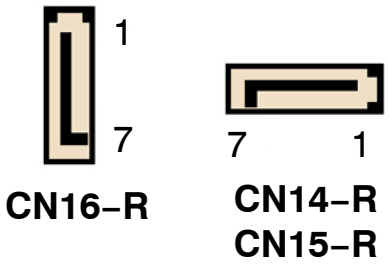


Figure 38: Onboard SATA Connectors

When using a Serial ATA cable, it is recommended to use a special right-angled Serial ATA cable due to possible space limitations within the system. For further information, contact Kontron's Technical Support.

6.5.5 GPIO Connector

Routed from RP1 to CN17-R connector (right angle HE10 10-pin connector male).

PIN	SIGNAL	FUNCTION
1	COM1 RXD	COM1 EIA-232Receive Data
2	COM1 CTS	COM1 EIA-232 Clear-To-Send
3	GND	Ground
4	GND	Ground
5	COM2 RXD	COM2 EIA-232Receive Data
6	COM2 CTS	COM2 EIA-232 Clear-To-Send
7	GPIO 1	General Purpose IO 1
8	GND	Ground
9	GPIO 2	General Purpose IO 2
10	GND	Ground

Table 38: Onboard GPIO Connector Pin Assignment

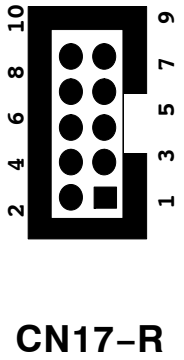


Figure 39: Onboard GPIO Connector

6.5.6 JTAG Connector

Routed from RP0 to CN18-R connector (right angle HE10 10-pin connector male).

PIN	SIGNAL	FUNCTION
1	TCK	JTAG Test Clock
2	GND	Ground
3	TDO	JTAG Test Data Out
4	3.3V sense	
5	TMS	JTAG Test Mode Select
6	N.C.	Not Connected
7	N.C.	Not Connected
8	TRST*	JTAG Test Reset
9	TDI	JTAG Test Data In
10	GND	Ground

* signal active when low

Table 39: Onboard JTAG Connector Pin Assignment

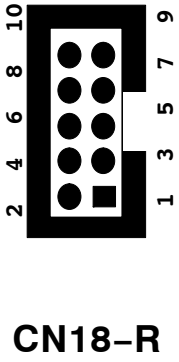


Figure 40: Onboard JTAG Connector

6.5.7 I2C System Management Connector

Routed from RP0 to CN20-R connector (right angle HE10 10-pin connector male).

PIN	SIGNAL	FUNCTION
1	I2C0 CLK	I2C 0 Serial Clock
2	I2C1 CLK	I2C 1 Serial Clock
3	GND	Ground
4	GND	Ground
5	I2C0 DAT	I2C 0 bi-directional serial data
6	I2C1 DAT	I2C 1 bi-directional serial data
7	+3V3_AUX	+3.3V auxiliary power supply
8	+3V3_AUX	+3.3V auxiliary power supply
9	N.C.	Not Connected
10	Reserved	Reserved

Table 40: Onboard I2C Connector Pin Assignment

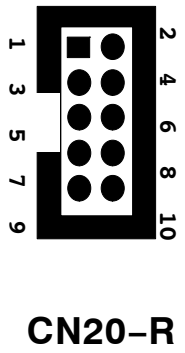
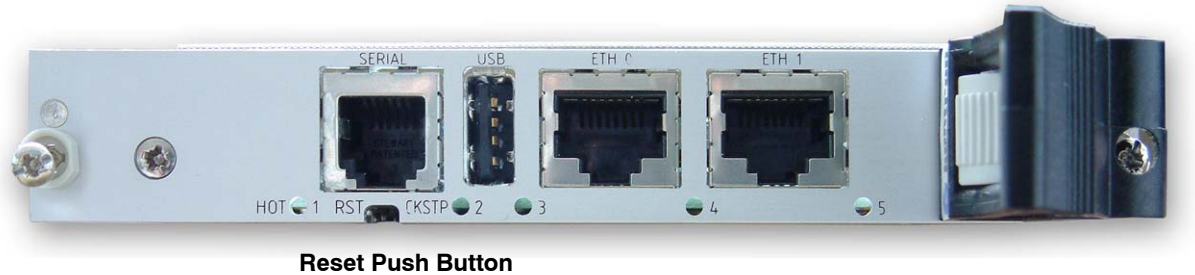


Figure 41: Onboard JTAG Connector

6.6 Reset



Reset Push Button

Figure 42: VX3240-RTM Reset Push Button

Reset and SW1 Reset Switch

The VX3240-RTM generates a system reset signal on the VPX bus at each +5V power-on for a duration of 140 ms to 560 ms.

In addition, the front panel reset push button of the VX3240-RTM is used to generate a VPX bus reset with the same minimum duration.

LEDs

The five LEDs are not connected, and unused.

6.7 Power Consideration

Only the 5V main power from the VPX is used.

The 3.3V and +12V VPX main power are not used in order to accomodate 6U VPX backplane.

Auxiliary VPX voltages 3.3V (I2C connector), +/- 12V (PIM J10 connector) are used.

The 3.3V on the J10 connector is regulated from the 5V input through a 1.5A max linear regulators.

6.8 Rear I/O Interfaces

The VX3240 Rear Transition Module conducts a wide range of I/O signals through the Rear I/O connectors RP0, RP1 and RP2.

- RP0: one 15-wafer 7-row connector
- RP1: one 16-wafer 7-row connector
- RP2: one 8-wafer 7-row connector

To support the Rear I/O feature a special backplane is necessary. Do not plug a Rear I/O configured board in a non-system slot Rear I/O backplane. Failure to comply with the above may result in damage to your board.

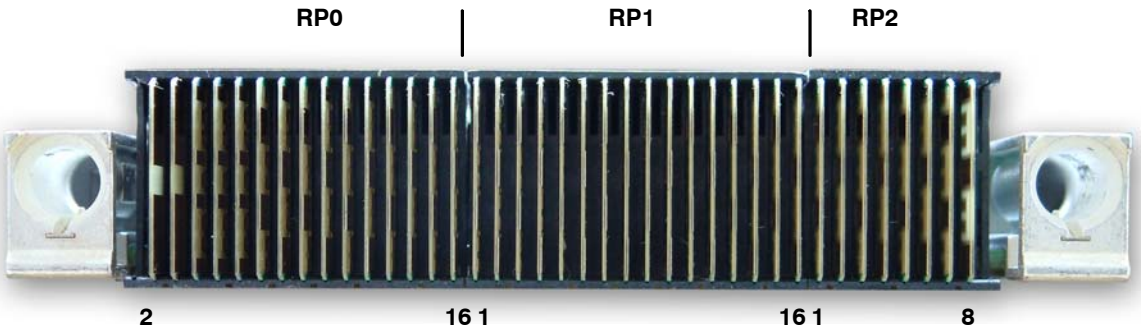


Figure 43: Rear I/O VPX Connectors

The VX3240-RTM provides the following interfaces:

- One USB 2.0 port
- Two Gigabit Ethernet ports without LED signals (ETH0 and ETH1 via RP1 connector)
- One SATA port
- Two GPIOs (GPIO1 and GPIO2 via RP1 connector)
- Two EIA-232 COM ports (COM1 via RP1 connector, COM2 via RP2 connector)

6.8.1 RP2 Connector

» RP2 Wafer Assignment

> Legend for Table 41:

COM*x* COM port

RPM Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	Board Wafer
1	COM2 RTS	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 w09
2	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 w10
3	COM2 TXD	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 w11
4	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 w12
5	COM2 CTS	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 w13
6	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 w14
7	COM2 RXD	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 w15
8	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 w16
CASE	GND							

Table 41: Rear I/O VPX Connector RP2 Wafer Assignment

» RP2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
COM2 CTS	Channel EIA-232 *x* Clear To Send
COM2 RTS	Channel EIA-232 *x* Ready To Send
COM2 RXD	Channel EIA-232 *x* Receive Data
COM2 TXD	Channel EIA-232 *x* Transmit Data
GND	Ground

Table 42: Rear I/O VPX Connector RP2 Signal Definition

6.8.2 RP1 Connector

» RP1 Wafer Assignment

> Legend for Table 43:

USB	USB	ETHx	Gigabit Ethernet Port
SATA	Serial ATA Port	COMx	COM Port

RPM Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	Board Wafer
1	USB PWR	GND	SATA TX-	SATA TX+	GND	SATA RX-	SATA RX+	P1 w09
2	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P1 w10
3	Reserved	GND	Reserved	Reserved	GND	Reserved	Reserved	P1 w11
4	GND	USB D-	USB D+	GND	Reserved	Reserved	GND	P1 w12
5	GPIO1	GND	ETH1 DB-	ETH1 DB+	GND	ETH1 DA-	ETH1 DA+	P1 w13
6	GND	ETH1 DD-	ETH1 DD+	GND	ETH1 DC-	ETH1 DC+	GND	P1 w14
7	GPIO2	GND	ETH0 DB-	ETH0 DB+	GND	ETH0 DA-	ETH0 DA+	P1 w15
8	GND	ETH0 DD-	ETH0 DD+	GND	ETH0 DC-	ETH0 DC+	GND	P1 w16
9	COM1 RTS	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 w01
10	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 w02
11	COM1 TXD	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 w03
12	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 w04
13	COM1 CTS	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 w05
14	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 w06
15	COM1 RXD	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 w07
16	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 w08
CASE	GND							

Table 43: Rear I/O VPX Connector RP1 Wafer Assignment

RP1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
COM*x* CTS	Channel EIA-232 *x* Clear To Send
COM*x* RTS	Channel EIA-232 *x* Ready To Send
COM*x* RXD	Channel EIA-232 *x* Receive Data
COM*x* TXD	Channel EIA-232 *x* Transmit Data
ETH*x* DA+/-	10/100/1000BASE-TX Ethernet *x:* First pair of Transmit/Receive data.
ETH*x* DB+/-	10/100/1000BASE-TX Ethernet *x:* Second pair of Transmit/Receive data.
ETH*x* DC+/-	10/100/1000BASE-TX Ethernet *x:* Third pair of Transmit/Receive data.
ETH*x* DD+/-	10/100/1000BASE-TX Ethernet *x:* Fourth pair of Transmit/Receive data.
GND	Ground
GPIO *x*	General Purpose I/O *x*
Reserved	Reserved
SATA RX+/-	Serial ATA Receive +/-
SATA TX+/-	Serial ATA Transmit +/-
USB D+/-	Differential Data Pair of USB link
USB PWR	USB Power

Table 44: Rear I/O VPX Connector RP1 Signal Definition

6.8.3 RP0 Connector

RP0 Wafer Assignment

RPM Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	Board Wafer
2	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	P0 w02
3	+5V	+5V	+5V	+5V	+5V	+5V	+5V	P0 w03
4	I2C1_CLK	I2C1_DAT	GND	-12V_AUX	GND	SYSRESET*	NVMRO	P0 w04
5	N.C.	N.C.	GND	3V3_AUX	GND	I2C0_CLK	I2C0_DAT	P0 w05
6	N.C.	N.C.	GND	+12V_AUX	GND	N.C.	N.C.	P0 w06
7	TCK	GND	TDO	TDI	GND	TMS	TRST*	P0 w07
8	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P0 w08
9	Reserved	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w01
10	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w02
11	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w03
12	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w04
13	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w05
14	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w06
15	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w07
16	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w08
CASE	GND							

* signal active when low

Table 45: Rear I/O VPX Connector RP0 Wafer Assignment

RP0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+/-12V_AUX	Auxiliary Power Supplies
3V3_AUX	3.3V Auxiliary Power, System Management
+5V	+5V Power Input
GND	Ground
I2C0	I2C Bus 0
I2C1	I2C Bus 1
NVMRO	Non-Volatile Memory Read Only
N.C.	Not Connected
SYSRESET*	System Reset
TCK	JTAG signal - Test Clock
TDI	JTAG signal - Test Data Input
TDO	JTAG signal - Test Data Output
TMS	JTAG signal - Test Mode Select
TRST*	JTAG signal - Test Reset

* signal active when low

Table 46: Rear I/O VPX Connector RP0 Signal Definition

6.9 PCI 64 PIM Connector

6.9.1 J10 Connector

J10 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
01	N.C.	02	+12V_AUX	03	N.C.	04	N.C.
05	+5V	06	N.C.	07	N.C.	08	N.C.
09	N.C.	10	+3.3V	11	N.C.	12	N.C.
13	GND	14	N.C.	15	N.C.	16	N.C.
17	N.C.	18	GND	19	N.C.	20	N.C.
21	+5V	22	N.C.	23	N.C.	24	N.C.
25	N.C.	26	+3.3V	27	N.C.	28	N.C.
29	GND	30	N.C.	31	N.C.	32	N.C.
33	N.C.	34	GND	35	N.C.	36	N.C.
37	+5V	38	N.C.	39	N.C.	40	N.C.
41	N.C.	42	+3.3V	43	N.C.	44	N.C.
45	GND	46	N.C.	47	N.C.	48	N.C.
49	N.C.	50	GND	51	N.C.	52	N.C.
53	+5V	54	N.C.	55	N.C.	56	N.C.
57	N.C.	58	+3.3V	59	N.C.	60	N.C.
61	-12V_AUX	62	N.C.	63	N.C.	64	N.C.

Signal Description

MNEMONIC	DESCRIPTION
+/-12V-AUX	Auxiliary Power Supplies
+3.3V	+3.3V Power Input
+5V	+5V Power Input
GND	Ground
N.C.	Not Connected

6.9.2 J14 Connector

J14 Connector Pin Assignment

PIN	SIGNAL	FUNCTION
01	N.C.	Not Connected
...	...	...
64	N.C.	Not Connected

Chapter 7 - Backplane Suggestions

Kontron can offer for development or deployement of the VX3240 the following backplane models:

Single Star x4, 8 Slots

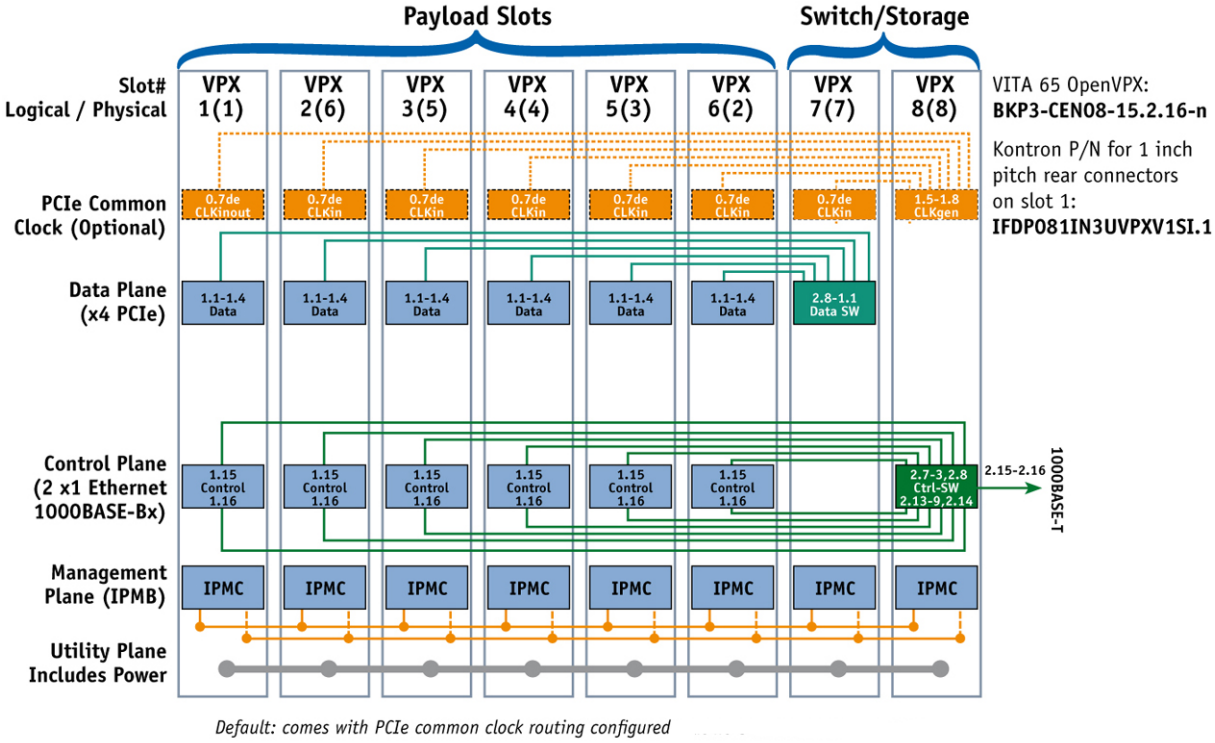


Figure 44: Single Star x4, 8 SlotsTopology

Single Star x4, 5 Slots

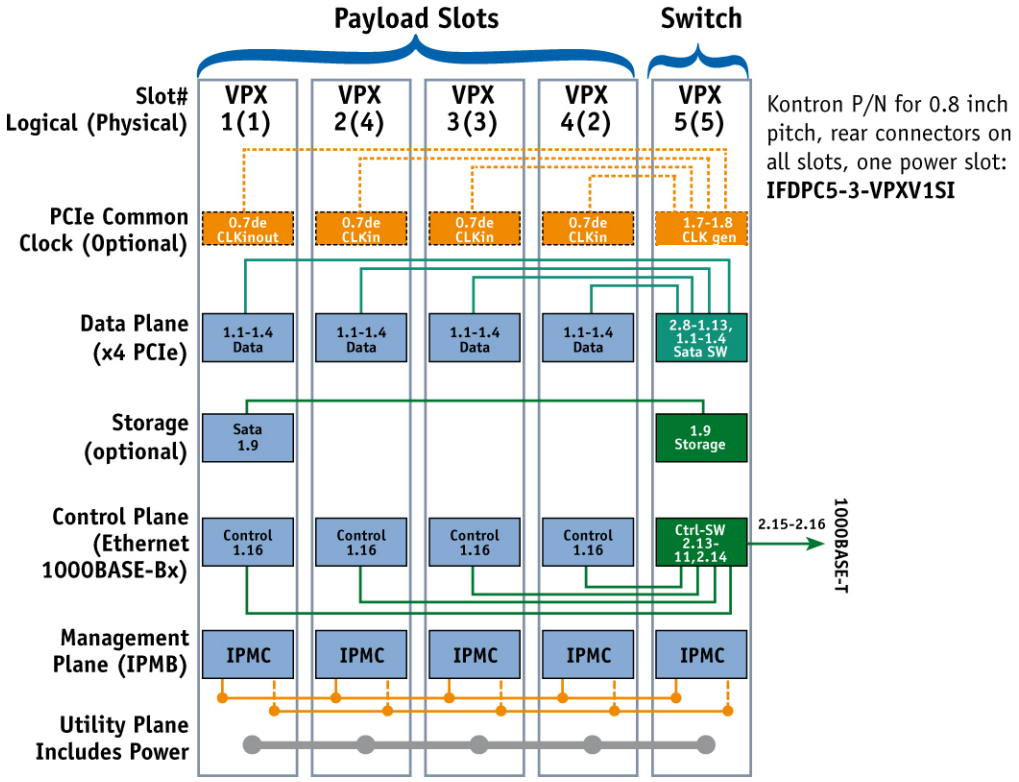


Figure 45: Single Star x4, 5 Slots Topology

Distributed, 2 Slots

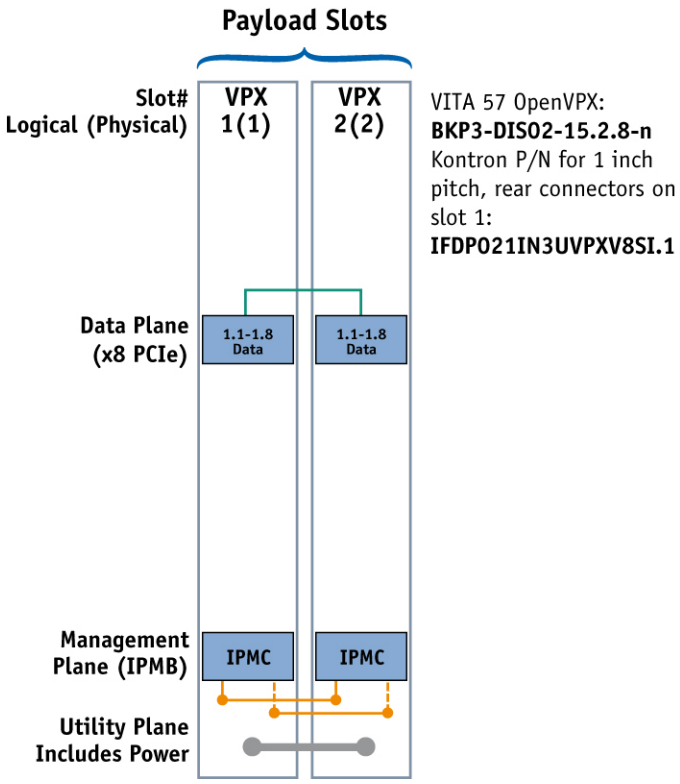


Figure 46: Distributed, 2 Slots Topology

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