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AP32085

THERE PAR

TriCore

A practical introduction to the TC1766 Memory Checker Module driver

Microcontrollers



Never stop thinking.

TriCore

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Introduction

1 Introduction

This Application Note explains the usage of the Memory Checker (MCHK) software driver. It assumes that the reader is already familiar with the Tricore architecture, the Tasking Compiler and the PLS debugger. The reader should also have read the chapter 4.1.11 Alternate Boot Mode and chapter 9 Direct Memory Access Controller (DMA) of the TC1766 User Manual (Table 1). The development environment used to build the sample program is listed in Table 2.

Table 1 Documents

| Title | Version |
|---|---------|
| TC1766, System Units, User Manual | 2.1 |
| TriBoard TC1766, Hardware Manual, User Manual | 1.0 |
| | |

| Tools | Version | Remarks |
|---------------------|------------|--|
| DAvE | 2.1r22 | http://www.infineon.com/dave |
| DAvE TC1766 Plug-in | 3.0 | available on request |
| SAG | 1.2 | |
| Tasking Vx Compiler | 2.1r2 | http://www.tasking.com |
| UDE Debugger | 1.10.02 | http://www.pls-mc.com/ |
| GNU bash | 2.05 | http://www.cygwin.com |
| GNU binutils | 2.13 | http://www.cygwin.com |
| tricore-readelf | 2.13 | http://www.hightec-rt.com/tricore.html |
| TriBoard TC1766 | TC1766.102 | |
| Windows 2000 | | |

Table 2 Tools

The MCHK driver is a thin software layer on top of the MCHK hardware module. For an architectural overview see Figure 2-1 in the TC1766 User Manual. The MCHK module allows checking the data consistency of memories and was especially developed to check the flash memory. The Program Flash and the Data Flash provide error correction (ECC) of single-bit errors within a 64-bit read double-word, resulting in an extremely low failure rate. Double-bit errors causes a Flash interrupt (see TC1766 User Manual chapter 7.2.9) but triple or even more-bit errors, which are hardly found by the hardware, can be detected with MCHK module. For this purpose the MCHK



Introduction

module implements a fast polynomial checksum calculation. A software implementation of the algorithm is given by:

```
unsigned long crc buffer(unsigned long crc,
                          const unsigned long *p,
                          unsigned long sz)
{
    const unsigned long poly = 0xEDB88320;
    unsigned long
                         tmp1, tmp2;
    while(sz--)
        tmp1 = 0;
        tmp2 = crc \& poly;
        for(int i = 0; i <=31; i++ )</pre>
            tmp1 ^{=} ((tmp2 >> i) \& 1);
        crc = *p++ ^ ((crc << 1) | tmp1) ;
    }
    return crc;
}
```

Within three steps this Application Note will guide you through the usage of the MCHK driver. First a simple program will be created using DAvE. The program will blink the on-board LED of the TriBoard. Next an MCHK driver will be added to the program. The driver calculates a checksum over a flash memory range. The Signature Analysis Generator (SAG) tool, which is distributed with this Application Note, is used to calculate the checksum in advance directly from the elf file. Finally an Alternate Boot Mode (ABM) header will be added to the application using SAG.



2 Build a sample program

Start DAvE and create a new TC1766 project (Figure 1).



Figure 1 DAvE New Project Dialog

If the TC1766 is not in the list of 32-Bit Microcontrollers the Plug-In has to be installed. The TC1766 Plug-In is part of this Application Note. Please follow the instructions in the DAvE manual how to install Plug-Ins.



| 💀 Project Settings | | | 2 | | | | |
|--------------------------------------|--|-------------------------------|--------------------------------|--|--|--|--|
| 🖄 🖚 🖓 | | | | | | | |
| General System Clock Inte | errupt System PCP System Pad Driver St | artup Configuration | Startup Configuration | | | | |
| External Clock Frequency | | | | | | | |
| External clock frequency [MHz] | 15 | D PLL Bypass of (pin BYPASS = | peration (fopu = foso) = 1) | | | | |
| Input divider (PDIV) | fp = fosc / 1 = 15,000 MHz | | | | | | |
| Voltage Controlled Oscillat | or (VCO) | | | | | | |
| VCO Bypass mode (VI | VCO Bypass mode (VCOBYP) | | | | | | |
| VC0 range (VC0SEL) 600 MHz - 700 MHz | | | | | | | |
| Feedback divider (NDIV) | fvco = fosc / P * 40 = 600,000 MHz | VCO output frequency [MHz] | 600,000 | | | | |
| - Output Divider | | | | | | | |
| Output divider (KDIV) | fcpu = fvco / 10 = 60,000 MHz | CPU Clock [MHz] | 60,00000000 | | | | |
| | 🔿 The ratio fopu / fsys is 2 / 1 | System Clock | 60,0000000 | | | | |
| | The ratio fcpu / fsys is 1 / 1 | [MHz] | | | | | |
| | | | | | | | |

Figure 2 DAvE Project Settings Dialog, Page System Clock

Open the "Project Settings" from the File menu. Keep the default settings on the "General" page and goto the "System Clock" page (Figure 2). In general the TC1766 TriBoard is shipped with a 15 MHz external quartz. Set the "External clock frequency [MHz]" to 15, set the "Feedback divider (NDIV)" to 600 MHz and keep the default values for the rest of the dialog. This configuration will lead to a CPU and System Clock of 60 MHz.



| 🖶 Configure Port 1 📉 🔀 | | | | | | | |
|------------------------|---------------------|-----------|-------------------|-----------------|--------|----------|--|
| | | | | | | | |
| Channels Channel Inv | version Port 1 Innu | it Charac | teristic Dutout C | haracteristic [| Notes | | |
| | | | | | | | |
| Crianneis | | | | | | | |
| Channel 16's Name | IO_P1_0 | Config | Output High 💌 | Dedicate | DIO | - | |
| Channel 17's Name | 10_P1_1 | Config | Unused 🔽 | Dedicate | DIO | ∇ | |
| Channel 18's Name | 10_P1_2 | Config | Unused 💌 | Dedicate | DIO | - | |
| Channel 19's Name | I0_P1_3 | Config | Unused 💌 | Dedicate | DIO | - | |
| Channel 20's Name | I0_P1_4 | Config | Unused 🔽 | Dedicate | DIO | - | |
| Channel 21's Name | 10_P1_5 | Config | Unused 🔽 | Dedicate | DIO | - | |
| Channel 22's Name | I0_P1_6 | Config | Unused 🔽 | Dedicate | DIO | - | |
| Channel 23's Name | 10_P1_7 | Config | Unused 🔽 | Dedicate | DIO | Y | |
| Channel 24's Name | I0_P1_8 | Config | Unused 🔽 | Dedicate | DIO | Y | |
| Channel 25's Name | I0_P1_9 | Config | Unused 🔽 | Dedicate | DIO | - | |
| Channel 26's Name | I0_P1_10 | Config | Unused 🔽 | Dedicate | DIO | - | |
| Channel 27's Name | I0_P1_11 | Config | Unused 💌 | Dedicate | DIO | - | |
| Channel 28's Name | I0_P1_12 | Config | Unused 💌 | Dedicate | DIO | - | |
| Channel 29's Name | I0_P1_13 | Config | Unused 💌 | Dedicate | DIO | - | |
| Channel 30's Name | I0_P1_14 | Config | Unused 💌 | Dedicate | DIO | - | |
| | | | | | , , | _ | |
| | | | | | | | |
| | | | | | | | |

Figure 3 Configure Port 1 Dialog, Page Channels

Finally pin 0 of port 1, which is connected to the LED of the board, needs to be configured. For detailed information read the TriBoard Manual. Click on the Port bubble in DAvE and on the "Ports" page press the "Configure Port 1" button. Configure the Channel 16, which is port 1 pin 0, to "Output High" (Figure 3).

Close the Dialog and go to the "Functions" page and check the Initialization Function. The configuration is done. Close the configuration dialogs and save the project as 'mchk.dav'. Generate the source files by selecting "Generate Code" from the File menu.

DavE generates the followings source and header files: The project initialization function 'MAIN.c', 'MAIN.h', the port driver 'LLD_DIO.c', 'LLD_DIO.h', C Startup code 'cstart.c', CAS data types definition 'LLD.h', 'CAS_DTYP.h' and the register definition file for the TC1766 'TC1766Regs.h'.

In the next step the elf file will be build using the Tasking compiler and linker. Open Tasking IDE and create a new project. Open the Project options and go to Processor->"Processor definitions". Select "TC1766". Go to "Compiler"->Optimization



and select "No Optimization" from the dropdown menu. Go to Processor->Startup and deselect the "Automatic copy and link cstart.asm to your project" checkbox. Go to Linker->"Script File"-> "Special Areas" and set the values to the following addresses:

| RESET start address | 0xA000000 |
|-------------------------------|------------|
| Libraries start address | 0xA0000400 |
| Interrupt table start address | 0xA0002000 |
| Trap table start address | 0xA0003F00 |

Go to Linker->"Script File"->"Internal Memory" and define the program flash

Name = pflash, Alloc = ON, Type = ROM, Size = 1504k

Close the project options. Open the project properties and add the files 'MAIN.c', 'LLD DIO.c' and 'cstart.c' to the project.

In <code>'LLD_DIO.h'</code> add two macros which were part of former plug-ins but did not make it to the TC1766 plug-in

```
// USER CODE BEGIN (IO_Header,3)
#define DIO_vTogglePin(PinName) TOGGLE##PinName
#define TOGGLEIO_P1_0 P1_OMR.I = 0x00010001
// USER CODE END
```

In MAIN.c add a delay function

and a forever loop which toggles the TriBoard LED.

```
// USER CODE BEGIN (Main,9)
while(1)
{
    DIO_vTogglePin(IO_P1_0);
    delay(8);
}
// USER CODE END
```

Build the elf file. Ensure the HW Boot Configuration DIP-switch is set to ON-OFF-ON-ON-OFF-ON-OFF-OFF. The ON position of the switch is equal to a logical LOW, that means HWCFG[3...0] is 0010 (See the TriBoard Manual chap. 5.1.1). The board will start from internal flash at 0xA0000000.

Open the UDE debugger and create a new workspace with a TC1766 target. Install the UDE memtool, select "Flash programming" from the Tools menu and enable the flash



by checking the box "Enable". Erase the Flash by pressing the "Erase..." button and exit the dialogs. Now you are ready to flash the program. Select "Load Program" from the File menu and open the 'mchk.elf' file. The UDE memory programming tool dialog pops up again. Press the "Program" button. Flashing will take up a minute. On success exit the dialogs. Reset the board and see the LED blinking.



3 Add a MCHK driver to the sample program

In the following step a MCHK driver will be added to the sample program. The driver will continuously calculate a checksum over a flash memory range. Open DAVE with the 'mchk.dav' project again and select the DMA module. The MCHK module is part of the DMA¹. Go to the "block 0" page. Pressing the "DMA Channel 00" button brings up the configuration dialog. Check "Use channel 00" and set the Reset Request Control (RROAT) to "Reset DMA Request Only After Transaction" and the Channel Data Width (CHDW) to "32 Bits (Word)".

| 😨 Configure DMA Channel 00 | × |
|--|-----|
| 💌 🗗 🖓 | |
| | |
| | |
| Shadow Control (SHCT) | |
| O Shadow register O Shadow register O Shadow register used for Source O used for Destination | on |
| Source Start Address (SADR) | |
| 0x00000000 | |
| Circular Buffer Length Source (CBLS) | |
| 32 kBytes No Address Modification |] [|
| Source Modification Factor (SMF) | |
| Data Width * 1 | |
| Increment Control of Source Address (INCS) | |
| Increment Decrement | |
| | |

Figure 4 Configure DMA Channel 00, Page Address Control

Go to the "Address Control" page of the "Configuration DMA Channel 00" dialog (Figure 4). Set the destination address (DADR) to the memory checker input register MCHK_IR value 0xF010C210 (see Table 19-24 in the TC1766 User Manual). The circular buffer length source (CBLS) must exceed the memory range that will be checked. Set it to the maximum of 32kBytes which is the limit of a DMA transaction.

¹ The MEMCK bubble on the overview will be deleted in a later version.



Set the Increment of source Address (INCS) to "Increment". The source address (SADR) will be set by the driver.

Close the "Configuration DMA Channel 00" dialog and go to the "Memory 0" page of the "Direct Memory Access (DMA)" dialog. Check the "SCU incl. WDT, MEMCHK" and "Program Flash Space"

Go to the MEMCHK page and check the "DMA CH0" box.

At last open the "Functions" page and check the functions OCDMA_vInit, OCCRC_InitSync, OCCRC_ResetSync and OCCRC_CalculateSync. When generating the code two new files 'DMA.c' and 'DMA.h' will be generated.

Add these files to the Tasking project and modify the 'MAIN.c' file:

```
// USER CODE BEGIN (Main,9)
const IO_ChannelType chnl = 0;
unsigned int ret;
OCCRC_InitSync(NULL);
while(1)
{
    DIO_vTogglePin(IO_P1_0);
    OCCRC_ResetSync(0xFFFFFFF, chnl);
    ret = OCCRC_CalculateSync((void*)0xA0000000, 1, chnl);
    if (ret == 0L)
        delay(8);
    else
        delay(1);
}
// USER CODE END
```

OCCRC_InitSync(NULL) inits the driver, OCCRC_ResetSync(0xFFFFFFF, chn) saves the seed value of the channel in a global array. The seed value is the init value for the checksum calculation which will be passed to the result register MCHK_RR before the calculation starts. The use of 0xFFFFFFF is equal to the procedure used in the ABM checksum calculation, were the checker result register MCHK_RR is preloaded with 0xFFFFFFF (see TC1766 User Manual chap. 4.1.11.2).

At that time the parameter values passed by OCCRC_CalculateSync are just placeholders. The correct values will be determined after a first build procedure. In this sample program a checksum will be calculated over the libc. After building the program, the correct values are given by the map file.



| * Section translation: | | | | | | |
|------------------------|--|------------|----|-----------|--|------------|
| | | | | | | |
| Section | | Size (MAU) | S | pace addr | | Chip addr |
| .text.libc | | 0x000002ac | 0: | xa0000400 | | 0x00000400 |

Section .text.libc starts at 0xA0000400 and has a size of 0x000002AC. 0x2AC is the size of 171 words. With the correct parameters the function call OCCRC_CalculateSync is modified to:

```
ret = OCCRC_CalculateSync((void*)0xA0000400, 171, chnl);
Debuild the olf file
```

Rebuild the elf file.

When the program is flashed now the LED will blink fast because OCCRC_CalculateSync will not return zero so that delay(1) will be called.

To calculate the correct checksum in advance the Signature Analysis Tool (SAG) which is part of the Application Note will be used. Create a text file 'mchk.smd' and add the following line:

-eav 0 0xA0000400 - 0xA00006A8

The end address 0xA00006A8 is 4 bytes less than the sum of the start address and the size because the end address is included in the memory range.

Execute the SAG tool and read the result file 'ifxcrc.inf' from the command line

\$ifxsag mchk.elf mchk.smd; cat ifxcrc.inf

0xd272b356

Put the result value in the compare condition, so that the code look like:



```
// USER CODE BEGIN (Main,9)
const IO_ChannelType chnl = 0;
unsigned int ret;
OCCRC_InitSync(NULL);
while(1)
{
    DIO_vTogglePin(IO_P1_0);
    OCCRC_ResetSync(0xFFFFFFF, chnl);
    ret = OCCRC_CalculateSync((void*)0xA0000400, 171, chnl);
    if (ret == 0xd272b35)
        delay(8);
    else
        delay(1);
}
```

Build, flash and run the program. The LED will blink slowly.



Add an Alternate Boot Mode (ABM) header to the sample program

4

Add an Alternate Boot Mode (ABM) header to the sample program

With the SAG Tool it is straightforward to add an ABM header to the elf file, so that a memory range is checked at start-up. Modify the SAG command file to:

-eavw 0 0xa0000400 - 0xa00006A8

Executing the following command

\$mchk.elf mchk.smd -write_abm_header -flash_internal -o mchk_abm.elf
will add an ABM header to a copy of the elf file.

Use the e.g. the GNU readelf utility to verify the section changes.

\$tricore-read -S mchk abm.elf Section Headers: [Nr] Name Addr Off Туре Size ES Flg Lk Inf Al [27] .abmheader1 PROGBITS a001ffe0 003a4c 000020 00 AX 0 0 1 [28] .abmheader2 PROGBITS a003ffe0 003a6c 000020 00 AX 0 0 1

Flash the program. Switch the Hardware configuration DIP 1 to OFF to select the Alternate Boot Mode. Reset the TriBoard and see again the LED blinking.

The SAG tool has many more options. To learn more about the complete functionality read the SAG manual.



Goodies

5 Goodies

This Application Note comes with two goodies.

5.1 CRC debugger macro

Install the macro file 'ifxcrc.dsm' as an UDE debugger macro. The file contains the macro ifxcrc. If the "Run" button is pressed in the Macro dialog an input parameter pops up. The ifxcrc macro needs 3 parameters: the initial crc value, the start and the end address. Use Visual Basic notation for hexadecimal values.



Figure 5 Input parameter dialog of the ifxcrc macro.

The result is shown in a Message Box dialog and also written to the command view window.

| Comm | Command Yiew | | | | | | |
|------|--|--|--|--|--|--|--|
| MSG: | UADCommDev: Connected to UAD 138246, running TriCore JTAG/OCDS Debug Protocol, Version: 2.11.2 | | | | | | |
| MSG: | UDEMemtool: FLASH programming for device '1,5 MByte OnChip Program FLASH' ready | | | | | | |
| MSG: | UDEMemtool: FLASH programming for device '32 KByte OnChip Data FLASH' ready | | | | | | |
| MSG: | UDEDebugServer: Connection to TC1766 target monitor established: TriCore (Core), ID: 100DB083h | | | | | | |
| MSG: | Checksum Macro: Start address: 0xA0000400, End address: 0xA00006A8, Signatur: 0x25415F4F | | | | | | |
| | | | | | | | |
| | | | | | | | |



Goodies

5.2 CRC command line tool

Use the 'ifxcrc.exe' command line tool to generate an ABM header as a source file to be linked to your project. 'ifxcrc.exe' comes as source code including a Makefile for GNU.

Execute

\$ ifxcrc -a -sA0000400 -eA00006A8 mchk.elf >abm1.c; cp abm1.c abm2.c

to create two new files 'abm1.c' and 'abm2.c'. Add both to a copy 'mchk_goody.pjt' of the previous project file 'mchk.pjt' and setup two Sections .rodata.abm1, .rodata.abm2 (Figure 6).

| TriCore VX-toolset Project Options [MCHK_GOODY.PJT] | | | | | | × | | |
|--|--|--|--|-----------------------------|--------------------|--------------------------|------------|------|
| | Processor | Sections | (- . | - | | | | 7 |
| | | Space | Sections | Group | Сору | Alloc | Location | |
| | | linear | .rodata.abm1 | ordered | NO | abs | 0xA001FFE0 | |
| | | linear | .rodata.abm2 | ordered | NO | abs | 0xA003FFE0 | |
| | PUP Assembler | | | | | | | |
| | 📮 Linker | | | | | | | - 11 |
| | Output Format | | | | | | | |
| Gript File Special Areas Defines/Stack/Heap Internal Memory | | | | | | | | |
| | | | | | | | | |
| | | Options string: | | | | | | |
| | - External Memory - Sections - Output Sections | format=elf - -WI-mcfkIMc -WI-OCDLS | o"mchk_goody.elf)QrSU -WI-L''\$(PRC TXY | ' -d''_mchkj)DDIR)\lib\ | _goody. \$(PROT | lsl'' -Ctc17 'ECTED)' | 766 -WI-M | |
| | | OK | Cancel | | De | efault | Help | |

Figure 6 Linker Section Settings

Rebuild the project. Verify the section header with the tricore-readelf utility

```
$ tricore-readelf -S mchk_goody.elf
...
Section Headers:
[Nr] Name Type Addr Off Size ES Flg Lk Inf Al
...
[22] .rodata.abm2 PROGBITS a003ffe0 002c37 000020 00 AT 0 0 4
[23] .rodata.abm1 PROGBITS a001ffe0 002c57 000020 00 AT 0 0 4
```

Flash the program and reset the TriBoard.

'ifxcrc.exe' has many other options. Type --help to display all options and explore the source code.



Goodies



Example code

6 Example code

The Application note comes with a code package ap3208510_tc1766_mchk.zip. The zip file contains the following files.

```
----mchk
      abm1.c
                            // Generated by ifxcrc.exe
                            // Generated by ifxcrc.exe
      abm2.c
      CAS DTYP.h
                            // Generated by DAvE mchk.dav Project
                           // Generated by DAvE mchk.dav Project
      cstart.c
      IFXCRC.INF
                            // SAG output file
      LLD.h
                           // Generated by DAvE mchk.dav Project
                           // Generated by DAvE mchk.dav Project
      LLD DIO.c
      LLD DIO.h
                           // Generated by DAvE mchk.dav Project
      LLD DMA.c
                           // Generated by DAvE mchk.dav Project
     LLD DMA.h
                           // Generated by DAvE mchk.dav Project
      MAIN.c
                           // Generated by DAvE mchk.dav Project
      MAIN.h
                           // Generated by DAvE mchk.dav Project
                           // DAvE Project file
      mchk.dav
      mchk.pjt
                           // Tasking EDE Project file
      mchk.psp
                           // Tasking EDE Project Workspace
      mchk.smd
                           // SAG Command file
                           // UDE Workspace
      MCHK.WSP
                           // Tasking EDE Project file
      mchk goody.pjt
                           // Generated by DAvE mchk.dav Project
      TC1766Reqs.h
  -SAG
       TriCore SAG Release V1.2 2004-12-14.zip // SAG Tool package
  -Goodies
     —ifxcrc
                         // ifxcrc source file
          ifxcrc.cpp
          makefile
                           // Makefile for ifxcrc.exe
     -pls
                           // UDE Debugger macro
          ifxcrc.dsm
```



Glossary

7 Glossary

| DAvE | Digital Application virtual Engineer. Code generator and Low level driver configurator Infineon Microcontroller. See http://www.infineon.com/daye |
|---------|--|
| UDE | Universal Debug Engine from PLS |
| PLS | Company name: Programmierbare Logik & Systeme GmbH Manufacturer of the UDE Debugger used in this Application Note. |
| Tasking | Company name: Tasking Manufacture of the Compiler used in this Application Note See <u>http://www.tasking.com/products/tricore/</u> |
| SAG | Signature Analysis Generator Tool for calculating the CRC value and attaching an ABM header to an elf file. |

http://www.infineon.com