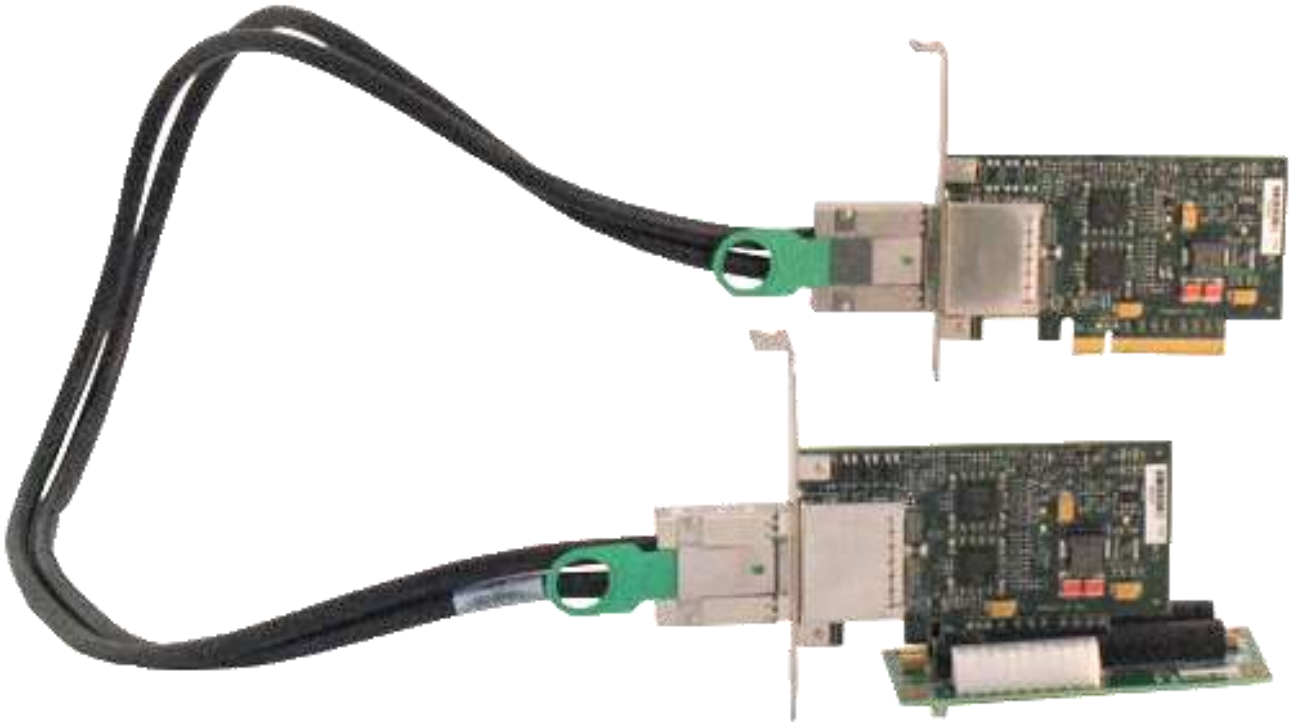


User Manual,
PCIe x8 Gen 2 Expansion Kit
(OSS-KIT-EXP-8000-2M)

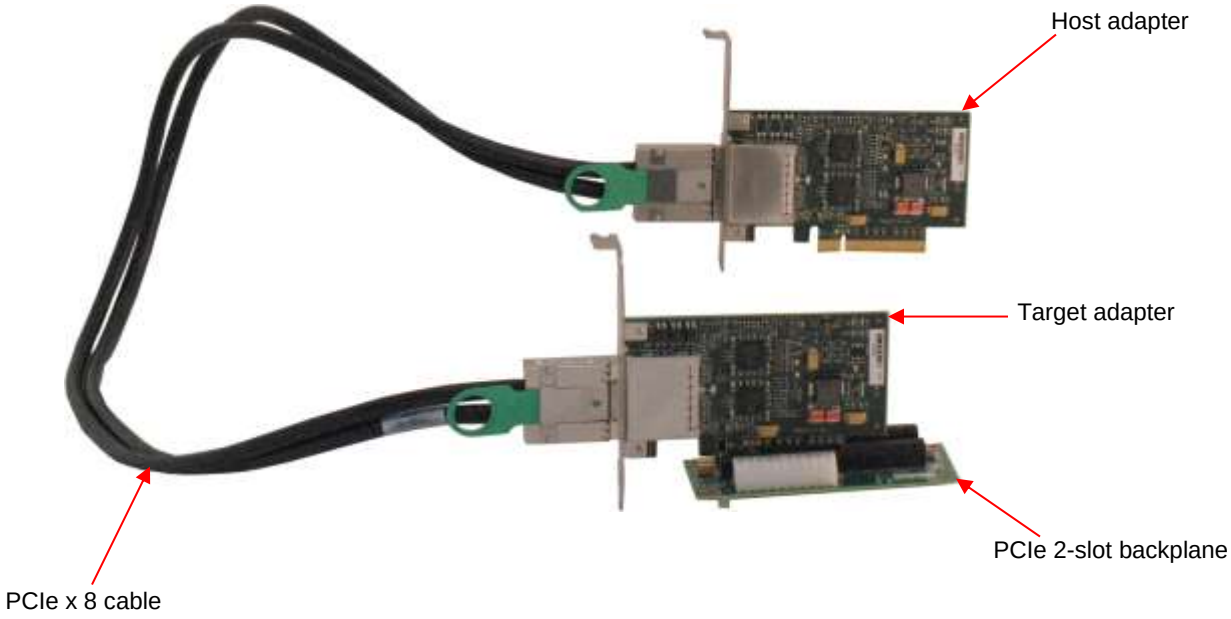
Table of Contents

1.a. Description

The PCIe x8 Gen 2 expansion kit is used to extend the PCI Express bus from a host server to an external PCIe I/O board. The host adapter card inserts into a PCIe slot of the server. It then cables to a downstream target adapter card. The target adapter card inserts in the OSS Gen 2, 2-slot backplane. The I/O board then inserts in the other slot of the backplane.

The host adapter installs in the PCIe x8, or x16 slot of the host motherboard. It then cables to the target adapter card and installs in the appropriate slot of the 2-slot backplane. A third party I/O card installs in the second slot of the 2-slot backplane. The I/O card then appears to the host system as host of that system.

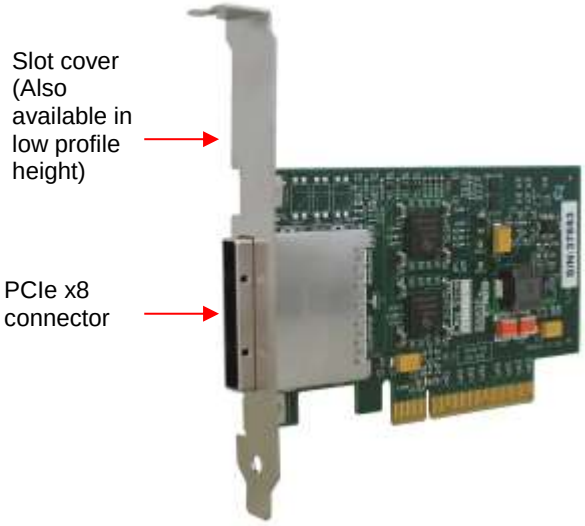
Gen 2 products operate at 5Gb/s per lane, or twice the bandwidth of Gen 1 products. Therefore, PCIe x8 Gen 2 products operate at 20Gb/s when inserted in a x8 or higher slot.



2. Components

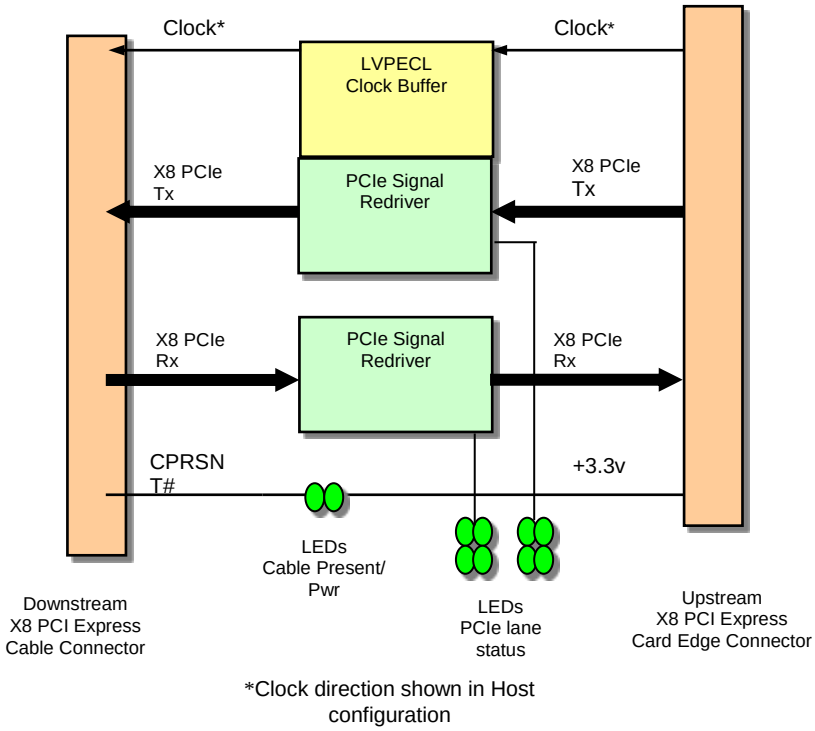
2.a. Host cable adapter

The PCIe x8 expansion kit contains two cable adapter boards, the *host* cable adapter and the *target* cable adapter. The host adapter inserts into the host computer's PCIe x8 or x16 slot. The host cable adapter (Part # OSS-PCIe-HIB25-x8-H) allows communication between a processor and an I/O point. The target adapter inserts into the slot closest to the ATX power connector of the 2-slot backplane.



2.b. Target cable adapter

The target adapter inserts into the slot closest to the ATX power connector of the 2-slot backplane.

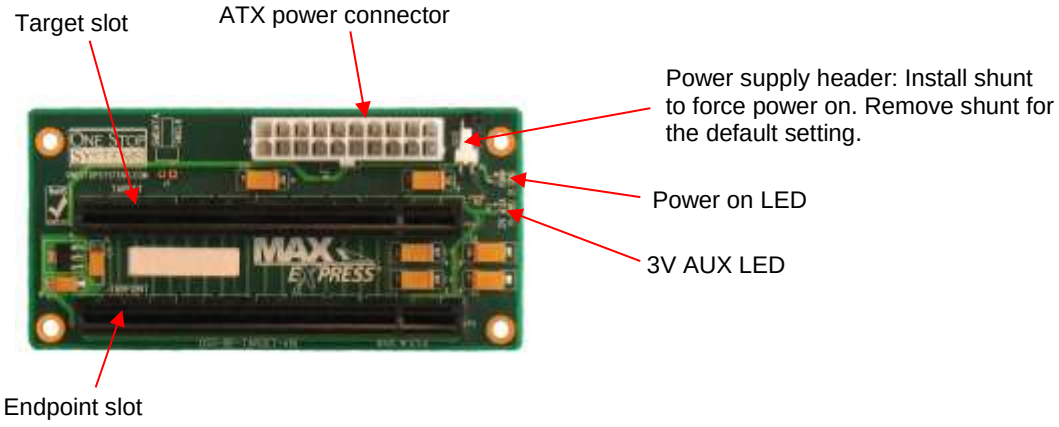


Host and Target Adapter Specifications

Electrical/Mechanical Specifications	
Form Factor:	PCIe x8 add-in card
Dimensions (H x L):	4.5 x 2.7 inches
Front Panel Connectors:	One PCIe x8 cable connector
Power Consumption (designed to meet the following conditions) 3.75W typical, 3.3@1.3A	
Operating Environment (designed to meet the following conditions)	
Temperature Range:	0° to 50°C (32° to 122°F)
Relative Humidity:	10 to 90% non-condensing
Shock:	30g acceleration peak (11ms pulse)
Vibration:	5-17 Hz 0.5” double amplitude displacement; 7-2000Hz, 1.5g acceleration.
Redriver: Pericom PI2EQX5804	
Agency Compliance: UL60950.FCC Class B, CE safety and emissions	

2.c. OSS 2-slot backplane

The 2-Slot backplane can be installed in a separate enclosure to support the target adapter and I/O card.
Note: See section 4. Technical Information for slot pin outs.



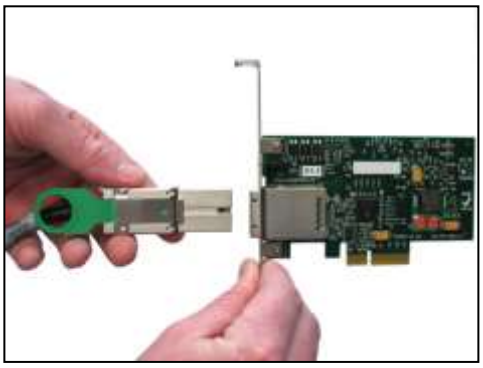
3. Installation Instructions

3.a. Installing the Adapter Kit

1) Insert the host cable adapter into an appropriate PCIe slot of the host computer. NOTE: For example, a PCIe x8 host board can be inserted into a PCIe x16 or a x8 slot. It will still operate at x8 speeds.

3.b. When using with the 2-slot Backplane:

2) Insert the target cable adapter into the PCIe slot closest to the white ATX power connector, labeled TARGET on the 2-slot backplane.
3) Connect the 2-slot backplane to an ATX power supply separate from the host system power supply. Note: Sometimes an external load is necessary for ATX power supplies to regulate properly. (i.e. – connecting hard drive power)
4) Insert the PCI add-in board in the I/O slot of the 2-slot backplane.
5) Connect the PCIe cable to both cable adapters.



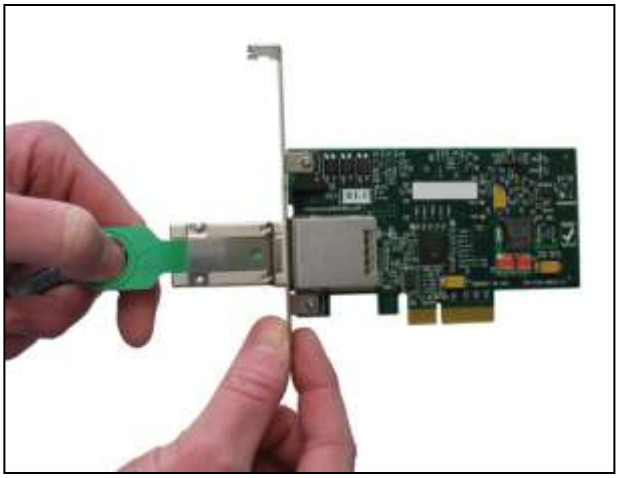
6) Power up the power supply to the 2-slot backplane. The 3V aux LED will light. NOTE: THE POWER SUPPLY AND 2-SLOT BACKPLANE WILL NOT POWER UP AT THIS TIME.
7) Power up the host system. The power and cable LEDs on the cable adapters will light. This powers up the one slot backplane
8) The I/O board will start automatically.

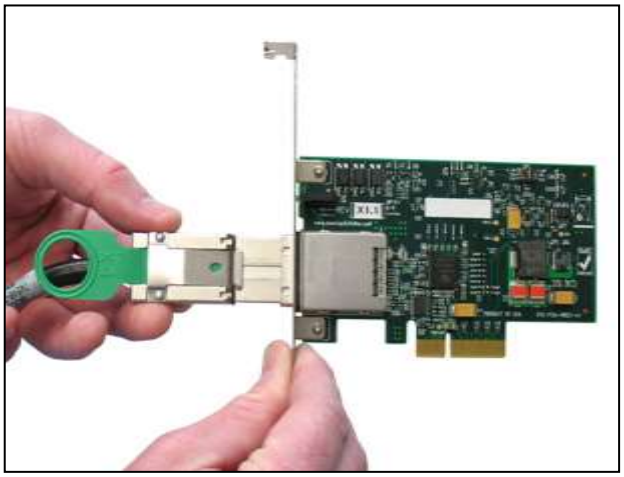
3.c. When using with any third party I/O device:

1) Install the downstream board in the appropriate PCIe slot.
2) Connect the external power source (separate from the host system power supply) to the downstream device if necessary.
3) Connect the PCIe cable to both the upstream host adapter and the downstream device.

3.d. Removing PCIe cable:

1) To remove PCIe cable pull back on green thumb tab to release metal pins and gently separate.





4. Technical Information

The transmit and receive signals on the OSS-HIB25-x8 are driven and conditioned by Pericom redriver chips. Adjustments can be made to equalization, de-emphasis and output swing. These controls are factory set by the use of zero Ohm resistors. In the following tables a 0 indicates that a zero Ohm resistor has been installed and a 1 indicates no resistor. In rare cases, mostly where non-OSS equipment is used with the OSS-HIB25-x8, these adjustments may need to be changed. The following tables are made available for this purpose. It is highly recommended to contact OSS customer support before making changes to these settings.

4.a. Signal Adjustment

Equalizer Selection

SEL_2[A:D]	SEL_1[A:D]	SEL_0[A:D]	@1.25 GHZ	@2.5 GHZ	
0	0	0	0.5dB	1.2dB	Edge Default
0	0	1	0.6dB	1.5dB	
0	1	0	1.0dB	2.6dB	
0	1	1	1.9dB	4.3dB	
1	0	0	2.8dB	5.8dB	
1	0	1	3.6dB	7.1dB	Cable Default
1	1	0	5.0dB	9.0dB	
1	1	1	7.7dB	12.3dB	

De-emphasis Adjustment

D2_[A:D]	D1_[A:D]	D0_[A;D]	De-emphasis	
0	0	0	0dB	SW=ON Default
0	0	1	-2.5dB	
0	1	0	-3.5dB	
0	1	1	-4.5dB	
1	0	0	-5.5dB	
1	0	1	-6.5dB	SW=OFF Default
1	1	0	-7.5dB	
1	1	1	-8.5dB	

Output Swing Control

S_1[A:D]	S_0[A:D]	Swing (Diff. VPP)	
0	0	1V	Cable Default
0	1	05V	
1	0	0.7V	Edge Default
1	1	0.9V	

4.b. Pin Assignments

Host and Target card connectors PCIe x8 Card Edge Connector

- The pins are numbered as shown with side A on the top of the centerline on the solder side of the board and side B on the bottom of the centerline on the component side of the board.
- The PCIe interface pins PETpx, PETnx, PERpx, and PERnx are named with the following convention: “PE” stands for PCIe high speed, “T” for Transmitter, “R” for Receiver, “p” for positive (+), and “n” for negative (-).
- Note that adjacent differential pairs are separated by two ground pins to manage the connector crosstalk.

Pin-out for the PCIe x8 Card Edge Connector on the Host Cable Adapter

Pin #	Side B		Side A	
	Name	Description	Name	Description
1	+12V	12V Power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V Power	+12V	12V Power
3	+12V	12V Power	+12V	12V Power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	3.3 V power	JTAG5	TMS (Test Mode Select)
9	JTAG1	TRST# (Test Reset)	+3.3V	3.3 V power
10	3.3Vaux	3.3 V auxiliary power	+3.3V	3.3 V power
11	WAKE#	Signal for link reactivation	PERST#	Fundamental reset
Mechanical key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Hot-Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential pair, Lane 1	RSVD	Reserved
20	PETn1		GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair, Lane 2	GND	Ground
24	PETn2		GND	Ground
25	GND	Ground	PERp2	Receiver differential pair, Lane 2
26	GND	Ground	PERn2	
27	PETp3	Transmitter differential pair, Lane 3	GND	Ground
28	PETn3		GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	RSVD	Reserved	PERn3	

31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential pair, Lane 4	RSVD	Reserved
34	PETn4		GND	Ground
35	GND	Ground	PERp4	Receiver differential pair, Lane 4
36	GND	Ground	PERn4	
37	PETp5	Transmitter differential pair, Lane 5	GND	Ground
38	PETn5		GND	Ground
39	GND	Ground	PERp5	Receiver differential pair, Lane 5
40	GND	Ground	PERn5	
41	PETp6	Transmitter differential pair, Lane 6	GND	Ground
42	PETn6		GND	Ground
43	GND	Ground	PERp6	Receiver differential pair, Lane 6
44	GND	Ground	PERn6	
45	PETp7	Transmitter differential pair, Lane 7	GND	Ground
46	PETn7		GND	Ground
47	GND	Ground	PERp7	Receiver differential pair, Lane 7
48	PRSNT2#	Hot-Plug presence detect	PERn7	
49	GND	Ground	GND	Ground

Notes:

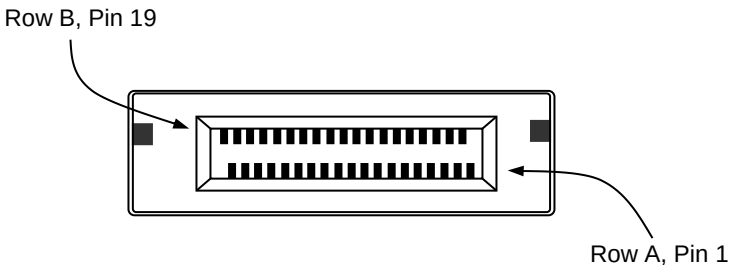
1. Optional signals that are not implemented are left as no connects on the board side connector.

2. Reserved signals are no connects on the board side connector.

3. Although support of CWAKE# is optional from the board side connector perspective, an allocated wire is mandated for the cable assembly.

4. Board side pin-outs on both sides of the Link are identical. The cable assembly incorporates a null modem for the PCIe transmit and receive pairs.

4.c. PCI Express x8 Connector Pin Assignment



Pin-out for the PCIe x8 Cable

	Row A	Row B		Row A	Row B		Row A	Row B
Pin #	Signal Name	Signal Name	Pin #	Signal Name	Signal Name	Pin #	Signal Name	Signal Name
1	GND	GND	13	GND	GND	24	PETn4	PERp4
2	PETp0	PERp0	14	CREFCLK+	PWR (3.3V)	25	GND	GND
3	PETn0	PERn0	15	CREFCLK-	PWR (3.3V)	26	PETp5	PERp5
4	GND	GND	16	GND	PWR (3.3V)	27	PETn5	PERn5
5	PETp1	PERp1	17	RSVD	PWR RTN	28	GND	GND
6	PETn1	PERn1	18	RSVD	PWR RTN	29	PETp6	PERp6
7	GND	GND	19	SB_RTN	PWR RTN	30	PETn6	PERn6
8	PETp2	PERp2	20	CPSRNT$#	CWAKE#	31	GND	GND
9	PETn2	PERn2	21	CPWRON	CPERST#	32	PETp7	PERp7
10	GND	GND	22	GND	GND	33	PETn7	PERn7
11	PETp3	PERp3	23	PETp4	PETp4	34	GND	GND
12	PETn3	PERn3	24	PETn4	PERp4			

Signal Descriptions

PETp(x)	PCI Express Transmit Positive signal of (x) pair.
PETn(x)	PCI Express Transmit Negative signal of (x) pair.
PERp(x)	PCI Express Receive Positive signal of (x) pair.
PERn(x)	PCI Express Receive Negative signal of (x) pair.
CREFCLK+/-	Cable REFerence CLocK: Provides a reference clock from the host system to the remote system.
SB_RTN	Side Band ReTurN: return path for single ended signals from remote systems.
CPRSNT#	Cable PReSeNT: Indicates the presence of a device beyond the cable.
PWR	PoWeR: Provides local power for in-cable redriver circuits. Only needed on long cables. Power does not go across the cable.)
PWR_RTN	PoWeR ReTurN: Provides local power return path for PWR pins.
CWAKE#	Cable WAKE
CPERST#	Cable PCI Express Reset

X16 Connector Pin Outs: Target Slot

Name	Pin #	Pin #	Name	
+12V	B1	A1	GND	
+12V	B2	A2	+12V	
+12V	B3	A3	+12V	
GND	B4	A4	GND	
SMCLK	B5	A5	NC	
SMDAT	B6	A6	**REFCLK1+**	
GND	B7	A7	**REFCLK1-**	
+3.3V	B8	A8	NC	
PS_ON#	B9	A9	+3.3V	Mechanical Key
3.3Vaux	B10	A10	+3.3V	

WAKE#	B11	A11	PERST#	
RSVD	B12	A12	GND	
GND	B13	A13	REFCLK2+	
PETp0	B14	A14	REFCLK2-	
PETn0	B15	A15	GND	
GND	B16	A16	PERp0	End of the
PRSNT_X1#	B17	A17	PERn0	x1
GND	B18	A18	GND	Connector
PETp1	B19	A19	RSVD	
PETn1	B20	A20	GND	
GND	B21	A21	PERp1	
GND	B22	A22	PERn1	
PETp2	B23	A23	GND	
PETn2	B24	A24	GND	
GND	B25	A25	PERp2	
GND	B26	A26	PERn2	
PETp3	B27	A27	GND	
PETn3	B28	A28	GND	
GND	B29	A29	PERp3	
RSVD	B30	A30	PERn3	End of the
PRSNT_X4#	B31	A31	GND	x4
GND	B32	A32	RSVD	Connector
PETp4	B33	A33	RSVD	
PETn4	B34	A34	GND	
GND	B35	A35	PERp4	
GND	B36	A36	PERn4	
PETp5	B37	A37	GND	
PETn5	B38	A38	GND	
GND	B39	A39	PERp5	
GND	B40	A40	PERn5	
PETp6	B41	A41	GND	
PETn6	B42	A42	GND	
GND	B43	A43	PERp6	
GND	B44	A44	PERn6	
PETp7	B45	A45	GND	
PETn7	B46	A46	GND	
GND	B47	A47	PERp7	End of the
PRSNT_X8#	B48	A48	PERn7	x8
GND	B49	A49	GND	Connector
PETp8	B50	A50	RSVD	
PETn8	B51	A51	GND	
GND	B52	A52	PERp8	
GND	B53	A53	PERn8	
PETp9	B54	A54	GND	
PETn9	B55	A55	GND	
GND	B56	A56	PERp9	
GND	B57	A57	PERn9	
PETp10	B58	A58	GND	
PETn10	B59	A59	GND	
GND	B60	A60	PERp10	
GND	B61	A61	PERn10	
PETp11	B62	A62	GND	
PETn11	B63	A63	GND	
GND	B64	A64	PERp11	
GND	B65	A65	PERn11	End of the
PETp12	B66	A66	GND	x16
PETn12	B67	A67	GND	Connector

GND	B68	A68	PERp12	
GND	B69	A69	PERn12	
PETp13	B70	A70	GND	
PETn13	B71	A71	GND	
GND	B72	A72	PERp13	
GND	B73	A73	PERn13	
PETp14	B74	A74	GND	
PETn14	B75	A75	GND	
GND	B76	A76	PERp14	
GND	B77	A77	PERn14	
PETp15	B78	A78	GND	
PETn15	B79	A79	GND	
GND	B80	A80	PERp15	
PRSNT_X16#	B81	A81	PERn15	
RSVD	B82	A82	GND	

Endpoint Slot

Pin #	Name	Pin #	Name	
B1	+12V	A1	GND	
B2	+12V	A2	+12V	
B3	+12V	A3	+12V	
B4	GND	A4	GND	
B5	SMCLK	A5	NC	
B6	SMDAT	A6	**REFCLK2+**	
B7	GND	A7	**REFCLK2-**	
B8	+3.3V	A8	NC	
B9	NC	A9	+3.3V	
B10	3.3Vaux	A10	+3.3V	Mechanical Key
B11	WAKE#	A11	PERST#	
B12	RSVD	A12	GND	
B13	GND	A13	REFCLK1+	
B14	PERp0	A14	REFCLK1-	
B15	PERn0	A15	GND	
B16	GND	A16	PETp0	
B17	PRSNT_X1#	A17	PETn0	End of the x1 Connector
B18	GND	A18	GND	
B19	PERp1	A19	RSVD	
B20	PERn1	A20	GND	
B21	GND	A21	PETp1	
B22	GND	A22	PETn1	
B23	PERp2	A23	GND	
B24	PERn2	A24	GND	
B25	GND	A25	PETp2	
B26	GND	A26	PETn2	
B27	PERp3	A27	GND	
B28	PERn3	A28	GND	
B29	GND	A29	PETp3	
B30	RSVD	A30	PETn3	
B31	PRSNT_X4#	A31	GND	End of the x4 Connector
B32	GND	A32	RSVD	
B33	PERp4	A33	RSVD	
B34	PERn4	A34	GND	
B35	GND	A35	PETp4	End of the x8 Connector
B36	GND	A36	PETn4	

B37	PERp5	A37	GND	
B38	PERn5	A38	GND	
B39	GND	A39	PETp5	
B40	GND	A40	PETn5	
B41	PERp6	A41	GND	
B42	PERn6	A42	GND	
B43	GND	A43	PETp6	
B44	GND	A44	PETn6	
B45	PERp7	A45	GND	
B46	PERn7	A46	GND	
B47	GND	A47	PETp7	
B48	PRSNT_X8#	A48	PETn7	
B49	GND	A49	GND	
B50	PERp8	A50	RSVD	
B51	PERn8	A51	GND	
B52	GND	A52	PETp8	
B53	GND	A53	PETn8	
B54	PERp9	A54	GND	
B55	PERn9	A55	GND	
B56	GND	A56	PETp9	
B57	GND	A57	PETn9	
B58	PERp10	A58	GND	
B59	PERn10	A59	GND	
B60	GND	A60	PETp10	
B61	GND	A61	PETn10	
B62	PERp11	A62	GND	
B63	PERn11	A63	GND	
B64	GND	A64	PETp11	
B65	GND	A65	PETn11	
B66	PERp12	A66	GND	
B67	PERn12	A67	GND	
B68	GND	A68	PETp12	
B69	GND	A69	PETn12	
B70	PERp13	A70	GND	
B71	PERn13	A71	GND	
B72	GND	A72	PETp13	
B73	GND	A73	PETn13	
B74	PERp14	A74	GND	
B75	PERn14	A75	GND	
B76	GND	A76	PETp14	
B77	GND	A77	PETn14	
B78	PERp15	A78	GND	
B79	PERn15	A79	GND	
B80	GND	A80	PETp15	End of the
B81	PRSNT_X16#	A81	PETn15	x16
B82	RSVD	A82	GND	Connector

5 Ordering Information

OSS-KIT-EXP-8000-2M

PCIe x8 Gen 2 expansion kit includes a PCIe x8 Gen 2 host cable adapter, a PCIe x8 Gen 2 target cable adapter, a PCIe 2-slot Gen 2 target backplane, and a PCIe x8 2M cable.