ST10F273M
Errata sheet

16-bit MCU with 512 KBytes Flash and 36 KBytes RAM memories

Introduction

This errata sheet describes all the functional and electrical problems known in the ABG silicon version of the ST10F273M.

The major revision of the device can be read in the IDCHIP register (@F07Ch) which is set to 1111h for all these devices.

Functional problems summary

Table 1.   Functional problems of the ST10F273M-ABG

Functional Problem	Short Description
ADC.2	Injected conversion stalling the ADC
BUS.9	Spurious BREQ pulse in slave mode during external bus arbitration phase
C-CAN.1	Concurrent transmission requests in DAR-mode
C-CAN.2	Disabling of transmission request
PWRDN.1	Execution of PWRDN Instruction

1 Functional problems description

1.1 ADC.2 - Injected conversion stalling the ADC

Description

Whenever a new Injection request is issued before the ADDAT2 register has been read by the CPU (i.e. the result of the previous injection request was not read), the ADC is stalled and no further conversions are performed.

Workarounds - Recovery actions

The following actions allows to unlock the ADC module:

1. Read the ADDAT2 register twice at the end of every injected conversion (also prevents stall condition to occur)

2. Disable then re-enable the Wait For Read mode

Detailed analysis

Channel Injection Mode allows the conversion of a specific analog channel (also while the ADC is running in a continuous or auto scan mode) without changing the current operating mode.
The following main points need to be highlighted:

●   Wait for ADDAT Read Mode is needed in order for the ADC Channel Injection mode to properly operate

●   At the end of the Injected conversion the data will be available in the alternate result register ADDAT2 and a Channel Injection Complete Interrupt request will be generated (ADEIR Flag)

●   If the temporary data register used for ADDAT2 Read Mode is full, the respective next conversion (standard or Injected) will be suspended. The temporary register can hold data for ADDAT (standard Conversion) or for ADDAT2 (injected conversion)

When the temporary data register used for ADDAT2 Read Mode is full and a new Injection request is issued then the new converted value is stored into a temporary data register until the previous one is read from ADDAT2.

For a correct functionality as soon as ADDAT2 register is read then the last converted value should be moved from temporary register to ADDAT2 and the ADEINT interrupt request should be issued. This would allow the CPU to read the last converted value. See *Figure 1*.

In the real situation as soon as ADDAT2 register is read then the last converted value is correctly moved from temporary register to ADDAT2 but **the ADEINT interrupt request is not received by the Interrupt Controller (see *Figure 2*).** As a consequence the CPU/PEC will never know that a new converted value is ready to be read in ADDAT2 register and therefore at the following injection request the ADC will fill the temporary register again (without generating any ADEINT interrupt request) and then will stall the ADC for any further conversion. The ADC will stay in the "wait for read ADDAT2 register" condition forever.
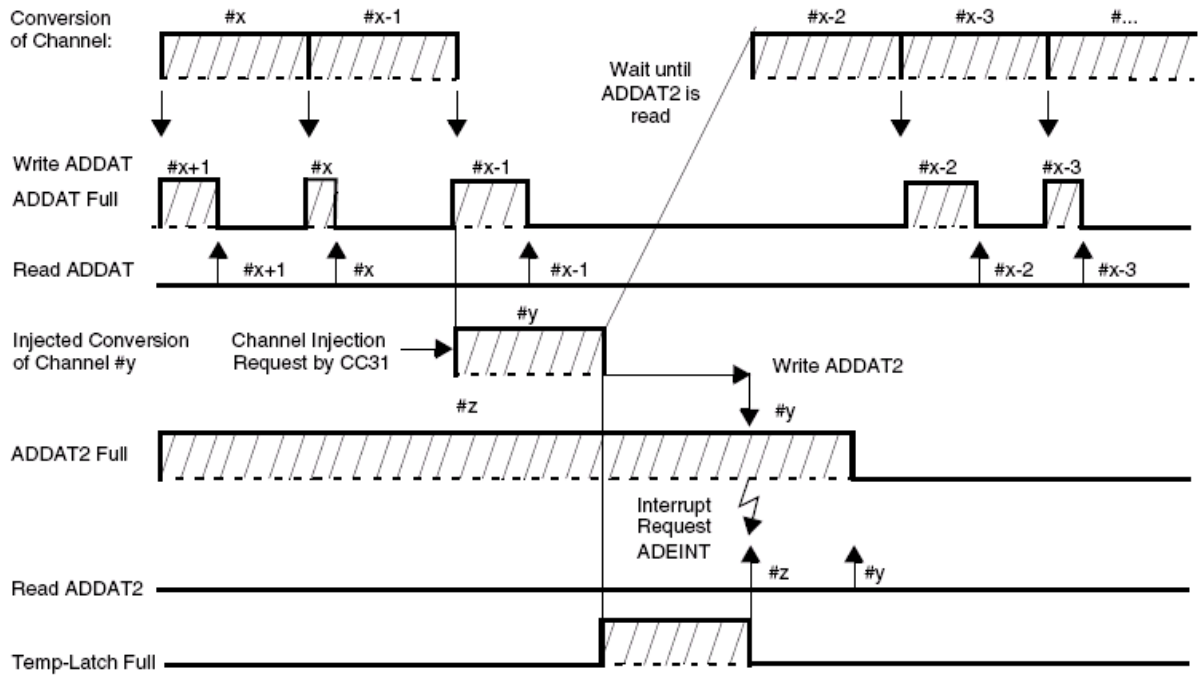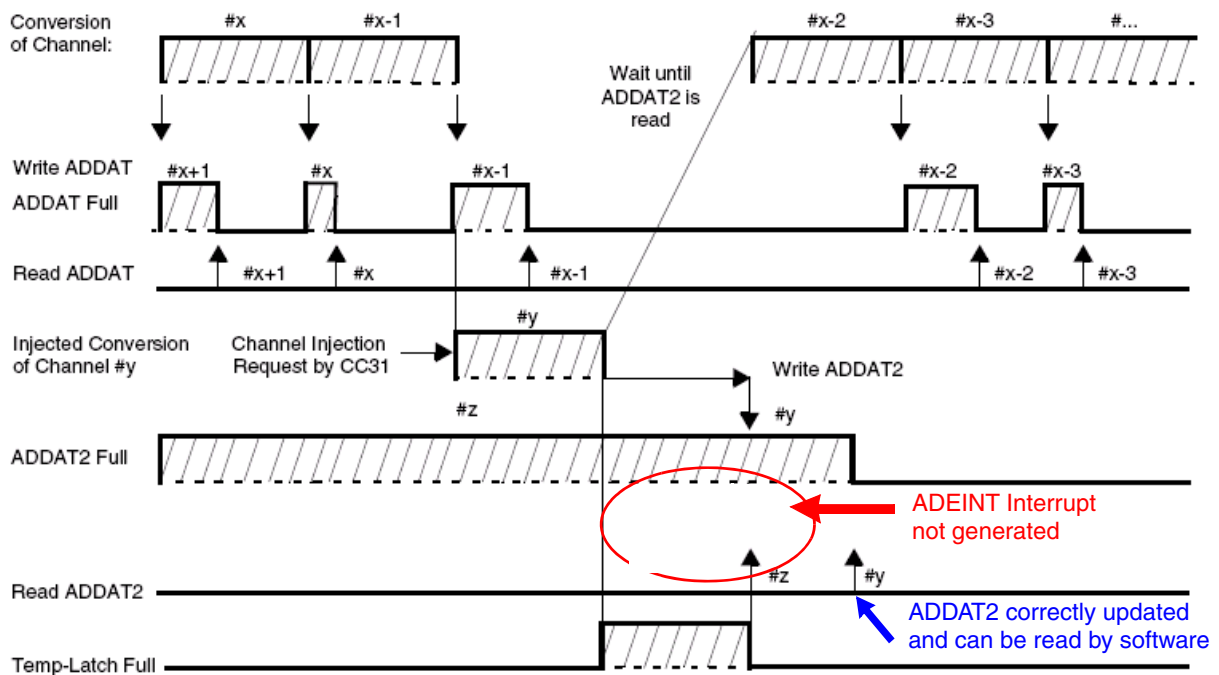
Figure 1.   ADC injection theoretical operation

Figure 2.   ADC injection actual operation

Application conditions

In an application, all the following conditions are needed to reach this state:

● Injection requests are hardware triggered (via CAPCOM channel 31 -CC31-)

● The result of injected conversion are read via a PEC transfer (prevents from reading twice ADDAT2 by software)

● A high level task is disabling the PEC transfer for a long time (2 analog conversions + interval between 2 injection requests)

Therefore ensuring, at application level, that no task can disable interrupts for a time such than 2 injection requests can be issued before a read operation is performed prevents the locking situation to occur.

1.2 BUS.9 - Spurious $\overline{\text{BREQ}}$ pulse in slave mode during external bus arbitration phase

When using external bus arbitration via HOLD-function with the ST10F272M/ST10F273M configured as a slave, sporadic bus errors may occurs.

After the slave has been granted the bus, the slave deactivates $\overline{\text{BREQ}}$ sporadically for a short time, even though the bus access of the slave has not been completed. The master then starts its own bus access, leading to a bus conflict between master and slave.

Workaround:

In order not to produce any spurious $\overline{\text{BREQ}}$ pulse during a Slave External Bus Arbitration Phase, it is necessary to guarantee that the distance between the $\overline{\text{HOLDA}}$ assertion (Bus Acknowledge from Master device) and the following $\overline{\text{HOLD}}$ falling edge (Bus Request from Master) is greater than three clock cycles.

This can be implemented by delaying the $\overline{\text{HOLD}}$ signal with a RC circuit as shown in the *Figure 3* below.

Figure 3.   ST10 in slave mode
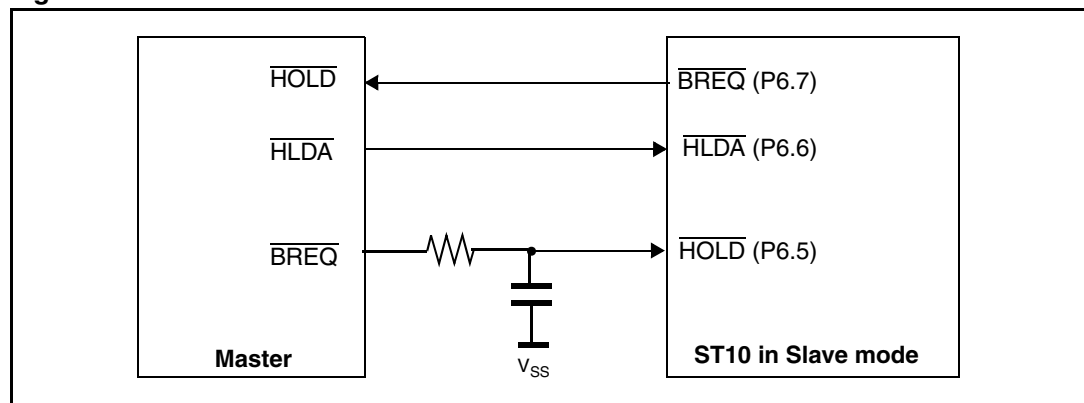
1.3   C-CAN.1 - Concurrent transmission requests in DAR-mode

Description:

When the C_CAN is configured to work in DAR-mode (Disable Automatic Retransmission) and the host requests the transmission of several messages at the same time, only two of these messages will be transmitted. For all other requested transmit messages, the TxRqst bits will be reset, but no transmission will be started, NewDat and IntPnd will be left unchanged. For the two messages that are transmitted, the TxRqst and NewDat bits will be reset and, if enabled by TxIE, IntPnd will be set.

The normal operation mode (DAR = 0) is not affected by this phenomenon.

Workaround:

The DAR-mode is intended to support time triggered operation (TTCAN level 1), where a message may be transmitted only in its dedicated time window. It would be an error to request the transmission of several messages at the same time. So no workaround is necessary for TTCAN applications.

The progress of a requested transmission can be monitored by checking the message object's TxRqst and NewDat [optionally IntPnd] bits. In DAR-Mode, a message that was requested to be transmitted, but that was not transmitted either because the transmission was disturbed or because the transmission was not started needs to be requested again.

1.4   C-CAN.2 - Disabling of the transmission request

Description:

When the host disables the pending transmission request of the message object with the lowest priority (number 32 in the default implementation) in the short time window where the message handler state machine has prepared the transmission of the message, but before the transmission has actually started, then the transmission request of this message object may remain stuck at disabled even if the host immediately re-enables it. Reading the transmission request bit of this message object will not show that it is stuck at disabled. This can only happen when this message object is the only one with a pending transmission request.

If the transmission request is stuck at disabled, it will be re-enabled by the first activity detected on the CAN bus or by setting the transmission request of any other message object.

The other message objects are not affected by this phenomenon.

Workaround:

Generally, it is not necessary to disable the transmission request of a message object. If the message object is to be used for another message, it is sufficient to prepare the new content for this message object in the CPU interface register (Identifier, DLC, Data, with TxRqst and NewDat [optionally TxIE] bits) and to transfer this content into the message object. The new content will be transmitted at the next opportunity, not influenced by a possibly ongoing transmission of the previous content of the same message object.

1.5 PWRDN.1 - Execution of PWRDN Instruction

When instruction PWRDN is executed while pin $\overline{\text{NMI}}$ is at a high level (if PWDCFG bit is cleared in SYSCON register) or while at least one of the port 2 pins used to exit from Power Down mode (if PWDCFG bit is set in SYSCON register) is at the active level, Power Down mode is not entered, and the PWRDN instruction is ignored.

However, under the conditions described below, the PWRDN instruction is not ignored, and no further instructions are fetched from external memory, i.e. the CPU is in a quasi-idle state.

This problem only occurs in the following situations:

a) The instructions following the PWRDN instruction are located in an external memory, and a **multiplexed bus** configuration **with memory tristate waitstate** (bit MTTCx = 0) is used.

Or

b) The instruction preceding the PWRDN instruction **writes** to external memory or an XPeripheral (XRAM, CAN, etc.), and the instructions following the PWRDN instruction are located in external memory. In this case, the problem occurs for any bus configuration.

Note: *The on-chip peripherals are still working correctly, in particular the Watchdog Timer, if not disabled, resets the device upon an overflow. Interrupts and PEC transfers, however, cannot be processed. In case $\overline{\text{NMI}}$ is asserted low while the device is in this quasi-idle state, Power Down mode is entered.*

No problem occurs if the $\overline{\text{NMI}}$ pin is low (if PWDCFG = 0) or if all P2 pins used to exit from Power Down mode are at inactive level (if PWDCFG = 1): the chip normally enters Power Down mode.

Workaround:

Ensure that no instruction that writes to external memory or to an XPeripheral precedes the PWRDN instruction, otherwise insert a NOP instruction in front of PWRDN. When a multiplexed bus with memory tristate wait state is used, the PWRDN instruction must be executed from internal RAM or XRAM.

2 Deviations from DC/AC specification

AC Timings

One limitation have been found:

● **T$_{LOCK}$**: PLL Lock-in time for x10 multiplication factor is 300us instead of 250us.

3 Documentation update - Modification of features

References:

- – ST10F273M Preliminary Data Sheet, Revision 1, April 2007
- – ST10F276 User Manual (UM404), Revision 1, March 2007

4   Revision history

Table 2.   Document revision history

Date	Revision	Changes
June-2007	1	Initial release.
24-Sep-2013	2	Updated Disclaimer.

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