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GFK-2241A

IMPORTANT PRODUCT INFORMATION

READ THIS INFORMATION FIRST

Product: IC693 CPU Module with Firmware Release 10.71

IC693CPU363-BH

Introduction

This document contains information that is not available in any other publication; therefore, we recommend you save it for future reference.

Version 10.71 of IC693CPU363 firmware provides an enhancement to the Modbus RTU master serial protocol on ports 1 and 2 that supports 32-bit register data. In addition, two problems are resolved by version 10.71. See “Problems Resolved by this Revision” on page 2 for details.

Hardware Identification

The following table shows the revision level of the circuit boards used in the current version of these CPUs.

CPU Catalog Number	*Circuit Board ID*	*Circuit Board Version*
IC693CPU363-BH	CX3A1	44A739579-G01R05 or later

Firmware Upgrade Kits

This firmware upgrade is optional. Applications that use the Modbus RTU master protocol to exchange 32-bit register data with a remote terminal unit should be upgraded to firmware version 10.71. Applications affected by the problems described in “Problems Resolved by this Revision” on page 2 should also be upgraded to version 10.71.

All previous versions are capable of being upgraded to version 10.71.

To upgrade a CPU363 to the latest firmware version (10.71), you must purchase the field upgrade kit 44A747766-G07 or download it at no charge from the web at http://www.geindustrial.com/cwc/gefanuc/support/ControllersIO/s9030-u.htm. Firmware upgrades require the IC690ACC901 Miniconverter and Cable Kit.

Firmware Identification

Board	*Main Firmware Version*	*Boot Firmware Version (No Change)*
CX3A1	10.71 (45A2)	9.00 (33A1)
ES3A1	10.11 (49A1)	2.00 (30A1)

New Features

Modbus RTU Master

Version 10.71 of CPU363 firmware adds support for 32-bit register data to the Modbus RTU master serial protocol. See *Modbus RTU Master Communications*, GFK-2220C or later for details.

Functional Compatibility

IC693CPU363 can be configured and programmed with any of the following PLC programming products: CIMPLICITY Machine Edition Logic Developer – PLC, VersaPro™, CIMPLICITY Control, or Logicmaster™ 90-30.

The following or newer versions are required to use C programming or SFC subroutines:

- CIMPLICITY Machine Edition Logic Developer – PLC version 2.11
- VersaPro version 1.11
- CIMPLICITY Control version 2.00
- Series 90-30 C toolkit version 4.00 or later must be used for C programming.

Logicmaster 90-30 software compatibility:

- Version 9.01 or later is required to configure a CPU363.
- Version 9.02 or later is required to use features in CPU363 firmware release 9.00 or later.

Problems Resolved by this Revision

Subject	*Description*
Using Port Setup COMMREQs to alternate between Serial I/O and SNP may cause the serial daughterboard to reset.	In previous versions of IC693CPU363 firmware, an Option Module Software Failure fault may occur in the PLC fault table when serial port 1 or 2 is configured for SNP, and Port Setup COMMREQ commands from the application are used to alternate the port between Serial I/O and SNP. This issue is corrected in version 10.71.
SNP slave protocol on Port 1 may fail to re-attach to the master.	During continuous communication on port 1 and 2 at 19,200 bps, SNP slave on port 1 may occasionally report protocol sequence errors and then disconnect temporarily. In version 10.70 of IC693CPU363 firmware, an SNP master attached to port 1 would occasionally be unable to re-attach after a disconnect. When this occurred, the PLC would need to be powered off and on again to re-establish communications. This issue is corrected in version 10.71.
Serial ports 1 and 2 always disconnect from SNP master when hardware configuration is downloaded.	In previous versions of IC693CPU363 firmware, a download of hardware configuration always forced both port 1 and port 2 to remove the old configuration and install the new configuration. This caused the ports to disconnect from an SNP master after every configuration download. In version 10.71 firmware, the SNP disconnect occurs only when: 1. The hardware configuration for either port 1 or port 2 has changed; or 2. The active settings for either port 1 or port 2 have been modified by a port setup COMMREQ. Note that port 1 or port 2 settings that were modified by a port setup COMMREQ may be restored to the configured values by re-downloading the hardware configuration. This may be done only while the CPU is in STOP mode.
Daughterboard version number displayed incorrectly.	In previous versions of IC693CPU363 firmware, the Daughterboard Firmware Version displayed by CIMPLICITY Machine Edition Logic Developer – PLC is incorrect (for example, 16.16 rather than 10.10). This issue is corrected in version 10.71.
Firmware update may fail after following power-up with Clear M/T and a write to flash	When Clear M/T is pressed on an attached Hand-Held Programmer during power-up and then the user performs a write to flash, attempting to upgrade CPU firmware through the power supply serial port may fail. Cycling power on the PLC will enable the upgrade to succeed.

Restrictions and Significant Open Issues

Subject	*Description*
CPU363 ports 1 and 2 do not handle parity errors in accordance with the SNP specification.	The SNP specification requires both slave and master devices to reply to messages that contain parity errors with a 2-byte NACK message indicating a BCC or Parity Error (code 0). The NACK triggers a re-try transmission from the communications partner. For CPU363 ports 1 and 2 however, parity errors are fatal. The ports do not send the NACK message as expected, and the SNP master must send a new Attach message to re-establish communications. During the time between the parity error and the new Attach message, CPU363 ports 1 and 2 do not respond to COMMREQs from the PLC application. For example, attempting to use a serial port setup COMMREQ to change the parity setting will fail if the first Attach message with parity that is different from the hardware configuration arrives at the port before the COMMREQ. If the master re-tries Attach messages more often than every 12 seconds, the COMMREQ will not be processed until the master stops sending Attach messages or the SNP cable is disconnected.
IC693CPU350, 351, 352, 360, 363, 364: Timing issue with ALG220/221 modules may result in incorrect %AI values read by CPU.	With IC693ALG220/221-F and earlier modules, the actual %AI values from the card may exhibit erratic behavior. This issue was resolved in modules with catalog number revision -G and later. Certain current or voltage levels applied to these modules that are within the configured input range could cause the %AI values to be reported incorrectly. The problem stems from the use of particular opto-couplers, which may exhibit timing issues with the listed CPU modules. IC693CPU341, 331, 321, 313, and 311 have not exhibited this timing problem reading %AI values.
Series 90-30 CPUs will generate a fatal fault if a ladder containing DOIO function block calls to a smart module is repeatedly placed in RUN then STOP mode.	When a Series 90-30 ladder program contains a call to a DOIO function block, the CPU may run out of system memory. This can occur when the PLC transitions between RUN and STOP modes several times. To clear the fault condition, store the hardware configuration to the PLC. This will free system memory, and the PLC will resume normal operation.
Series 90-30 CPUs may generate a fatal fault during store of folders with large configurations	A Series 90-30 PLC CPU may generate a fatal fault during a store of a folder with an especially large hardware configuration and/or program logic size. This problem can be minimized by clearing PLC memory before attempting the store and by storing hardware configuration and program logic separately.
PID Integral Contribution	The PID Integral Contribution is not calculated correctly when an integral rate of 0 or 1 is used.
Reading corrupted data from FLASH memory may cause a Watch Dog Time-out	If data in FLASH memory becomes corrupted, the PLC Watch Dog Timer may be triggered. This can be corrected by storing the data to FLASH.
Series 90-30 CPUs may generate a fatal fault when configuring a module with the HHP following a Maximum Size store to the PLC.	A Series 90-30 PLC CPU may generate a FATAL fault when the user attempts to configure a module with the Series 90-30 Hand-Held Programmer following a store of a folder with an especially large hardware configuration and/or program logic size.

Documentation

Instructions for using this CPU can be found in the latest versions of the following manuals. These manuals are available at http://www.gefanuc.com/support/plc/s9030.htm in the Manuals section.

IC693 Installation and Hardware Manual, GFK-0356
IC693 PLC System Manual, GFK-1411
IC693 PLC CPU Instruction Set Reference Manual, GFK-0467
Modbus RTU Master Communications, GFK-2220
Serial Communications User's Manual, GFK-0582

IC693CPU363 Data

CPU Type	Single slot CPU module
Total Baseplates per System	8 (CPU baseplate + 7 expansion and/or remote)
Load Required from Power Supply	890 milliamps from +5 VDC supply
Processor Speed	25 MHz
Processor Type	80386EX
Typical Scan Rate	0.22 milliseconds per 1K of logic (Boolean contacts)
User Memory (total)	240K (245,760) Bytes. Note: Actual size of available user program memory depends on the amounts configured for the %R, %AI, and %AQ configurable word memory types (described below).
Discrete Input Points - %I	2,048
Discrete Output Points - %Q	2,048
Discrete Global Memory - %G	1,280 bits
Internal Coils - %M	4,096 bits
Output (Temporary) Coils - %T	256 bits
System Status References - %S	128 bits (%S, %SA, %SB, %SC - 32 bits each)
Register Memory - %R	Configurable in 128 word increments, from 128 to 16,384 words with DOS programmer, and from 128 to 32,640 words with Windows programmer Ver. 2.2 or later, or VersaPro version 1.0 or later.
Analog Inputs - %AI	Configurable in 128 word increments, from 128 to 8,192 words with DOS programmer, and from 128 to 32,640 words with Windows programmer Ver 2.2 or later, or VersaPro version 1.0 or later.
Analog Outputs - %AQ	Configurable in 128 word increments, from 128 to 8,192 words with DOS programmer, and from 128 to 32,640 words with Windows programmer Ver. 2.2 or later, or VersaPro version 1.0 or later.
System Registers (for reference table viewing only; cannot be referenced in user logic program)	28 words (%SR)
Timers/Counters	>2,000 (depends on available user memory)
Shift Registers	Yes
Built-in Serial Ports	3 (one uses connector on PLC power supply). Supports SNP/SNPX slave (on all three ports) and RTU slave and Serial I/O (on Ports 1 and 2). Requires CMM module for CCM and PCM module for RTU master.
Communications	*LAN* – Supports multidrop. Also supports Ethernet, FIP, Profibus, GBC, GCM, and GCM+ option modules.
Override	Yes
Battery Backed Clock	Yes
Interrupt Support	Supports the periodic subroutine feature.
Type of Memory Storage	RAM and Flash
PCM/CCM Compatibility	Yes
Floating Point Math Support	Yes, firmware-based