DIGITAL-LOGIC
smart embedded computers

TECHNICAL USER'S MANUAL FOR:

smartModule 480 BUS

INTEGRATION MANUAL

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ATTENTION:
All information in this manual and the product are subject to change without prior notice.

REVISION HISTORY:

Prod.-Serialnumber: From: To:	smart-bus Version	BIOS Version	Doc. Version	Date/Vis:	Modification: Remarks, News, Attention:
			V1.0	***09.2000***	***Initial Version***
	V2.0		V1.01	10.2000	Min. Modifikations, ICP Port defined
	V2.1		V1.1	12.2000 STP	smart design dimensions, 480bus definitions, schematic added
	V2.2		V1.2f	01.2001 KUF	SMGX modifications, new DK schematic, typo errors, application tips, etc
	V2.2		V1.3	04.2001 STP	smart dimensions and 480bus signals corrected, new schematics
	V2.2		V1.4	04.2001 STP	Pin1 position smart480 connector corrected
	V2.2		V1.5	06.2001 STP	AC97 codec taken out, new schematic of the DK,
	V2.2		V1.6	09.2001 STP	New cooler dimensions
	V2.2		V1.7	08.2003 KUF	LCD-Bus to 3.3V only corrected.

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1 PREFACE

This manual is for integrators of systems based on the smartModule480 family. It contains information on hardware requirements, interconnections, and details of how to program the system. The specifications given in this manual were correct at the time of printing; advances mean that some may have changed in the meantime.

1.1 How to use this manual

This manual is written for the original equipment manufacturer (OEM) who plans to build computer systems based on the system on chip units. It provides instructions for designing, installing and configuring the unit, and describes the system and setup requirements.

1.2 Disclaimer

DIGITAL-LOGIC AG makes no representations or warranties with respect to the contents of this manual and specifically disclaims any implied warranty of merchantability or fitness for any particular purpose. DIGITAL-LOGIC AG shall under no circumstances be liable for incidental or consequential damages or related expenses resulting from the use of this product, even if it has been notified of the possibility of such damage. DIGITAL-LOGIC AG reserves the right to revise this publication from time to time without obligation to notify any person of such revisions

1.3 Who should use this product

- Electronic engineers with know-how in PC-technology.
- Without electronic know-how we expect you to have questions. This manual assumes, that you have a general knowledge of PC-electronics.
- Because of the complexity and the variability of PC-technology, we can't give any warranty that the product will work in any particular situation or combination.
- Pay attention to the electrostatic discharges. Use a CMOS protected workplace.
- Power supply OFF when you are working on the board or connecting any cables or devices.

This is a high technology product.
You need know-how in electronics and PC-technology to install the system !

1.4 Limited Warranty

DIGITAL-LOGIC AG warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from DIGITAL-LOGIC AG, Switzerland. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, DIGITAL-LOGIC AG will repair or replace, at its discretion, any defective product or part at no additional charge, provided that the product is returned, shipping prepaid, to DIGITAL-LOGIC AG. All replaced parts and products become property of DIGITAL-LOGIC AG.

Before returning any product for repair, customers are required to contact the company.

This limited warranty does not extend to any product which has been damaged as a result of accident, misuse, abuse (such as use of incorrect input voltages, wrong cabling, wrong polarity, improper or insufficient ventilation, failure to follow the operating instructions that are provided by DIGITAL-LOGIC AG or other contingencies beyond the control of DIGITAL-LOGIC AG), wrong connection, wrong information or as a result of service or modification by anyone other than DIGITAL-LOGIC AG. Neither, if the user has not enough knowledge of these technologies or has not consulted the product manual or the technical support of DIGITAL-LOGIC AG and therefore the product has been damaged.

Except, as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose, and DIGITAL-LOGIC AG expressly disclaims all warranties not stated herein. Under no circumstances will DIGITAL-LOGIC AG be liable to the purchaser or any user for any damage, including any incidental or consequential damage, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

1.5 smart Support Request Form (smart-SRF)

1. Send this SRF with your problem description to:

DIGITAL-LOGIC AG
smartModule DesignIn Center
Nordstr. 11/F
CH-4542 Luterbach (SWITZERLAND)
Fax: ++41 32 681 58 01
E-Mail: support@digitallogic.com
Internet www.digitallogic.com

Support request form (fill in and send via fax to DIGITAL-LOGIC AG support center):

SRF No:	**S118_____**		**Date:**	
Customer name:			Customer company:	
Customer tel.no.:			Customer e-mail:	
Customers Address:			Customers country:	
smart type:	SM		Processing date:	
Request type:	Support report:		Operating system:	
	DesignIn aid:		OS version:	V___.____
	BIOS adaption:		BIOS version:	V___.____
	Manual correction:			
	Others:			

Problem description:
Solution / answer (will be filled in by DIGITAL-LOGIC AG smart DesignIn Center):

Support date:			Support statistics:	
Support sign:			Comment:	
Support cost:	yes no		Offered costs for serving design support:	CHF/USD/DEM:
DesignIn no.:			Effective time / costs:	

1.6 smart DesignIn Center (smart – DIC)

DIGITAL-LOGIC AG offers a DesignIn support from a specialized engineering group in the smart DesignIn Center (smart – DIC). To initialize a DesignIn Support, please fill in the smart-SRF form. The DesignIn Support can be offered in each phase of a DesignIn procedure. Only the ordered support value will be charged. The charge fees are as follow:

Design Phase	No.	Support type	Fee	Charged
Evaluation	01	Consultation	CHF 200.--	per hour
	02	Training	CHF 200.--	per hour
	03	Design of the customers specification	CHF 150.--	per hour
Schematics	10	Consultation	CHF 200.--	per hour
	11	Design of the schematics	CHF 150.--	per hour
	12	Review / inspection of customers schematics	CHF 300.--	per sheet
	13	Development of circuits / schematics	CHF 200.--	per hour
Layout	20	Consultation	CHF 200.--	per hour
	21	Design of the layout	CHF 150.--	per hour
	22	Review / inspection of customers layout	CHF 300.--	per sheet
	23	Development of circuits / layout	CHF 200.--	per hour
BIOS	30	Consultation	CHF 200.--	per hour
	31	Modification / test of the BIOS sourcecode	CHF 1500.--	per day
	32	Review / inspection of customers software	CHF 300.--	per hour
	33	Development of software	CHF 200.--	per hour
Prototype	40	Consultation	CHF 200.--	per hour
	41	Test of customers system	CHF 1200.--	per day
	42	Review / inspection of customers system	CHF 300.--	per hour
	43	Development of test entvironment	CHF 200.--	per hour

All costs are payable in advance.

2 OVERVIEW

The following information is only a summary. Please refer to the product manual to receive the latest information of a specific smartModule product.

2.1 Features

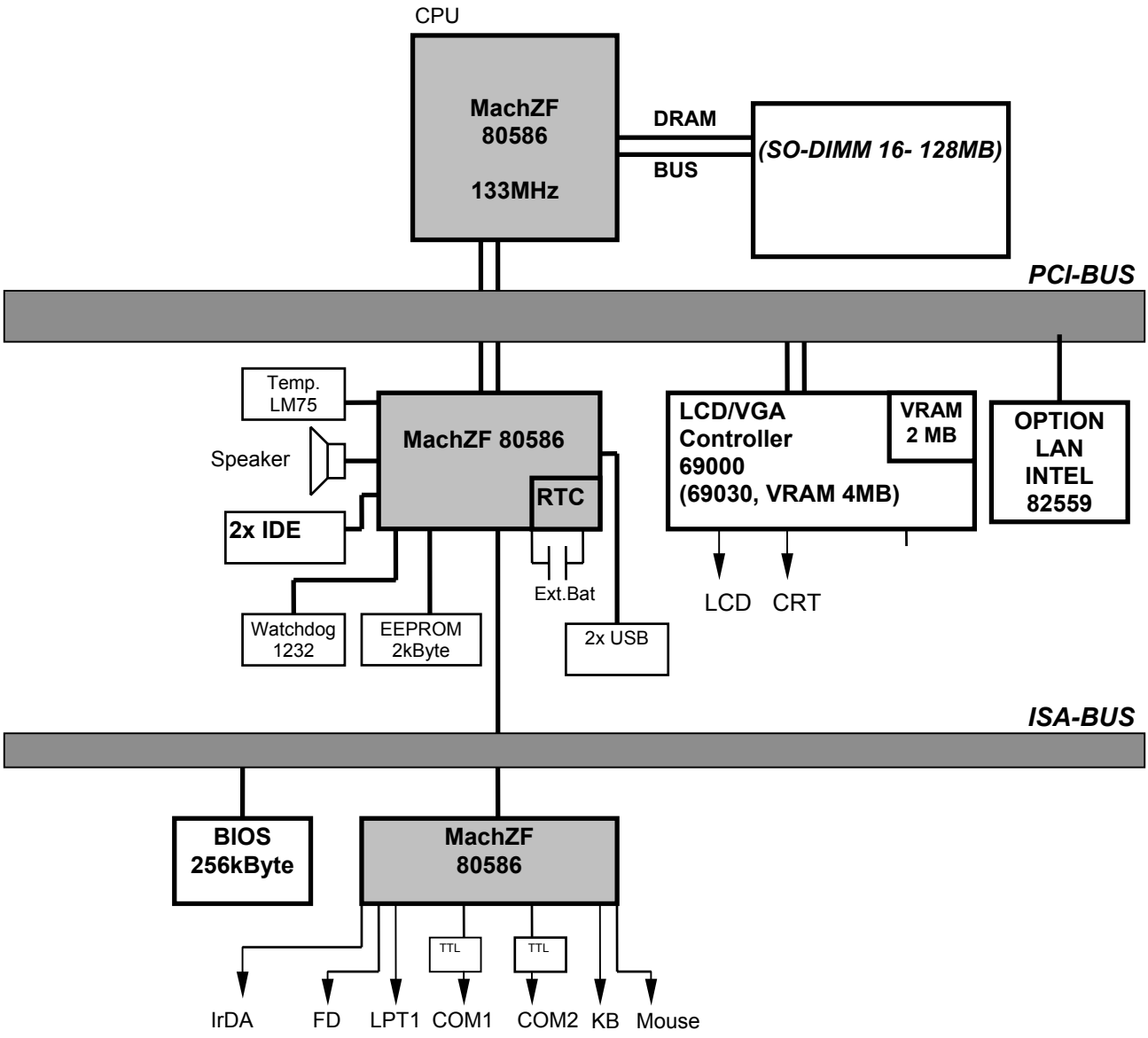
The smartModule is a miniaturized PC system on chip unit incorporating the major elements of a PC/AT compatible computer. It includes standard PC/AT compatible elements, such as:

- Powerful Pentium P5/P3, GEODE or 80586 core
- BIOS Flash AMD 29F010 or ATMEL 29C020
- SODIMM socket for 16 - 128MB
- AT Timers
- AT DMA
- Real-time clock
- 2k EEPROM
- LPT1
- COM1and COM2 (as TTL's)
- IrDA interface
- Speaker interface
- AT-keyboard interface
- PS/2 mouse interface
- 2x USB V1.0
- Floppydisk interface
- 2x ATA-IDE harddisk interface
- VGA/LCD video controller 3.3V (5V)
- JTAG Incircuit-Testport
- Embedded smartBUS480
- Support for ATX-Powermanagement
- 3.3V CPU- CORE- power supply (switched mode)
- PCI (33MHz) bus and ISA-bus (8MHz)
- External SDRAM expansion with 66/100MHz
- Remote BIOS function for control over serial link with host

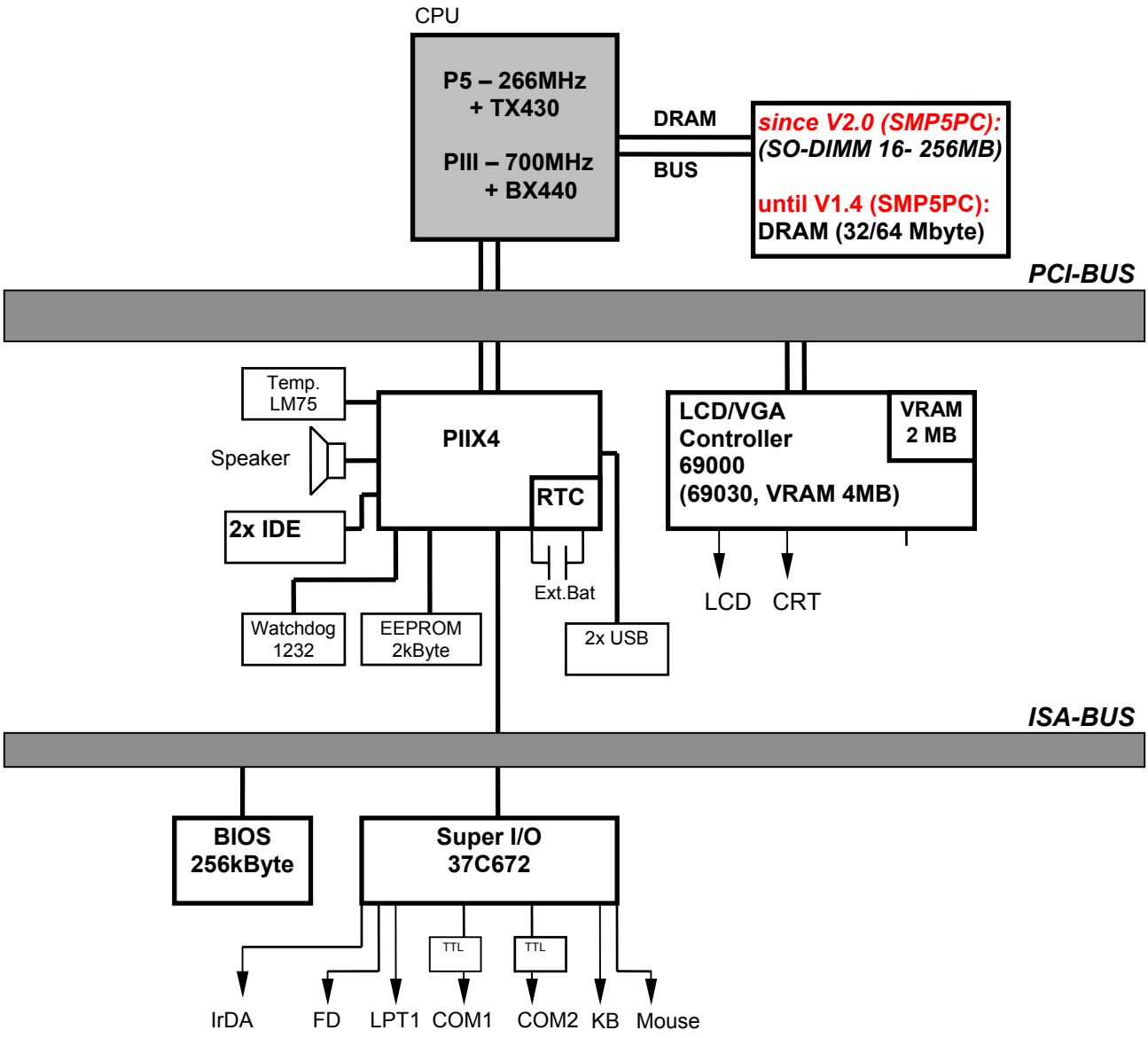
2.2 Optional features (must be ordered separately)

- SMGXPCX and SM586PCX with onboard module 100Base-T LAN
- SMGXPC with soundfunktion (onboard AC97 codec), new since integration manual version V1.5

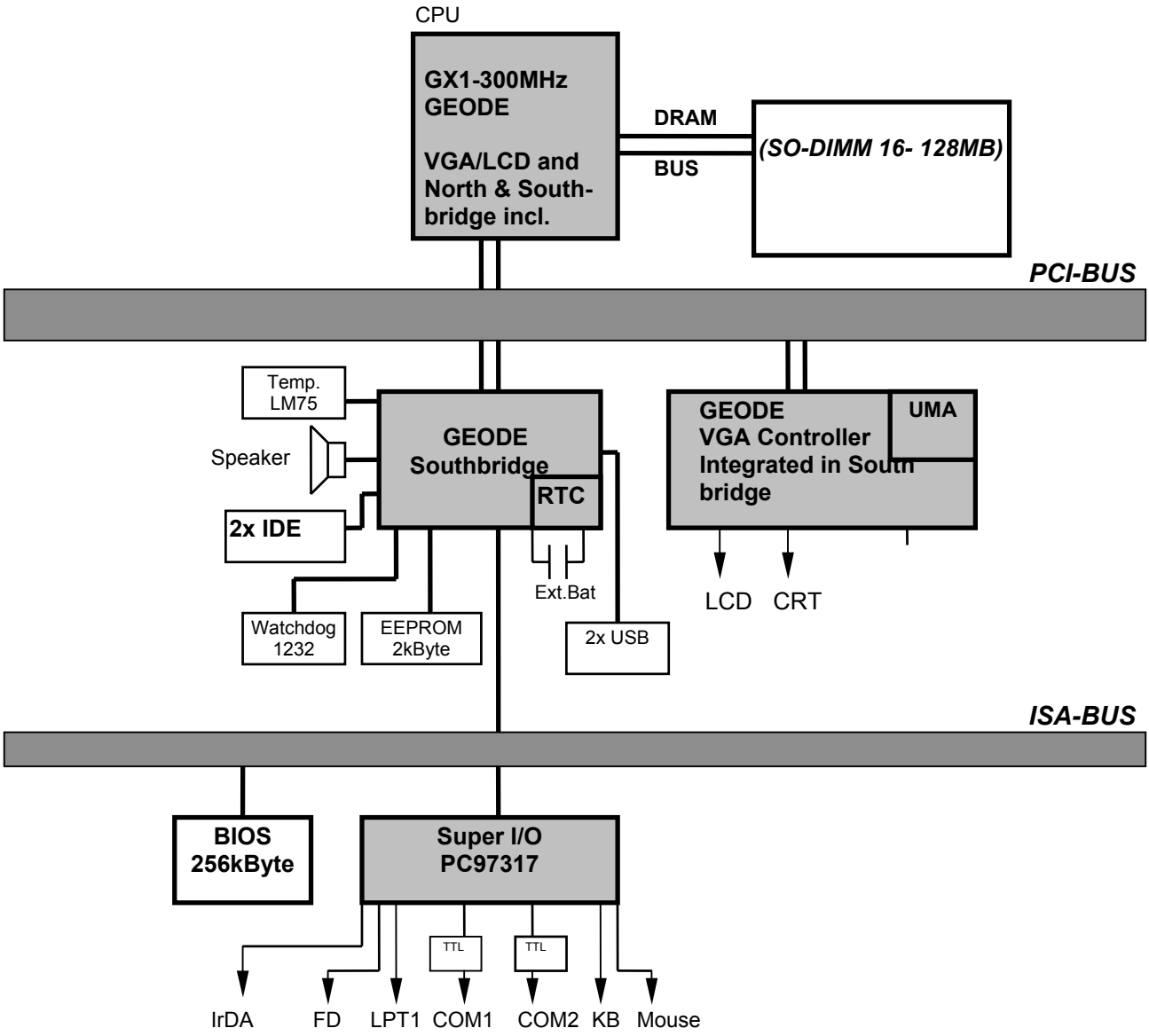
2.3 SM586PC block diagram



2.4 SMP5PC & SMP3PC block diagram



2.5 SMGXPC block diagram



2.6 Specifications

CPU:	
CPU:	ZF 80586-133MHz Pentium P5 166/266MHz Pentium PIII 400-700MHz GEODE 300MHz
Mode:	Real / Protected
Compatibility:	8086 – 80386
1. Level Cache:	16 & 16kByte write-back
Word Size:	64 Bits
Physical Addressing:	32 lines
Virtual Addressing:	64 Mbytes
Clock Rates:	Depending from the modultype
Math. Coprocessor:	
	Available on the CPU
Power Management:	
available	Defined by the BIOS
DMA:	
8237A comp.	2 channels 8 Bits
Interrupts:	
8259 comp.	8 + 2 levels PC compatible
Timers:	
8254 comp.	3 programmable counter/timers
Memory:	
DRAM	SODIMM 144pin holder (16 – 128Mbyte), externally expandable For TX and BX chipset up to 256MB or higher depending on market
Video:	
Controller:	80586, P5 and P3: 69000 (69030) PCI-BUS CRT: 2Mbyte (4MB) LCD: 36Bit up to 1024 x 768 x 256 colors Panel: TFT up to 36Bit, STN, EL Plasma GEODE: CRT: up to 2Mbyte **UMA (Unified Memory Architecture)** LCD: 18Bit TFT LCD Panel: TFT 18Bit

Mass Storage:

FD:	Floppy disk interface, for max. 2 floppies
HD:	2x IDE interface, AT - Type, for max. 4 harddisks

Standard AT Interfaces:

Serial:

Device Name	FIFO	Std.-IRQs	Addr.	Signals:	Remarks
COM1	yes	IRQ4	3F8		
COM2	yes	IRQ3	2F8		

(Baudrates: 50 – 115 KBaud programmable)

Parallel:	LPT1 printer interface, Modes: SPP (output) , EPP (bidir.)
Keyboard:	AT- or PS/2-keyboard
Mouse:	PS/2
Speaker:	0.1 W output drive
RTC:	Integrated into the PIIX4 or SuperIO with CMOS-RAM 256byte
Backup current:	<5 µA at 3.0V
Battery:	Not assembled, must be connected external

Supervisory:

Watchdog:	LTC1232 with power-fail detection, strobe time max. 1 sec.

BUS:

ISA:	IEEE-996 standard bus
Clock:	8 MHz
PC/104plus	IEEE-996 standard bus, buffered
Clock:	33 MHz defined by the design
USB	Defined by the chipsset
DRAM	66Mhz or 100MHz (Pentium-III), defined by the chipset

Power Supply:

Working:	5 Volts ± 5%, 3.3V onboard switch mode regulator
Power Rise Time:	> 100µs (0V --> 4,75V)

Physical Characteristics:

Dimensions:	Length:	85 mm +/- 0.1mm
	Depth:	66 mm +/- 0.1mm
	Height:	12 mm +/- 0.2mm (with 5mm bus connectors) + 12 mm (active or passive cooler)
Weight:	90 gr / 9 ounces	
PCB Thickness:	1.6 mm / 0.0625 inches nominal	
PCB Layer:	Multilayer	

Operating Environment:

Relative Humidity:	5 - 90% non condensing
Vibration:	5 to 2000 Hz
Shock:	10 G
Temperature:	Refer to the product manual

EMI / EMC (IEC1131-2 refer MIL 461/462):	
ESD Electro Static Discharge:	IEC 801-2, EN55101-2, VDE 0843/0847 Part 2 metallic protection needed separate Ground Layer included 15 kV single peak
REF Radiated Electromagnetic Field:	IEC 801-3, VDE 0843 Part 3, IEC770 6.2.9. not tested
EFT Electric Fast Transient (Burst):	IEC 801-4, EN50082-1, VDE 0843 Part 4 250V - 4kV, 50 ohms, Ts=5ns Grade 2: 1KV Supply, 500 I/O, 5Khz
SIR Surge Immunity Requirements:	IEC 801-5, IEEE587, VDE 0843 Part 5 Supply: 2 kV, 6 pulse/minute I/O: 500 V, 2 pulse/minute FD, CRT: none
High-frequency radiation:	EN55022

Any information is subject to change without notice.

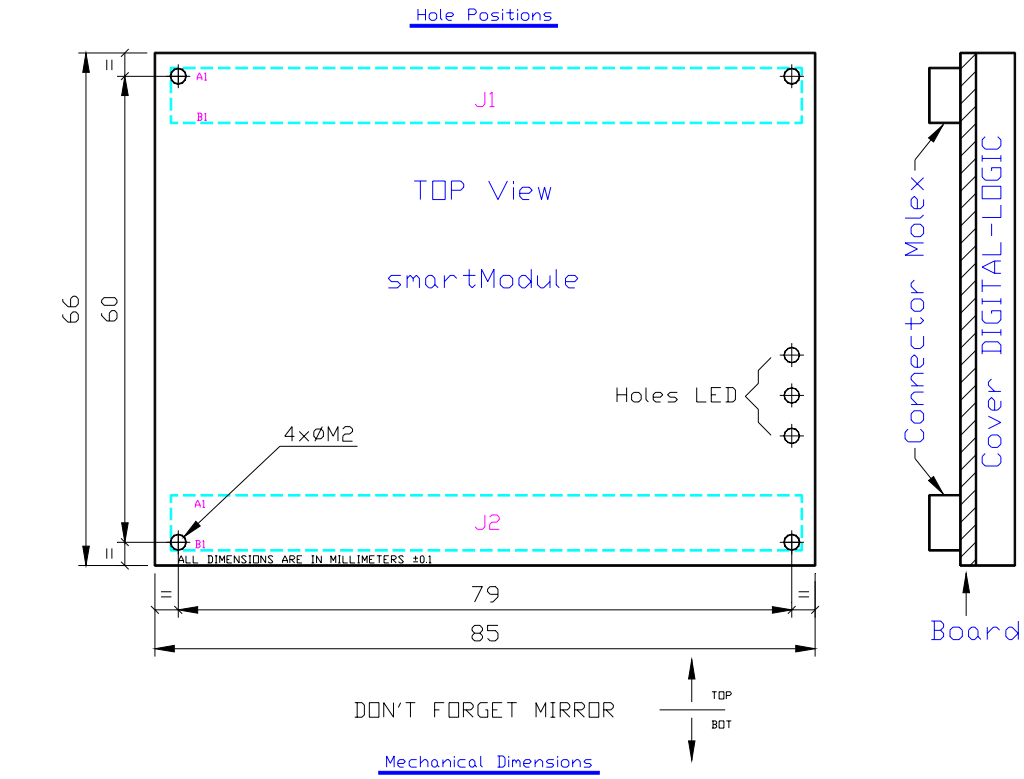
2.7 Ordercodes

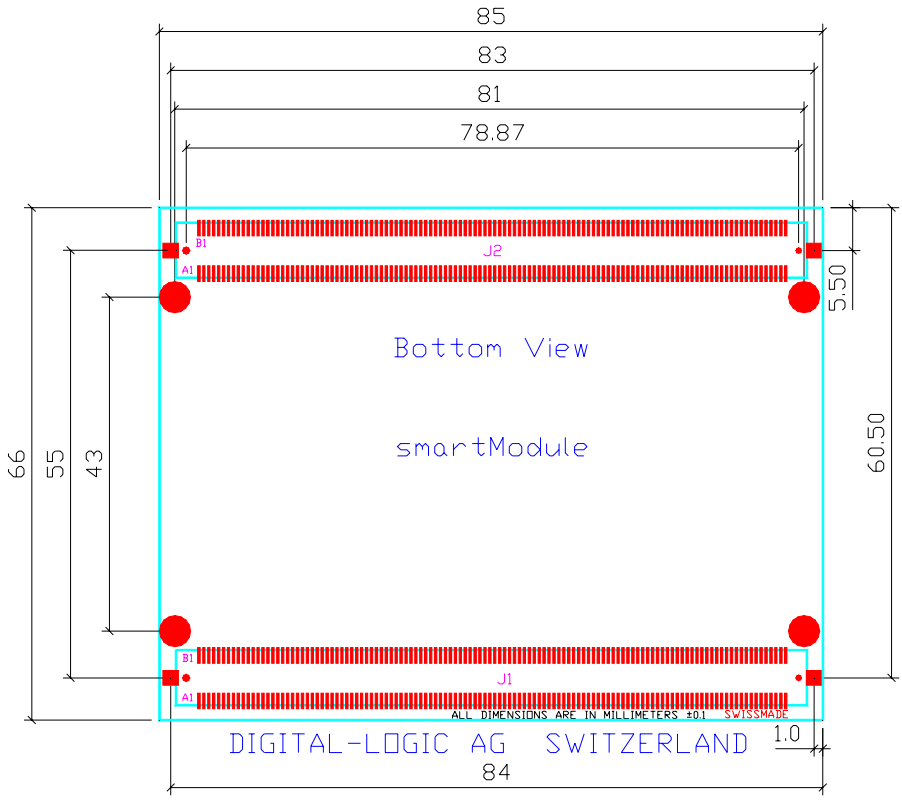
To get the actual status of the partnumbers, customers are advised to ask for them via our sales department or distributors.
The list below has to be treated as a momentary screenshot and is might not up to date anymore.

Family/order code:	Based CPU	Standard with VGA	Option: No VGA	Option: With LAN
smartModule486	ELAN400 (66MHz)	SM486PCX	SM486PCN	SM486PCX
smartModule586	ZF586 (133MHz)	SM586PC	SM586PCN	SM586PCX
smartModuleGX	GEODE 200MHz	SMGXPC-200	Not available	SMGXPCX-200
	GEODE 300MHz	SMGXPC-300		SMGXPCX-300
smartModuleP5	Pentium 166MHz	SMP5PC-166	SMP5PCN-166	Not available
	Pentium 266MHz	SMP5PC-266	SMP5PCN-266	
smartModuleP3	Pentium 400C MHz	SMP3PC-400C	SMP3PCN-400C	Not available
	Pentium-III 700MHz	SMP3PC-700		

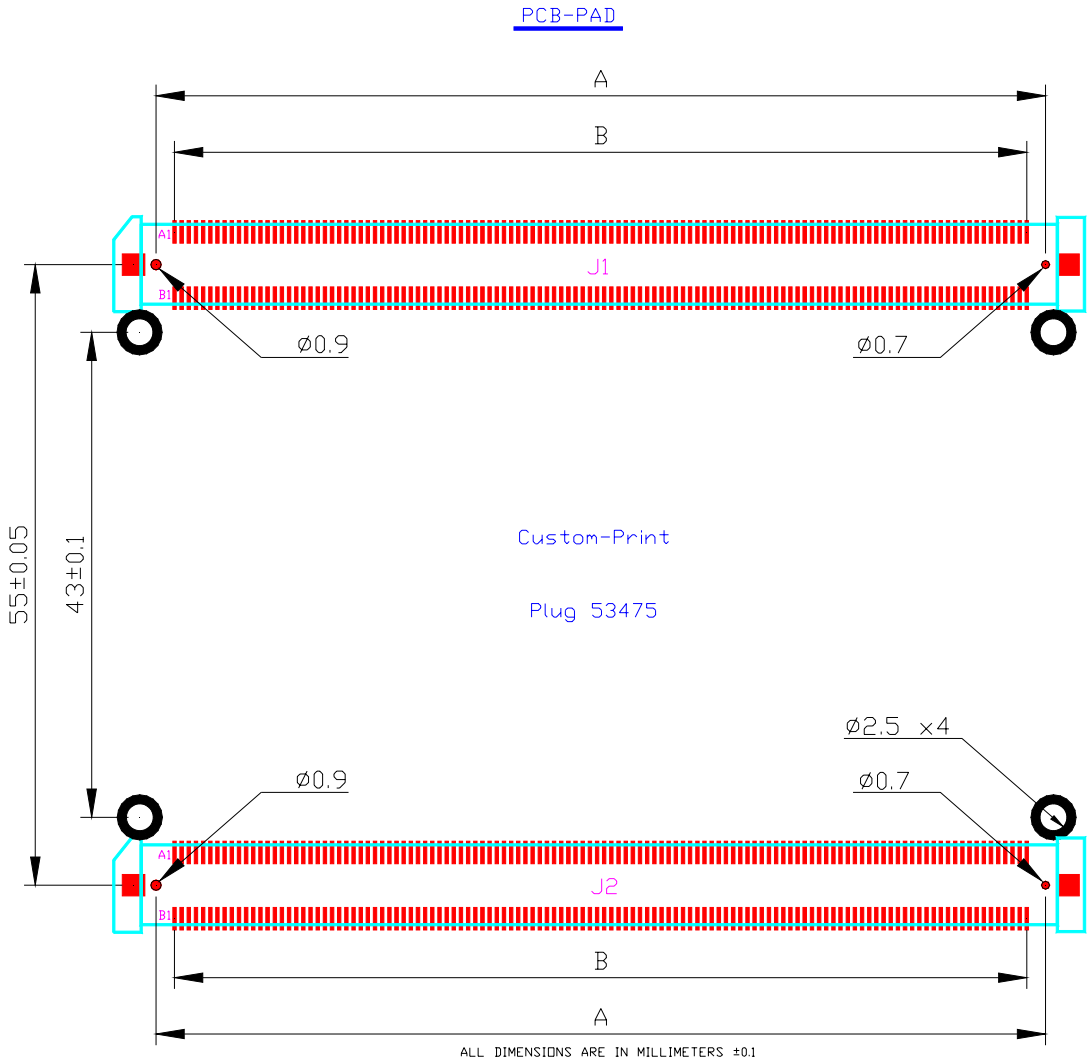
3 DESIGNIN WITH smart

3.1 Mechanical dimensions, SMxxxPC





3.1.1 Mechanical PCB pad dimensions on the carrier-board



Customer board

53475-2409	Dimension mm (inches)	
Circuits	A	B
240	78.07 (3.070)	75.565 (2.970)

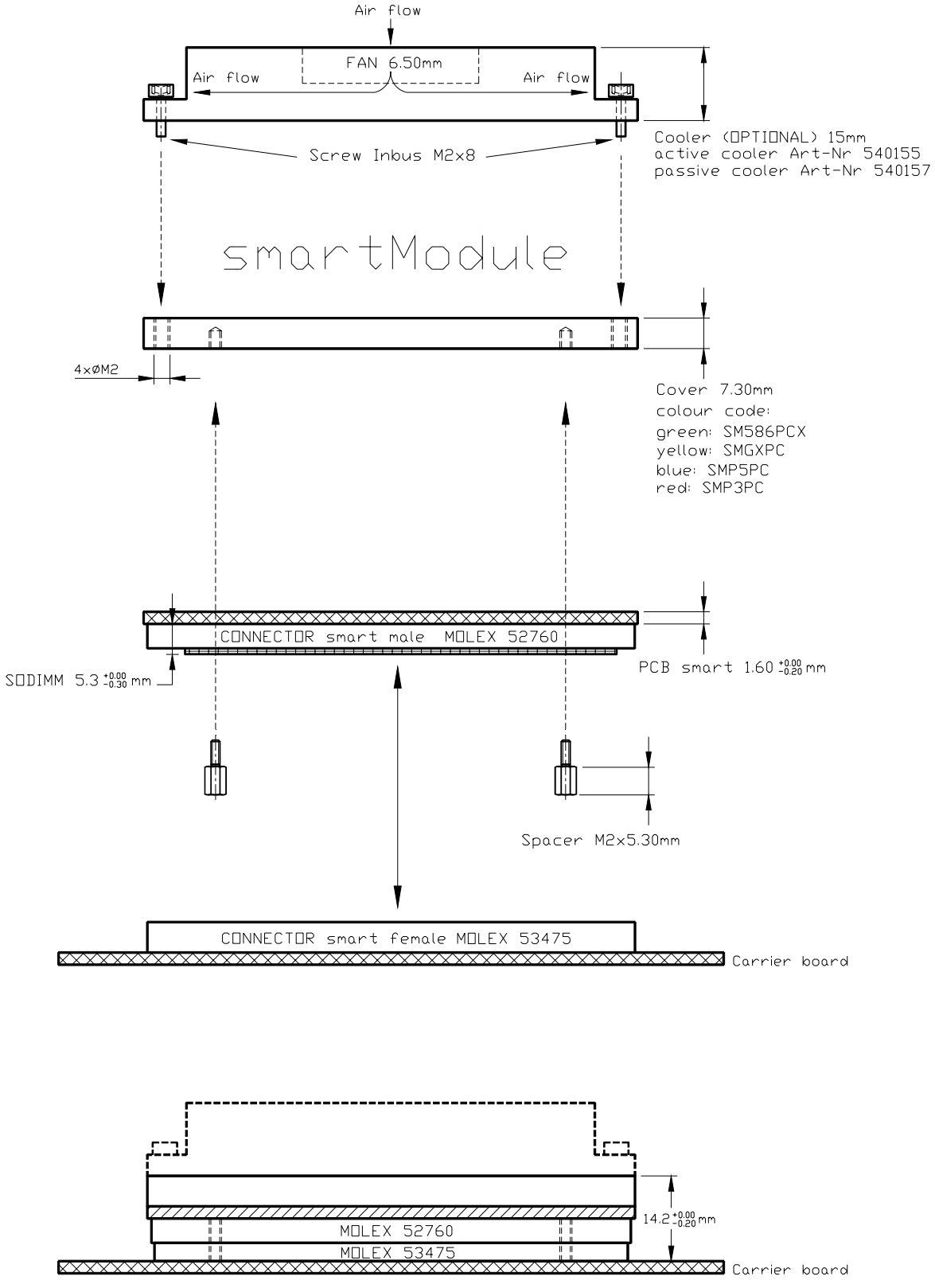
DIGITAL-LOGIC / Art_Nr : 439004 Connected: 5.00mm

smartModule

52760-2409	Dimension mm (inches)	
Circuits	A	B
240	78.87 (3.105)	75.565 (2.970)

DIGITAL-LOGIC / Art_Nr : 439003 Receptable

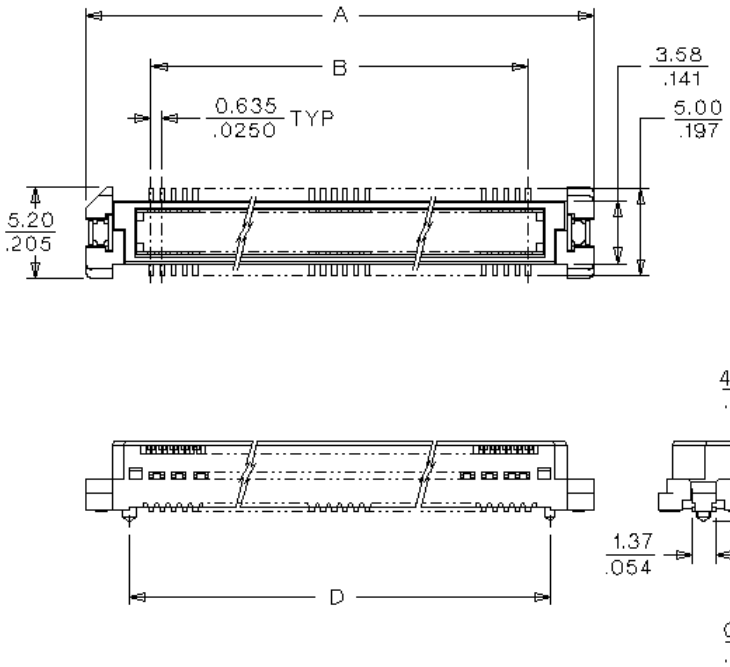
3.1.2 PCB to SMxxxPC height



3.1.3 Mechanical dimensions of the PCB, plug

Must be mounted onto the customers electronicboard (carrierboard).

Standard height: 5.0mm (do not place components below the smartModule)
Expanded height: 7.0mm (place max. 2.0mm components below the smartModule)



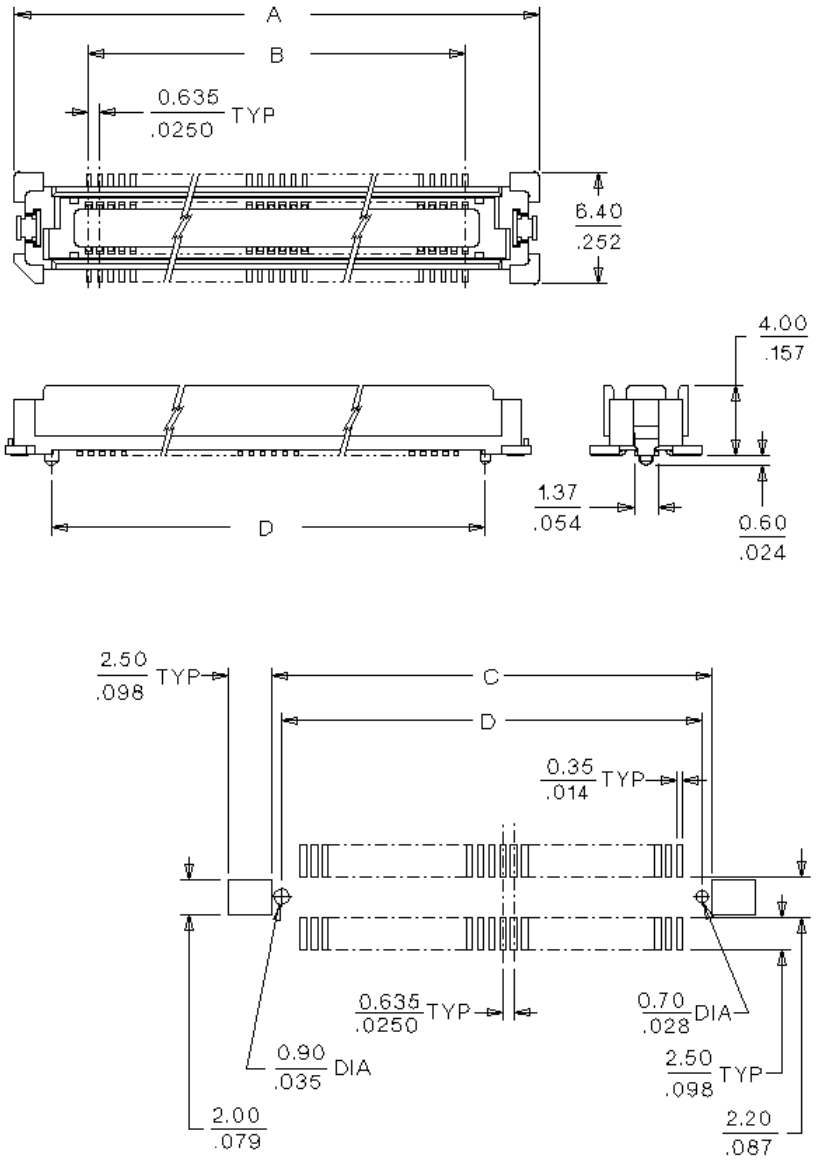
PCB LAYOUT : COMPONENT SIDE

53475-2409 **Circuits**	Dimension **mm** (inches)			
	A (Overall Length)	**B (1st to Last Ckt)**	**C**	**D**
240	**83.07**(3.270)	**75.565**(2.970)	**79.17**(3.110)	**78.07**(3.070)

DLAG partnumber: 439004

3.1.4 Mechanical dimensions of the SMxxxPC, receptacle

Mounted on the smartModule xxPC, as a reference only



PCB LAYOUT: COMPONENT SIDE

52760-2409 **Circuits**	Dimension **mm** (inches)			
	A	**B**	**C**	**D**
240	**84.07(3.309)**	**75.565(2.970)**	**80.47(3.168)**	**78.87(3.105)**

DLAG part number: 439003

4 BOARD TO BOARD CONNECTORS

4.1 The generic smartModule480 bus, (sinceVers. 2.2)

smart 480 BUS connector J1 Pin 1-40 (Vers. 2.2 SM520PC, SMGXPC, SMP5/3PC)

Pin	Group	Volt	SMxxxPC	Pin	Group	Volt	SMxxxPC
A1	POWER		VCC (5V)	B1	ISA	5 i	IRQ1 used by keyboard
A2	ISA	5 o	RESDRV	B2	ISA	5 i	IRQ9
A3	ISA	5 i	SBHE#	B3	ISA	5 i	IRQ3 used by COM2
A4	ISA	5 i	MEMCS16#	B4	ISA	5 i	IRQ4 used by COM1
A5	ISA	5 i	IOCS16#	B5	ISA	5 i	IRQ5
A6	ISA	5 o	IOW#	B6	ISA	5 i	IRQ6 used by FDD
A7	ISA	5 o	IOR#	B7	ISA	5 i	IRQ7 used by LPT1
A8	ISA	5 o	SYSCLK	B8	ISA	5 i	IRQ10
A9	ISA	5 o	TC	B9	ISA	5 i	IRQ11
A10	ISA	5 o	ALE	B10	ISA	5 i	IRQ12 used by PS/2 mouse
A11	ISA	5 i/o	SD7	B11	ISA	5 i	IRQ14 used by P-IDE
A12	ISA	5 i/o	SD6	B12	ISA	5 i	IRQ15 used by S-IDE
A13	ISA	5 i/o	SD5	B13	CORE	3/5 i	Only factory: COREBIOS
A14	ISA	5 i/o	SD4	B14	CORE	3/5 i	Only factory: VGABIOS
A15	ISA	5 i/o	SD3	B15	ISA	5 o	SA21 = LA21
A16	ISA	5 i/o	SD2	B16	ISA	5 o	SA20 = LA20
A17	ISA	5 i/o	SD1	B17	ISA	5 o	LA19
A18	ISA	5 i/o	SD0	B18	ISA	5 o	LA18
A19	ISA	5 o	IOCHRDY	B19	ISA	5 o	LA17
A20	ISA	5 o	AEN	B20	ISA	5 i/o	SD8
A21	ISA	5 o	SA19	B21	ISA	5 i/o	SD9
A22	ISA	5 o	SA18	B22	ISA	5 i/o	SD10
A23	ISA	5 o	SA17	B23	ISA	5 i/o	SD11
A24	ISA	5 o	SA16	B24	ISA	5 i/o	SD12
A25	ISA	5 o	SA15	B25	ISA	5 i/o	SD13
A26	ISA	5 o	SA14	B26	ISA	5 i/o	SD14
A27	ISA	5 o	SA13	B27	ISA	5 i/o	SD15
A28	ISA	5 o	SA12	B28	ISA	5 i	DRQ 0
A29	ISA	5 o	SA11	B29	ISA	5 i	DRQ 1
A30	ISA	5 o	SA10	B30	ISA	5 i	DRQ 2
A31	ISA	5 o	SA9	B31	ISA	5 i	DRQ 3
A32	ISA	5 o	SA8	B32	ISA	5 i	DRQ 5
A33	ISA	5 o	SA7	B33	ISA	5 i	DRQ 6
A34	ISA	5 o	SA6	B34	ISA	5 o	OSC (14.31MHz)
A35	ISA	5 o	SA5	B35	ISA	5 o	DMA0#
A36	ISA	5 o	SA4	B36	ISA	5 o	DMA1#
A37	ISA	5 o	SA3	B37	ISA	5 o	DMA2#
A38	ISA	5 o	SA2	B38	ISA	5 o	DMA3#
A39	ISA	5 o	SA1	B39	ISA	5 o	DMA5#
A40	ISA	5 o	SA0	B40	ISA	5 o	DMA6#

** These signals (LA17-LA19) correspond with the SA17-SA19.

Remarks:

5 o = 5V output 5 i/o = 5V input/output
3 o = 3V output 3 i/o = 3V input/output

# (-)= active low signal o.c. = open collector output NC = not connected
RES= pin function depending of the CPU, reserved

smart 480 BUS connector J1 Pin 41-80 (Vers. 2.2 SM520PC, SMGXPC, SMP5/3PC)

Pin	Group	Volt	SMxxxPC	Pin	Group	Volt	SMxxxPC
A41	S/DRAM	3 o	CAS0- / DQMB0	B41	CORE	5 o	Speaker
A42	S/DRAM	3 o	CAS1- / DQMB1	B42	ISA	5 i	ZWS#
A43	S/DRAM	3 o	CAS2- / DQMB2	B43	ISA	5 o	REF#
A44	S/DRAM	3 o	CAS3- / DQMB3	B44	ISA	5 o	MEMR#
A45	S/DRAM	3 o	CAS4- / DQMB4	B45	ISA	5 o	SMEMR#
A46	S/DRAM	3 o	CAS5- / DQMB5	B46	ISA	5 o	MEMW#
A47	S/DRAM	3 o	CAS6- / DQMB6	B47	ISA	5 o	SMEMW#
A48	S/DRAM	3 o	CAS7- / DQMB7	B48	S-IDE	5 i/o	IDE HD 0
A49	DRAM	3 i/o	MD0	B49	S-IDE	5 i/o	IDE HD 1
A50	DRAM	3 i/o	MD1	B50	S-IDE	5 i/o	IDE HD 2
A51	DRAM	3 i/o	MD2	B51	S-IDE	5 i/o	IDE HD 3
A52	DRAM	3 i/o	MD3	B52	S-IDE	5 i/o	IDE HD 4
A53	DRAM	3 i/o	MD4	B53	S-IDE	5 i/o	IDE HD 5
A54	DRAM	3 i/o	MD5	B54	S-IDE	5 i/o	IDE HD 6
A55	DRAM	3 i/o	MD6	B55	S-IDE	5 i/o	IDE HD 7
A56	DRAM	3 i/o	MD7	B56	S-IDE	5 i/o	IDE HD 8
A57	POWER		GROUND	B57	S-IDE	5 i/o	IDE HD 9
A58	DRAM	3 i/o	MD8	B58	S-IDE	5 i/o	IDE HD 10
A59	DRAM	3 i/o	MD9	B59	S-IDE	5 i/o	IDE HD 11
A60	DRAM	3 i/o	MD10	B60	S-IDE	5 i/o	IDE HD 12
A61	DRAM	3 i/o	MD11	B61	S-IDE	5 i/o	IDE HD 13
A62	DRAM	3 i/o	MD12	B62	S-IDE	5 i/o	IDE HD 14
A63	DRAM	3 i/o	MD13	B63	S-IDE	5 i/o	IDE HD 15
A64	DRAM	3 i/o	MD14	B64	S-IDE	5 o	IDE CS0#
A65	DRAM	3 i/o	MD15	B65	S-IDE	5 o	IDE CS1#
A66	POWER		GROUND	B66	S-IDE	5 o	IDE IOR#
A67	DRAM	3 i/o	MD16	B67	S-IDE	5 o	IDE IOW#
A68	DRAM	3 i/o	MD17	B68	SDRAM	3 o	SDCLK2
A69	DRAM	3 i/o	MD18	B69	SDRAM	3 o	CKE0
A70	DRAM	3 i/o	MD19	B70	SDRAM	3 o	CKE1
A71	DRAM	3 i/o	MD20	B71	SDRAM	3 o	SCASA
A72	DRAM	3 i/o	MD21	B72	SDRAM	3 o	SCASB
A73	DRAM	3 i/o	MD22	B73	SDRAM	3 o	SRASA
A74	DRAM	3 i/o	MD23	B74	SDRAM	3 o	SDASB
A75	DRAM	3 o	MA0	B75	SDRAM	3 o	RAS4 (TX)
A76	DRAM	3 o	MA1	B76	SDRAM	3 o	RAS5 (TX)
A77	DRAM	3 o	MA2	B77	DRAM	3 o	MA13
A78	DRAM	3 o	MA3	B78	SDRAM	3 o	S DCLK0
A79	DRAM	3 o	MA4	B79	SDRAM	3 o	S DCLK1
A80	DRAM	3 o	MA5	B80	RES	3 o	RES- function 7/ 24MHz

Remarks:

5 o = 5V output 5 i/o = 5V input/output
3 o = 3V output 3 i/o = 3V input/output

# (-)= active low signal o.c. = open collector output NC = not connected
RES= pin function depending of the CPU, reserved

P5 CPU with 64Bit memorybus:
CASL0-CASL3 Bank 0,2 CAS0 .... CAS7 to all banks
CASH0-CASH3 Bank 1,3

smart 480 BUS connector J1 Pin 81-120 (Vers. 2.2 SM520PC, SMGXPC, SMP5/3PC)

Pin	Group	Volt	SMxxxPC	Pin	Group	Volt	SMxxxPC
A81	DRAM	3 o	MA 6	B81	POWER		Ground
A82	DRAM	3 o	MA 7	B82	DRAM	3 i/o	NC/ MD48
A83	DRAM	3 o	MA 8	B83	DRAM	3 i/o	NC/ MD49
A84	DRAM	3 o	MA 9	B84	DRAM	3 i/o	NC/ MD50
A85	DRAM	3 o	MA 10	B85	DRAM	3 i/o	NC/ MD51
A86	DRAM	3 o	MA 11	B86	DRAM	3 i/o	NC/ MD52
A87	DRAM	3 o	MA 12	B87	DRAM	3 i/o	NC/ MD53
A88	POWER		Ground	B88	DRAM	3 i/o	NC/ MD54
A89	DRAM	3 i/o	MD24	B89	DRAM	3 i/o	NC/ MD55
A90	DRAM	3 i/o	MD25	B90	POWER		GROUND
A91	DRAM	3 i/o	MD26	B91	DRAM	3 i/o	NC/ MD56
A92	DRAM	3 i/o	MD27	B92	DRAM	3 i/o	NC/ MD57
A93	DRAM	3 i/o	MD28	B93	DRAM	3 i/o	NC/ MD58
A94	DRAM	3 i/o	MD29	B94	DRAM	3 i/o	NC/ MD59
A95	DRAM	3 i/o	MD30	B95	DRAM	3 i/o	NC/ MD60
A96	DRAM	3 i/o	MD31	B96	DRAM	3 i/o	NC/ MD61
A97	POWER		GROUND	B97	DRAM	3 i/o	NC/ MD62
A98	DRAM	3 i/o	MD32	B98	DRAM	3 i/o	NC/ MD63
A99	DRAM	3 i/o	MD33	B99	POWER		GROUND
A100	DRAM	3 i/o	MD34	B100	S-IDE	5 i/o	IDE-DACK#
A101	DRAM	3 i/o	MD35	B101	S-IDE	5 i/o	IDE-DRQ
A102	DRAM	3 i/o	MD36	B102	S-IDE	5 i/o	IRQ (assigned to IRQ15)
A103	DRAM	3 i/o	MD37	B103	S-IDE	5 i/o	IDE-IORDY
A104	DRAM	3 i/o	MD38	B104	S-IDE	5 i/o	IDE-A0
A105	DRAM	3 i/o	MD39	B105	S-IDE	5 i/o	IDE-A1
A106	POWER		GROUND	B106	S-IDE	5 i/o	IDE-A2
A107	DRAM	3 i/o	MD40	B107	SDRAM	3 o	BA0
A108	DRAM	3 i/o	MD41	B108	Core	5 i#	WDOG Strobe
A109	DRAM	3 i/o	MD42	B109	Core	5 i#	WDOG Enable
A110	DRAM	3 i/o	MD43	B110	SDRAM	3 o	BA1
A111	DRAM	3 i/o	MD44	B111	Xbus	3 o	KM-P10/ XD0
A112	DRAM	3 i/o	MD45	B112	Xbus	3 o	KM-P11/ XD1
A113	DRAM	3 i/o	MD46	B113	Xbus	3 o	KM-P12/ XD2
A114	DRAM	3 i/o	MD47	B114	Xbus	3 o	KM-P13/ XD3
A115	S/DRAM	3 o	RAS0# / (S0 @ SDRAM)	B115	Xbus	3 o	KM-P14/ XD4
A116	S/DRAM	3 o	RAS1# / (S1 @ SDRAM)	B116	Xbus	3 o	KM-P15/ XD5
A117	S/DRAM	3 o	RAS2# / (internally used)	B117	Xbus	3 o	KM-P16/ XD6
A118	S/DRAM	3 o	RAS3# / (free)	B118	Xbus	3 o	KM-P17/ XD7
A119	DRAM	3 o	MWEA#	B119	Xbus	3 o	KM-WRMTRX/ XD CS#
A120	DRAM	3 o	MWEB#	B120	RES		KM-RDMTRX/ VCC (+5V)

Remarks:

5 o = 5V output 5 i/o = 5V input/output
3 o = 3V output 3 i/o = 3V input/output

# (-)= active low signal o.c. = open collector output NC = not connected
RES= pin function depending of the CPU, reserved

Memorybus width: P5: 64Bit (MD0 – MD63))

smart 480 BUS connector J2 Pin 1-40 (Vers. 2.2 SM520PC, SMGXPC, SMP5/3PC)

Pin	Group	Volt	SMxxxPC	Pin	Group	Volt	SMxxxPC
A1	PRINTER	5 o	Strobe#	B1	COM1	5 o	DCD1
A2	PRINTER	5 o	Auto#	B2	COM1	5 i	DSR1
A3	PRINTER	5 o	Error#	B3	COM1	5 i	RXD1
A4	PRINTER	5 o	Init#	B4	COM1	5 o	RTS1
A5	PRINTER	5 o	Slctin#	B5	COM1	5 o	TXD1
A6	PRINTER	5 i/o	PRINTER data 0	B6	COM1	5 i	CTS1
A7	PRINTER	5 i/o	PRINTER data 1	B7	COM1	5 o	DTR1
A8	PRINTER	5 i/o	PRINTER data 2	B8	COM1	5 i	RI1
A9	PRINTER	5 i/o	PRINTER data 3	B9	COM2	5 o	DCD2
A10	PRINTER	5 i/o	PRINTER data 4	B10	COM2	5 i	DSR2
A11	PRINTER	5 i/o	PRINTER data 5	B11	COM2	5 i	RXD2
A12	PRINTER	5 i/o	PRINTER data 6	B12	COM2	5 o	RTS2
A13	PRINTER	5 i/o	PRINTER data 7	B13	COM2	5 o	TXD2
A14	PRINTER	5 i	Acknowledge#	B14	COM2	5 i	CTS2
A15	PRINTER	5 i	Busy	B15	COM2	5 o	DTR2
A16	PRINTER	5 i	Paper end#	B16	COM2	5 i	RI2
A17	PRINTER	5 i	Select#	B17	FLOPPY	5 i	Index#
A18	KBD	5 i/o	Keyboard data	B18	FLOPPY	5 o	Drive select 1#
A19	KBD	5 o	Keyboard clock	B19	FLOPPY	5 i	Disk change#
A20	MOUSE	5 o	MOUSE clock	B20	FLOPPY	5 o	Motor on 1
A21	MOUSE	5 i/o	MOUSE data	B21	FLOPPY	5 o	Direction#
A22	POWER		Ground	B22	FLOPPY	5 o	Step impulse#
A23	P-IDE	5 i/o	IDE HD 0	B23	FLOPPY	5 o	Write data#
A24	P-IDE	5 i/o	IDE HD 1	B24	FLOPPY	5 o	Write gate#
A25	P-IDE	5 i/o	IDE HD 2	B25	FLOPPY	5 i	Track zero#
A26	P-IDE	5 i/o	IDE HD 3	B26	FLOPPY	5 i	Write protected#
A27	P-IDE	5 i/o	IDE HD 4	B27	FLOPPY	5 i	Read data#
A28	P-IDE	5 i/o	IDE HD 5	B28	FLOPPY	5 o	Head select#
A29	P-IDE	5 i/o	IDE HD 6	B29	FLOPPY	5 o	Drive select 0
A30	P-IDE	5 i/o	IDE HD 7	B30	FLOPPY	5 o	Motor on 0
A31	P-IDE	5 i/o	IDE HD 8	B31	APM	5 i	PWRBTN#
A32	P-IDE	5 i/o	IDE HD 9	B32	P-IDE	5 o	IDE RESET#
A33	P-IDE	5 i/o	IDE HD 10	B33	APM	5 i	LID#
A34	P-IDE	5 i/o	IDE HD 11	B34	USB	5 i/o	USB-P0+
A35	P-IDE	5 i/o	IDE HD 12	B35	USB	5 i/o	USB-P0-
A36	P-IDE	5 i/o	IDE HD 13	B36	P-IDE	5 o	IDE-A 0
A37	P-IDE	5 i/o	IDE HD 14	B37	P-IDE	5 o	IDE-A 1
A38	P-IDE	5 i/o	IDE HD 15	B38	P-IDE	5 o	IDE-A 2
A39	P-IDE	5 o	IDE CS0#	B39	P-IDE	5 o	IDE-IORDY
A40	P-IDE	5 o	IDE CS1#	B40	LCD	5 o	LCD D32

Remarks:

5 o = 5V output 5 i/o = 5V input/output

3 o = 3V output 3 i/o = 3V input/output

(-)= active low signal o.c. = open collector output NC = not connected

RES= pin function depending of the CPU, reserved

smart 480 BUS connector J2 Pin 41-80 (Vers. 2.2 SM520PC, SMGXPC, SMP5/3PC)

Pin	Group	Volt	SMxxxPC	Pin	Group	Volt	SMxxxPC
A41	P-IDE	5 o	DACK#	B41	IrDA	5 o	IrDA TX
A42	P-IDE	5 o	DRQ	B42	IrDA	5 i	IrDA RX
A43	P-IDE	5 i	IDE-IRQ (to IRQ14)	B43	LCD	3.3/5 o	LCD D33
A44	P-IDE	5 o	IDE-IOR#	B44	LCD	3.3/5 o	LCD D34
A45	P-IDE	5 o	IDE-IOW#	B45	LCD	3.3/5 o	LCD D35
A46	POWER		VCC (5V)	B46	POWER	3 i	Battery 3.0V-3.6V for RTC
A47	PCI	3 i/o	AD0	B47	PCI	3 i/o	AD16
A48	PCI	3 i/o	AD1	B48	PCI	3 i/o	AD17
A49	PCI	3 i/o	AD2	B49	PCI	3 i/o	AD18
A50	PCI	3 i/o	AD3	B50	PCI	3 i/o	AD19
A51	PCI	3 i/o	AD4	B51	PCI	3 i/o	AD 20
A52	PCI	3 i/o	AD5	B52	PCI	3 i/o	AD 21
A53	PCI	3 i/o	AD6	B53	PCI	3 i/o	AD 22
A54	PCI	3 i/o	AD7	B54	PCI	3 i/o	AD 23
A55	PCI	3 i/o	AD8	B55	PCI	3 i/o	AD 24
A56	PCI	3 i/o	AD9	B56	PCI	3 i/o	AD 25
A57	PCI	3 i/o	AD10	B57	PCI	3 i/o	AD 26
A58	PCI	3 i/o	AD11	B58	PCI	3 i/o	AD 27
A59	PCI	3 i/o	AD12	B59	PCI	3 i/o	AD 28
A60	PCI	3 i/o	AD13	B60	PCI	3 i/o	AD 29
A61	PCI	3 i/o	AD14	B61	PCI	3 i/o	AD 30
A62	PCI	3 i/o	AD15	B62	PCI	3 i/o	AD 31
A63	PCI	3 o	C-BE0#	B63	PCI	3 i	PIRQA#
A64	PCI	3 o	C-BE1#	B64	PCI	3 i	PIRQB#
A65	PCI	3 o	C-BE2#	B65	PCI	3 i	PIRQC#
A66	PCI	3 o	C-BE3#	B66	PCI	3 i	PIRQD#
A67	POWER		VCC (5V)	B67	POWER		VCC (5V)
A68	PCI	3 o	PCI-CLK1	B68	PCI	3 o	PCI-CLK2
A69	PCI	3 i	REQ0#	B69	PCI	3 o	GNT0#
A70	PCI	3 i	REQ1#	B70	PCI	3 o	GNT1#
A71	PCI	3 i	REQ2#	B71	PCI	3 o	GNT2#
A72	PCI	3 i	REQ3#	B72	PCI	3 o	GNT3#
A73	RES	i/o	RES.- function 5 DRAM_SEL	B73	POWER		VCC (5V)
A74	PCI	3 i/o	FRAME#	B74	PCI	3 i/o	IRDY#
A75	PCI	3 i/o	TRDY#	B75	PCI	3 i/o	STOP#
A76	PCI	3 i/o	DEVSEL#	B76	PCI	3 i/o	PAR#
A77	PCI	3 i/o	SERR#	B77	PCI	3 i/o	LOCK#
A78	RES	i/o	RES.-function 4	B78	PCI	3 o	PCI-RESET#
A79	CORE	5 i	Resetinput / POWERgood	B79	ISA	5 i	DRQ7
A80	RES	i/o	RES.- function 6	B80	ISA	5 0	DACK7#

All PCI signals are left open, if the smartModule does not support the PCI bus.

Remarks:

5 o = 5V output 5 i/o = 5V input/output
3 o = 3V output 3 i/o = 3V input/output

# (-)= active low signal o.c. = open collector output NC = not connected
RES= pin function depending of the CPU, reserved

smart 480 BUS connector J2 Pin 81-120 (Vers. 2.2 SM520PC, SMGXPC, SMP5/3PC)

Pin	Group	Volt	SMxxxPC	Pin	Group	Volt	SMxxxPC
A81	LCD	3 o	LCD D24	B81	USB	5 i/o	USB-P1+
A82	LCD	3 o	LCD D25	B82	USB	5 i/o	USB-P1-
A83	LCD	3 o	LCD D26	B83	USB	5 i/o	USB-OC0
A84	LCD	3 o	LCD D27	B84	USB	5 i/o	USB-OC1
A85	LCD	3 o	LCD D28	B85	ISA	5 o	LA22
A86	LCD	3 o	LCD D29	B86	ISA	5 o	LA23
A87	LCD	3 o	LCD D30	B87	PCI	5 i/o	PERR-
A88	LCD	3 o	LCD D31	B88	RES	i/o	RES.-function 1
A89	RES	i/o	RES.- function 2	B89	I2C	3 i/o	SMB-DAT
A90	RES	i/o	RES.- function 3	B90	I2C	3 o	SMB-CLK
A91	POWER		3.3V	B91	POWER		3.3V
A92	OPTION	i/o	INTERN LAN TX+	B92	ISA	5 i	MASTER#
A93	OPTION	i/o	INTERN LAN TX-	B93	ISA	5 i	IOCHCK
A94	OPTION	i/o	INTERN LAN RX+	B94	CORE	5 i	JTAG-TCK (DASP)
A95	OPTION	i/o	INTERN LAN RX-	B95	CORE	3 i	JTAG-TDI (DIAG)
A96	APM	3 o	SSTAT2	B96	CORE	3 o	JTAG-TDO (SEL)
A97	POWER	5 i	VCC-SUSPEND +5Volt	B97	CORE	3 i	JTAG-TMS
A98	APM	3 i/o	SUSA- (LAN0)	B98	VGA	3 o	VESA VDDA
A99	APM	3 i/o	SUSB- (LAN1)	B99	VGA	3 o	VESA VDDC
A100	APM	3 i/o	SUSC- (LAN2)	B100	APM	3 i	STAT1
A101	VGA	o	VGA Analog Green	B101	VGA	o	Analog ground
A102	VGA	o	VGA Analog Blue	B102	VGA	5 o	VSynch
A103	VGA	o	VGA Analog Red	B103	VGA	5 o	HSynch
A104	LCD	5 o	LCD ENAVEE	B104	LCD	3 o	LCD ENAVDD
A105	POWER		GROUND	B105	LCD	3 o	LCD SHCLK
A106	LCD	3 o	LCD FLM/VS	B106	LCD	3 o	LCD LP/HS
A107	LCD	3 o	LCD D12	B107	LCD	3 o	LCD D0
A108	LCD	3 o	LCD D13	B108	LCD	3 o	LCD D1
A109	LCD	3 o	LCD D14	B109	LCD	3 o	LCD D2
A110	LCD	3 o	LCD D15	B110	LCD	3 o	LCD D3
A111	LCD	3 o	LCD D16	B111	LCD	3 o	LCD D4
A112	LCD	3 o	LCD D17	B112	LCD	3 o	LCD D5
A113	LCD	3 o	LCD D18	B113	LCD	3 o	LCD D6
A114	LCD	3 o	LCD D19	B114	LCD	3 o	LCD D7
A115	LCD	3 o	LCD D20	B115	LCD	3 o	LCD D8
A116	LCD	3 o	LCD D21	B116	LCD	3 o	LCD D9
A117	LCD	3 o	LCD D22	B117	LCD	3 o	LCD D10
A118	LCD	3 o	LCD D23	B118	LCD	3 o	LCD D11
A119	LCD	3 o	LCD ENABKL	B119	LCD	3 o	LCD M
A120	POWER	3 o	LCD VCC OUTPUT (3.3V)	B120	POWER	2 o	CPU CORE OUTPUT (VCC2)

Remarks:

5 o = 5V output 5 i/o = 5V input/output

3 o = 3V output 3 i/o = 3V input/output

(-)= active low signal o.c. = open collector output NC = not connected

RES= pin function depending of the CPU, reserved

4.2 SM480BUS pullup/down resistor specification

SM480BUS pullup/down-resistor, connector J1 Pin 1-40
(Vers. 2.2 SM586PC, SMGXPC, SMP5/3PC)

Pin	Pull *)	Chip	Description	Pin	Pull *)	Chip	Description
A1			VCC (5V)	B1	iPU10k /5V	PIIX4	IRQ1 used by keyboard
A2	TTL-Output	HCT04	RESDRV	B2	iPU10k /5V	PIIX4	IRQ9
A3	ePU1k /5V	PIIX4	SBHE# 1)	B3	iPU10k /5V	PIIX4	IRQ3 used by COM2
A4	ePU1k /5V	PIIX4	MEMCS16# 1)	B4	iPU10k /5V	PIIX4	IRQ4 used by COM1
A5	ePU1k /5V	PIIX4	IOCS16# 1)	B5	iPU10k /5V	PIIX4	IRQ5
A6	iPU10k /5V	PIIX4	IOW#	B6	iPU10k /5V	PIIX4	IRQ6 used by FDD
A7	iPU10k /5V	PIIX4	IOR#	B7	iPU10k /5V	PIIX4	IRQ7 used by LPT1
A8			SYSCLK	B8	iPU10k /5V	PIIX4	IRQ10
A9			TC	B9	iPU10k /5V	PIIX4	IRQ11
A10	iPU10k /5V	PIIX4	ALE	B10	iPU10k /5V	PIIX4	IRQ12 used by PS/2
A11	iPU10k /5V	PIIX4	SD7	B11	iPU10k /5V	PIIX4	IRQ14 used by P-IDE
A12	iPU10k /5V	PIIX4	SD6	B12	iPU10k /5V	PIIX4	IRQ15 used by S-IDE
A13	iPU10k /5V	PIIX4	SD5	B13			Only factory: COREBIOS
A14	iPU10k /5V	PIIX4	SD4	B14			Only factory: VGABIOS
A15	iPU10k /5V	PIIX4	SD3	B15	iPU10k /5V	PIIX4	SA21 = LA21
A16	iPU10k /5V	PIIX4	SD2	B16	iPU10k /5V	PIIX4	SA20 = LA20
A17	iPU10k /5V	PIIX4	SD1	B17	iPU10k /5V	PIIX4	LA19
A18	iPU10k /5V	PIIX4	SD0	B18	iPU10k /5V	PIIX4	LA18
A19	ePU1k /5V	PIIX4	IOCHRDY 1)	B19	iPU10k /5V	PIIX4	LA17
A20	iPU10k /5V	PIIX4	AEN	B20	iPU10k /5V	PIIX4	SD8
A21	iPU10k /5V	PIIX4	SA19	B21	iPU10k /5V	PIIX4	SD9
A22	iPU10k /5V	PIIX4	SA18	B22	iPU10k /5V	PIIX4	SD10
A23	iPU10k /5V	PIIX4	SA17	B23	iPU10k /5V	PIIX4	SD11
A24	iPU10k /5V	PIIX4	SA16	B24	iPU10k /5V	PIIX4	SD12
A25	iPU10k /5V	PIIX4	SA15	B25	iPU10k /5V	PIIX4	SD13
A26	iPU10k /5V	PIIX4	SA14	B26	iPU10k /5V	PIIX4	SD14
A27	iPU10k /5V	PIIX4	SA13	B27	iPU10k /5V	PIIX4	SD15
A28	iPU10k /5V	PIIX4	SA12	B28	iPD1k /5V	PIIX4	DRQ 0
A29	iPU10k /5V	PIIX4	SA11	B29	iPD1k /5V	PIIX4	DRQ 1
A30	iPU10k /5V	PIIX4	SA10	B30	iPD1k /5V	PIIX4	DRQ 2
A31	iPU10k /5V	PIIX4	SA9	B31	iPD1k /5V	PIIX4	DRQ 3
A32	iPU10k /5V	PIIX4	SA8	B32	iPD1k /5V	PIIX4	DRQ 5
A33	iPU10k /5V	PIIX4	SA7	B33	iPD1k /5V	PIIX4	DRQ 6
A34	iPU10k /5V	PIIX4	SA6	B34	iSE 33	PIIX4	OSC (14.31MHz)
A35	iPU10k /5V	PIIX4	SA5	B35		PIIX4	DMA0#
A36	iPU10k /5V	PIIX4	SA4	B36		PIIX4	DMA1#
A37	iPU10k /5V	PIIX4	SA3	B37		PIIX4	DMA2#
A38	iPU10k /5V	PIIX4	SA2	B38		PIIX4	DMA3#
A39	iPU10k /5V	PIIX4	SA1	B39		PIIX4	DMA5#
A40	iPU10k /5V	PIIX4	SA0	B40		PIIX4	DMA6#

*) ePU = external required resistor
iPU = internal placed resistor
eSE = external serial resistor needed
iSE = internal serial resistor
iPD = internal pulled down

1) Internal with 10k to 5V pullup, for ISA-Bus application an external 1k pullup resistor is recommended

- Shaded resistors must be placed externally on the motherboard as close as possible to the module
- PIIX4 treat also as SOUTHBRIDGE
- TX treat also as NORTHBRIDGE

SM480BUS pullup/down-resistor, connector J1 Pin 41-80
(Vers. 2.2 SM586PC, SMGXPC, SMP5/3PC)

Pin	Pull *)	Chip	Description	Pin	Pull *)	Chip	Description
A41	eSe 33	TX	CAS0#	B41			Speaker
A42	eSe 33	TX	CAS1#	B42	iPU10k /5V	PIIX4	ZWS#
A43	eSe 33	TX	CAS2#	B43	iPU10k /5V	PIIX4	REF#
A44	eSe 33	TX	CAS3#	B44	iPU10k /5V	PIIX4	MEMR#
A45	eSe 33	TX	CAS4#	B45	iPU10k /5V	PIIX4	SMEMR#
A46	eSe 33	TX	CAS5#	B46	iPU10k /5V	PIIX4	MEMW#
A47	eSe 33	TX	CAS6#	B47	iPU10k /5V	PIIX4	SMEMW#
A48	eSe 33	TX	CAS7#	B48	eSe 10	PIIX4	SIDE – D0
A49		TX	MD0	B49	eSe 10	PIIX4	SIDE – D1
A50		TX	MD1	B50	eSe 10	PIIX4	SIDE – D2
A51		TX	MD2	B51	eSe 10	PIIX4	SIDE – D3
A52		TX	MD3	B52	eSe 10	PIIX4	SIDE – D4
A53		TX	MD4	B53	eSe 10	PIIX4	SIDE – D5
A54		TX	MD5	B54	eSe 10	PIIX4	SIDE – D6
A55		TX	MD6	B55	eSe 10	PIIX4	SIDE – D7
A56		TX	MD7	B56	eSe 10	PIIX4	SIDE – D8
A57			GROUND	B57	eSe 10	PIIX4	SIDE – D9
A58		TX	MD8	B58	eSe 10	PIIX4	SIDE – D10
A59		TX	MD9	B59	eSe 10	PIIX4	SIDE – D11
A60		TX	MD10	B60	eSe 10	PIIX4	SIDE – D12
A61		TX	MD11	B61	eSe 10	PIIX4	SIDE – D13
A62		TX	MD12	B62	eSe 10	PIIX4	SIDE – D14
A63		TX	MD13	B63	eSe 10	PIIX4	SIDE – D15
A64		TX	MD14	B64	eSe 10	PIIX4	SIDE - CS0#
A65		TX	MD15	B65	eSe 10	PIIX4	SIDE – CS1#
A66			GROUND	B66	eSe 10	PIIX4	SIDE – IOR#
A67		TX	MD16	B67	eSe 10	PIIX4	SIDE – IOW#
A68		TX	MD17	B68	iSe 10	TX	SDRAM – CLK2
A69		TX	MD18	B69	iSe 10	TX	SDRAM – CKE0
A70		TX	MD19	B70	iSe 10	TX	SDRAM – CKE1
A71		TX	MD20	B71	iSe 10	TX	SDRAM – SCASA
A72		TX	MD21	B72	iSe 10	TX	SDRAM – SCASB
A73		TX	MD22	B73	iSe 10	TX	SDRAM – SRASA
A74		TX	MD23	B74	iSe 10	TX	SDRAM – SRASB
A75	eSE 33	TX	MA0	B75	eSe 33	TX	RAS4
A76	eSE 33	TX	MA1	B76	eSe 33	TX	RAS5
A77	eSE 33	TX	MA2	B77	eSe 33	TX	MA13
A78	eSE 33	TX	MA3	B78	iSe 10	TX	SDRAM – CLK0
A79	eSE 33	TX	MA4	B79	iSe 10	TX	SDRAM – CLK1
A80	eSE 33	TX	MA5	B80		RES	RES. –function 7/ 24MHz

*) ePU = external required resistor
iPU = internal placed resistor
eSE = external serial resistor needed
iSE = internal serial resistor
iPD = internal pulled down

2) Internal with 10k to 5V pullup, for ISA-Bus application an external 1k pullup resistor is recommended

- Shaded resistors must be placed externally on the motherboard as close as possible to the module
- PIIX4 treat also as SOUTHBRIDGE
- TX treat also as NORTHBRIDGE

SM480BUS pullup/down-resistor, connector J1 Pin 81-120
(Vers. 2.2 SM586PC, SMGXPC, SMP5/3PC)

Pin	Pull: *)	Chip	Description	Pin	Pull: *)	Chip	Description
A81	eSE 33	TX	MA 6	B81		TX	Ground
A82	eSE 33	TX	MA 7	B82		TX	NC/ MD48
A83	eSE 33	TX	MA 8	B83		TX	NC/ MD49
A84	eSE 33	TX	MA 9	B84		TX	NC/ MD50
A85	eSE 33	TX	MA 10	B85		TX	NC/ MD51
A86	eSE 33	TX	MA 11	B86		TX	NC/ MD52
A87	eSE 33	TX	MA 12	B87		TX	NC/ MD53
A88		TX	Ground	B88		TX	NC/ MD54
A89		TX	MD24	B89		TX	NC/ MD55
A90		TX	MD25	B90		TX	GROUND
A91		TX	MD26	B91		TX	NC/ MD56
A92		TX	MD27	B92		TX	NC/ MD57
A93		TX	MD28	B93		TX	NC/ MD58
A94		TX	MD29	B94		TX	NC/ MD59
A95		TX	MD30	B95		TX	NC/ MD60
A96		TX	MD31	B96		TX	NC/ MD61
A97		TX	GROUND	B97		TX	NC/ MD62
A98		TX	MD32	B98		TX	NC/ MD63
A99		TX	MD33	B99		TX	GROUND
A100		TX	MD34	B100	eSe 33	PIIX4	SIDE – DACK
A101		TX	MD35	B101	iPD1k/0V	PIIX4	SIDE – DRQ
A102		TX	MD36	B102	eSE 33	PIIX4	SIDE – IRQ
A103		TX	MD37	B103	iPU1k/5V	PIIX4	SIDE – RDY
A104		TX	MD38	B104	eSE 33	PIIX4	SIDE – A0
A105		TX	MD39	B105	eSE 33	PIIX4	SIDE – A1
A106		TX	GROUND	B106	eSE 33	PIIX4	SIDE – A2
A107		TX	MD40	B107	eSE 10	TX	BA0
A108		TX	MD41	B108		LT1232	WDOG Strobe
A109		TX	MD42	B109		LT1232	WDOG ENABLE
A110		TX	MD43	B110	eSE 10	TX	BA1
A111		TX	MD44	B111		PIIX4	KM-P10/ XD0
A112		TX	MD45	B112		PIIX4	KM-P11/ XD1
A113		TX	MD46	B113		PIIX4	KM-P12/ XD2
A114		TX	MD47	B114		PIIX4	KM-P13/ XD3
A115	eSE 10	TX	RAS0# / (S0 @ SDRAM)	B115		PIIX4	KM-P14/ XD4
A116	eSE 10	TX	RAS1# / (S1 @ SDRAM)	B116		PIIX4	KM-P15/ XD5
A117	eSE 10	TX	RAS2# / (internally used)	B117		PIIX4	KM-P16/ XD6
A118	eSE 10	TX	RAS3# / (free)	B118		PIIX4	KM-P17/ XD7
A119	eSE 10	TX	MWEA#	B119		PIIX4	KM-WRMTRX/ XD_CS#
A120	eSE 10	TX	MWEB#	B120		RES	KM-RDMTRX/ VCC (+5V)

*) ePU = external required resistor
iPU = internal placed resistor
eSE = external serial resistor needed
iSE = internal serial resistor
iPD = internal pulled down

3) Internal with 10k to 5V pullup, for ISA-Bus application an external 1k pullup resistor is recommended

- Shaded resistors must be placed externally on the motherboard as close as possible to the module
- PIIX4 treat also as SOUTHBRIDGE
- TX treat also as NORTHBRIDGE

SM480BUS pullup/down-resistor, connector J2 Pin 1-40
(Vers. 2.2 SM586PC, SMGXPC, SMP5/3PC)

Pin	Pull: *)	Chipt	Description	Pin	Pull: *)	Chip	Description
A1	iPU1k/5V	37C672	strobe#	B1		37C672	DCD1
A2	iPU1k/5V	37C672	auto#	B2		37C672	DSR1
A3	iPU1k/5V	37C672	error#	B3		37C672	RXD1
A4	iPU1k/5V	37C672	init#	B4		37C672	RTS1
A5	iPU1k/5V	37C672	slctin#	B5		37C672	TXD1
A6	ePU1k/5V	37C672	PRINTER data 0	B6		37C672	CTS1
A7	ePU1k/5V	37C672	PRINTER data 1	B7		37C672	DTR1
A8	ePU1k/5V	37C672	PRINTER data 2	B8		37C672	RI1
A9	ePU1k/5V	37C672	PRINTER data 3	B9		37C672	DCD2
A10	ePU1k/5V	37C672	PRINTER data 4	B10		37C672	DSR2
A11	ePU1k/5V	37C672	PRINTER data 5	B11		37C672	RXD2
A12	ePU1k/5V	37C672	PRINTER data 6	B12		37C672	RTS2
A13	ePU1k/5V	37C672	PRINTER data 7	B13		37C672	TXD2
A14	iPU1k/5V	37C672	acknowledge#	B14		37C672	CTS2
A15	iPU1k/5V	37C672	busy	B15		37C672	DTR2
A16	iPU1k/5V	37C672	paper end#	B16		37C672	RI2
A17	iPU1k/5V	37C672	Select#	B17	iPU1k/5V	37C672	Index#
A18	iPU1k/5V	37C672	keyboard data	B18		37C672	Drive select 1#
A19	iPU1k/5V	37C672	keyboard clock	B19	iPU1k/5V	37C672	Disk change#
A20	iPU1k/5V	37C672	MOUSE clock	B20		37C672	Motor on 1
A21	iPU1k/5V	37C672	MOUSE data	B21		37C672	Direction#
A22			Ground	B22		37C672	Step impulse#
A23	eSE 10	PIIX4	PIDE HD 0	B23		37C672	Write data#
A24	eSE 10	PIIX4	PIDE HD 1	B24		37C672	Write gate#
A25	eSE 10	PIIX4	PIDE HD 2	B25	iPU1k/5V	37C672	Track zero#
A26	eSE 10	PIIX4	PIDE HD 3	B26	iPU1k/5V	37C672	Write protected#
A27	eSE 10	PIIX4	PIDE HD 4	B27	iPU1k/5V	37C672	Read data#
A28	eSE 10	PIIX4	PIDE HD 5	B28		37C672	Head select#
A29	eSE 10	PIIX4	PIDE HD 6	B29		37C672	Drive select 0
A30	eSE 10	PIIX4	PIDE HD 7	B30		37C672	Motor on 0
A31	eSE 10	PIIX4	PIDE HD 8	B31	iPU10k/3V	PIIX4	PWRBTN#
A32	eSE 10	PIIX4	PIDE HD 9	B32	eSE 10	PIIX4	IDE RESET#
A33	eSE 10	PIIX4	PIDE HD 10	B33	iPU10k/3V	PIIX4	LID#
A34	eSE 10	PIIX4	PIDE HD 11	B34	extern	PIIX4	USB-P0+
A35	eSE 10	PIIX4	PIDE HD 12	B35	extern	PIIX4	USB-P0-
A36	eSE 10	PIIX4	PIDE HD 13	B36	eSE 10	PIIX4	P-IDE-A 0
A37	eSE 10	PIIX4	PIDE HD 14	B37	eSE 10	PIIX4	P-IDE-A 1
A38	eSE 10	PIIX4	PIDE HD 15	B38	eSE 10	PIIX4	P-IDE-A 2
A39	eSE 10	PIIX4	PIDE CS0# (1Fx)	B39	eSE 10	PIIX4	P-IDE-IORDY
A40	eSE 10	PIIX4	PIDE CS1# (3Fx)	B40		69000	LCD D32

*) ePU = external required resistor
iPU = internal placed resistor
eSE = external serial resistor needed
iSE = internal serial resistor
iPD = internal pulled down

4) Internal with 10k to 5V pullup, for ISA-Bus application an external 1k pullup resistor is recommended

- Shaded resistors must be placed externally on the motherboard as close as possible to the module
- PIIX4 treat also as SOUTHBRIDGE
- TX treat also as NORTHBRIDGE

SM480BUS pullup/down-resistor, connector J2 Pin 41-80
(Vers. 2.2 SM586PC, SMGXPC, SMP5/3PC)

Pin	Pull: *)	Chip:	Description	Pin	Pull: *)	Chip	Description
A41	eSE 10	PIIX4	PDACK#	B41		SIO	IrDA TX
A42	iPD1k/0V	PIIX4	PREQ	B42		SIO	IrDA RX
A43	eSE 10	PIIX4	PIDE IRQ	B43		69000/30	LCD D33
A44	eSE 10	PIIX4	PIDE IOR#	B44		69000/30	LCD D34
A45	eSE 10	PIIX4	PIDE IOW#	B45		69000/30	LCD D35
A46			VCC (5V)	B46			Battery 3.0V for RTC
A47		PCI	AD0	B47		PCI	AD16
A48		PCI	AD1	B48		PCI	AD17
A49		PCI	AD2	B49		PCI	AD18
A50		PCI	AD3	B50		PCI	AD19
A51		PCI	AD4	B51		PCI	AD20
A52		PCI	AD5	B52		PCI	AD21
A53		PCI	AD6	B53		PCI	AD22
A54		PCI	AD7	B54		PCI	AD23
A55		PCI	AD8	B55		PCI	AD24
A56		PCI	AD9	B56		PCI	AD25
A57		PCI	AD10	B57		PCI	AD26
A58		PCI	AD11	B58		PCI	AD27
A59		PCI	AD12	B59		PCI	AD28
A60		PCI	AD13	B60		PCI	AD29
A61		PCI	AD14	B61		PCI	AD30
A62		PCI	AD15	B62		PCI	AD31
A63		PCI	C-BE0#	B63	iPU10k/3V	PIIX4	PIRQA#
A64		PCI	C-BE1#	B64	iPU10k/3V	PIIX4	PIRQB#
A65		PCI	C-BE2#	B65	iPU10k/3V	PIIX4	PIRQC#
A66		PCI	C-BE3#	B66	iPU10k/3V	PIIX4	PIRQD#
A67			VCC (5V)	B67			VCC (5V)
A68	iSE 33	CLK	PCI-CLK1	B68	iSE 33	CLK	PCI-CLK2
A69	iPU10k/3V	PIIX4	REQ0#	B69	iPU1k/3V	PIIX4	GNT0#
A70	iPU10k/3V	PIIX4	REQ1#	B70	iPU1k/3V	PIIX4	GNT1#
A71	iPU10k/3V	PIIX4	REQ2#	B71	iPU1k/3V	PIIX4	GNT2#
A72	iPU10k/3V	PIIX4	REQ3#	B72	iPU1k/3V	PIIX4	GNT3#
A73		RES	RES. –function 5/ SDRAM_SEL	B73			VCC (5V)
A74	iPU10k/3V	PIIX4	FRAME#	B74	iPU10k/3V	PIIX4	IRDY#
A75	iPU10k/3V	PIIX4	TRDY#	B75	iPU10k/3V	PIIX4	STOP#
A76	iPU10k/3V	PIIX4	DEVSEL#	B76	iPU10k/3V	PIIX4	PAR#
A77	iPU10k/3V	PIIX4	SERR#	B77	iPU10k/3V	PIIX4	LOCK#
A78			RES FKT 4	B78	iPU10k/3V	PIIX4	PCI-RESET#
A79	iPU1k/5V	LT1232	resetinput / POW-	B79	iPD1k/0V	PIIX4	DRQ7
A80	iPU1k/3.3V	PIIX4	RES FKT 6	B80		PIIX4	DACK7

*) ePU = external required resistor
iPU = internal placed resistor
eSE = external serial resistor needed
iSE = internal serial resistor
iPD = internal pulled down

5) Internal with 10k to 5V pullup, for ISA-Bus application an external 1k pullup resistor is recommended

- Shaded resistors must be placed externally on the motherboard as close as possible to the module
- PIIX4 treat also as SOUTHBRIDGE
- TX treat also as NORTHBRIDGE

SM480BUS pullup/down-resistor, connector J2 Pin 81-120
(Vers. 2.2 SM586PC, SMGXPC, SMP5/3PC)

Pin	Pull: *)	Chip	Description	Pin	Pull:	Chip	Description
A81		69000/30	LCD D24	B81	extern	PIIX4	USB-P1+
A82		69000/30	LCD D25	B82	extern	PIIX4	USB-P1-
A83		69000/30	LCD D26	B83	extern	PIIX4	USB-OC0
A84		69000/30	LCD D27	B84	extern	PIIX4	USB-OC1
A85		69000/30	LCD D28	B85	iPU10k/5V	PIIX4	S/LA22
A86		69000/30	LCD D29	B86	iPU10k/5V	PIIX4	S/LA23
A87		69000/30	LCD D30	B87	iPU10k/3V	PIIX4	PERR-
A88		69000/30	LCD D31	B88	RES FKT1		RES FKT1
A89	RES-FKT2	37C672	DRVDEN1 (IrDA-SEL)	B89	iPU10k/3V	PIIX4	SMB-DATA
A90	RES-FKT3	37C672	DRVDEN0 (IrDA-SEL)	B90	iPU10k/3V	PIIX4	SMB-CLOCK
A91			3.3V	B91			3.3V
A92	Option	82C559	INTERN TX100+	B92	iPU1k/5V	PIIX4	MASTER#
A93	Option	82C559	INTERN TX100-	B93	iPU1k/5V	PIIX4	IOCHCK
A94	Option	82C559	INTERN RX100+	B94	ICP		TCK
A95	Option	82C559	INTERN RX100-	B95	ICP		TDI
A96		PIIX4	SUS-STAT2	B96	ICP		TDO
A97		POWER	VCC-SUSPEND	B97	ICP		TMS
A98		PIIX4	SUSA-	B98		69000	VESA: DDA
A99		PIIX4	SUSB-	B99		69000	VESA: DDC
A100		PIIX4	SUSC-	B100	iPU10k/3V	PIIX4	SUS-STAT1
A101	iPD 75	69000/30	analog green	B101		VGA	Analog ground VIDEO
A102	iPD 75	69000/30	analog blue	B102		69000/30	VSynch
A103	iPD 75	69000/30	analog red	B103		69000/30	HSynch
A104		69000/30	LCD ENAVEE	B104		69000/30	LCD ENAVDD
A105		69000/30	GROUND	B105		69000/30	LCD SHCLK
A106		69000/30	LCD FLM/VS	B106		69000/30	LCD LP/HS
A107		69000/30	LCD D12	B107		69000/30	LCD D0
A108		69000/30	LCD D13	B108		69000/30	LCD D1
A109		69000/30	LCD D14	B109		69000/30	LCD D2
A110		69000/30	LCD D15	B110		69000/30	LCD D3
A111		69000/30	LCD D16	B111		69000/30	LCD D4
A112		69000/30	LCD D17	B112		69000/30	LCD D5
A113		69000/30	LCD D18	B113		69000/30	LCD D6
A114		69000/30	LCD D19	B114		69000/30	LCD D7
A115		69000/30	LCD D20	B115		69000/30	LCD D8
A116		69000/30	LCD D21	B116		69000/30	LCD D9
A117		69000/30	LCD D22	B117		69000/30	LCD D10
A118		69000/30	LCD D23	B118		69000/30	LCD D11
A119		69000/30	LCD ENABKL	B119		69000/30	LCD M
A120		POWER	LCD VCC (3,3V)	B120		CPU	CPU CORE output

*) ePU = external required resistor
iPU = internal placed resistor
eSE = external serial resistor needed
iSE = internal serial resistor
iPD = internal pulled down

6) Internal with 10k to 5V pullup, for ISA-Bus application an external 1k pullup resistor is recommended

- Shaded resistors must be placed externally on the motherboard as close as possible to the module
- PIIX4 treat also as SOUTHBRIDGE
- TX treat also as NORTHBRIDGE

4.2.1 Differences between the smartModules

	SM486PCX	SM586PC	SMP5PC	SMP3PC	SMGXPC	
EXT. MEMORY						
Type:	EDO	SDRAM	SDRAM	SDRAM	SDRAM	
Width	32Bit	32Bit	64Bit	64Bit	64Bit	
MD00 – MD31	yes	yes	yes	yes	Yes	
MD32 – MD63	n.c.	n.c.	yes	yes	Yes	
PCI-BUS	no	yes	yes	yes	Yes	
EXTERNAL BIOS						
BIOSCSin/out	yes	yes (XD bus)	yes (XD bus)	yes (XD bus)	yes (XD bus)	
S-IDE / SDRAM	no	yes	yes	yes	Yes	
J1-B48 – B67	PCMCIA	S-IDE	S-IDE	S-IDE	S-DIE	
J1 B68 – B79	PCMCIA	SDRAM	SDRAM	SDRAM	SDRAM	
Option LAN	Yes	Yes	no	no	Yes	
J1 B100 – B107	Base-T10		n.c.	n.c.	n.c.	
J2 A89 – A90	Base-2	n.c.	IrDA-Select.	IrDA-Select	Audio	
J2 A91 – A95	Base-2	Base-T100	n.c.	n.c.	Base-T100	
J1 B107 & B110	LAN-LED	Ext.SDRAM	Ext.SDRAM	Ext.SDRAM	Ext.SDRAM	
COM3/LCD	24Bit	36Bit	36Bit	36Bit	18Bit	
J2 A81 – A88	COM3	LCD D24-31	LCD D24-31	LCD D24-31	n.c.	
J2 B40	n.c.	LCD D32	LCD D32	LCD D32	n.c.	
J2 B43 – B45	n.c.	LCD D33-35	LCD D33-35	LCD D33-35	n.c.	
USB:						
J2 B34 – B35	n.c.	USB 0	USB 0	USB 0	USB 0	
J2 B81 – B84	n.c.	USB 1	USB 1	USB 1	USB 1	
Specials / APM						
J1 – B80	1.8MHz/ BL0	24MHz	24MHz	24MHz	24MHz	
J2 – A96	BL2	n.c.	SUS-STAT2	SUS-STAT2	n.c.	
J2 – A97	FL_IN	5V-SUS	5V-SUS	5V-SUS	5V-SUS	
J2 – A98	LAN0	GPIO0	SUSA#	SUSA#	n.c.	
J2 – A99	LAN1	GPIO1	SUSB#	SUSB#	n.c.	
J2 – A100	LAN2	GPIO2	SUSC#	SUSC#	SUSC#	
J2 – B31	Sus/Resume	n.c.	PWRBTN#	PWRBTN#	n.c.	
J2 – B33	Sleep Input	GPIO4	LID#	LID#	SLEEP#	
J2 – B100	BL1	GPIO3	SUS-STAT1	SUS-STAT1	n.c.	
J2 – A80	AC Input	PWM	SMI#	SMI#	SMI#	
J2 – B98	ROMWR	DDA	DDA	DDA	DDA	
J2 – B99	ROMRD	DDC	DDC	DDC	DDC	
J2 B94 – B96	CF	n.c.	JTAG	JTAG.	JTAG	
J2 – B88	n.c.	RES1	RES1	RES1	Audio AC97	
J2 B89 – B90	I2C	I2C	SMB	SMB	I2C	
J2 – A97, B97	FLASH	n.c.	JTAG	JTAG	JTAG	
J2 – A89	LAN	RES2	DEN1 (IrDA**)	DEN1 (IrDA**)	Audio AC97	
J2 – A90	LAN	RES3	DEN0 (IrDA**)	DEN0 (IrDA**)	Audio AC97	
J2 – B120	3.3V	2.5V	1.8V	1.3V	2.0V	
J1 B110 – B120	Keymatrix	-	IC-BIOS XD	IC-BIOS XD	IC-BIOS XD	
J2 – A73	n.c.	SDRAM_SEL	SDRAM_SEL	SDRAM_SEL	Audio AC97	
J2 - A78	n.c.	RES4	RES4	PCS0#	Audio AC97	

*) Only for in-circuit test in the production

**) IrDA mode select of the SMC37C672 (Fast IrDA)

4.2.2 Signal lines

Signal or Group	CPU	Type	Current [mA]	Volt [V]	Pullup	Group	Description
A0 – A25	**E**	3 o	8	3.3	none	corebus	addressbus from elan400 for vesa extension
AD0-AD31	**P**	3 i/o	8	3.3	none	PCI	not used on the ELAN400, not connected pins
D0 – D32	**E**	3 i/o	20	3.3	none	corebus	32bit databus for dram and vesa extension
MA0-MA12	**EP**	3 o	20	3.3	none	dram	dram memory address lines for dram extension
MWE	**EP**	3 o	20	3.3	none	dram	dram write enable
RAS 0-3	**EP**	3 o	8	3.3	none	dram	row adress for dram extension
CASH 0-3	**EP**	3 o	8	3.3	none	dram	column adress for dram extension
CASL 0-3	**EP**	3 o	8	3.3	none	dram	column adress for dram extension
KB dat/clk	**EP**	5 o	8	5	1k	kbd	keyboard interface
MS dat/clk	**EP**	5 o	8	5	1k	mouse	mouse interface
COM	**E**	5 o	8	5	none	uart	COM1 if internal ELAN400 uart is enabled
IrDA	**E**	5 o	8	5	none	IrDA	Infrared datalines of the ELAN400
IRQx	**EP**	5 o	8	5	10k	ISA	interrupt request lines
DMAx	**EP**	5 o	4	5	none	ISA	DMA acknowledge
DRQx	**EP**	5 i		5	1k	ISA	DMA request signals
MEMW	**EP**	3 o	4	3.3	none	dram/ISA	write signal for dram and ISA**
MEMR	**EP**	3 o	4	3.3	none	dram/ISA	read signal for dram and ISA**
IOR, IOW	**EP**	5 o	8	5	none	ISA	I/O control lines for ISA bus
SD0-SD15	**EP**	5 i/o	8	5	10k	ISA	ISA datalines
SA0-SA25	**EP**	5 o	8	5	none	ISA	ISA adresslines
LA17-LA19	**EP**	5 o	8	5	none	ISA	ISA latched adresslines, equal to SA17-SA19***
							BIOS & FLASHDISK control lines from ELAN400
BIOSC-Sout	**E**	5 o	4	5	1k	core	Chipselect for the BIOS device must be connected to the BIOSCSin
BIOSCSin	**E**	5 i		5	1k	core	29F040 biosdevice chipselect must be connected to the BIOSCSout
FLASHCS out	**E**	5 o	4	5	1k	core	Chipselect for the FLASHDISK device must be connected to the FLASHCSin
FLASHCSin	**E**	5 i		5	1k	core	29F016 biosdevice chipselect must be connected to the FLASHCSout
SLEEP (B32)	**E**	5 o	4	5	none	core/PM	Power for peripherals: 1 = sleep / 0 = powered ex. MAX211, VGA chip, others, this signal is controlled from the bios powermanagement.
RUN (A33)	**EP**	5 o	4	5	none	core/PM	invers signal of SLEEP: 1= full powered
BLx	**E**	3 i			10k	core/PM	Battery Level sense inputs
							SMC37C6XX Super I/O controller
IDExx	**E**	5 o	8	5	none	ide	peripheral control lines needs 2 x 74HCT245 buffer to control
LPT signals	**EP**	5 i/o	20	5	10k	printer	printer data and control lines, pullup resistors only on the controllines
FD signals	**EP**	5 i/o	20	5	1k	floppy	floppydisk data and control lines
COM1	**EP**	5 i/o	8	5	none	uart	COM1 EXT
COM2	**EP**	5 i/o	8	5	none	uart	COM2 EXT
IrDA	**P**	5 i/o		5	none	IrDA	Fast IrDA

Signal or Group	CPU	Type	Current [mA]	Volt [V]	Pullup	Group	Description ELAN400
LAN	**E**	3 o	2	5.0	none	LAN	10-Base-T and 10-BASE-2 from 91C94/96 SMC controller, The transformator must be placed externally in both interface cases.
LCD	**EP**	3/5 o	8	5.0	none	LCD	VGA digital signals from the VGA Controller
VGA	**EP**	var	-	5.0	none	VGA	CRT output for a VGA Monitor
CF	**EP**	5 i/o	8	5.0	none	CF	CompactFlash control lines
DDA,DDC	**EP**	3 i/o	2	3.3	none	VGA	VESA: Digital Display Control
LAN-LED1	**E**	3 i	10	3.3	none	LAN	ACTIVITY LED (Cathode) LED-Anode over serial resistor to 3.3V connected.
LAN-LED2	**E**	3 i	10	3.3	none	LAN	LINK LED (Cathode) LED-Anode over serial resistor to 3.3V connected.
DX-Bus	**EP**	3 i/o	8	3.3	none	PIIX4	Bus for BIOS-Flashdevice (ext/int) BIOSCS controlls the devices-select. MEMR- and MEMW- controls the datadirection.
AUDIO	**G**	3 i/o	8	3.3	none	GEODE	AC97 codec interface

The **CPU** colon is a hint for which smartModule the signals are refered to:
E = ELAN400
P = PENTIUM
EP = ELAN400 and PENTIUM
G = GEODE

Remarks:
** Must be buffered with 74HCT244 to receive 5V MEMW/MEMR
*** The LA17-LA19 lines are only available to be compatible with ISA busses. On the SMxxPC they are internally connected to the SA17-SA19 signals.

- Please note, that when 3.3/5 signal are mentioned, that this does not mean that both supplies are available on **one** single board.
  It is rather meant, that 5V are for the SM486PCX and all new smartModule are 3.3V signals.
  Check always the appropriate smartManual for details or ask DLAG if you are uncertain.

4.2.3 LCD interface signaldefinition, only for C&T 69000 / 69030 (not for GEODE)

Pin 480BUS	LCD Line	Mono SS 8Bit	Mono DD 8Bit	Mono DD 16Bit	TFT 9/12/16Bit	TFT 18/24Bit	TFT HR 18/24Bit	STN DD 8Bit	STN DD 16Bit	TFT 36Bit
B107	D0	-	UD3	UD7	B0	B0	B00	R1	UR0	O-B0
B108	D1	-	UD2	UD6	B1	B1	B01	G1	UG0	O-B1
B109	D2	-	UD1	UD5	B2	B2	B02	B1	UB0	O-B2
B110	D3	-	UD0	UD4	B3	B3	B03	R2	UR1	O-B3
B111	D4	-	LD3	UD3	B4	B4	B10	G2	LR0	O-B4
B112	D5	-	LD2	UD2	G0	B5	B11	B2	LG0	O-B5
B113	D6	-	LD1	UD1	G1	B6	B12	R3	LB0	E-B0
B114	D7	-	LD0	UD0	G2	B7	B13	G3	LR1	E-B1
B115	D8	P0	-	LD7	G3	G0	G00	B3	UG1	E-B2
B116	D9	P1	-	LD6	G4	G1	G01	R4	UB1	E-B3
B117	D10	P2	-	LD5	G5	G2	G02	G4	UR2	E-B4
B118	D11	P3	-	LD4	R0	G3	G03	B4	UG2	E-B5
A107	D12	P4	-	LD3	R1	G4	G10	R5	LG1	O-G0
A108	D13	P5	-	LD2	R2	G5	G11	G5	LB1	O-G1
A109	D14	P6	-	LD1	R3	G6	G12	B5	LR2	O-G2
A110	D15	P7	-	LD0	R4	G7	G13	R6	LG2	O-G3
A111	D16	-	-	-	-	R0	R00	-	-	O-G4
A112	D17	-	-	-	-	R1	R01	-	-	O-G5
A113	D18	-	-	-	-	R2	R02	-	-	E-G0
A114	D19	-	-	-	-	R3	R03	-	-	E-G1
A115	D20	-	-	-	-	R4	R10	-	-	E-G2
A116	D21	-	-	-	-	R5	R11	-	-	E-G3
A117	D22	-	-	-	-	R6	R12	-	-	E-G4
A118	D23	-	-	-	-	R7	R13	-	-	E-G5
									-	
A81	D24									O-R0
A82	D25									O-R1
A83	D26									O-R2
A84	D27									O-R3
A85	D28									O-R4
A86	D29									O-R5
A87	D30									E-R0
A88	D31									E-R1
B40	D32									E-R2
B43	D33									E-R3
B44	D34									E-R4
B45	D35									E-R5
A106	VS/FLM	FRAME	S	FLM	VSYN	VSYN	VSYN	YD	YD	VS
B106	HS/LP	LOAD	CP1	CL1	HSYN	HSYN	HSYN	LP	LP	HS
B105	SHFCLK	CP	CP2	CL2	CK	CK	CK	XCKL	XCK	SH-Clk
B119	M	DF	-	M	ENAB	ENAB	-	-	-	M
PANEL		Generic	LM64P80 SHARP	LCM-5491 SANYO	LQ9D011 SHARP	LQ10D311 SHARP	LQ10DX01 SHARP	LM64C031 SHARP	LM64C08 Sharp	

4.2.4 CRT monitor signaldefinition

Pin:	Name:	Function:
A101	green	analog output green
A102	blue	analog output blue
A103	red	analog output red
B101	gnd	analog ground
B102	vsynch	vertical synchron signal to the CRT
B103	hsynch	horizontal synchron singla to the CRT

4.2.5 Power lines signaldefinition, SM486PCX

Signal or Group	I/O	Current [mA]	Volt [V]	Toler-ance	Group	Description
VCC	i	950	5.0	+/- 5%	power	Main power supply for CPU and peripheral. From this supply, the onboard switch mode converter generates the 3.3V supply, available on the 3.3V out pins.
VCC_SUS	i	30mA	5.0V	+/- 5%	power	Main power to supply the 3.3V_SUS plane in the module. In powermanagement solutions, this voltage must be ON, even when the main 5V are switched off.
GND	i		0.0		power	Ground
3.3V Out	o	max. 100	3.3	+/- 2%	power	Output of the 3.3V generator of the module, used to supply external 3.3V devices
RTC backup	i	<5 uA	3.0	+ 20%	power	RTC backup supply (3.0V – 3.6V Li-battery). NOT CHARGEABLE !!! This supply must be powered anytime, otherwise the RTC information will be lost. With the onboard battery option, this pin is not connected. Do never charge a Lithium battery !
CORE-VCC Sense pin	o	max.1mA	Core	+/-3%	power	This voltage output is for controlling purposes in the production process only, do not use this pin.

* Normally connected directly to the 3.3V Out power lines.
** May be powered with 3.3V or with 5V supply (depending on the LCD voltage)

4.3 Power supply of the smartModule-480Bus

Supply.:	Voltage / direction:	Current	Tolerance and ripple
VCC	5.0V Input	0.1 – 2Amp	+-5% / 50mV
VCC_SUSPEND	5.0V Input	max. 0.2 Amp	+-5% / 50mV
VCC3	3.3V Output	max. 1 Amp. for external DRAM and PCI-devices	+-5% / 50mV
VBAT	3.6V	0.1 – 2µA	for RTC-backup
VCC2, VCCCORE	1.1V to 2.0V output	for tests only	+-5% / 30mV

4.3.1 Connector specifications

The DIGITAL LOGIC AG smartModule- SMxxPC module connectors are surface mount 0.635mm pitch, 240pin connectors.

Parameter:	Condition:	Specification:
Material:	Contact: Housing:	Beryllium Copper Thermoplast Molded
Electrical:	Current:	0.5 Amp
	Voltage:	100 VAC
	Termination Resistance:	20mOhms
	Insulation Resistance:	500MOhm
Mechanical:	Mating Cycles:	50
	Connector Mating Force:	1N per contact
	Connector Unmating Force:	0.4N per contact
	Pitch:	0.635mm
	Number of pins:	240

The manufacturer of the connector is:

Source on SMxxPC module *:	Part-Name:	Part-Number:
On customers board to hold a SMxxPC h=5mm		
MOLEX 240pin		(53475-2409 *)
	Alternatives:	
	h=6mm (PCB-PCB)	(53467-2409 *)
	h=7mm (PCB-PCB)	(53481-2409 *)
SMxxPC connector h=5mm		
MOLEX 240pin	Mating connector	52760-2409

* Only as a reference.

4.3.2 Suspend mode description

Power state	SUSSTATx	SUSA-	SUSB-	SUSC-
Normal ON	1	1	1	1
Power On Suspend	0	0	1	1
Suspend to RAM	0	0	0	1
Suspend to disk	0	0	0	0
OFF	0	0	0	0

Suspend events:
- LID
- Power button
- SMI
- Timer

Resume events:
- LID
- Power button
- SMI
- Timer

Signal description:
- SUSA- Control of clock PLL supply (currently not used)
- SUSB- Control of CPU supply, DRAM, RTC, TX
- SUSC- Control of all Vcc exept of the PIIX VCCSUS

4.4 Thermal specifications

Each product will undergo a BurnIn-Test of 10 cycles of 30 min. between the operating temperatures of –25°C to +70°C or higher if extended ranges are required.

The critical point is to meet the max. Tcase temperature of the CPU.

This temperature is specified by 110°C for the SQFP case. The tables show the allowable ambient temperature at various airflows and with different heatsink configurations.

CPU: T (case) = 90°C Power consumption:

CPU frequency	Air temperature	T case no Airflow 0 m/sec	T case Airflow 3 m/sec	T case Airflow 6 m/sec
166MHz	70°C			
266MHz	60°C			

These values have to be definitely defined when having series status. See the appropriate manual.

5 PCI ASSIGNMENTS

5.1 Onmodule PCI assignments

Device:	ID-select on address	IRQ-assignments	REQ/GNT-assignments
PIIX4 Southbridge	AD_18	PCI: none ISA-IRQ's: USB, IDE0, IDE1	none
VGA 69000/030	AD_31	none	none
Option LAN 82C559 /ER	(AD_29)	(PIRQA)	(GNT1/REQ1)

5.2 PC/104plus PCI assignments

From the BIOS assigned resources:

Device:	ID-select on address	IRQ-assignments	REQ/GNT-assignments
SLOT1 / MODULE1	AD_20	PIRQA	0
SLOT2 / MODULE2	AD_21	PIRQB	1
SLOT3 / MODULE3	AD_22	PIRQC	2
SLOT4 / MODULE4	AD_23	PIRQD	3

5.3 CompactPCI assignments

From the BIOS assigned resources:

Device:	ID-select on address	IRQ-assignments	REQ/GNT-assignments
PER-SLOT2	AD_31		0
PER-SLOT3	AD_30		1
PER-SLOT4	AD_29		2
PER-SLOT5	AD_28		3
PER-SLOT6	AD_27		4
PER-SLOT7	AD_26		5
PER-SLOT8	AD_25		6

One additional PCI device is allowed on the CompactPCI SystemSlotBoard and uses ID-selects in the range of AD11 to AD24. Also PCI devices on a segment behind a PCI2PCI bridge uses the ID-Select AD11 to AD24.

5.4 ATX-board PCI-BUS assignments

From the BIOS assigned resources:

Device:	ID-select on address	IRQ-assignments	REQ/GNT-assignments
PER-SLOT1	AD_	PIRQ-A	0
PER-SLOT2	AD_	PIRQ-B	1
PER-SLOT3	AD_	PIRQ-C	2
PER-SLOT4	AD_	PIRQ-D	3

(not defined yet)

6 DESIGNIN BLOCK SCHEMATICS

ATTENTION:

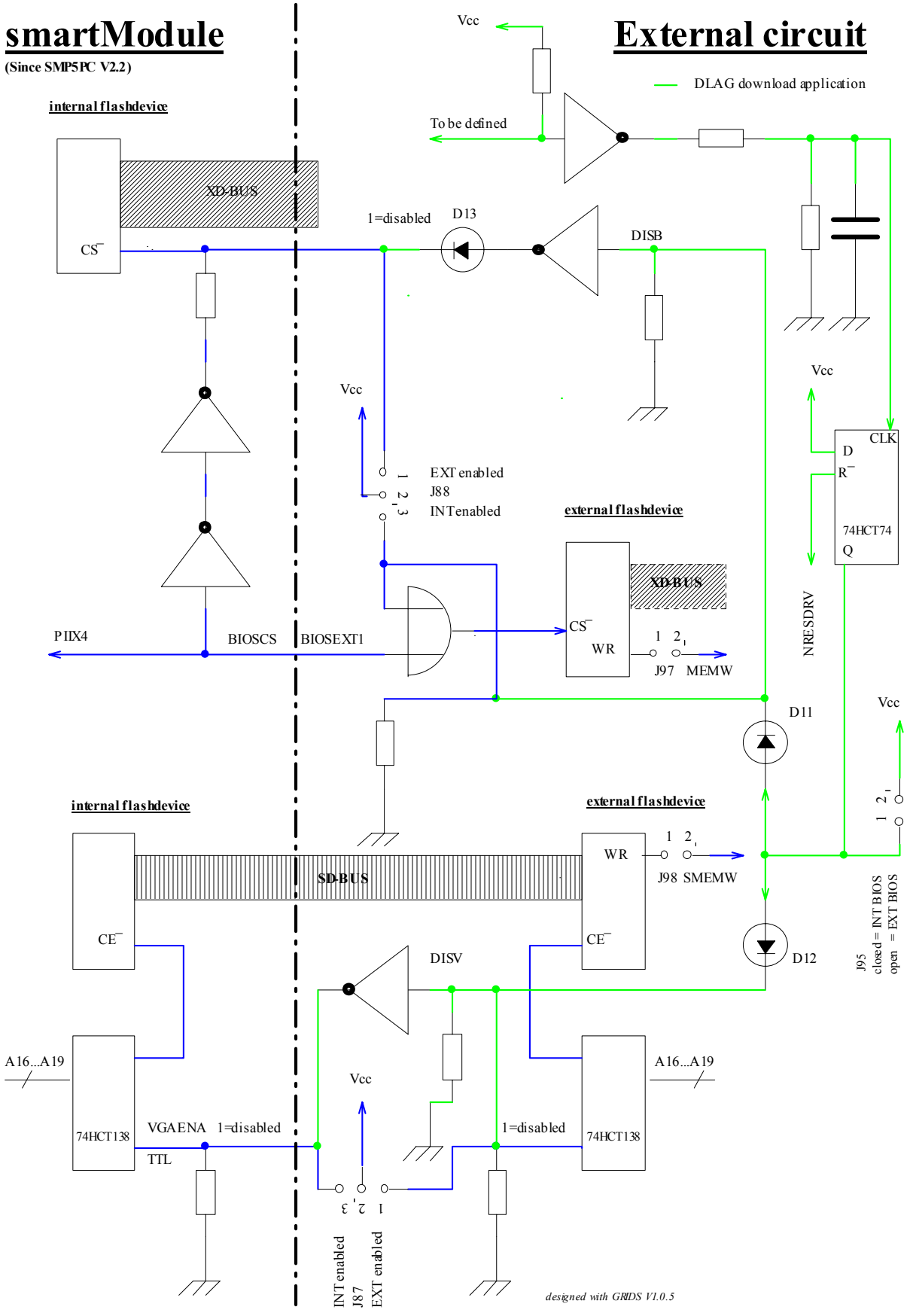
Very important information for smartModule integrators.

1. The minimum schematics to operate with the smartModule-P5PCX is described further on.
   Place on the 5Volt line 10x 100nF capacitors nearest possible at the powerpins.
2. Place on the 5Volt line 4 x 100µF/16V and 2 x 330µF tantal capacitors.
3. Use a separate ground and 5Volt plane in the OEM PCB.
4. If 3.3V DRAM extension are used, integrate a 3.3V powerplane to supply the DRAMs and other 3.3V parts.
   The 3.3V supply may be loaded with max. 300mA.
   Place also on the 3.3V plane 5 to 10 x 100nF and 2 x 100µF capacitors, nearest possible to the supply pins of each components.
   Place the DRAMs directly under the smartModule.
5. To meet all EMI/EMC parameters, place on every peripheral line (go to external cables) a ferrite (TDK) and a 47pF capacitor to ground.
6. All generic pullup resistor should be 10k typ
7. All generic buffers are recommended to be 74HCT245/244 or 74ABT245/244 type.
8. If using SODIMM's, please refer to our overview list, which is also on our CD. Cleaning the contacts on the SODIMM and the socket with e.g. pure alcohol is highly recommended to may eliminate memory errors.
9. For any questions, we are providing a DesignIn support. Please fill out the form in chapter 1.5 to initialize a DesignIn support.

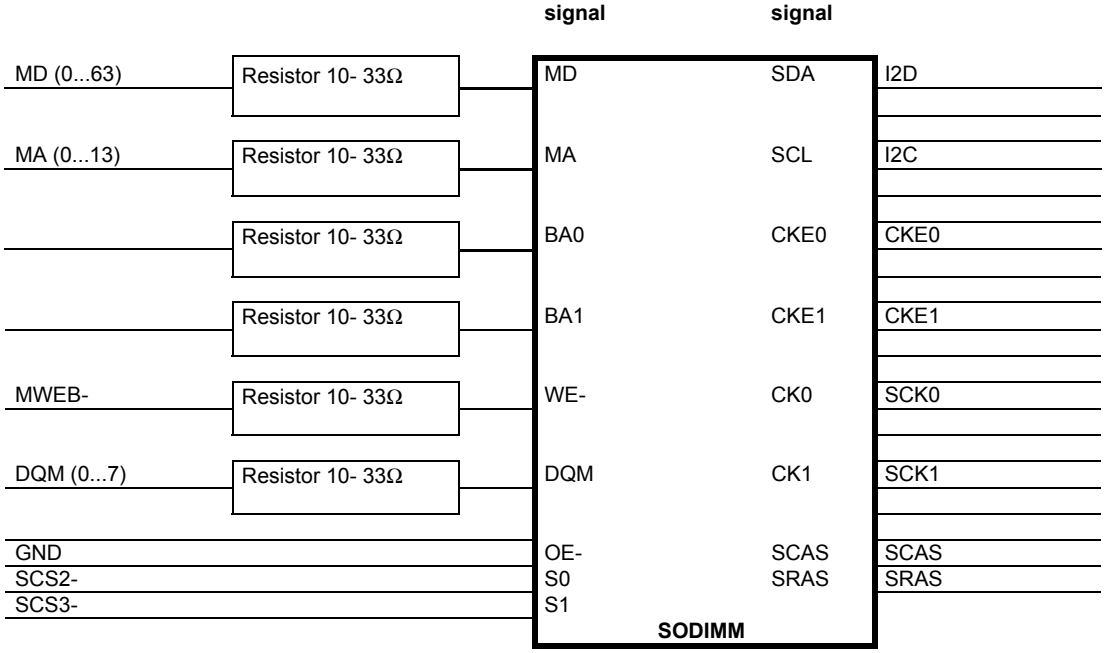
6.1 Samples Schematics SMP5PC- DK and SM486PCX- EK

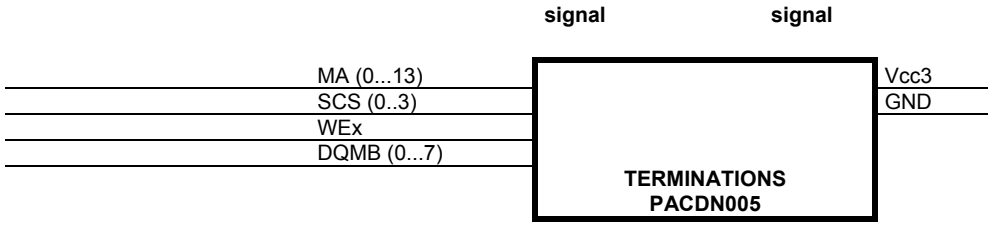
On the following pages, one will see the schematics for the SMP5PC- (V2.1) and SM486PCX- development kit .

6.2 Application to use the downloadtool for the external VGA BIOS.

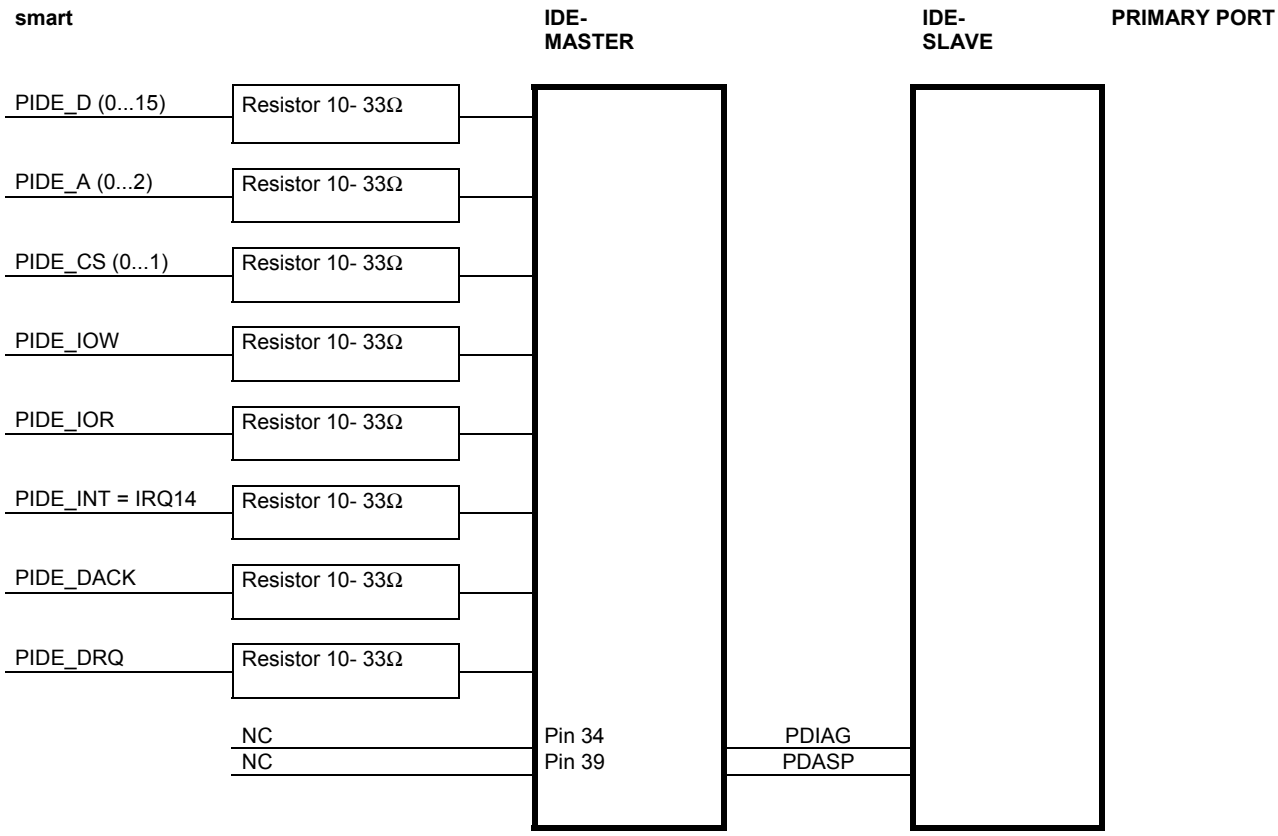


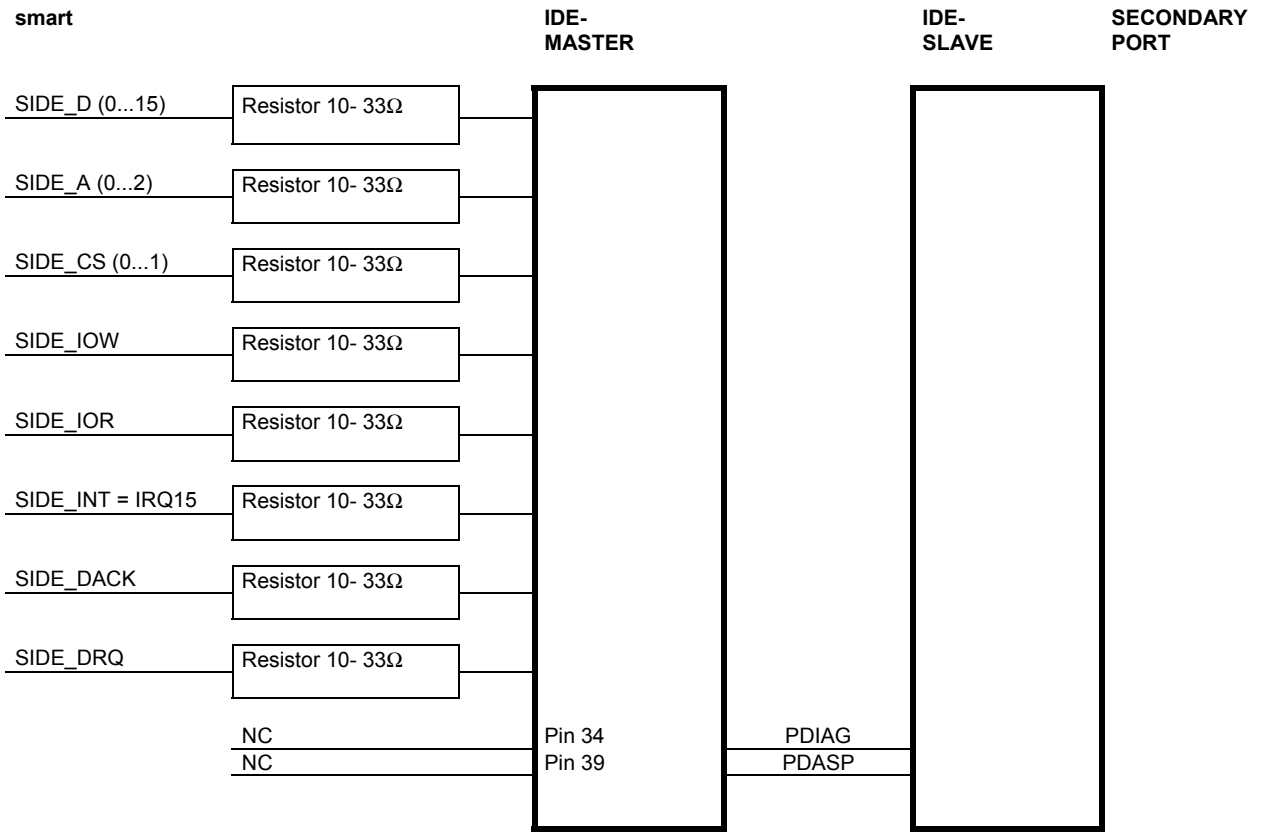
6.3 Application for external DRAM (SODIMM 144pins)



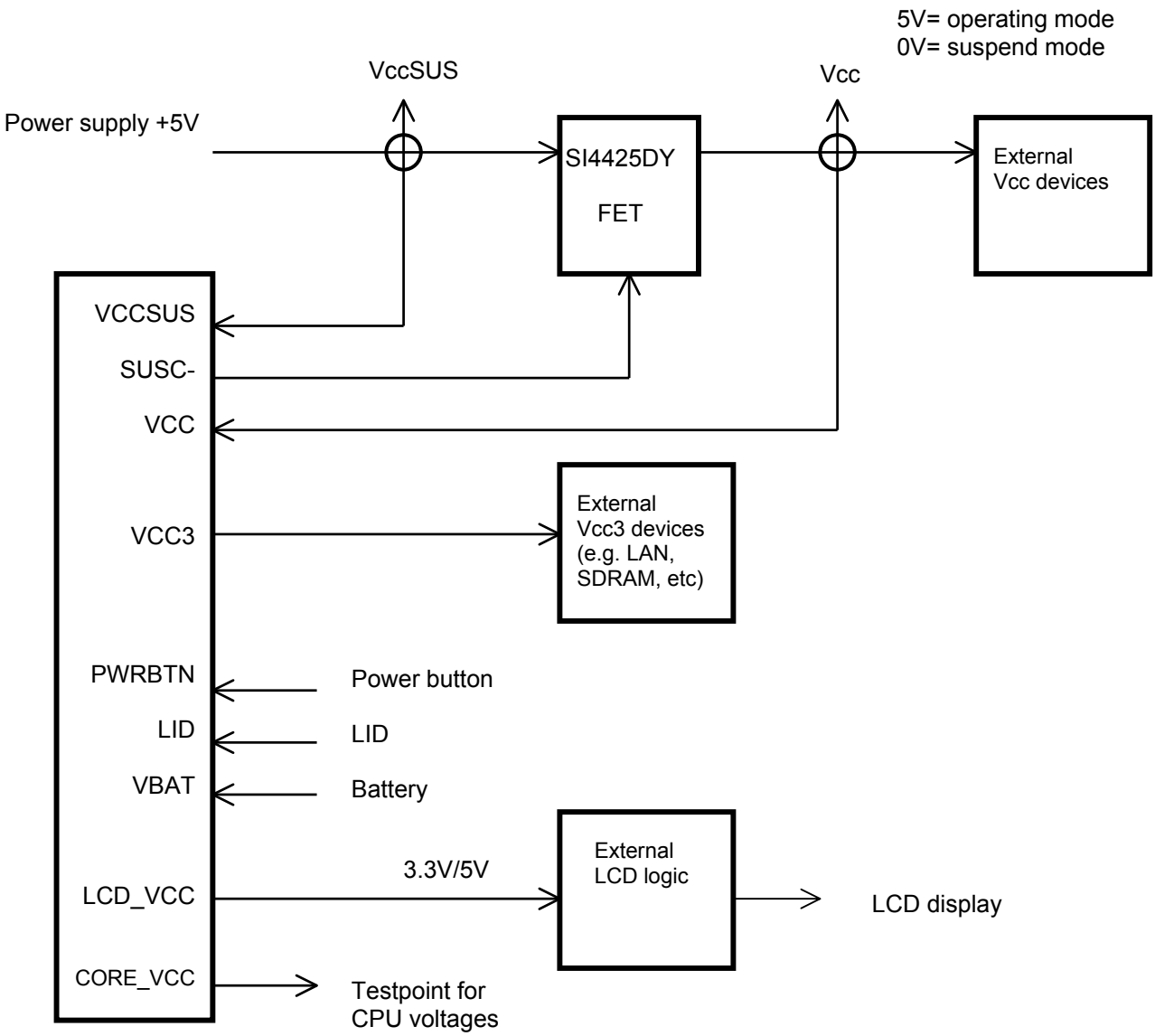


6.4 Application for external IDE's



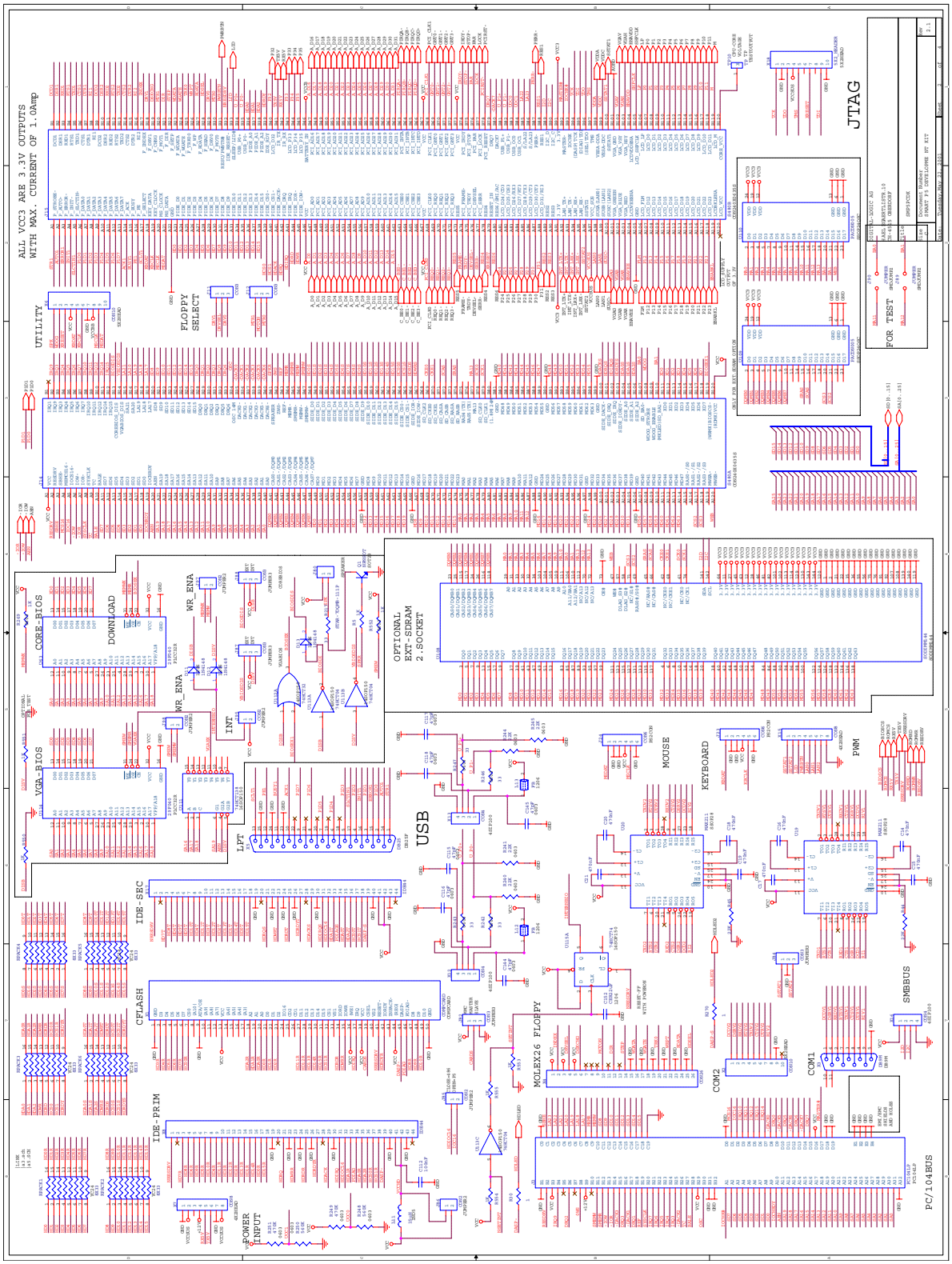


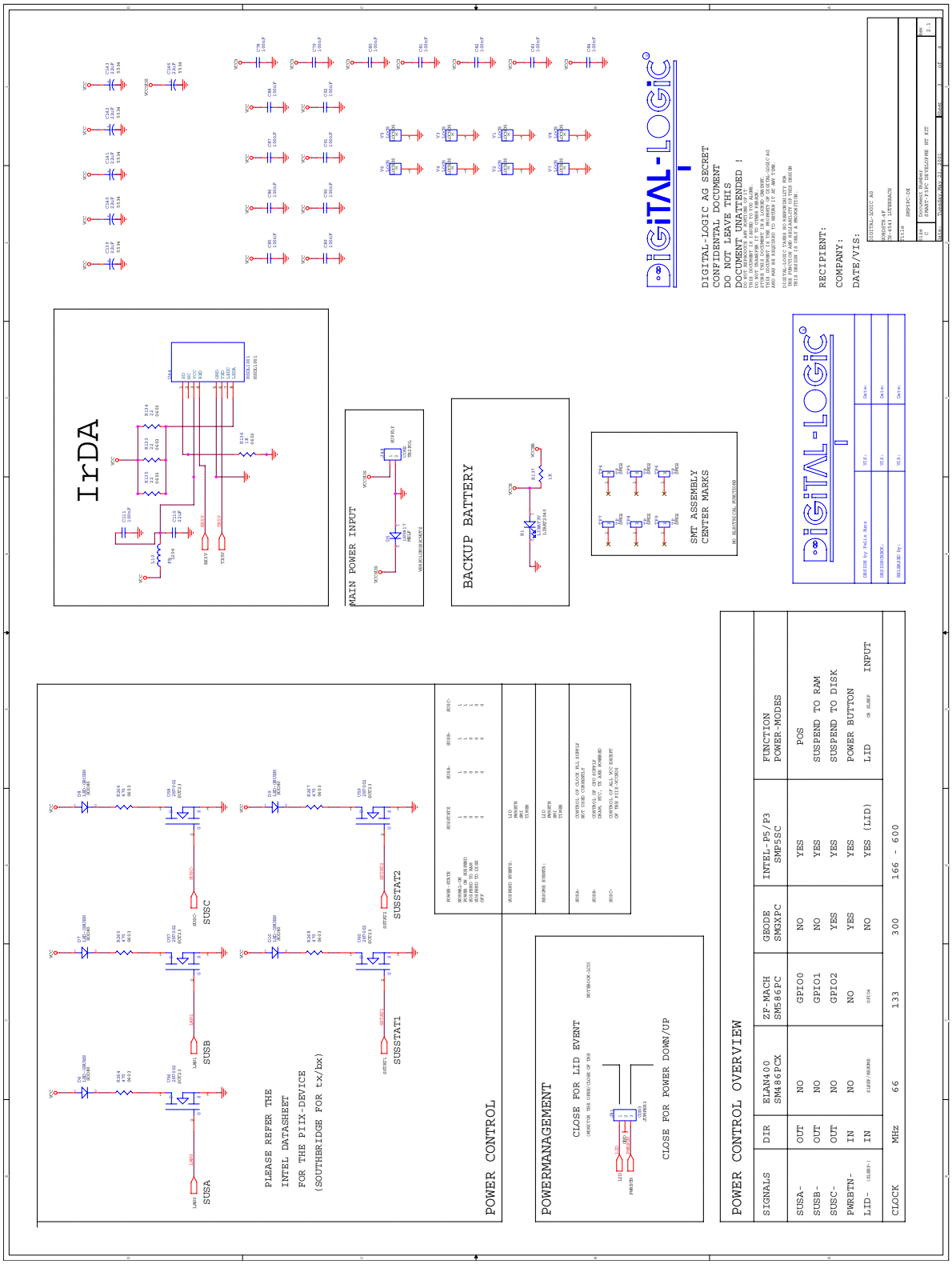
6.5 Application for the ATX power supply

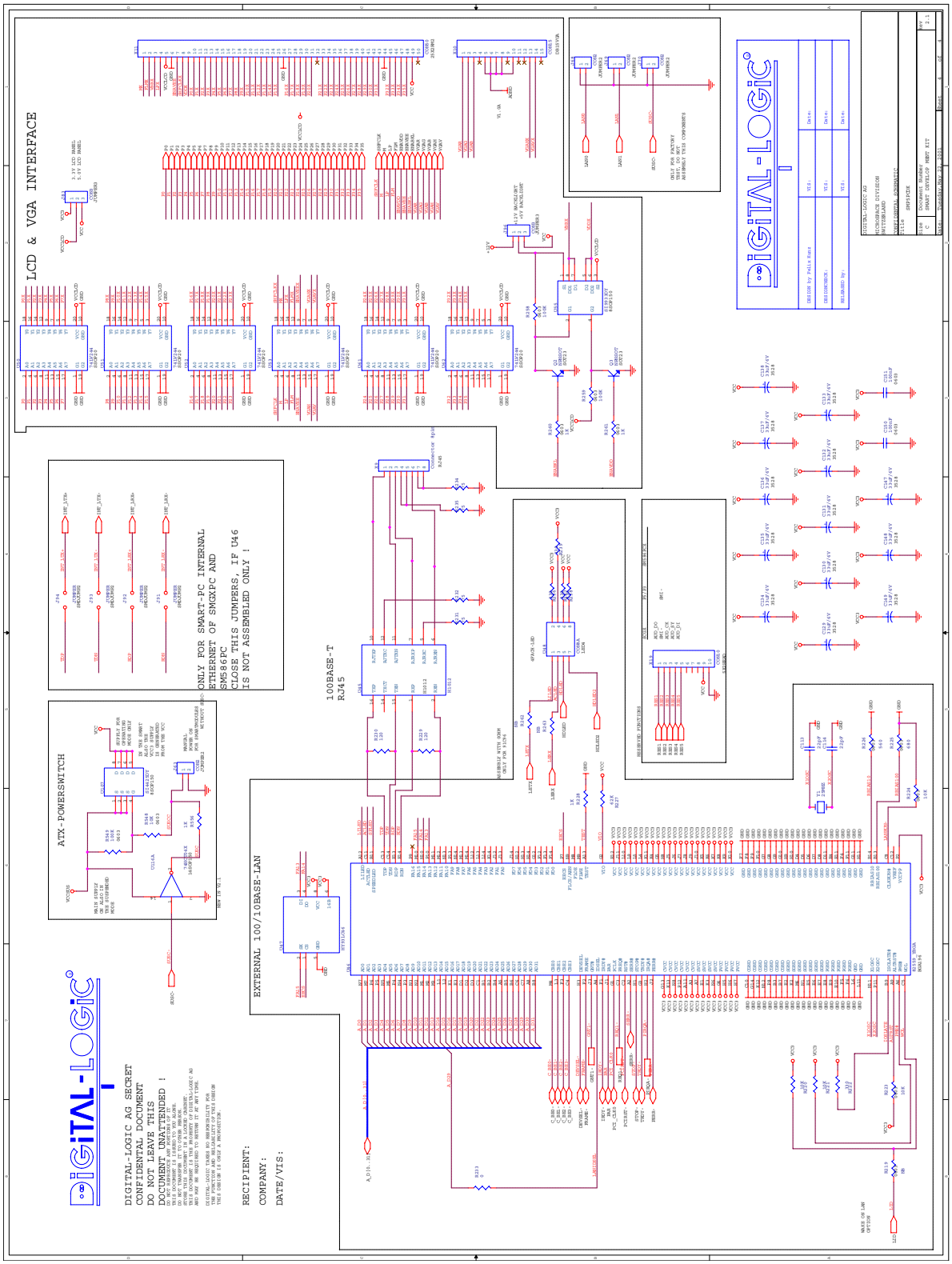


6.6 Application AC97 CODEC for the SMGXPC

Is now part of the smartModule (optional).

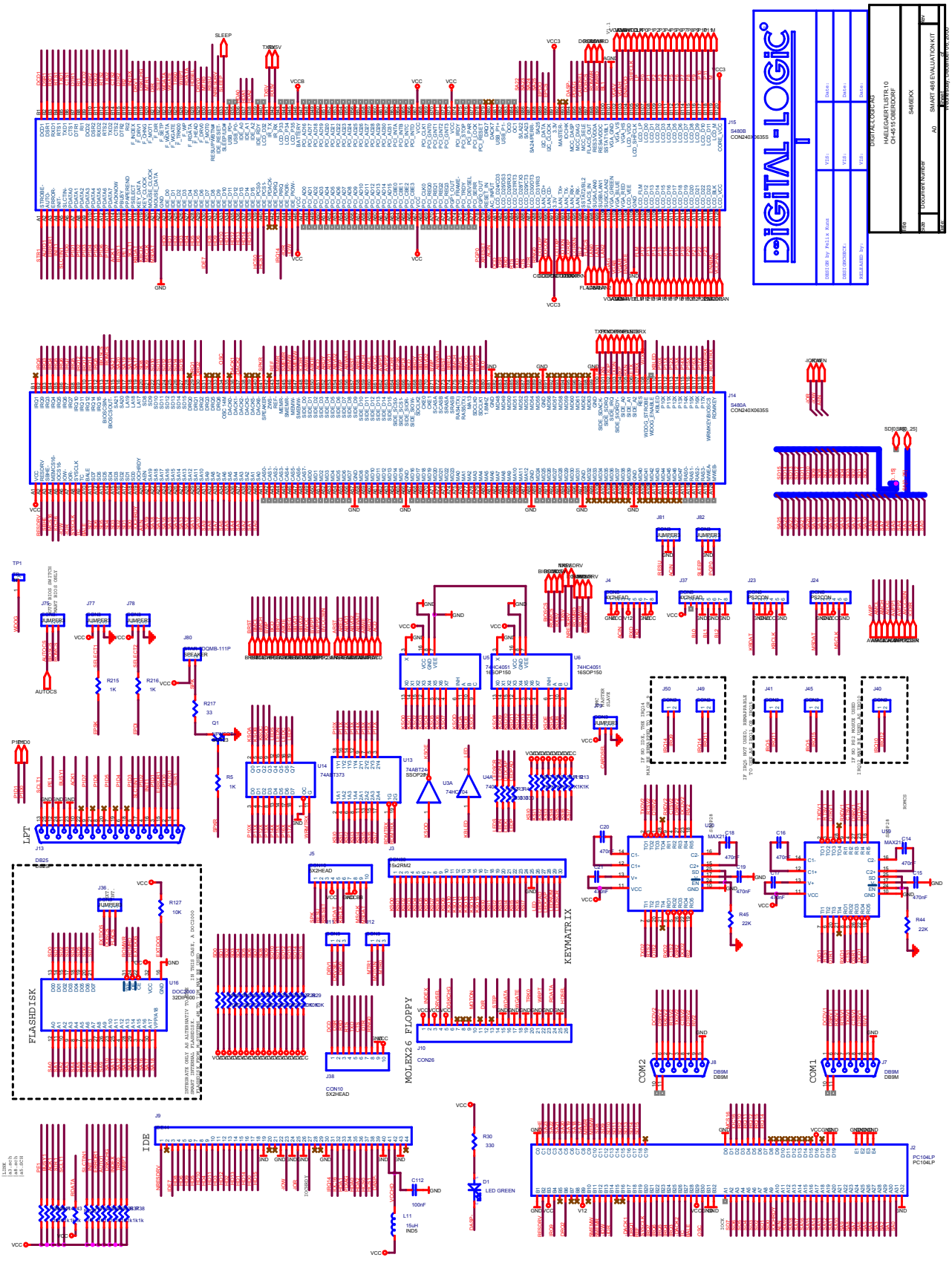

ALL VCC3 ARE 3.3V OUTPUTS
WITH MAX. CURRENT OF 1.0Amp
JTAG
FOR TEST
UTILITY
FLOPPY SELECT
CORE-BIOS
DOWNLOAD
VGA-BIOS
WR_ENA
INT
OPTIONAL EXT-SDRAM 2.SOCKET
USB
LPT
MOUSE
KEYBOARD
PWM
SMBBUS
IDE-SEC
IDE-PRIM
CFLASH
MOLEX26 FLOPPY
COM2
COM1
POWER INPUT
PC/104BUS


IrDA
MAIN POWER INPUT
BACKUP BATTERY
SMT ASSEMBLY
CENTER MARKS
POWER CONTROL
SUSA
SUSB
SUSC
SUSSTAT1
SUSSTAT2
PLEASE REFER THE
INTEL DATASHEET
FOR THE PIIX-DEVICE
(SOUTHBRIDGE FOR tx/bx)
POWERMANAGEMENT
CLOSE FOR LID EVENT
CLOSE FOR POWER DOWN/UP
POWER CONTROL OVERVIEW
SIGNALS
DIR
ELAN400 SM486PCX
ZF-MACH SM586PC
GEODE SMGXPC
INTEL-P5/P3 SMP5SC
FUNCTION POWER-MODES
SUSA- OUT NO GPIO0 NO YES POS
SUSB- OUT NO GPIO1 NO YES SUSPEND TO RAM
SUSC- OUT NO GPIO2 YES YES SUSPEND TO DISK
PWRBTN- IN NO NO YES YES POWER BUTTON
LID- IN NO NO YES YES (LID) LID INPUT
CLOCK MHz 66 133 300 166 - 600
DIGITAL-LOGIC AG SECRET
CONFIDENTIAL DOCUMENT
DO NOT LEAVE THIS
DOCUMENT UNATTENDED !
RECIPIENT:
COMPANY:
DATE/VIS:


LCD & VGA INTERFACE
ATX-POWERSWITCH
100BASE-T
RJ45
EXTERNAL 100/10BASE-LAN
ONLY FOR SMART-PC INTERNAL
ETHERNET OF SMG3PC AND
SM586PC
CLOSE THIS JUMPERS, IF U46
IS NOT ASSEMBLED ONLY !
DIGITAL-LOGIC AG SECRET
CONFIDENTIAL DOCUMENT
DO NOT LEAVE THIS
DOCUMENT UNATTENDED !
RECIPIENT:
COMPANY:
DATE/VIS:

6.7 SM486PCX- EK

On the following pages are the schematics for the SM486PCX- EK.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DIGITAL-LOGIC AG
HAELEGAERTLISTR 10
CH-4515 OBERDORF
S480BX
SMART 486 EVALUATION KIT
A0
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CON240X0635S
S480A
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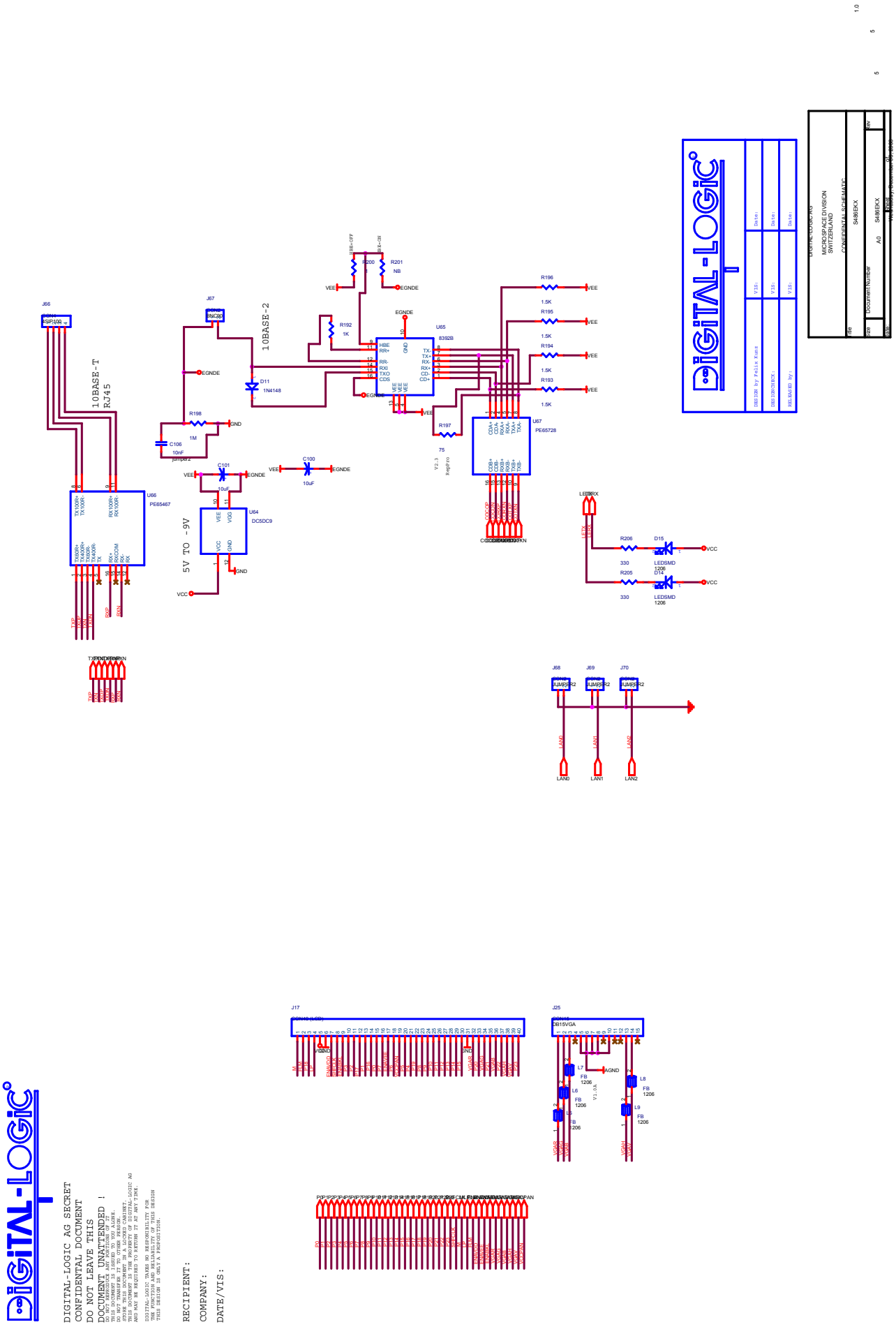
IDE
FLOPPY
MOLEX2.6
KEYMATRIX
COM2
COM1
PC104LP


10BASE-T
RJ45
10BASE-2
5V TO -9V
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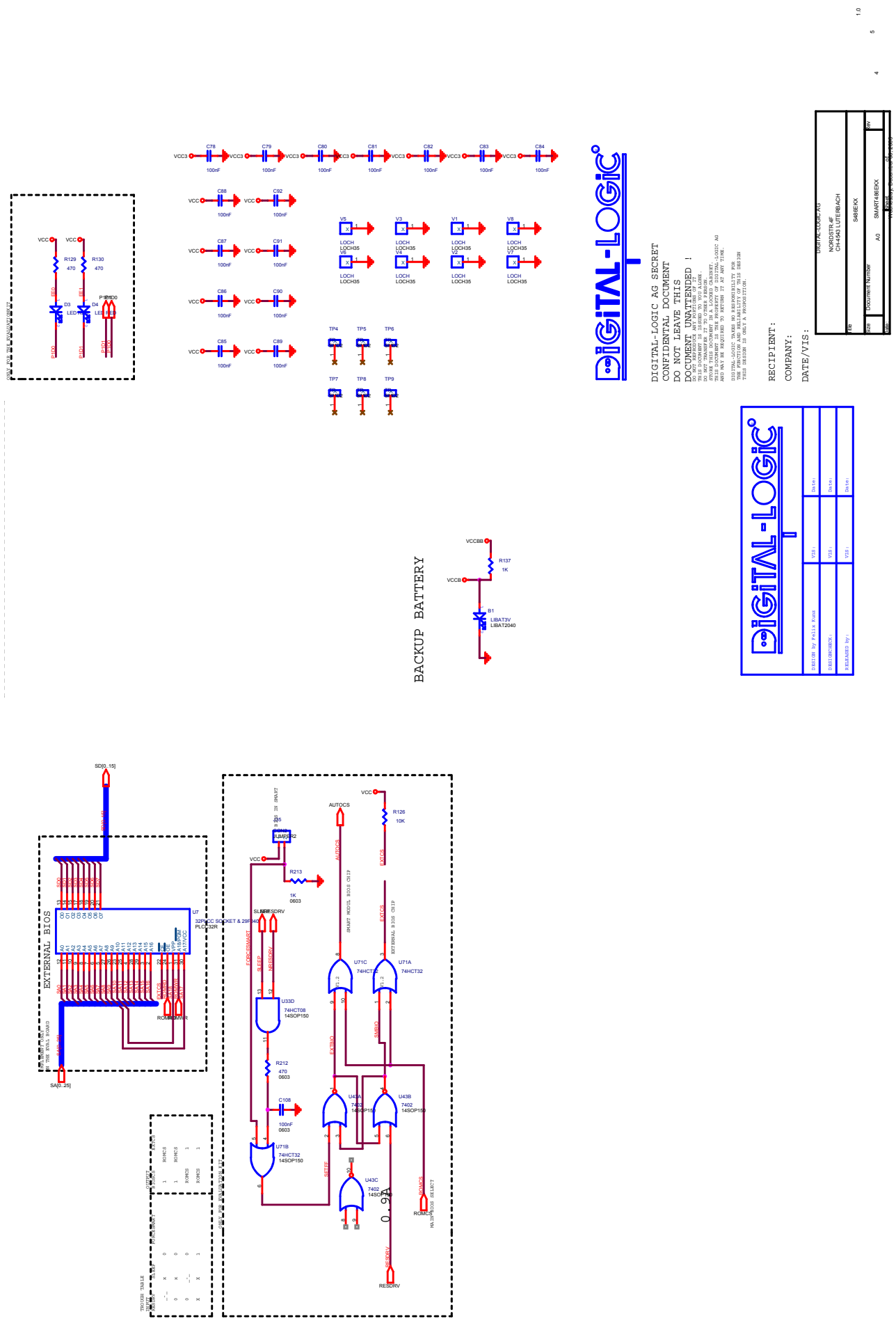
RECIPIENT:
COMPANY:
DATE/VIS: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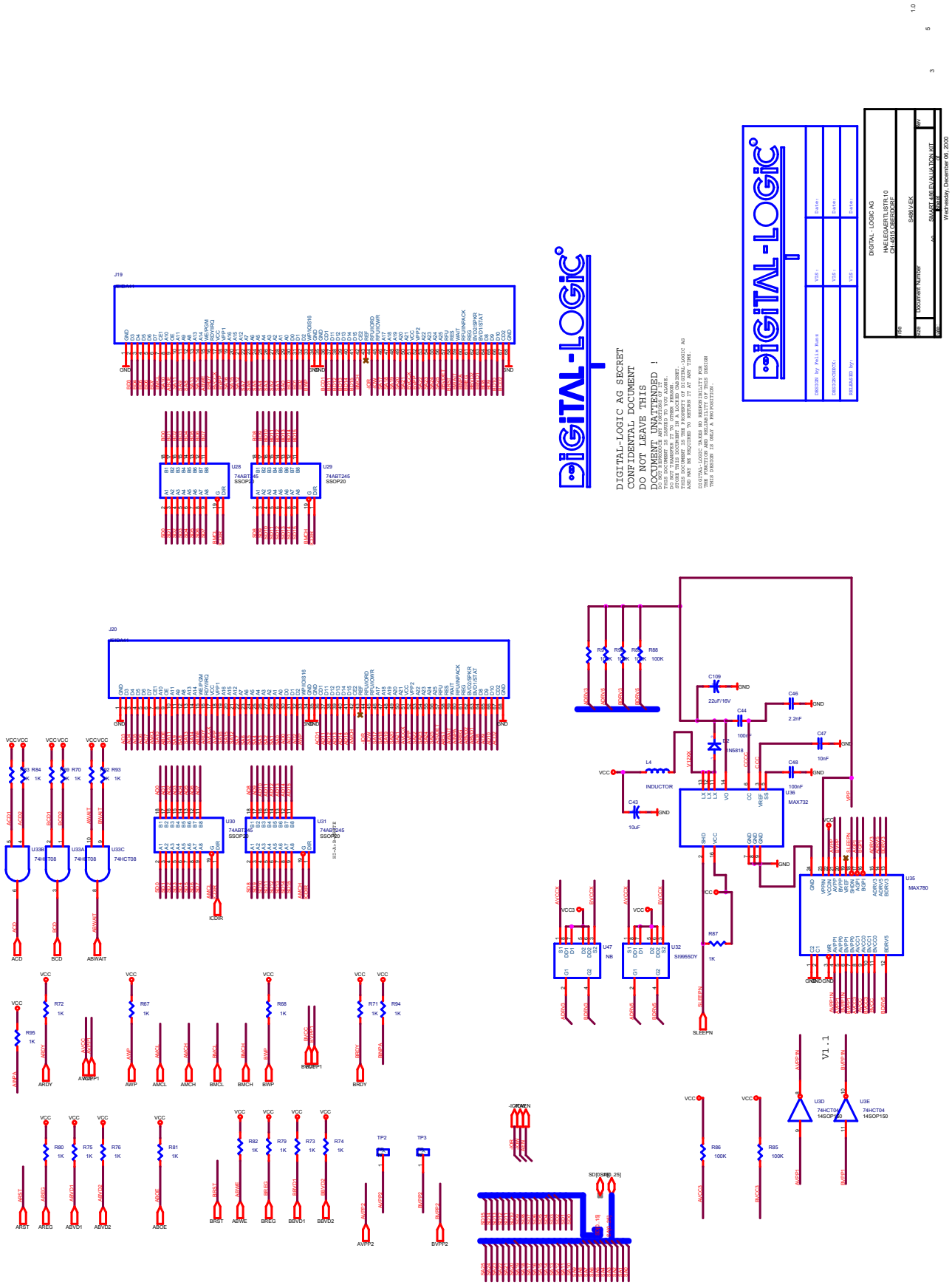
DO NOT LEAVE THIS
DOCUMENT UNATTENDED !
RECIPIENT:
COMPANY:
DATE/VIS:
BACKUP BATTERY
EXTERNAL BIOS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DIGITAL-LOGIC AG
HAELEGAERTLISTR.10
CH-4515 OBERDORF
S480V-EK
SM480 EVALUATION KIT
Wednesday, December 06, 2000
J19
J20
U28
74ABT245
SSOP20
U29
74ABT245
SSOP20
U30
74ABT245
SSOP20
U31
74ABT245
SSOP20
U33B
74HCT08
U33A
74HCT08
U33C
74HCT08
U36
MAX732
U35
MAX780
U47
NB
U32
SI9955DY
U3D
74HCT04
14SOP150
U3E
74HCT04
14SOP150
L4
INDUCTOR
C109
22uF/16V
C46
2.2nF
C44
100nF
C47
10nF
C48
100nF
C43
10uF
R87
1K
R88
100K
R86
100K
R85
100K
R95
1K
R72
1K
R67
1K
R68
1K
R71
1K
R94
1K
R80
1K
R75
1K
R76
1K
R81
1K
R82
1K
R79
1K
R73
1K
R74
1K
TP2
TP3
ACD
BCD
ABWAIT
ICDIR
ARDY
AWP
AMCL
AMCH
BMCL
BMCH
BWP
BRDY
ARST
AREG
ABVD1
ABVD2
ABDE
BRST
ABWE
BREG
BBVD1
BBVD2
AVPP2
BVPP2
SLEEPN
V1.1

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