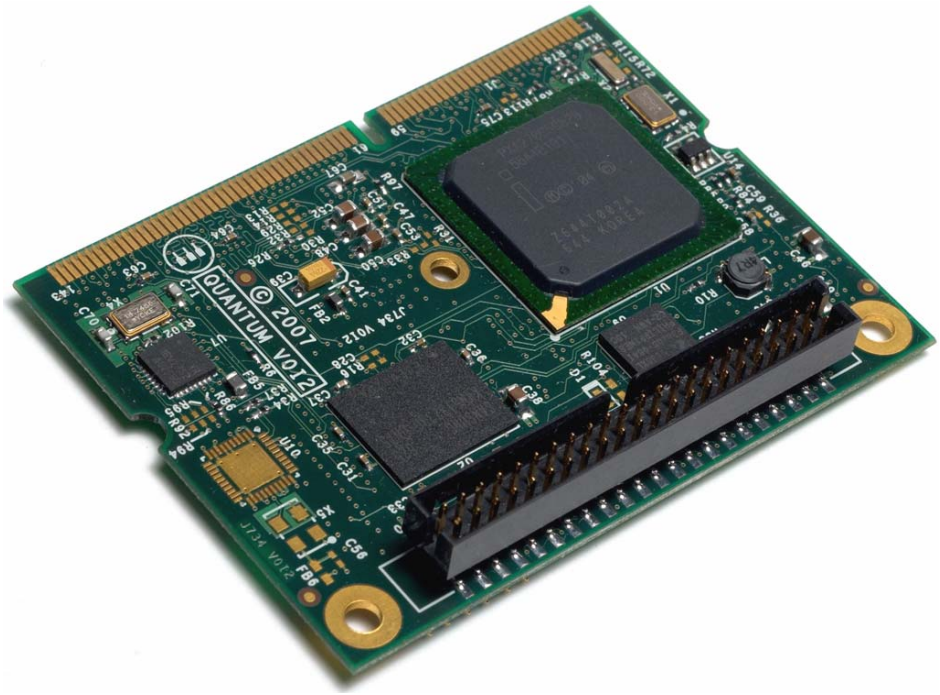
QUANTUM

Intel PXA270 XScale RISC based SODIMM Single Board Computer

Technical Manual



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Revision History

Manual	*PCB*	*Date*	*Comments*
Issue A	V0 Issue 2	1st October 2007	First full release for QUANTUM Version 0I2.

For contact details, see page 55.

ISO 9001
FM12961

Contents

Product handling and environmental compliance

Anti-static handling

This board contains CMOS devices that could be damaged in the event of static electricity being discharged through them. At all times, please observe anti-static precautions when handling the board. This includes storing the board in appropriate anti-static packaging and wearing a wrist strap when handling the board.

Packaging

Please ensure that should a board need to be returned to Eurotech Ltd, it is adequately packed, preferably in the original packing material.

Electromagnetic compatibility (EMC)

The QUANTUM is classified as a component with regard to the European Community EMC regulations and it is the user's responsibility to ensure that systems using the board are compliant with the appropriate EMC standards.

RoHS compliance

The European RoHS Directive (Restriction on the use of certain Hazardous Substances – Directive 2002/95/EC) limits the amount of six specific substances within the composition of the product. The QUANTUM and associated accessory products are available as RoHS-6 compliant options and are identified by a -R6 suffix in the product order code. A full RoHS Compliance Materials Declaration Form is included in Appendix G – RoHS-6 compliance - Materials Declaration Form, page 21. Further information about RoHS compliance is available on the Eurotech Ltd web site at www.eurotech-ltd.co.uk.

Introduction

The QUANTUM is an ultra low-power, low-cost single board computer, based on the Intel PXA270 XScale® processor. The PXA270 is an implementation of the Intel XScale micro-architecture combined with a comprehensive set of integrated peripherals, including a flat panel graphics controller, interrupt controller, Real Time Clock and various serial interfaces. The QUANTUM board is based on the standard SO-DIMM form factor module. The QUANTUM board offers a wide range of features, making it ideal for power-sensitive embedded communications, asset monitoring solutions and compact MMI solutions.

The board is available in the following seven variants (the standard variant is QUANTUM 520-M64-F32-04, others are available on request):

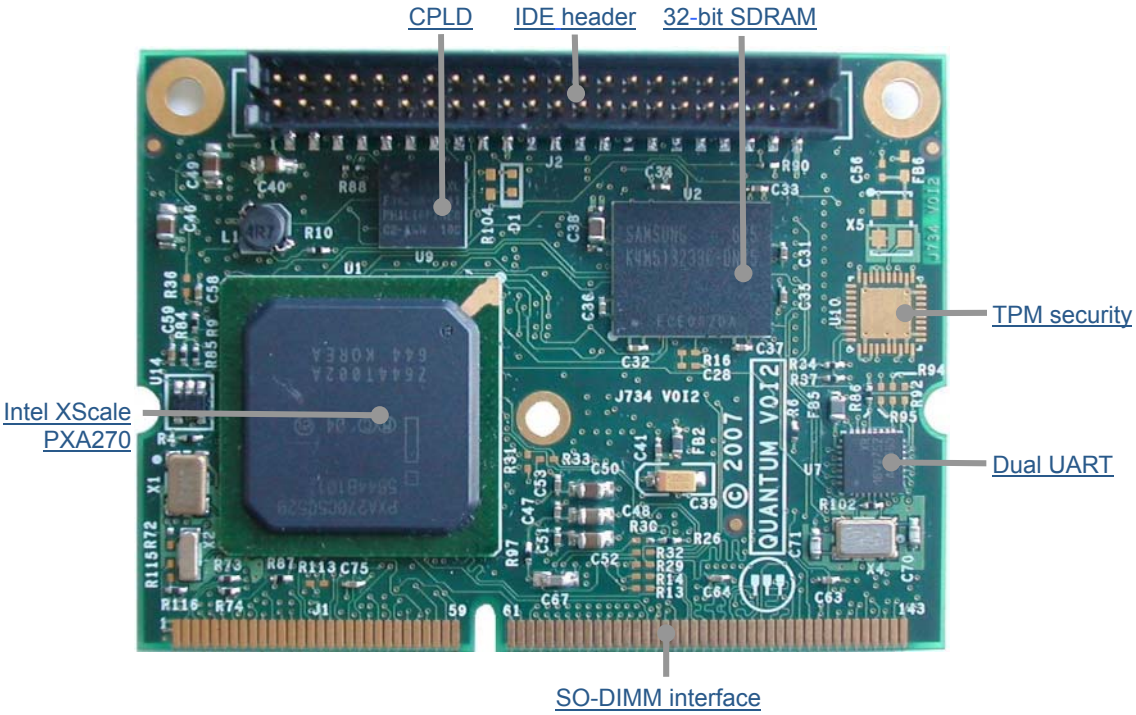
QUANTUM 312-M64-F1-01	312MHz PXA270, 64MB SDRAM, 1MB Flash. No AC'97 on-board, no external RTC on-board.
QUANTUM 520-M64-F64-02	520MHz PXA270, 64MB SDRAM, 64MB Flash. No AC'97 on board, external RTC on-board.
QUANTUM 312-M64-F32-03	312MHz PXA270, 64MB SDRAM, 32MB Flash. No AC'97 on-board, external RTC on-board.
QUANTUM 520-M64-F32-04	520MHz PXA270, 64MB SDRAM, 32MB Flash. AC'97 on-board, external RTC on-board.
QUANTUM 312-M64-F32-05	312MHz PXA270, 64MB SDRAM, 32MB Flash. AC'97 on-board, external RTC on-board.
QUANTUM 520-M64-F64-06	520MHz PXA270, 64MB SDRAM, 64MB Flash. No AC'97 on-board, no external RTC on-board.
QUANTUM 520-M64-F1-07	520MHz PXA270, 64MB SDRAM, 1MB Flash. No AC'97 on-board, no external RTC on-board.

An industrial temperature version is available on request. The QUANTUM board is fully RoHS-6 compliant.

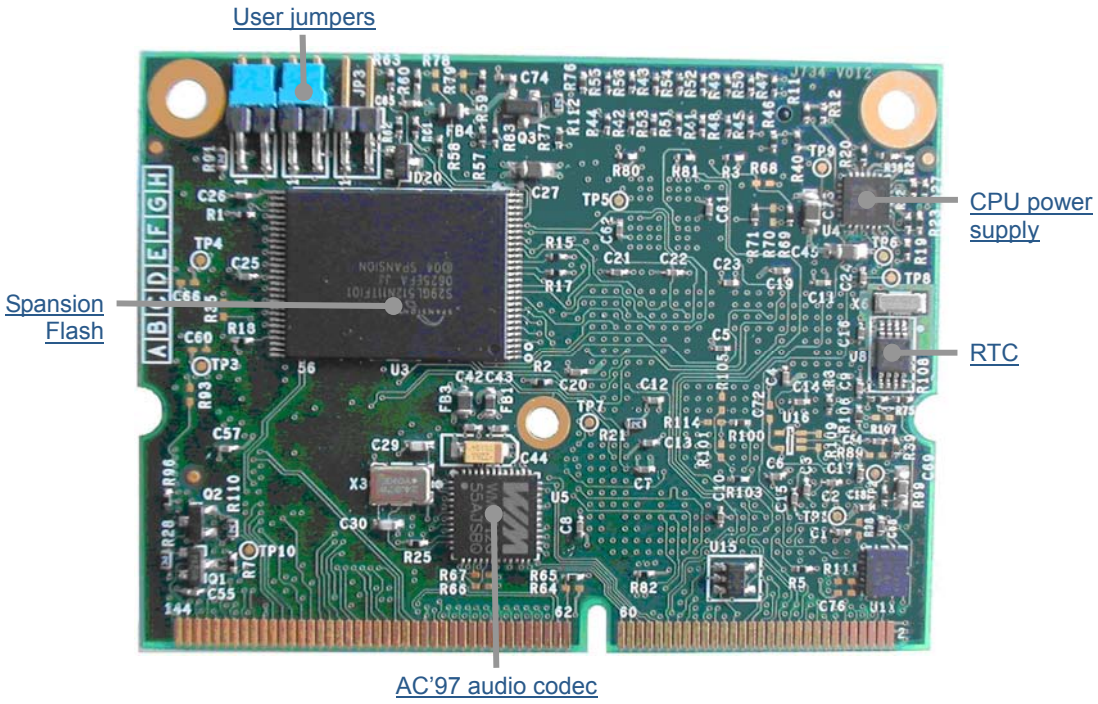
For alternative board configurations, please contact Eurotech Ltd (see Appendix A – Contacting Eurotech Ltd, page 55, for contact details).

QUANTUM ‘at a glance’

Top view



Bottom view



QUANTUM features

Processor	Intel PXA270 312/416/520MHz XScale® Processor 520MHz as standard
System memory	Fixed on-board Up to 64MB SDRAM (32-bit wide SDRAM data bus)
Silicon disk	Fixed on-board memory 1/16/32/64MB on-board Flash
5 serial ports	Three UART serial ports: • FFUART • BTUART • Standard UART Dual extra high-speed full function UART: • 16C2552 compatible UART • RS485 half-duplex direction control
USB support	USB 1.1 host/client controller port supporting 12Mb/s and 1.5Mb/s speeds USB 1.1 host controller port supporting 12Mb/s and 1.5Mb/s speeds
Extension interfaces	IDE/bus extension on-board interface (for 3.3V devices only) MMC/SD/SDIO interface I^2C bus CompactFlash interface bus Two synchronous serial ports (SSP)
Video	16-bit flat panel interface (for STN and TFT displays)
Audio codec and touchscreen	AC'97 compatible codec Line In, Line Out, Microphone In Touchscreen support – 4-wire analogue resistive
RTC	Battery-backed RTC device**
TPM	Atmel Trusted Platform module device, TCG v1.2 compatible (optional)
GPIO	Up to seventy eight (depends on used interfaces)
PWM	Two (Four optionally) x PWM output
Test support	JTAG interface
Power requirements	3.3V/0.7A maximum

Mechanical	SO-DIMM factor, 67.6mm x 50mm
Environmental	Operating temperature: • Industrial: -40 to +85°C* * • Commercial: -20 to +70°C* * RoHS Directive: Compliant

** The battery is not a part of the board, it should be connected to the dedicated SO-DIMM pin

QUANTUM support products

The QUANTUM is supported by the following products:

QUANTUM Base Board

The QUANTUM Base Board (V2 – J764 V1I1) is offered as part of the QUANTUM development kit and enables the following QUANTUM peripheral connectivity:

- CompactFlash card socket (on-board WLAN module optionally).
- MMC/SD (miniSD) card socket.
- FFUART, BTUART and IRUART serial ports (on-board Bluetooth® module on BTUART optionally).
- Two Ext UART serial ports.
- Four standard USB host ports (for standard client devices, i.e. mouse, keyboard, USB flash disk, etc).
- B or mini B-format USB connector (these two connectors have a parallel connection, allowing the QUANTUM module to be connected in client mode to a USB host).
- Three analogue audio jack plugs (stereo Line In, stereo Line Out and Microphone In) provided by QUANTUM WM9712 AC'97 codec.
- Hitachi 3.8" TX09D50VM1CCA LCD connector, universal 2x17 pin header for other LCDs and a 5-pin header for a touchpanel.
- Two 10 pin headers for SPI1, SPI2, I2C, RS485, PWM outputs and GPIO.
- Two 22 pin bus expansion headers, providing:
  - IDE interface, or
  - 16-bit expansion bus, for the addition of add-on modules.
- VGA and composite Video-Out provided by Focus FS453 data video encoder.

QUANTUM Ethernet module

QUANTUM Ethernet module is a DoM (Disk-on-Module) form factor board which extends the QUANTUM module by Ethernet connectivity. The module includes the magnetics and a standard RJ-45 Ethernet port connector. This can be particularly beneficial for Windows CE installation, commissioning and application download. This module could be used by customers during their own commissioning processes. The Ethernet port can be connected via a standard RJ45 or alternatively, a low-profile header. More information about the Ethernet Davicom DM9000A device can be found at www.davicom.com.tw/eng/products/dm9000a.htm.

About this manual

This manual describes the operation and use of the QUANTUM module. It is designed to be a reference and user manual and includes information about all aspects of the board.

Conventions

Symbols

The following symbols are used in this guide:

Symbol	Explanation
	Note - information that requires your attention.
	Tip - a handy hint that may provide a useful alternative or save time.
	Caution – proceeding with a course of action may damage your equipment or result in loss of data.
	Jumper is fitted.
	Jumper is not fitted.

Getting started

A *QUANTUM Quickstart Manual* is provided with each development kit to help you set up and start using the QUANTUM board. Please read this manual and follow the steps explaining how to set up the board and get it up and running.

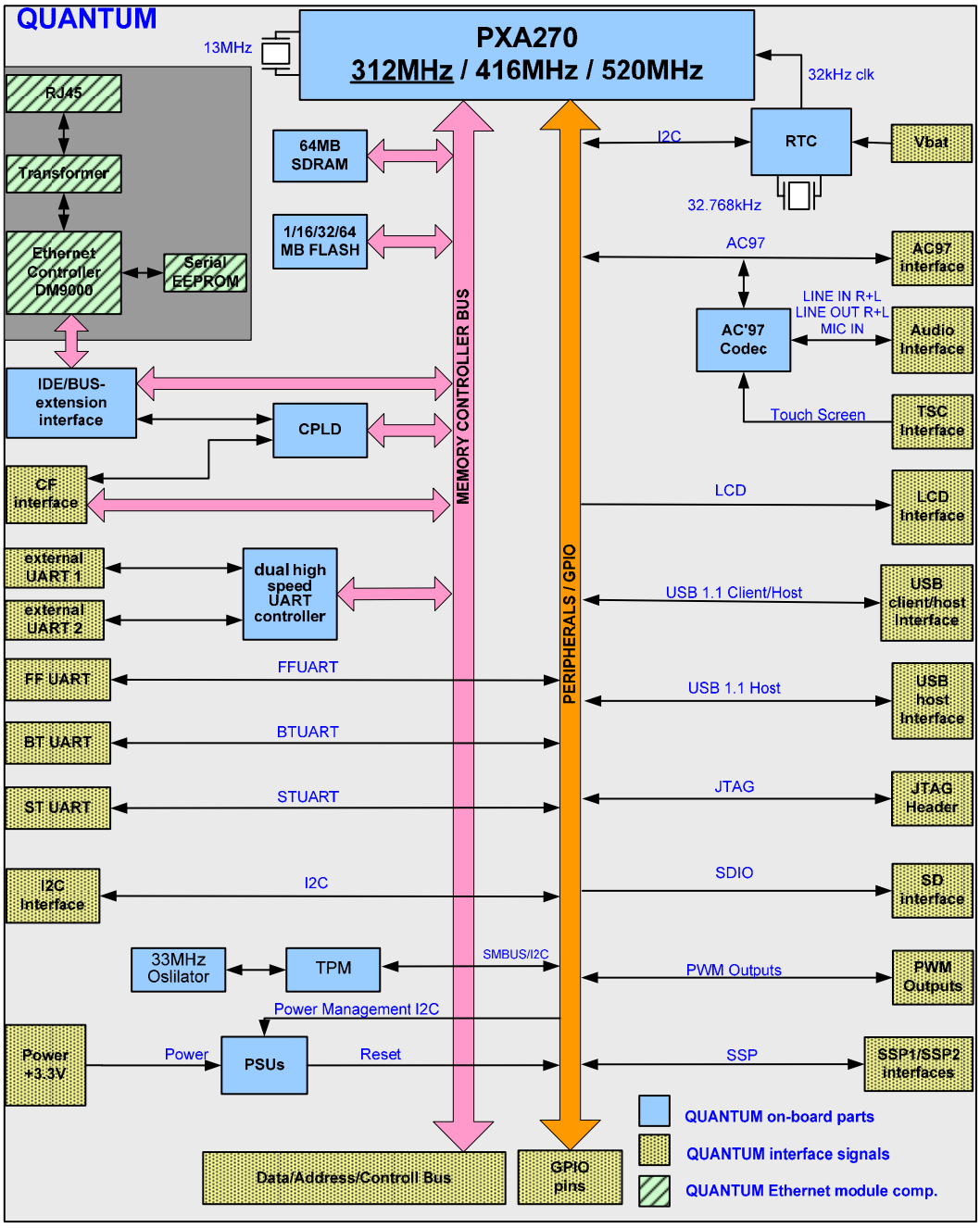
Once you have done this, you can then start adding further peripherals and begin development.

Detailed hardware description

This section provides a detailed description of the functionality provided by the QUANTUM. This information may be required during development, when adding peripherals or when using the embedded features.

QUANTUM block diagram

The following diagram shows the functional organisation of the QUANTUM module:



QUANTUM address map

PXA270 chip select	Physical address	Bus width	Description
CS0#	0x00000000 – 0x03FFFFFE	16-bit	FLASH memory (U3)
CS1#	0x04000000 – 0x0400000E	16-bit	Dual UART – Ext UART 2
CS1#	0x04000010 – 0x0400001E	16-bit	Dual UART – Ext UART 1
CS1#	0x04000020 – 0x07FFFFFE	-	Reserved
CS2#	0x08000000 – 0x0BFFFFFE	16-bit	SO-DIMM bus expansion
CS3#	0x0C000000 – 0x0FFFFFFF	-	Reserved
CS4#	0x10000000 – 0x101FFFFE	16-bit	Ethernet on DoM interface
CS4#	0x10200000 – 0x103FFFFE	16-bit	SO-DIMM bus expansion
CS4#	0x10400000 – 0x13FFFFFF	-	Reserved
CS5#	0x14000000 – 0x17FFFFFE	16-bit	DoM interface - IDE device
-	0x18000000 – 0x1FFFFFFF	-	Reserved
-	0x20000000 – 0x2FFFFFFE	16-bit	CompactFlash
-	0x30000000 – 0x3FFFFFFE	16-bit	Reserved (CompactFlash 2)
-	0x40000000 – 0x43FFFFFC	32-bit	PXA270 peripherals[1]
-	0x44000000 – 0x47FFFFFC	32-bit	LCD control registers[1]
-	0x48000000 – 0x4BFFFFFC	32-bit	Memory controller registers [1]
-	0x4C000000 – 0x4FFFFFFC	32-bit	USB host registers [1]
-	0x50000000 – 0x53FFFFFC	32-bit	Capture interface registers [1]
-	0x54000000 – 0x57FFFFFC	32-bit	Reserved
-	0x58000000 – 0x5BFFFFFC	32-bit	Internal memory control [1]
-	0x5C000000 – 0x5C00FFFC	32-bit	Internal SRAM bank 0
-	0x5C010000 – 0x5C01FFFC	32-bit	Internal SRAM bank 1
-	0x5C020000 – 0x5C02FFFC	32-bit	Internal SRAM bank 2
-	0x5C030000 – 0x5C03FFFC	32-bit	Internal SRAM bank 3
-	0x5C040000 – 0X7FFFFFFF	-	Reserved
SDCS0#	0xA0000000 – 0xA3FFFFFC	32-bit	SDRAM (U2)
SDCS1#	0xA4000000 – 0xA7FFFFFC	32-bit	Reserved

[1] Details of the internal registers are in the *Intel® developer's manual* (available on the development kit CD).

PXA270 GPIO pin assignments

The following table summarises the use of the 118 PXA270 GPIO pins, their direction, alternate functions and active levels:

Key:

No: GPIO number.
AF: Alternate Function number.
Dir: Pin direction.
Active: Function active level or edge.

GPIO No	AF	Signal name	Dir	Active	Function	Wake-up source	See section...
0	0	AC97_IRQ	Input	↑	On-board AC'97 interrupt	✓	Audio power management, page 46.
1	0	GPIO1	Input	↓	GPIO/deep sleep WakeUp	✓	General purpose I/O, page 38.
3	0	PWR_SCL	Output		PXA270 power manager I^2C		I^2C bus, page 36.
4	0	PWR_SDA	I/O				
5	N/A	PWR_CAP0	Power		Dedicated function - to achieve low power during sleep		-
6	N/A	PWR_CAP1	Power				
7	N/A	PWR_CAP2	Power				
8	N/A	PWR_CAP3	Power				
9	0	CLK_PIO	Input	-	N.C.	✓	-
10	0	UART2_INT	Input	High	Ext UART2 interrupt	✓	External interrupts, page 21.
11	0	UART1_INT	Input	High	Ext UART1 interrupt	✓	External interrupts, page 21.
12	0	IDE_INT	Input	↓	DoM interface interrupt	✓	External interrupts, page 21.
13	0	CLK_EXT	Input	N/A	N.C.	✓	-

GPIO No	AF	Signal name	Dir	Active	Function	Wake-up source	See section...
14	0	IRQ_CF#	Input	↓	CF slot interrupt	✓	External interrupts, page 21.
15	2	CS1/CS_UART	Output	Low	Chip select 1 – dual UART	✓	Serial UART ports, page 35.
16	2	PWM0	Output	N/A	PWM0 output	✓	Pulse-Width Modulation (PWM), page 37.
17	2	PWM1	Output	N/A	PWM1 output	✓	
18	1	SA_RDY/GPIO18	Input	Low	RDY for bus expansion		Disk-on-Module/ IDE interface, page 26.
19	0	MMC/CF_EN	Output	Low	MMC/CF power enable		CompactFlash, page 28.
20	0	GPIO001	I/O	N/A	Programmable GPIO		Disk-on-Module/ IDE interface, page 26.
21	0	GPIO002	I/O	N/A	Programmable GPIO		
22	0	33MHz_EN	Output	Low	Enables 33MHz oscillation for TPM		Atmel Trusted Platform Module (TPM), page 37.
23	0/2	SSP_CLK	Output	N/A	GPIO/SSP clock		Synchronous Serial Protocol (SSP) ports, page 36.
24	0/2	SSP_FRM	Output	N/A	GPIO/SSP frame		
25	0/2	SSP_TXD	Output	N/A	GPIO/SSP transmit data		
26	0/1	SSP_RXD	Input	N/A	GPIO/SSP received data		
27	0/1	SSP_EXTCLK	Inout	N/A	GPIO/SSP external clock		
28	1	AC97_BITCLK	Input	↑	AC'97 BIT CLOCK		Audio, page 32.
29	1	AC97_DIN	Input	N/A	AC'97 DATA IN		
30	2	AC97_DOUT	Output	N/A	AC'97 DATA OUT		
31	2	AC97_SYNC	Output	↑	AC'97 SYNC	✓	
32	2	MMCLK	Output	N/A	MMC/SD/SDIO clock		Secure Digital Input/Output (SDIO), page 32.

GPIO No	AF	Signal name	Dir	Active	Function	Wake-up source	See section...
33	2	CS5/CS_IDE	Output	Low	Chip select 5 – DoM interface		Complex Programmable Logic Device (CPLD), page 26.
34	1	FFRXD	Input	N/A	FFUART receive data	✓	
35	1	FFCTS	Input	N/A	FFUART clear to send	✓	
36	1	FFDCD	Input	N/A	FFUART data carrier detect	✓	
37	1	FFDSR	Input	N/A	FFUART data sender ready	✓	Serial UART ports, page 35.
38	1	FFRI	Input	N/A	FFUATR ring indicator	✓	
39	2	FFTXD	Output	N/A	FFUART transmit data	✓	
40	2	FFDTR	Output	N/A	FFUART data terminal ready	✓	
41	2	FFRTS	Output	N/A	FFUART request to send		
42	1	BTRXD	Input	N/A	BTUART receive data		
43	2	BTTXD	Output	N/A	BTUART transmit data		Serial UART ports, page 35.
44	1	BTCTS	Input	N/A	BTUART clear to send		
45	2	BTRTS	Output	N/A	BTUART request to send		
46	2	STDRXD/PWM2	Input	N/A	STUART receive data		Serial UART ports, page 35.
47	1	STDTXD/PWM3	Output	N/A	STUART transmit data		
48	2	CF_POE#	Output	Low	Card bus output enable		
49	2	CF_PWE#	Output	Low	Card bus write enable		CompactFlash, page 28.
50	2	CF_PIOR#	Output	Low	Card bus I/O read		
51	2	CF_PIOW#	Output	Low	Card bus I/O write		
52	0	N.C.	Input	N/A	N.C.		-
53	0	GPIO003	I/O	N/A	Programmable GPIO	✓	Disk-on-Module/ IDE interface, page 26.
54	2	CF_PCE2#	Output	Low	Card bus high byte enable		
55	2	CF_PREG#	Output	Low	Card bus register space select		CompactFlash, page 28.
56	1	CF_WAIT#	Input	Low	Card bus WAIT#		
57	1	CF_PIOCS16#	Input	Low	Card bus IOIS16#		

GPIO No	AF	Signal name	Dir	Active	Function	Wake-up source	See section...
58	2	LCD_D0	Output	N/A	LCD data bit 0		
59	2	LCD_D1	Output	N/A	LCD data bit 1		
60	2	LCD_D2	Output	N/A	LCD data bit 2		
61	2	LCD_D3	Output	N/A	LCD data bit 3		
62	2	LCD_D4	Output	N/A	LCD data bit 4		
63	2	LCD_D5	Output	N/A	LCD data bit 5		
64	2	LCD_D6	Output	N/A	LCD data bit 6		
65	2	LCD_D7	Output	N/A	LCD data bit 7		
66	2	LCD_D8	Output	N/A	LCD data bit 8		
67	2	LCD_D9	Output	N/A	LCD data bit 9		Flat panel display, page 29
68	2	LCD_D10	Output	N/A	LCD data bit 10		
69	2	LCD_D11	Output	N/A	LCD data bit 11		
70	2	LCD_D12	Output	N/A	LCD data bit 12		
71	2	LCD_D13	Output	N/A	LCD data bit 13		
72	2	LCD_D14	Output	N/A	LCD data bit 14		
73	2	LCD_D15	Output	N/A	LCD data bit 15		
74	2	LCD_FCLK	Output	N/A	LCD frame clock		
75	2	LCD_LCLK	Output	N/A	LCD line clock		
76	2	LCD_PCLK	Output	N/A	LCD pixel clock		
77	2	LCD_BIAS	Output	N/A	LCD bias		
78	2	CS2/GPIO78	Output	Low	Chip select 2		Complex Programmable Logic Device (CPLD), page 26.
79	1	CF_PSKTSEL	Output	Low	Card bus socket select		CompactFlash, page 28.

GPIO No	AF	Signal name	Dir	Active	Function	Wake-up source	See section...
80	2	CS4/GPIO80	Output	Low	Chip select 4		Complex Programmable Logic Device (CPLD), page 26.
81	0(1)	SSP3_TXD	Output	N/A	SSP transmit data		
82	0(1)	SSP3_RXD	Input	N/A	SSP receive data		Synchronous Serial Protocol (SSP) ports, page 36.
83	0(1)	SSP3_FRM	Output	Low	SSP chip select	✓	
84	0(1)	SSP3_CLK	Output	N/A	SSP clock		
85	1	CF_PCE1#	Output	Low	Card bus low byte enable		CompactFlash, page 28.
86	0	MMC_WP	Input	High	MMC write protect		Secure Digital Input/Output (SDIO), page 32.
87	0	CF_CD1#	Input	Low	CF card detect 1		CompactFlash, page 28.
88	0/1	USB_OC1#	Input	↓	GPIO/USB port 1 over current detection		USB ports, page 34.
89	0/2	USB_PWE1	Output	High	GPIO/USB port 1 power enable		
90	0	CF_RST	Output	Low	CF card RESET	✓	CompactFlash, page 28.
91	0	CF_CD2#	Input	Low	CF card detect 2	✓	
92	1	MMDAT0	Bidir.	N/A	MMC/SD/SDIO data 0		Secure Digital Input/Output (SDIO), page 32.
93	0	N.C.	Input	N/A	N.C.	✓	-
94	0	N.C.	Input	N/A	N.C.	✓	
95	0	MMC_DET	Input	High	MMC/SD/SDIO card detect	✓	Secure Digital Input/Output (SDIO), page 32.
96	0	N.C.	Input	N/A	N.C.	✓	-

GPIO No	AF	Signal name	Dir	Active	Function	Wake-up source	See section...
97	0	JP1	Input	Low	JP1 – flashing enable	✓	Jumpers, page 48.
98	0	N.C.	Input	N/A	N.C.	✓	
99	0	GPIO10	Input	N/A	Programmable GPIO	✓	
100	0	PWR_IDE	Output	Low	Enable DoM interface power	✓	
101	0	WD_EN	Output	High	WATCHDOG function enable	✓	-
102	0	N.C.	Input	N/A	N.C.	✓	
103	0	WD_IN	Output	N/A	WATCHDOG refresh		
104	0	N.C.	Input	N/A	N.C.		
105	0	JMP_JP2	Input	N/A	JP2 status		Jumpers, page 48.
106	0	N.C.	Input	N/A	N.C.		
107	0	N.C.	Input	N/A	N.C.		-
108	0	N.C.	Input	N/A	N.C.		
109	1	MMDAT1	I/O	N/A	MMC/SD/SDIO data 1		
110	1	MMDAT2	I/O	N/A	MMC/SD/SDIO data 2		Secure Digital Input/Output (SDIO), page 32
111	1	MMDAT3	I/O	N/A	MMC/SD/SDIO data 3		
112	1	MMCMD	I/O	N/A	MMC/SD/SDIO command		
113	2	AC97_RST#	Output	Low	AC'97 reset	✓	Audio, page 32.
114	0	GPIO22	Input	N/A	Programmable GPIO		-
115	0	GPIO12	Output	N/A	Programmable GPIO		-
116	0	USB_DET	Input	Low	USB client device detection	✓	USB, page 34.
117	1	I2C _SCL	Output	N/A	I^2C clock		I^2C bus, page 36.
118	1	I2C _SDA	I/O	N/A	I^2C data		

For details of pin states during sleep modes and reset, see the Pin Usage table in the *Intel® PXA27x Processor Family Electrical, Mechanical, and Thermal Specification*.

Interrupt assignments

Internal interrupts

For details on the PXA270 interrupt controller and internal peripheral interrupts please see the *Intel® PXA270 developer's manual* on the development kit CD.

External interrupts

The following table lists the PXA270 signal pins used for external interrupts.

PXA270 pin	Signal name	Peripheral	Active
GPIO0	AC97_IRQ	On-board audio*	↑
	RTC_IRQ	On-board RTC*	↓
	DIMM_GPIO	SO-DIMM socket*	TBD
GPIO1	GPIO1	Vdd_fault monostable	↓
GPIO10	UART2_INT	UART expander	↑
GPIO11	UART1_INT	UART expander	↑
GPIO12	IDE_INT	DoM interface**	↓
GPIO14	IRQ_CF#	CF interface	↓
GPIO87	CF_CD1#	Card detect 1***	↓
GPIO91	CF_CD2#	Card detect 2***	↓
GPIO95	MMC_DET	Indicates insertion/ejection of MMC/SD card****	↑ ↓
GPIO99	GPIO10	Universal GPIO	↑ ↓
GPIO116	USB_DET	Indicates connected/disconnected USB client device*****	↑ ↓
GPIO20	GPIO001	Universal GPIO on IDE interface	TBD

* GPIO0: Only one of three possible GPIO pin assignments is applicable, AC97_IRQ is the default functionality (others are available using factory fitted resistors).

** IDE_INT: This interrupt is connected to 44 pin IDE header. When Disk-on-Module is used, it is an interrupt from the IDE interface. If the QUANTUM Ethernet module is used, this represents an interrupt from the Ethernet chip.

*** CF_CD1#, CF_CD2#: If only one CF socket is active, the logical expression CF_CD1# or CF_CD2# indicates card insertion. If two sockets are active (e.g. IPS-100), CF_CD1# can indicate Card 1 insertion and CF_CD2# can indicate Card 2 insertion (log 0 – card is inserted).

**** MMC_DET: Log 1 indicates MMC/SD card insertion.

***** USB_DET: Log 1 indicates connection of a USB client device.

PXA270 processor

The QUANTUM board is based on an Intel® PXA270 XScale® processor, information on which can be found on the development kit CD.

The PXA270 processor is an integrated system-on-a-chip microprocessor for high-performance, low-power, portable, handheld and handset devices. It incorporates Intel XScale technology, with on-the-fly voltage, frequency scaling and sophisticated power management.

The PXA270 processor complies with the ARM Architecture V5TE instruction set (excluding floating point instructions) and follows the ARM programmer's model. The PXA270 processor also supports Intel Wireless MMX™ integer instructions in applications such as those that accelerate audio and video processing.

The features of PXA270 processor include:

- Intel XScale core.
- Power management.
- Internal memory - 256KB of on-chip RAM.
- Interrupt controller.
- Operating system timers.
- Pulse-Width Modulation unit (PWM).
- Real Time Clock (RTC)
- General Purpose I/O (GPIO).
- Memory controller.
- DMA controller.
- Serial ports:
  - Three UARTs.
  - Fast Infrared port.
  - I^2C bus port.
  - AC'97 codec interface.
  - I^2S codec interface.
  - USB host controller (two ports).
  - USB client controller.
  - Three Synchronous Serial Ports (SSP).
- LCD panel controller.
- Multimedia Card (MMC), SD memory card and SDIO card controller.
- Memory stick host controller.
- Mobile Scalable Link (MSL) interface.
- Keypad interface.
- Universal Subscriber Identity Module (USIM) interface.
- Quick capture camera interface.
- JTAG interface.
- 356 pin VF-BGA packaging.

The design supports 520, 416 and 312MHz speed variants of the Intel PXA270 processor. The standard variant of the QUANTUM board is fitted with a 312MHz version of the Intel® PXA270. A 13MHz external crystal is used to run the PXA270 processor; all other clocks are generated internally in the processor.

The Intel PXA270 processor family provides multimedia performance, low power capabilities, and rich peripheral integration. Designed for wireless clients, it incorporates the latest Intel advances in mobile technology over its predecessor, the Intel PXA255 processor. The Intel PXA270 processor features scalability by operating from 104MHz up to 520MHz, providing enough performance for the most demanding control and monitoring applications.

PXA270 is the first Intel Personal Internet Client Architecture (PCA) processor to include Intel Wireless MMX™ technology, enabling high performance, low-power multimedia acceleration with a general purpose instruction set. Intel Quick Capture technology provides flexible and powerful camera interfacing for capturing digital images and video. Power consumption is also a critical component. Wireless Intel SpeedStep® technology provides these new capabilities in low-power operation.

The processor requires a number of power supply rails. All voltage levels are generated on-board from either the DC/DC PSU or from the single +3.3V power input. The QUANTUM uses specialised power management IC that supports Intel SpeedStep technology.

The PXA270 processor is a low-power device and does not require a heat sink for operating temperatures up to 85°C.

Real Time Clock (RTC)

The QUANTUM uses an external RTC (Intersil ISL1208) to store the date and time and provide power management events. The RTC is connected to the I^2C bus of the PXA270 processor and is accessible through I^2C bus address 0x6F. It can be battery backed, if the backup battery is connected to pin 32 (+VBAT_IN) of the SO-DIMM interface connector.

The accuracy of the RTC is based on the operation of the 32.768KHz watch crystal. The calibration tolerance is ±20ppm, which provides an accuracy of ±1 minute per month when the board is operated at an ambient temperature of +25°C. When the board is operated outside this temperature, the accuracy may be degraded by 0.035ppm/°C ±10% typical. The watch crystal's accuracy will age by ±3ppm maximum in the first year, then ±1ppm maximum in the year after, decreasing logarithmically in subsequent years.

The Intersil ISL1208 RTC provides the following basic functions:

- Real Time Clock/calendar:
  - Tracks time in hours, minutes, and seconds.
  - Includes day of the week, day, month, and year.
- Single alarm:
  - Settable to the second, minute, hour, day of the week, day, or month.
  - Single event or pulse interrupt mode.
- Two bytes of battery-backed user SRAM.
- I^2C interface.

Watchdog timer

The PXA270 processor has internal support for a watchdog timer. A 32-bit internal register is incremented on the rising edge of the internal 3.25MHz clock. On reaching the preset value, the output pin nRESET_OUT is asserted; a reset is applied to the PXA270 processor and most internal states are cleared. The only way to clear this pin is with a reset function (hardware reset, sleep-exit reset, watchdog reset, or GPIO reset).

The internal watchdog timer can be used to protect against erroneous software. Timeout periods can be adjusted from 307ns to around 22 minutes. When a timeout occurs the entire board is reset. On reset, the watchdog timer is disabled until it is enabled again by the software.

In addition, an external WD timer is included on the QUANTUM. This external watchdog is not a part of the standard QUANTUM configuration: contact Eurotech Ltd for availability (for full contact details, please see Appendix A – Contacting Eurotech Ltd, page 55). TPS3828 is used as a reset monitor with watchdog function.

If an external WD timer is used, WD_EN(GPIO101)=log 1 activates watchdog functionality and WD_N(GPIO103) is used for WD refresh.

For further details, see the Eurotech Ltd operating system technical manual and the *Intel® developer's manual* on the development kit CD.

Memory

The QUANTUM has three types of memory fitted:

- 1, 16, 32 or 64MB resident FlashDisk containing:
  - Bootloader to boot operating system.
  - Operating system (except 1MB size).
  - Application images.
- 64(32)MB of SDRAM for system memory.
- Static RAM: 256KB of SRAM internal to the PXA270.

Flash memory/silicon disk

The QUANTUM supports two basic concepts of Flash memory configuration:

- Small capacity FlashDisk (1MB Spansion Flash memory).
- High capacity FlashDisk (16/32/64MB MirrorBit Flash Spansion memory).

The Flash memory is arranged as 16Mbit x 16-bit (32MB device) or as 32Mbit x 16-bit (64MB device).

The Flash memory array is divided into equally-sized symmetrical blocks that are 64-Kword in size (128 KB) sectors. A 256Mbit device contains 256 blocks, and a 512Mbit device contains 512 blocks.

SDRAM

QUANTUM is designed for use with one 512/256 MBit SDRAM chip (64/32MB). SAMSUNG K4M513233C is assembled as a standard. The 512MBit is configured as 16M x 32-bit, and the 256MBit as 8M x 32-bit.

The SDRAM memory controller is set to run at a frequency of 104MHz.

Static RAM

The PXA270 processor provides 256KB of internal memory-mapped SRAM. The SRAM is divided into four banks, each consisting of 64KB.

Bus extension interfaces

There are several extension interfaces on the QUANTUM, which are interconnected to the main SO-DIMM interface or the on-board Disk-on-Module/IDE interface. These interfaces are controlled by the Xilinx CPLD device.

They are the:

- Static memory bus extension interface.
- CompactFlash interface.
- Disk-on-Module/QUANTUM Ethernet module interface.

Complex Programmable Logic Device (CPLD)

The Xilinx device XC9536XL-7CSG48I is used for control logic for the IDE interface, the QUANTUM Ethernet module bus interface and the CompactFlash interface. Depending on which module is connected to the Disk-On-Module interface, jumper JP2 has to be set (see JP2 – User jumper (Disk-On-Module interface functionality), page 48). The status of JP2 can be also read on GPIO105 of PXA270.

Static memory bus extension

The memory controller of the PXA270 processor supports three different memory spaces: SDRAM, static memory, and PC card space. The SDRAM has four partitions, the static memory has six partitions, and the PC card space has two partitions (or sockets).

The static memory interface is used for connecting Flash, UARTs, IDE interfaces and bus extensions. As a result of this, two CS signals (NCS2 and NCS4) are connected to the SO-DIMM pins. The static memory space bus extension is available via the D0-D15 data pins and the SA0-SA10 and SA21 address pins. Pin 89 of the SO-DIMM interface (PXa270 GPIO114) can be used as an interrupt signal from the bus extension interface.

Disk-on-Module/IDE interface

The 44 pin IDE connector is designed for connecting a 3.3V Disk-on-Module device (for a signal description, see J2 – IDE/bus extension connector, page 54). The IDE interface is implemented in static memory space (via NCS5) glue to logic in CPLD and it is addressed by signal CS5 and A21, A22 address pins. The same connector is designed for the QUANTUM Ethernet Module (QEM) also. It is the HW configurable option (see JP2 – User jumper (Disk-On-Module interface functionality), page 48).

Because Disk-on-Module devices and the Quantum Ethernet module (QEM) have a power consumption of only 1-10mA , in low power modes, there is a power supply switch included to switch off the 3.3V supply to the Disk-On-Module interface. It is controlled by GPIO100:

GPIO100 level	3.3V IDE supply
Low	Enable
High	Disable (OFF)

The addressing of the Disk-on-Module device is as follows:

Address range (A21,A22)	Region name
0x14400000 (MA21=0, MA22=1)	First set of registers (addressed by A1,A2,A3) – IDE_CS0
0x14200000 (MA21=1, MA22=0)	Second set of registers (addressed by A1,A2,A3) – IDE_CS1

The interface supports the following signals:

Signal name	Description
NRESET#	IDE/QEM reset signal
SA_D0 – SA_D15	16-bit data bus
SA_A1-SA_A4, SA_21	Selected address bus signals
IDEIOW#(nPWE/nWR)	IOW# for IDE or nWR for QEM
IDEIOR#(nOE)	IOR# for IDE or nOE for QEM
IDE_IRQ(IRQ)	Interrupt form IDE/QEM
IDECSO#(CS1)	IDE_CS0 for IDE or CS for QEM
CS3FX#(CS2)	IDE_CS1 for IDE
SA_RDY#_GPIO18	Data RDY for IDE
GPIO001	Not used for IDE or button status for QEM
GPIO002	Not used for IDE or LED1 for QEM
GPIO003	Not used for IDE or LED2 for QEM

QUANTUM Ethernet Module (QEM)

The QEM was designed for debugging and developing purposes, but can be used generally as well. Because QEM is plugged into J2, you cannot use it at the same time as the Disk-on-Module.

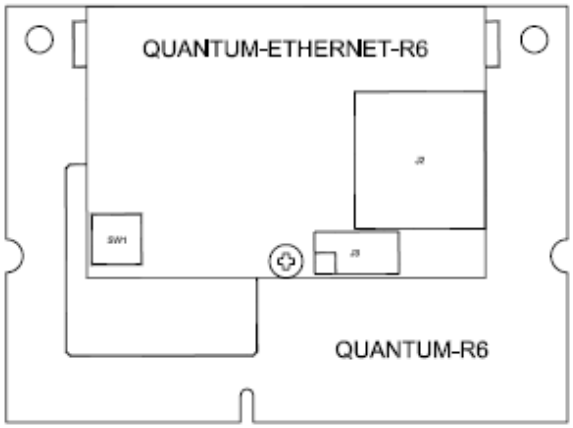
There is one difference between the mapping of the Disk-on-Module device and that of the QEM: while the IDE device is mapped into CS5 memory space, QEM is mapped into CS4 memory space (it is addressed by the address signal lines A1 and A21), but both devices use the same interrupt signal. Address line A21 selects whether the DoM Ethernet chip or secondary Ethernet (connected via SO-DIMM bus interface, e.g. QUANTUM Base Board V2) is selected (by CPLD).

If QEM is used, JP2 must be plugged in.

The addressing of the DM9000A QEM Ethernet chip is as follows:

Address (addressed by A1, A21=0)	Region name
0x10000000	DM9000A device INDEX port
0x10000002	DM9000A device DATA port

Correct placement of the QEM on the QUANTUM is illustrated below:



CompactFlash

A CompactFlash extension interface for full I/O mode operation is provided using slot 0 (and slot 1 optionally) of the PXA270 PC card controller, and supports type I and II CF+ cards. It appears in PC card memory space socket 0.

Address	Region name
0x20000000 – 0x23FFFFFF	Socket 0 I/O space.
0x24000000 – 0x27FFFFFF	Reserved.
0x28000000 – 0x2BFFFFFF	Socket 0 attribute memory space.
0x2C000000 – 0x2FFFFFFF	Socket 0 common memory space.
0x30000000 – 0x33FFFFFF	Socket 1 I/O space.
0x34000000 – 0x37FFFFFF	Reserved.

Address	Region name
0x38000000 – 0x3BFFFFFF	Socket 1 attribute memory space.
0x3C000000 – 0x3FFFFFFF	Socket 1 common memory space.

As a default configuration, only one CF socket (slot 0) is supported. This is a hot-swappable 3.3V interface. The external power switch can be controlled by the MMC/CF_EN signal. The card insertion is detected by the zero level on pins CF_CD1# and CF_CD2#. The CompactFlash interrupt signal (IRQ_CF#) is on PXA270 pin GPIO14.

If the application requires two CF slots (e.g. a IPS-100 board), the second CF slot uses the PXA270 GPIO 27 signal as an interrupt pin, in case the SSP port doesn't support external clocking for the SPP interface. CF slots don't support power control (because the MMC/CF_EN signal, GPIO19, is used for CF2 RESET functionality) and CF_CD2# is used as a CF2 card insert detection (CF1 uses CD_CF1# only in this case, instead of both CD_CF1# and CD_CF2#, when only one CF socket is used).

Many CF+ cards require a reset once they have been inserted. Resetting the CompactFlash interface is possible by low level on the CF_RST(GPIO90) pin – CF Slot 0 – or GPIO19 (if two CF slots are used).

CF+ is a small form factor card standard. It encompasses CompactFlash (CF) data storage cards; magnetic disk cards and I/O cards (including serial cards); Ethernet cards and fax/modem cards; digital phone cards; USB devices; barcode scanners; Bluetooth®; IEEE802.11b (WiFi); wireless digital cell phone cards etc. For more details about CF+ standards and the availability of particular CF+ peripherals, visit the website www.compactflash.org.

The CF+ card provides high capacity data storage and I/O functions that comply with the Personal Computer Memory Card International Association (PCMCIA) standard.

Except standard PXA270 CF-interface signals, there is a designed signal PADDREN, generated by CPLD. This can be used (on external board) to address buffers enable.

Flat panel display

The Intel PXA270 processor contains an integrated LCD display controller. It is capable of supporting both colour and monochrome single and dual-scan display modules. It supports active (TFT) and passive (STN) LCD displays from 1x1 to 800x600 pixels.

The PXA270 can drive displays with a resolution up to 800x600, but as the PXA270 has a unified memory structure, the bandwidth to the application decreases significantly. If the application makes significant use of memory - such as when video is on-screen - you may also experience FIFO under-runs, causing the frame rates to drop or display image disruption. Reducing the frame rate to the slowest speed possible gives the maximum bandwidth to the application. The display quality for an 800x600 resolution LCD is dependant on the compromises that can be made between the LCD refresh rate and the application. The PXA270 is optimised for 640x480 display resolution.

A full explanation of the graphics controller operation can be found in the *PXA270 developer's manual* included on the support CD.

The flat panel data and control signals are routed to the board interface connector J1. See the section J1 – Module Interface Connector, page 49, for pin assignments.

The following tables provide a cross-reference between the flat panel data signals and their function when configured for different displays.

TFT panel data bit mapping to the QUANTUM

Panel data bus bit	18-bit TFT	12-bit TFT	9-bit TFT
LCD_15	R5	R3	R2
LCD_14	R4	R2	R1
LCD_13	R3	R1	R0
LCD_12	R2	R0	-
LCD_11	R1	-	-
GND	R0	-	-
LCD_10	G5	G3	G2
LCD_9	G4	G2	G1
LCD_8	G3	G1	G0
LCD_7	G2	G0	-
LCD_6	G1	-	-
LCD_5	G0	-	-
LCD_4	B5	B3	B2
LCD_3	B4	B2	B1
LCD_2	B3	B1	B0
LCD_1	B2	B0	-
LCD_0	B1	-	-
GND	B0	-	-

The PXA270 can directly interface with 18-bit displays, but from a performance point of view it is better to use 16 bits only. 18-bit operation requires twice the bandwidth of 16-bit operation.

STN panel data bit mapping to the QUANTUM

Panel data bus bit	Dual scan colour STN	Single scan colour STN	Dual scan mono STN
LCD_15	DL7(G)	-	-
LCD_14	DL6(R)	-	-
LCD_13	DL5(B)	-	-
LCD_12	DL4(G)	-	-
LCD_11	DL3(R)	-	-
LCD_10	DL2(B)	-	-
LCD_9	DL1(G)	-	-
LCD_8	DL0(R)	-	-
LCD_7	DU7(G)	D7(G)	DL3
LCD_6	DU6(R)	D6(R)	DL2
LCD_5	DU5(B)	D5(B)	DL1
LCD_4	DU4(G)	D4(G)	DL0
LCD_3	DU3(R)	D3(R)	DU3
LCD_2	DU2(B)	D2(B)	DU2
LCD_1	DU1(G)	D1(G)	DU1
LCD_0	DU0(R)	D0(R)	DU0

Below is a table covering the clock signals required for passive and active type displays:

QUANTUM	Active display signal (TFT)	Passive display signal (STN)
LCD_PCLK	Clock	Pixel clock
LCD_LCLK	Horizontal sync	Line clock
LCD_FCLK	Vertical sync	Frame clock
LCD_BIAS	DE (Data Enable)	Bias

The display signals are +3.3V compatible. The QUANTUM doesn’t contain power control circuitry for the flat panel logic supply and backlight supply.

Secure Digital Input/Output (SDIO)

The SDIO interface is connected directly from PXA270's MMC/SD/SDIO controller to the SO-DIMM interface. It consists of 4/1 (MMDAT0-MMDAT3) data, one clock (MMCLK) and one command (MMCMD) line.

The MMC/SD/SDIO controller supports MultiMedia Cards (MMC) , Secure Digital (SD) and Secure Digital I/O (SDIO) communications protocols. The MMC controller supports the MMC system, a low-cost data storage and communications system. The MMC controller in the PXA270 processor is based on the standards outlined in the *Multimedia Card System Specification Version 3.2*. The SD controller supports one SD or SDIO card based on the standards outlined in the *SD Memory Card Specification Version 1.01* and *SDIO Card Specification Version 1.0 (Draft 4)*.

The MMC/SD/SDIO controller features:

- Data-transfer rates of up to 19.5Mbps for MMC, 1-bit SD/SDIO, and SPI mode data transfers.
- Data-transfer rates of up to 78Mbps for 4-bit SD/SDIO data transfers.
- Support for all valid MMC and SD/SDIO protocol data-transfer modes.

This is a hot-swappable 3.3V interface, controlled by the detection of an inserted card (falling edge on MMC_DET-GPIO95 when a SD card has been inserted, and a rising edge when a SD card is removed).

SD card write-protection is connected to PXA270's MMC_WP-GPIO86 signal.

A variety of SDIO cards are available, such as Bluetooth® and IEEE802.11b (WiFi). More information can be found at www.sdcard.org/about/sdio.

Audio

A Wolfson WM9712L AC'97 audio codec is used to support the audio features of the QUANTUM. Audio inputs supported by the WM9712L are a stereo Line In and a mono microphone input.

The following analogue signals are on the QUANTUM interface:

Function	Interface pin	Signal	Signal levels (max)	Frequency response (Hz)
Microphone	60	MIC input	1Vrms	20 – 20K
Line In	56	Line input left	1Vrms	20 – 20K
	58.	Line input right		
Line Out	52	Line output left	1Vrms	20 – 20K
	54	Line output right		
	62	Audio ground reference		

In the EuroTech-compatible version (variants 01, 03 and 06, Wolfson WM9712 is not fitted), the wires used for analogue signals in the previous table are used for AC'97 bus connectivity to the SO-DIMM interface. Factory-fitted resistors are used for this purpose.

Touchscreen controller

The QUANTUM supports 4-wire analogue resistive touchscreens, using the touchscreen controller available on the Wolfson WM9712L audio codec. The touchscreen controller supports the following functions:

- X co-ordinate measurement.
- Y co-ordinate measurement.
- Pen down detection with programmable sensitivity.
- Touch pressure measurement.

The touchscreen can be used as a wake-up source for PXA270 from sleep mode.

The touchscreen interface is broken out on the SO-DIMM interface J1. For details see J1 – Module interface connector, page 49.

The following signals are used for touchscreens on the QUANTUM interface:

Interface pin	Signal	Alternative functionality
64	PWM0/TPX+	PWM0 output.
66	PWM1/TPX-	PWM1 output.
93	TPY+	USB host 2 - USB_DR2+.
95	TPY-	USB host 2 - USB_DR2-.

For variants of the QUANTUM module without on-board AC'97 codec (variants 01 and 03), these signals have an alternative functionality. Use of these alternative functions is dependant on the factory-fitted resistors.

USB ports

There are two USB host interfaces available on the QUANTUM. These comply with the Universal Serial Bus Specification Rev. 1.1, supporting data transfer at full-speed (12Mbit/s) and low-speed (1.5Mbit/s).

There is no power management circuitry implemented on QUANTUM. USB power control switches must be implemented on the Base Board to control the power and protect against short-circuit conditions.

The USB port 2 can be configured as a client port internally within the PXA270 USB controller, or alternatively can be connected to SO-DIMM interface J1.

Below is a table covering the USB port 2 signals assignment to the SO-DIMM interface:

PXA270 signal	SO-DIMM interface pin no.	USB port 2 mode
USB_DR2+	93	USB host
USB_DR2-	95	
USB_DR2+	3	USB client
USB_DR2-	5	

More information about the USB bus and the availability of particular USB peripherals can be found at the website www.usb.org.

The mode of the USB 2 channel is depend on factory-fitted resistors, and can't be changed by software configuration only. The default is client mode.

Serial UART ports

The PXA270 processor has three UARTs:

- Full-function (FFUART).
- Bluetooth® (BTUART).
- Standard (STUART).

These UARTs use the 16550 programming model. The transmit and receive buffers are 64 bytes deep. Each serial port contains a UART, and a slow infrared transmit encoder and receive decoder that conforms to the IrDA serial infrared specification.

FFUART supports full modem-control capability; the maximum baud rate is 921.6Kbaud.

STUART does not support modem control capability; the maximum baud rate is 921.6Kbaud.

BTUART is a high-speed UART that supports baud rates of up to 921.6Kbaud. It supports only two modem control pins (CTS# and RTS#).

Further information can be found in the *Intel® developer's manual*, available on the development kit CD .

In addition to these three serial ports, an external dual UART controller device is included on QUANTUM to provide two additional 16C550 compatible serial ports (the Exar XR16V2752: product information is available at www.exar.com/product.php?ProdNumber=XR16V2752&areaID=3). The UART controller uses a 14.7456MHz clock input and will support data rates up to 921.6Kbaud. It supports only two modem control signals: CTS# and RTS#. It also supports automatic RS485 half-duplex direction control output via RTS#. The UART device is connected to the memory controller interface of PXA270.

Port	Address	IRQ	FIFO Rx/Tx	Signals
Ext UART1	0x04000010 – 0x0400001E	GPIO11	64/64	EXT1_RXD,EXT1_TXD, EXT1_CTS, EXT1_RTS
Ext UART2	0x04000000 – 0x0400000E	GPIO10	64/64	EXT2_RXD,EXT2_TXD, EXT2_CTS, EXT2_RTS

The first channel of the dual UART, Ext UART1, is connected directly to the SO-DIMM interface. The second channel, Ext UART2 has signal lines shared with the SSP3 synchronous serial port.

The standard version of QUANTUM uses signals 14, 16, 18, and 20 of SO-DIMM as a fifth serial port. To enable the use of the SSP3 interface (a factory-fitted option) contact Eurotech Ltd (see Appendix A – Contacting Eurotech Ltd, page 55, for details).

Synchronous Serial Protocol (SSP) ports

There are two SSP (Synchronous Serial Protocol) ports on QUANTUM. These interfaces connect to a variety of external analogue-to-digital (A/D) converters; audio and telecommunication codecs; and many other devices that use serial protocols for data transfer. The SSP ports provide support for the following protocols:

- Texas Instruments (TI) Synchronous Serial Protocol (SSP).
- Motorola Serial Peripheral Interface (SPI) protocol.
- National Semiconductor Microwire.
- Programmable Serial Protocol (PSP).

The SSP ports operate as full-duplex devices for the SPI, PSP and TI Synchronous Serial protocols, and as a half-duplex device for the Microwire protocol.

The SSP1 is a 5-wire bus and has dedicated pins on the SO-DIMM interface (see the section J1 – Module interface connector, page 49, for pin assignments). The SSP3 is a 4-wire bus (which doesn't include EXT_CLK support), and has a pin shared with the Ext UART2 serial port (see the section Serial UART ports, page 35, for details).

I²C bus

There are two I²C buses on the PXA270: a standard I²C bus and a secondary I²C bus, dedicated for the power management control. There are two devices on the QUANTUM board, connected to the main I²C bus; an RTC ISL1208 and an AT97SC3203S TPM chip (optional: contact Eurotech Ltd for availability – see Appendix A – Contacting Eurotech Ltd, page 55). A standard PXA270 I²C interface is connected to the SO-DIMM interface as well, see the table below:

Bus	Signal name	SO-DIMM pin no.
Standard I²C bus	I2C_SDA	25
	I2C_SCL	23
PM I²C bus	PWR_SDA	NC
	PWR_SCL	NC

The I²C unit supports a fast-mode operation of 400Kbits/sec and a standard-mode of 100Kbits/s. Fast-mode devices are downward-compatible and can communicate with standard-mode devices in a 0 to 100Kbits/s I²C bus system. As standard-mode devices, however, are not upward compatible, they should not be incorporated into a fast-mode I²C bus system as they cannot follow the higher transfer rate and so unpredictable states would occur.

Pulse-Width Modulation (PWM)

Two PWM outputs (GPIO16 and GPIO17) are dedicated on the SO-DIMM interface. If not required, they can be used as a standard GPIO. These PWM outputs can't be used if an on-board AC'97 codec is fitted. Optionally, if the serial port STUART is not being used, GPIO 46 and GPIO 47 can be used as two additional PWM outputs.

Atmel Trusted Platform Module (TPM)

The Atmel Trusted Platform Module device is included on the QUANTUM module. A 33MHz clock (e.g. Jauch: 0 33.0 JO53-A-3.3-2) is necessary for the AT97SC3203S TPM chip. This solution provides full TGC v1.2 compatibility. It is connected to the system via an I^2C bus. The TPM device is not a part of standard configuration; contact Eurotech Ltd for availability (see Appendix A – Contacting Eurotech Ltd, page 55, for details). For the 33MHz oscillator disable (power save modes), GPIO22 is used:

GPIO22 level	33MHz oscillator
Low	Disable
High or NC	Enable

General purpose I/O

There are no free PXA270 pins (except GPIO115) dedicated for GPIO functionality only. Dependant on the peripherals being used, there are up to seventy eight GPIOs which can be used for alternative functions. The table below gives a list of these GPIOs with their alternative functions:

Signal name	GPIO no.	SO-DIMM pin no.	Used by interface
SA_FF_RI	GPIO38	7	
SA_FF_DCD	GPIO36	9	
SA_FF_DSR	GPIO37	11	
SA_FF_DTR	GPIO40	13	FFUART
SA_FF_RTS	GPIO41	15	
SA_FF_CTS	GPIO35	17	
SA_FF_TXD	GPIO39	19	
SA_FF_RXD	GPIO34	21	
SA_I2C_SCL	GPIO117	23	I^2C
SA_I2C_SDA	GPIO118	25	
IR_TXD/PWM3	GPIO47	27	STUART
IR_RXD/PWM2	GPIO46	29	
SA_BT_RTS	GPIO45	41	
SA_BT_CTS	GPIO44	43	BTUART
SA_BT_TXD	GPIO43	45	
SA_BT_RXD	GPIO42	47	
SA_RDY	GPIO18	49	Bus extension
NPCD0	GPIO87	51	
CF_RESET	GPIO90	55	CompactFlash interface
NPCD1	GPIO91	57	
IRQ_CF	GPIO14	59	

continued...

Signal name	GPIO no.	SO-DIMM pin no.	Used by interface
SA_NPOE	GPIO48	63	
SA_NPWE	GPIO49	65	
SA_NPIOR	GPIO50	67	
SA_PIOW	GPIO51	69	
SA_NPCE_1	GPIO85	71	CompactFlash interface
SA_NPCE_2	GPIO54	73	
SA_PSKTSEL	GPIO79	75	
SA_NPREG	GPIO55	77	
SA_NPWAIT	GPIO56	79	
SA_NIOIS16	GPIO57	81	
SA_NOE	GPIO48	83	
SA_NWE	GPIO49	85	Bus extension/Ethernet module
CPLD_OUT	GPIO114	89	
L_DD_0	GPIO58	101	
L_DD_1	GPIO59	103	
L_DD_2	GPIO60	105	
L_DD_3	GPIO61	107	
L_DD_4	GPIO62	109	LCD
L_DD_5	GPIO63	111	
L_DD_6	GPIO64	113	
L_DD_7	GPIO65	115	
L_DD_8	GPIO66	117	
L_DD_9	GPIO67	119	
L_DD_10	GPIO68	121	

continued…

Signal name	GPIO no.	SO-DIMM pin no.	Used by interface
L_DD_11	GPIO69	123	
L_DD_12	GPIO70	127	
L_DD_13	GPIO71	129	
L_DD_14	GPIO72	131	
L_DD_15	GPIO73	133	LCD
L_FCLK	GPIO74	135	
L_LCLK	GPIO75	137	
L_PCLK	GPIO76	139	
L_BIAS	GPIO77	141	
SSP_EXTCLK	GPIO27	4	
SSP_SFRM	GPIO24	6	
SSP_SCLK	GPIO23	8	SSP1 port
SSP_TXD	GPIO25	10	
SSP_RXD	GPIO26	12	
SSP3_RXD	GPIO82	14	
SSP3_TXD	GPIO81	16	SSP3 port/Ext UART2
SSP3_SFRM	GPIO83	18	
SSP3_CLK	GPIO84	20	
SA_MMC_CMD	GPIO112	38	
SA_MMC_DAT0	GPIO92	40	
SA_MMC_CLK	GPIO32	42	
SA_MMC_DAT3	GPIO111	44	MMC/SD interface.
MMC_DETECT	GPIO95	46	
MMC_ON	GPIO19	48	
MMC_WP	GPIO86	50	

Signal name	GPIO no.	SO-DIMM pin no.	Used by interface
PWM_0/TPX+	GPIO16	64	PWM channels/on-board AC'97.
PWM_1/TPX-	GPIO17	66	
USBC_DET	GPIO116	128	USB client.
USBHPEN0	GPIO89	130	USB host.
SA_MMC_DAT1	GPIO109	132	MMC/SD interface.
USBHPWR0	GPIO88	134	USB host.
SA_MMC_DAT2	GPIO110	136	MMC/SD interface.
SA_NCS_2	GPIO78	138	Bus extension/Ethernet module.
SA_NCS_4	GPIO80	140	
GPIO115	GPIO115	142	-

JTAG and debug access

Debug access to the PXA270 XScale® processor is via the JTAG interface, which is also interconnected to the module interface connector J1. The Macraigor Wiggler probe can be used to debug the PXA270 processor on the QUANTUM board. There are many other debug tools that can be interfaced with the QUANTUM for access to the JTAG interface of the Intel XScale PXA270 processor.

In addition to PXA270, there is one CPLD (XC9536XL-CS48) in the JTAG chain on the QUANTUM. The BSDL file can be found on the website www.xilinx.com.

Power and power management

Power supplies

The QUANTUM is designed to operate from a single +3.3V±5% (+3.15V to +3.45V) supply. Alternatively, the battery backup can be connected. The 3.3V is supplied from the three pins of connector J1, one pin of which is dedicated for VBat (the backup battery).

Input voltage to the module must be stabilised. There is no over voltage protection on the module and voltage higher then 3.6V can cause unrecoverable damage to the QUANTUM module.

On-board supplies

There are five on-board supply voltages derived from the input Vcc (+3.3V) supply. These are listed in the following table:

Supply rail	Power domains	Voltage	Reset threshold
VCC_BATT	PXA270 sleep-control subsystem, oscillators and Real Time Clock	3.3V	2.93V
VCC_CORE	PXA270 core and other internal units	0.85V-1.55V	92% of nominal
VCC_PLL	PXA270 phase-locked loops	1.3V	1.2V
VCC_SRAM	PXA270 internal SRAM units	1.1V	1V
+3.3V	PXA270 I/O, PXA270 internal units and on-board peripherals	3.3V	2.93V

A reset is generated if the supplies fall below the thresholds shown in the table.

Power management IC

A Linear Technology LTC3445 is used to provide the power supply for the PXA270. It is specifically designed for the PXA27x family of microprocessors.

The LTC3445 contains a high efficiency buck regulator (VCC_CORE), two LDO regulators (VCC_PLL, VCC_SRAM), a PowerPath controller and an I^2C interface. The buck regulator has a 6-bit programmable output range of 0.85V to 1.55V. Also, the buck regulator uses either a constant (1.5MHz) or a spread spectrum switching frequency. Using the spread spectrum option allows for a lower noise regulated output as well as low noise at the input. In addition, the regulated output voltage slew rate is programmable via the I^2C interface.

Each LDO is capable of delivering up to 50mA.

The LTC3445 device is connected to the PM I^2C interface of the PXA270.

Battery backup

For the ISL1208 on-board RTC, a backup supply can be connected on pin 32 of the SO-DIMM interface. It provides an RTC backup supply when no Vcc is applied.

The table below shows the typical and maximum current loads on the backup battery:

Device load on battery	Typical (µA)	Maximum (µA)
ISL1208 RTC (with Clock Out on)	1.4	5
ISL1208 RTC (with Clock Out off)	0.4	0.95

Processor power management

First available in the PXA270 processor, wireless Intel SpeedStep® Technology dynamically adjusts the power and performance of the processor, based on CPU demand. This can result in a significant decrease in power consumption.

In addition to the capabilities of Intel Dynamic Voltage Management, a function already built into the Intel XScale® microarchitecture, the PXA27x family incorporates three new low-power states: deep idle, standby and deep sleep. It is possible to change both the voltage and frequency 'on-the-fly' by intelligently switching the processor into the various low power modes, saving additional power while still providing the necessary performance to run rich applications.

Wireless Intel SpeedStep technology includes the following features:

- Five reset sources: power-on, hardware, watchdog, GPIO, and exit from sleep and deep-sleep modes (sleep-exit).
- Multiple clock-speed controls to adjust frequency, including frequency change, turbo mode, half-turbo mode, fast-bus mode, memory clock, 13M mode, A-bit mode and AC'97.
- Switchable clock source.
- Functional-unit clock gating.
- Programmable frequency-change capability.
- One normal-operation power mode (run mode) and five low-power modes to control power consumption (idle, deep-idle, standby, sleep, and deep-sleep modes).
- Programmable I^2C-based external regulator interface to support changing dynamic core voltage, frequency change and power mode coupling.

The PXA270 power consumption depends on the operating voltage and frequency, peripherals enabled, external switching activity, external loading and other factors. The tables below contain the power consumption information at room temperature for different modes: active, idle and low power. For active power consumption data, no PXA270 peripherals are enabled, except for UARTs.

Frequency (MHz)	System bus frequency	Active power consumption typical (mW)	Idle power consumption typical (mW)	Conditions VCC_SRAM = 1.1V; VCC_PLL = 1.3V; VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V; VCC_IO, VCC_BATT,VCC_USB=3.0V
520	208 MHz	747	222	VCC_CORE = 1.45V
416	208 MHz	570	186	VCC_CORE = 1.35V
312	208 MHz	390	154	VCC_CORE = 1.25V
312	104 MHz	375	109	VCC_CORE = 1.1V
208	208 MHz	279	129	VCC_CORE = 1.15V
104	104 MHz	116	64	VCC_CORE = 0.9V
13	CCCR[CPDIS]=1	44.2	-	VCC_CORE = 0.85V

PXA270 low power modes	Active power consumption typical (mW)	Conditions VCC_MEM, VCC_BB, VCC_USIM, VCC_LCD = 1.8V VCC_IO, VCC_BATT, VCC_USB= 3.0V
13MHz idle mode (LCD On)	15.4	VCC_CORE, VCC_SRAM, VCC_PLL = 0.85V
13MHz idle mode (LCD Off)	8.5	VCC_CORE, VCC_SRAM, VCC_PLL = 0.85V
Deep sleep mode	0.1014	VCC_CORE, VCC_SRAM, VCC_PLL = 0V
Sleep mode	0.1630	VCC_CORE, VCC_SRAM, VCC_PLL = 0V
Standby mode	1.7224	VCC_CORE, VCC_SRAM, VCC_PLL = 1.1V

Wake-up sources

PXA270 sleep mode offers lower power consumption by powering most internal units off. There is no activity inside the processor, except for the units programmed to retain their state in the PSLR register, the Real Time Clock (RTC), and the clocks and power manager. Because internal activity has stopped, recovery from sleep mode must occur through an external or an internal RTC event. External wake-up sources are GPIO<n> edge detects and are listed in the section PXA270 GPIO pin assignments, page 15.

Deep-sleep mode offers the lowest power consumption by powering most units off. There is no activity inside the processor, except for the RTC and the clocks and power manager. Because internal activity has stopped, recovery from deep-sleep mode must be through an external event or an RTC event.

In deep-sleep mode, all the PXA270 power supplies excluding VCC_BATT (i.e. VCC_CORE, VCC_SRAM, VCC_PLL and VCC_IO) can be powered off for minimised power consumption. On the QUANTUM, the main +3.3V rail supplies the VCC_IO power domain of PXA270. In case that +3.3V supply is switched off in deep-sleep mode, all the on-board peripherals are powered off and it is not possible to use external wake-up sources. In that case, recovery from deep-sleep mode must be through an internal RTC event.

For more information on PXA270 power management see *Section 3.6* in the *Intel PXA27x Processor Family Developer's Manual*, available on the development kit CD.

Peripheral devices power management

The following table gives the estimated power consumption of on-board peripherals:

On-board peripheral	Power consumption		Low-power mode	
	Typical	Maximum.	Typical	Operating mode
Dual UART	8.25mW (2.5mA@3.3V)	8.25mW (2.5mA@3.3V)	0.1mW (30uA@3.3V)	Idle
AC'97 WM9712L	81mW (24.5mA@3.3V)	81mW (24.5mA@3.3V)	0.001mW (0.5uA@3.3V)	OFF
SDRAM	363mW (110mA@3.3V)	495mW (150mA@3.3V)	2.64mW (800uA@3.3V)	Self refresh
Flash	198mW (60mA@3.3V)	297mW (90mA@3.3V)	0.0033mW (1uA@3.3V)	Standby
CPLD	33mW (10mA@3.3V)	66mW (20mA@3.3V)	0.33mW (100uA@3.3V)	Idle
RTC	0.132mW (40uA@3.3V)	0.4mW (120uA@3.3V)	0.0046mW (1.4uA@3.3V)	Idle
Atmel TPM security	148mW (45mA@3.3V)	231mW (70mA@3.3V)	0.132mW (40uA@3.3V)	Idle
Total	832mW (252mA)	1178mW (357mA)	3.21mW (972uA)	

Audio power management

The audio codec (Wolfson WM9712L) supports the standard power-down control register defined by AC'97 standard (26h). In addition, the individual sections of the chip can be powered down through register 24h. Significant power savings can be achieved by disabling the parts of WM9712L that are not being used.

Shutting down all the clocks and digital and analogue sections can reduce WM9712L consumption to near zero (1.65µW).

Using AC97_IRQ (GPIO0) it is possible to wake up PXA270 from low power mode.

For more information about power management, refer to the WM9712L datasheet at www.wolfson.co.uk/products/WM9712.

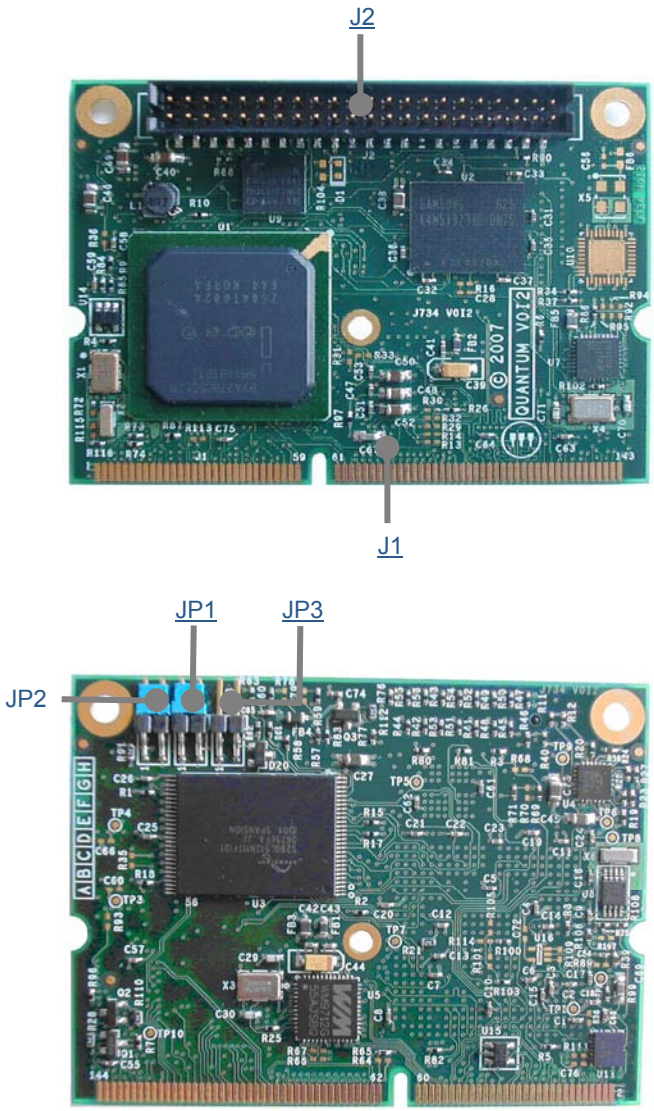
Add-on modules power management

The following table gives the estimated power consumption of add-on module devices that can be connected to QUANTUM (through the Disk-on-Module interface):

Add-on device	Power consumption		Low power mode	
	Typical	Maximum	Maximum	Operating mode
QEM	287mW (87mA@3.3V)	304mW (92mA@3.3V)	23.1mW (7mA@3.3V)	Power down
PQI Disk-On-Module device	50mW (15mA@3.3V)	99mW (30mA@3.3V)	9.9mW (3mA@3.3V)	Sleep

Jumpers and connectors

The following diagram shows the location of the connectors and jumpers on the QUANTUM:



The connectors on the following pages are shown in the same orientation as the pictures above, unless otherwise stated.

Jumpers

There are three user-configurable jumpers on the QUANTUM, as outlined below.

Connector: 2-way, 2mm single row SMT header Samtec MMT-102-02-S-SH.

JP1 – User jumper (factory flashing enable)

Pin	Signal name	Pin	Signal name	GPIO
1	GND	2	JP1	CPU_GPIO97

JP1	Description
	Firmware upgrade enable.
	Firmware upgrade disable (default).

JP2 – User jumper (Disk-On-Module interface functionality)

Pin	Signal name	Pin	Signal name	GPIO
1	GND	2	CPLD_JMP	CPLD pin B4

JP2	Description
	Disk-On-Module interface in mode ‘QUANTUM Ethernet module’.
	Disk-On-Module interface in mode ‘Disk-On-Module support’ (default).

JP3 – JTAG (programming enable)

When the JTAG port is used, JP3 must be plugged in.

JP2	Description
	JTAG programming mode.
	Normal mode (default).

Connectors

There are two connectors on the QUANTUM:

Connector	Function	Connector details in section...
J1	Interface SO-DIMM connector	J1 – Module interface connector, see below.
J2	IDE/bus extension connector	J2 – IDE/bus extension connector , page 54.

J1 – Module interface connector

Mating connector: AMP 390322-1.

No.	Signal	Description
1	GND	GND
3	SA_UDCP	USB client POSITIVE
5	SA_UDCN	USB client NEGATIVE
7	SA_FF_RI	FFUART – Ring
9	SA_FF_DCD	FFUART – DCD
11	SA_FF_DSR	FFUART – DSR
13	SA_FF_DTR	FFUART – DTR
15	SA_FF_RTS	FFUART – RTS
17	SA_FF_CTS	FFUART – CTS
19	SA_FF_TXD	FFUART – TXD
21	SA_FF_RXD	FFUART – RXD
23	SA_I2C_SCL	I^2C – clock
25	SA_I2C_SDA	I^2C – data I/O
27	IR_TXD/PWM3	STUATR – TXD
29	IR_RXD/PWM2	STUART - RXD
31	+3.3V	3.3V power supply
33	UART_TXD	Ext UART 1 – TXD
35	UART_RTS	Ext UART 1 – RTS
37	UART_RXD	Ext UART 1 – RXD
39	UART_CTS	Ext UART 1 - CTS
41	SA_BT_RTS	BTUART – RTS
43	SA_BT_CTS	BTUART – CTS

No.	Signal	Description
45	SA_BT_TXD	BTUART – TXD
47	SA_BT_RXD	BTUART – RXD
49	SA_RDY/GPIO18	Bus READY signal/GPIO18
51	NPCD0/GPIO87	CF Card detect 0 signal/GPIO87
53	PADDREN	CPLD output (Ext Buffer ENABLE)
55	CF_RESET/GPIO90	CF card RESET/GPIO90
57	NPCD1/GPIO91	CF card detect 1 signal/GPIO91
59	IRQ_CF/GPIO14	INT from CF card/GPIO14
61	GND	GND
63	SA_NPOE/GPIO48	POE/GPIO48
65	SA_NPWE/GPIO49	PWE/GPIO49
67	SA_NPIOR/GPIO50	PIOR/GPIO50
69	SA_PIOW/GPIO51	PIOW/GPIO51
71	SA_NPCE_1/GPIO85	PCE1/GPIO85
73	SA_NPCE_2/GPIO54	PCE2/GPIO54
75	SA_PSKTSEL/GPIO79	PSKTSEL/GPIO79
77	SA_NPREG/GPIO55	nPREG/GPIO55
79	SA_NPWAIT/GPIO56	nPWAIT/GPIO56
81	SA_NIOIS16/GPIO57	NIOIS16/GPIO57
83	SA_NOE	Memory bus nOE
85	SA_NWE	Memory bus nWE
87	SA_A21	Address bus SA21
89	GPIO114/CPLD_OUT	GPIO114/CPLD_OUT
91	+3.3V	3.3V power supply
93	SA_UDCP/TPY+	USB host port 2/TPY+
95	SA_UDCN/TPY-	USB host port 2/TPY-
97	H_D1+	USB host port 1 +
99	H_D1-	USB host port 1 -
101	L_DD_0	LCD data 0
103	L_DD_1	LCD data 1
105	L_DD_2	LCD data 2
107	L_DD_3	LCD data 3
109	L_DD_4	LCD data 4

No.	Signal	Description
111	L_DD_5	LCD data 5
113	L_DD_6	LCD data 6
115	L_DD_7	LCD data 7
117	L_DD_8	LCD data 8
119	L_DD_9	LCD data 9
121	L_DD_10	LCD data 10
123	L_DD_11	LCD data 11
125	+3.3V	3.3V power supply
127	L_DD_12	LCD data 12
129	L_DD_13	LCD data 13
131	L_DD_14	LCD data 14
133	L_DD_15	LCD data 15
135	L_FCLK	LCD pixel clock
137	L_LCLK	LCD line clock
139	L_PCLK	LCD frame clock
141	L_BIAS/GPIO77	LCD BIAS/GPIO77
143	GND	GND
2	GND	GND
4	SSP_EXTCLK/GPIO27	SSP1_EXTCLK/GPIO27
6	SSP_SFRM/GPIO24	SSP1_FRM/GPIO24
8	SSP_SCLK/GPIO23	SSP1_CLK/GPIO23
10	SSP_TXD/GPIO25	SSP1_TXD/GPIO25
12	SSP_RXD/GPIO26	SSP1_RXD/GPIO26
14	SSP3_RXD/GPIO82	SSP3_RXD/Ext UART 2 – RXD
16	SSP3_TXD/GPIO81	SSP3_TXD/Ext UART 2 – TXD
18	SSP3_SFRM/GPIO83	SSP3_SFRM/Ext UART 2 – RTS
20	SSP3_CLK/GPIO84	SSP3_CLK/Ext UART 2 – CTS
22	JTAG_NRST	JTAG interface – nTRST
24	JATG_TDI	JTAG interface – TDI
26	JTAG_TMS	JTAG interface – TMS
28	JTAG_TCK	JTAG interface – TCK
30	JTAG_TDO	JTAG interface – TDO
32	+VBAT_IN	Backup supply for RTC

No.	Signal	Description
34	NRESET	NRESET output
36	EXT_RST_IN	External RESET input
38	SA_MMC_CMD	MMC/SD/SDIO – CMD
40	SA_MMC_DAT0	MMC/SD/SDIO – DAT0
42	SA_MMC_CLK	MMC/SD/SDIO – CLK
44	SA_MMC_DAT3	MMC/SD/SDIO – DAT3
46	MMC_DETECT/GPIO95	MMC/SD/SDIO – card detect
48	MMC_ON/GPIO19	MMC/SD/SDIO – switch ON
50	MMC_WP/GPIO86	MMC/SD/SDIO – write protect
52	AC97_RST/L_OUT_L	AC'97 reset/GPIO113/LineOut_L
54	AC97_SYNC/L_OUT_R	AC'97 SYNC/LineOut_R
56	AC97_DATA_OUT/L_IN_L	AC'97 SDATA out/LineIn_L
58	AC97_DATA_IN/L_IN_R	AC'97 SDATA in/LineIn_R
60	AC97_BITCLK/MIC_IN	AC'97 BITCLK/MicIn
62	GND/AGND	GND/AGND
64	PWM_0/GPIO16/TPX+	PWM0/GPIO16/TPX+
66	PWM_1/GPIO17/TPX-	PWM1/GPIO17/TPX-
68	SA_A0	Address bus SA0
70	SA_A1	Address bus SA1
72	SA_A2	Address bus SA2
74	SA_A3	Address bus SA3
76	SA_A4	Address bus SA4
78	SA_A5	Address bus SA5
80	SA_A6	Address bus SA6
82	SA_A7	Address bus SA7
84	SA_A8	Address bus SA8
86	SA_A9	Address bus SA9
88	SA_A10	Address bus SA10
90	SA_RD_NWR	Bus signal RDnWR
92	+3.3V	3.3V power supply
94	SA_D0	Data bus SD0
96	SA_D1	Data bus SD1
98	SA_D2	Data bus SD2

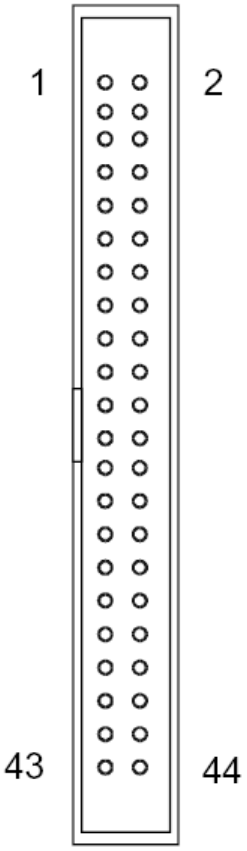
No.	Signal	Description
100	SA_D3	Data bus SD3
102	SA_D4	Data bus SD4
104	SA_D5	Data bus SD5
106	SA_D6	Data bus SD6
108	SA_D7	Data bus SD7
110	SA_D8	Data bus SD8
112	SA_D9	Data bus SD9
114	SA_D10	Data bus SD10
116	SA_D11	Data bus SD11
118	SA_D12	Data bus SD12
120	SA_D13	Data bus SD13
122	SA_D14	Data bus SD14
124	SA_D15	Data bus SD15
126	+3.3V	3.3V power supply
128	GPIO116/USBC_DET	GPIO116/USBC_DET
130	A97_IRQ/USBHPEN0/GPIO89	Ext AC97_IRQ/USBHPEN0/GPIO89
132	SA_MMC_DAT1	MMC/SD/SDIO – DAT1
134	USBHPWR0/GPIO88	USBHPWR0/GPIO88
136	SA_MMC_DAT2	MMC/SD/SDIO – DAT2
138	SA_NCS_2/GPIO78	Bus signal CS2/GPIO78
140	SA_NCS_4/GPIO80	Bus signal CS4/GPIO80
142	GPIO115	GPIO115
144	GND	GND

J2 – IDE/bus extension connector

Connector: Molex 87832-4420

Mating connector: Samtec TLE-122-01-G-DV-A

Pin no.	Signal	Pin no.	Signal
1	NRESET#	2	GND
3	SA_D7	4	SA_D8
5	SA_D6	6	SA_D9
7	SA_D5	8	SA_D10
9	SA_D4	10	SA_D11
11	SA_D3	12	SA_D12
13	SA_D2	14	SA_D13
15	SA_D1	16	SA_D14
17	SA_D0	18	SA_D15
19	GND	20	NC(GPIO001)
21	NC(GPIO002)	22	GND
23	IDEIOW#(nOE)	24	GND
25	IDEIOR#(nWE)	26	GND
27	SA_RDY#_GPIO18	28	GND
29	DMACK#(GPIO003)	30	GND
31	IDE_IRQ(IRQ)	32	IOCS16#(SA_A21)
33	SA_A2	34	PDIAG#(SA_A4)
35	SA_A1	36	SA_A3
37	IDECSO#(CS1)	38	CS3FX#(CS2)
39	NC	40	GND
41	+3.3V	42	+3.3V
43	GND	44	TYPE



The IDE interface on the QUANTUM doesn't support devices with a 5V supply voltage (such as standard 3.5" or 2.5" hard drives), so be sure that connected devices support a 3.3V supply.

Appendix A – Contacting Eurotech Ltd

Eurotech Ltd sales

Eurotech Ltd's sales team is always available to assist you in choosing the board that best meets your requirements.

Eurotech Ltd
3 Clifton Court
Cambridge
CB1 7BN
UK

Tel: +44 (0)1223 403410
Fax: +44 (0)1223 410457
Email: sales@eurotech-ltd.co.uk

Comprehensive information about our products is also available at our web site: www.eurotech-ltd.co.uk.

While Eurotech Ltd's sales team can assist you in making your decision, the final choice of boards or systems is solely and wholly the responsibility of the buyer. Eurotech Ltd's entire liability in respect of the boards or systems is as set out in Eurotech Ltd's standard terms and conditions of sale. If you intend to write your own low level software, you can start with the source code on the disk supplied. This is example code only to illustrate use on Eurotech Ltd's products. It has not been commercially tested. No warranty is made in respect of this code and Eurotech Ltd shall incur no liability whatsoever or howsoever arising from any use made of the code.

Eurotech Ltd technical support

Eurotech Ltd has a team of dedicated technical support engineers available to provide a quick response to your technical queries.

Tel: +44 (0)1223 412428
Fax: +44 (0)1223 410457
Email: support@eurotech-ltd.co.uk

Eurotech Ltd Group

Eurotech Ltd is a subsidiary of Eurotech Group. For further details see www.eurotech.com

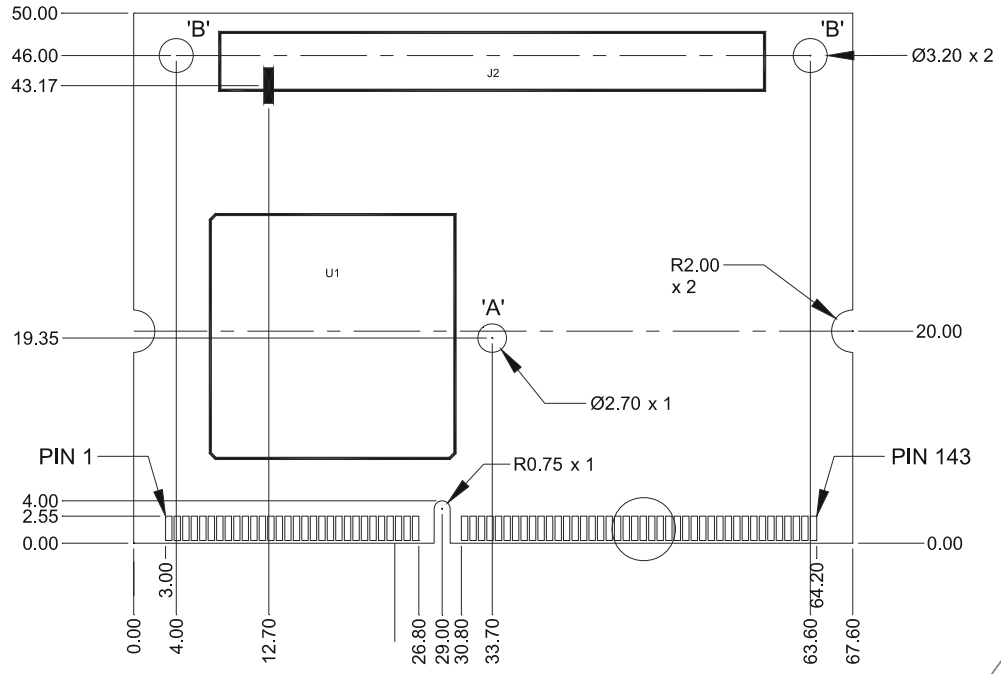
Appendix B – Specification

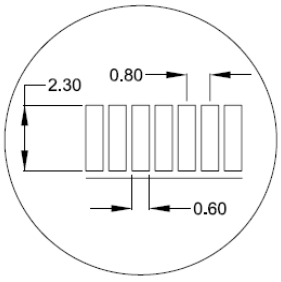
Processor	Intel PXA270 312/416/520MHz XScale® processor (520MHz as standard).
System memory	Fixed on-board 64MB SDRAM (32-bit wide SDRAM data bus).
Silicon disk	Fixed on-board memory, 1/16/32/64MB on-board Flash.
5 serial ports	Three UART serial ports: • FFUART serial port. • BTUART serial port. • Standard UART serial port. Dual extra high speed Full Function UART (FFUART): • 16C2552 compatible UART. • RS485 half-duplex direction control.
USB support	USB 1.1 host/client controller port supporting 12Mb/s and 1.5Mb/s speeds. USB 1.1 host controller port supporting 12Mb/s and 1.5Mb/s speeds.
Extension buses	IDE/bus extension on-board interface (for 3.3V devices only). MMC/SD/SDIO interface. I^2C bus. CF interface bus. Two Synchronous Serial Ports (SSP).
Video	16-bit flat panel interface. For STN and TFT displays.
Audio codec, touchscreen	AC'97 compatible codec. Line In, Line Out, Microphone In. Touchscreen support – 4-wire analogue resistive.
RTC	Battery-backed RTC device. *
TPM	Atmel Trusted Platform module device, TCG v1.2 compatible (optional).
GPIO	Up to 78 (depends on used interfaces).
PWM	2(4) x PWM output.
Test support	JTAG interface.

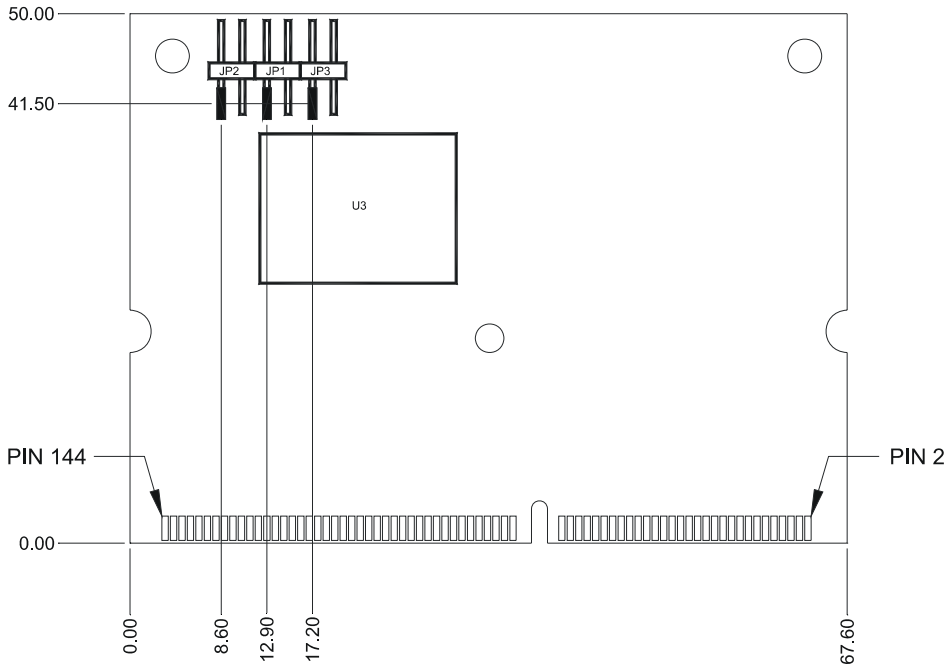
* The battery is not part of the board; it should be connected to the dedicated SO-DIMM pin.

Power requirements	Maximum 3.3V/0.7A.
Mechanical	SO-DIMM factor, 67.6mm x 50mm.
Environmental	Operating temperature: • Industrial: -40 to +85°C . • Commercial: -20 to +70°C. RoHS Directive: Compliant.

Appendix C – QUANTUM mechanical diagram



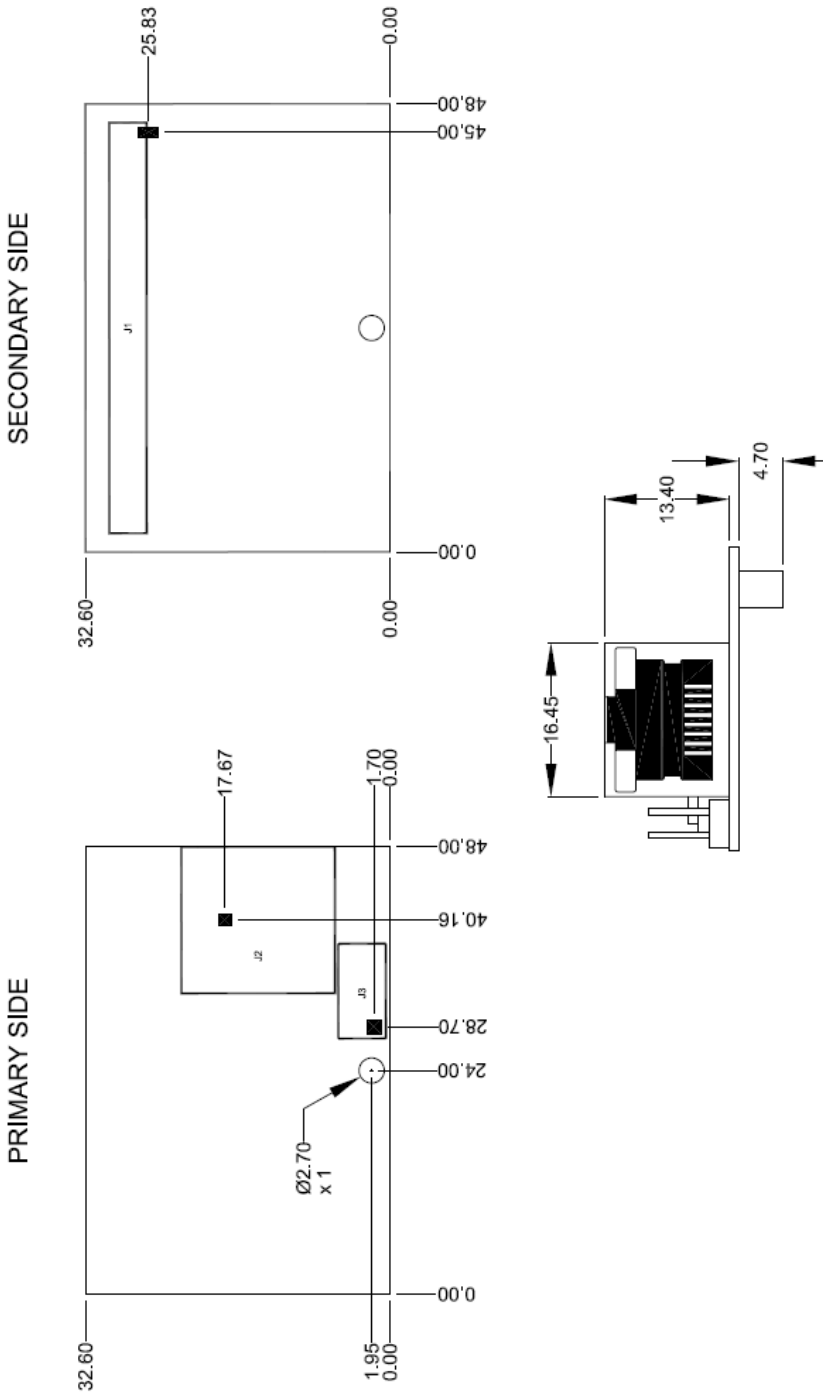




Please note:

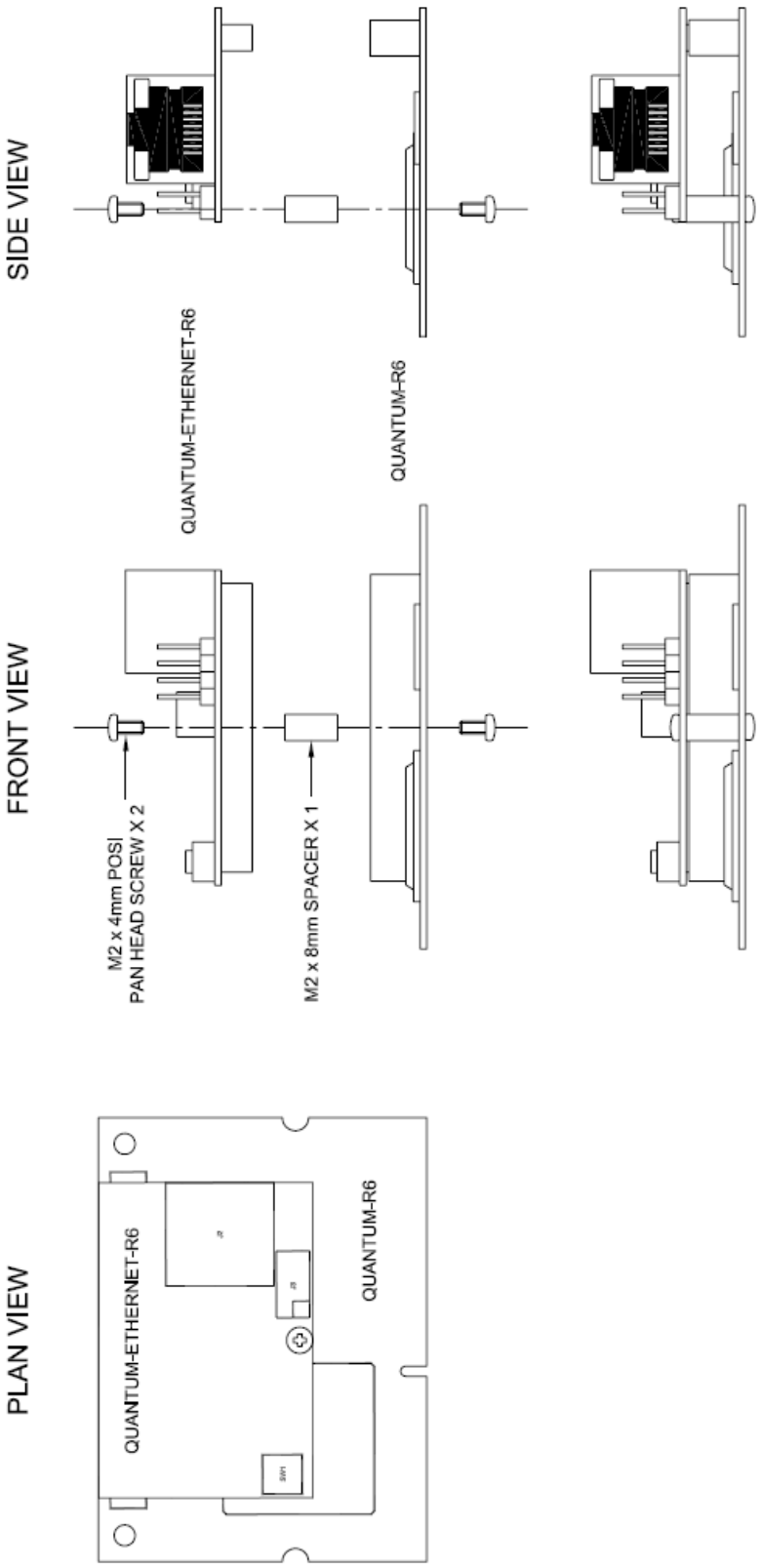
- All connector distances are taken from PIN 1.
- Board thickness is 1.00mm.

Appendix D – QUANTUM Ethernet module



Please note:

- All connector distances are taken from PIN 1.
- Board thickness is 1.00mm.


SIDE VIEW
QUANTUM-ETHERNET-R6
QUANTUM-R6
FRONT VIEW
M2 x 4mm POSI
PAN HEAD SCREW X 2
M2 x 8mm SPACER X 1
PLAN VIEW
QUANTUM-ETHERNET-R6
QUANTUM-R6

Appendix E - Reference information

Product Information

Product notices, updated drivers, support material, 24hr-online ordering:

www.eurotech-ltd.co.uk

USB Information

Universal Serial Bus (USB) Specification and product information:

www.usb.org

SDIO card information

SD Card Association and product information:

www.sdcard.org

www.sdcard.com

CompactFlash information

CompactFlash Association and product information:

www.compactflash.org

Davicom Semiconductor Inc

Davicom DM9000A Ethernet Controller documentation:

www.davicom.com.tw/eng/products/dm9000a.htm

Exar Corporation

Exar XR16C554DCQ Quad UART documentation:

www.exar.com/product.php?ProdNumber=XR16V2752&areaID=3

Wolfson Microelectronics

Wolfson WM9712L AC'97 codec documentation:

www.wolfson.co.uk/products/WM9712

Spansion

S29GL-N MirrorBit™ Flash family documentation:

www.spansion.com

Intersil

RTC ISL1208 documentation:

www.intersil.com/cda/deviceinfo/0,1477,ISL1208,0.html

Atmel

Atmel Trusted Platform Module device AT97SC3203S:

www.atmel.com/dyn/products/product_card.asp?part_id=3781

Appendix F - Acronyms and abbreviations

BGA	Ball Grid Array
BSDL	Boundary Scan Description Language
BTUART	Bluetooth®Universal Asynchronous Receiver/Transmitter
CF	Compact Flash
CODEC	Coder/Decoder
COM	Communication Port
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit (PXA270)
CMOS	Complementary Metal Oxide Semiconductor
DIMM	Dual In-line Memory Module
DMA	Direct Memory Access
DoM	Disk-on-Module
DUART	Dual Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Erasable and Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EPROM	Erasable and Programmable Read-Only Memory
FFUART	Full Function Universal Asynchronous Receiver/Transmitter
FIFO	First-In First-Out
FLASH	A non-volatile memory that is preserved even if the power is lost
GPIO	General Purpose Input/Output
I^2C	(=IIC) Intra Integrated Circuit bus
ICE	In-Circuit-Emulator
IDE	Integrated Drive Electronics
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
JTAG	Joint Test Action Group of IEEE
LED	Light Emitting Diode
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MMC	MultiMedia Card
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NA	Not Applicable
NC	No Connect
NU	Not Used
OS	Operating System
PCB	Printed Circuit Board
PROM	Programmable Read-Only Memory
PSU	Power Source Unit
PWM	Pulse-Width Modulation
QEM	QUANTUM Ethernet module
RAM	Random Access Memory
Reg	Regulator
RTC	Real Time Clock
Rx	Receive

SBC	Single Board Computer
SD	Secure Digital
SDIO	Secure Digital Input/Output
SDRAM	Synchronous Dynamic Random Access Memory
SMT	Surface Mount Technology
SO-DIMM	Small Outline Dual In-line Memory Module
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
STN	Super Twisted Nematic, technology of passive matrix liquid crystal
STUART	Standard Universal Asynchronous Receiver/Transmitter
SVGA	Super Video Graphics Adapter, display resolution 800 x 640 pixels
TFT	Thin Film Transistor, a type of LCD flat-panel display screen
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WD	WatchDog
VGA	Video Graphics Adapter, display resolution 640 x 480 pixels

Appendix G – RoHS-6 compliance - Materials Declaration Form

EuroTech Ltd
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Confirmation of Environmental Compatibility for Supplied Products

Substance	Maximum concentration
Lead	0.1% by weight in homogeneous materials
Mercury	0.1% by weight in homogeneous materials
Hexavalent chromium	0.1% by weight in homogeneous materials
Polybrominated biphenyls (PBBs)	0.1% by weight in homogeneous materials
Polybrominated diphenyl ethers (PBDEs)	0.1% by weight in homogeneous materials
Cadmium	0.01% by weight in homogeneous materials

The products covered by this certificate include:

Product Name	Eurotech Ltd Part Number
QUANTUM	QUANTUM-R6 (all variants)
QUANTUM Ethernet	QUANTUM-ETHERNET-R6

Eurotech Ltd has based its material content knowledge on a combination of information provided by third parties and auditing our suppliers and sub-contractor's operational activities and arrangements. This information is archived within the associated Technical Construction File. Eurotech Ltd has taken reasonable steps to provide representative and accurate information, though may not have conducted destructive testing or chemical analysis on incoming components and materials.

Additionally, packaging used by Eurotech Ltd for its products complies with the EU Directive 2004/12/EC in that the total concentration of the heavy metals cadmium, hexavalent chromium, lead and mercury do not exceed 100 ppm.

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