User's Manual LA-2132 LVDS LA-2132 Series LA-2164 Expand Logic Analyzer

Revision II Software Win 98/me/2000/xp/Vista Version



Item Checklist	3
System Requirements	4
Installing Hardware	4
Installing LA-2132 LVDS or LA-2132 Series with USB 2.0 Cable.	4
Installing Software	4
I/O Pin Location	5
Expand To 64 Channels	6
Guide To Operations	7
Hardware	7
Connecting Wires to Logic Analyzer	7
LVDS (Low Voltage Differential Signal)	8
Main Screen	9
Timing Window	10
Multi-Window	11
Capture Mode	14
Trigger Mode Setup (Trigger Menu)	14
Trigger Levels Specifications of LA-2132 Series:	14
How to Set Trigger Word	
Trigger Position	17
Trigger Word Setup	17
Width Bit	19
Width Bit With Timing	22
Width Bit By Rising (Falling) Clock	24
1 Bit Data By Rising Clock	26
I ² C	27
Threshold Voltage Setup	28
Clock Menu	28
External Clock	29
Magnify (Timing)	29
Zoom Combo	30
Zoom	30
Timing Window	30
Setting Up Group	32
Setting Up The State/Timing Window	33
Setting Channel Names And Colors	34
Search By Cursor	34
Search By Group	35
Export (File Menu)	

File Menu Commands	
Hardware Specifications	
Expand to 64 Channels Is Available	
LA-2132 LVDS Series Hardware Specifications	40
LA-2132 Series Hardware Specifications	41
LA-2164 Series Hardware Specifications	42
Window USB Driver Install	43
Windows 98/ME USB driver install	43
Windows 2000 USB driver install	44
Windows XP USB driver install	48
Windows Vista USB driver install	50
Threshold Voltage Calibration	54
Trigger Word and Position Calibration	54
Trigger Sequential Calibration	55
Clock Source Calibration	55
Technical Support	56
Software Updates	56

Item Checklist

1. The LA-2132 LVDS or LA-2132 Series Plastic unit.

There are two Models is available for LA-2132 LVDS:

LA-2132 LVDS: (32 channels only, can't expand to 64 Channels).

- K2 (250MHz, 256K Memory, 2 Trigger Levels, support LVDS, LPECL).
- G512 (1GHz, 4Mega Memory, 512 Trigger Levels, support LVDS, LPECL).

There are nine Models is available for LA-2132 Series:

LA-2132K Series: (Expand to 64 channels is available, without support LVDS, LPECL).

- K2 (250MHz, 256K Memory, 2 Trigger Levels).
- ☐ K8 (250MHz, 256K Memory, 8 Trigger Levels).
- K512 (250MHz, 256K Memory, 512 Trigger Levels).

LA-2132M Series: (Expand to 64 channels is available, without support LVDS, LPECL).

- ☐ M2 (500MHz, 1Mega Memory, 2 Trigger Levels).
- ☐ M8 (500MHz, 1Mega Memory, 8 Trigger Levels).
- M512 (500MHz, 1Mega Memory, 512 Trigger Levels).

LA-2132G Series: (Expand to 64 channels is available, without support LVDS, LPECL).

- G2 (1GHz, 4Mega Memory, 2 Trigger Levels).
- G8 (1GHz, 4Mega Memory, 8 Trigger Levels).
- G512 (1GHz, 4Mega Memory, 512 Trigger Levels).
- 2. One 20 pin flat cable (Length is 25 CM).

[This 20 pin flat cable use for LA-2132 Expand to 64 Channels only].

- 3. Two harness with each 32 color wires and 50 Easy Hook clips.
- 4. Ten pieces color wires with Easy Hook clips [this is for LA-2132 LVDS only].
- 5. One LA-2132 LVDS / Series User's Manual.
- 6. One CD for LA-2132 Series driver.
- 7. One USB 2.0 cable (Mini Type).
- 8. One special USB 2.0 cable (Mini Type) with 2 head connector.

[This special 2 head connector USB 2.0 cable use for LA-2132 Expand to 64 Channels only].

System Requirements

In order to use the Logic Analyzer, the following equipment is necessary: Computer System : Support USB interface (USB 1.1 or 2.0 version) Memory : A minimum of 128 Mega free RAM. 512 Mega or 1024 Mega is better. Mass Storage : At least one CD drives and hard disk drives. Display Adapter : At least one of VGA Adapter. Two display interface are better [Resolution 1440 X 900 is better]. Monitor : Any monitor compatible with the above display adapter. Two monitor is better.

Operation System : Windows me / 2000 / XP / Vista.

Installing Hardware Installing LA-2132 LVDS or LA-2132 Series with USB 2.0 Cable.

Please follow these instructions for installing the Logic Analyzer with USB cable.

- 1. Turn off the computer and all peripherals connected. Remove the computer power cord from the wall outlet. Locate an available USB interface (version USB 2.0 or USB 1.1).
- 2. Connect the included USB cable to USB interface.
- 3. Connect the other end of the USB cable to the LA-2132 USB port.
- 4. After checking all connections, turn on the computer and peripherals. You are now ready to install the software.

Installing Software

- 1. Insert the distribution CD into drive E: ("E" is CD driver).
- 2. Run Windows.
- 3. Select File menu.
- 4. Select Run option.
- 5. Enter file to run setup.exe
- 6. Follow the on screen instructions.

I/O Pin Location

LA-2132-LVDS: (32 channels only, can't expand to 64 channels).



LA-2132 Series: (Expand to 64 channels is available, without support LVDS).

	" LA-2132 Series	
1	" DC Basad	
1::1	PC Based	
1		
4	66 LOGIC Analyzer	
		40
1		12
1::		- 10
1::1		512
	12 G2 G8 G5	512
	13	
	14	
1	15	
_		
•••	16	
	16	
	16 17 18	
	16 17 18 19	
	16 17 18 19 20 21	••
	16 17 18 19 20 21 22	::
	17 17 18 19 20 21 22 23 4 2	::
	16 17 18 19 20 21 22 23 23 24 24	::
	16 17 18 19 20 21 22 23 24 25 26 24 25 25	
	16 17 18 19 20 21 22 23 24 24 25 24 25 26 26 26 26 26 26 26 26 26 26 26 26 26	::
	17 17 18 19 20 21 22 23 24 25 25 26 27 27 27 20 20 27 20 20 20 20 21 20 20 20 20 20 20 20 20 20 20 20 20 20	
	16 17 18 19 20 21 22 23 24 25 24 25 26 20 28 20 28 20 20 20 20 20 20 20 20 20 20	
	16 17 18 19 20 21 22 23 24 25 26 26 27 28 26 27 28 28 26 20 29 29 29 29 29 20 20 20 21 20 21 22 23 24 20 22 20 22 23 24 20 25 20 20 20 20 20 20 20 20 20 20 20 20 20	· · · · · · · · · · · · · · · · · · ·
	16 17 18 19 20 21 22 23 24 25 26 26 26 27 28 26 20 26 20 20 20 20 20 20 20 20 20 20	· · · · · · · · · · · · · · · · · · ·
	16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 (Ext. CLK)	· · · · · · · · · · · · · · · · · · ·

Expand To 64 Channels

The LA-2132 Series can be Expanded to 64 Channels by use one 20 pin flat cable from #1 LA-2132 connect to #2 LA-2132, (it only support 32 channels trigger word even it is 64 channels now).



Note: It can Expand to 64 channels when the two LA-2132 Series connect together By one 20 pins flat cable (But LA-2132 LVDS can not Expand to 64 channels). Please take a notice in order to support enough current, it is better to use 2 head of Special USB 2.0 cable insert to USB 2.0 port of your computer.

Guide To Operations

Hardware

When making measurements with the Logic Analyzer, meaningful data can only be captured with some prior knowledge of the characteristics of the circuit under test. Before initiating any capture cycles, the Logic Analyzer must be configured using the control program. See the software section later in the manual for instructions on these procedures. To connect the Logic Analyzer to the test circuit, a series of mini-clips on the Logic Analyzer input channels. The LA-2132 Logic Analyzer has inputs for 32 channels ch0 to ch31. the ch31 channel is the external clock input.

At times, it may also be necessary to connect the test circuit to the computer system itself. This will eliminate more noise in the test application due to ground level differentials. This is especially true when dealing with high speed timing analysis. Use a heavy gauge wire to make a connection between the test circuit ground and the case of the computer.

Connecting Wires to Logic Analyzer

It has 64 pins [dual in line 32 pins posts]. They are organized as follows: Right side:

00..31 Channels 0..31

ch 31 External clock input

Left side all pins are **Ground** connection

The wires and the clips are modular. the wires and clips can all be disconnected from each other by gently pulling them apart. Removing just the clips, but leaving the wires connected to the pods allows connections to be made to wires and posts of the test circuit of up to 0.64 mm (0.025 in).

Do not insert wires or posts greater than this diameter as that will expend the contacts in the wire beyond the allowed limit, possibly damaging the connector.

LVDS (Low Voltage Differential Signal)

LA-2132 LVDS has another connector header [dual in line10 pins posts]

it has 4 LVDS signals 1 tri-state control input signal. 1 trigger out.

The following diagram show 2 channels bi-direction LVDS with 1 channel tri-state control and 2 channels LVDS input signal and 1 trigger out.

/Tri-State control line is pulled low to 10 Kohm.

It can out 100 MHz and 50 MHz LVDS signal if /Tri-State is pulled high or connected to 5V. LVDS0, LVDS1, LVDS2, LVDS3 are LVDS signal. LVDS0, LVDS1 has 1 Kohm cross it. It also can accept LPECL signal. LVDS0 can work as external clock.



Caution: All these signals only accept 0 - 5 Volts, exceed this range will damage this Logic Analyzer.

Vcc inhibit short to ground otherwise your computer will damage.

Main Screen

🗷 LA-2	132-	G512 (1 (GHz, 4 Me	ga Men	nory,5	512 le	vels) - [Tin	ning vi	iew 1	time	of last dat) es	win
📴 Eile	View	/ Timing	<u>R</u> eset Tri	g <u>e</u> r Y	Vindow	∕ <u>H</u> e	lp		15				
😡 🐠	TRIG	Status	Count	0990.mV	Normal	÷ 8k	250Mhz	xxxxxx	111 XXXX	Xxxx XXX	XXXXXX XXXXX		ND ÷
Cursor A	602	A-B -720.nS	Curso	rT. zoom 🧧	•								
Cursor B	782	A-T -1.52uS	Magr	ifu 1									
Trigger	982	B-T -800.nS											
ana ana ang ang ang ang ang ang ang ang		Screen 582	ئے سے				أحنيه						
Hex31-0	000		24242424				2B2B2B2B			202	2C2C2C		
Dec31-0	000		707406378				724249387			741	1092396		
ASCII 31-0	000))** •)***	****	***+	**++	*+++	++++	+++,	++,, +	m m	1	m	
Binary31-0	00 0												
Chan D 0	011								No. Ale				
Chan D 1	111												
Chan D 2	000												
Chan D 3	111												

Menu bar



Tool bar



State list

Data is displayed in state list format in this window.

Chan D 24	000							
Chan D 25	000							
Chan D 26	000							
Chan D 27	000-		11					
	•	Position	i i Hexdecimal	Decimal	ASCII	Binary	Example	USER1
		0	000000	0		000000000000000000000000000000000000000	/read	
		1	000000	0		000000000000000000000000000000000000000	/read	
	1	2	000000	0		000000000000000000000000000000000000000	/read	
partition of	-	3	000000	0		000000000000000000000000000000000000000	/read	
timing and	-	4	000000	0		000000000000000000000000000000000000000	/read	
state	-	5	000000	0		000000000000000000000000000000000000000	/read	
		6	000000	0		000000000000000000000000000000000000000	/read	
Memory	1	7	000000	0		000000000000000000000000000000000000000	/read	
position		. 8	000000	0		000000000000000000000000000000000000000	/read	
		A 9	000000	0		000000000000000000000000000000000000000	/read	
		10	000000	0		000000000000000000000000000000000000000	/read	
		B 11	000000	0		000000000000000000000000000000000000000	/read	
		T 12	000000	0		000000000000000000000000000000000000000	/read	
		13	000000	0		000000000000000000000000000000000000000	head	

Timing Window



Multi-Window

Software open more timing if system free memory have a lot. So use 512 Mega or 1024 Mega memory will be better.

Data1- 4 to timing by point User point which timing memory should be placed for captured data, it can let user captured 2 or 4 set different data to buffer and display, the sequence pointed by user, this function let user have 1Mega*4 memory size.

Data1- 4 to timing by auto The same is true for it, it automatically capture 2 or 4 sets data to buffer, the sequence is 10,9,8,7,6,5,4,3,2 then 1.

Timing1- 4<-data Activate timing display. we suggest user use more than 1 monitor to get better show.

This software is a revolution software, it have a lot of new function, even tradition famous oscilloscope have not these powerful function.

this software show a lot of timing, let user easy to compare and analyzer timing, tradition software no matter it is stand alone or computer base oscilloscope only show one timing, these one timing software only analyzer one segment of buffer, unlike this software it can look buffer in beginning and buffer in middle and buffer in end at the same time. The following picture part A show it is locate at beginning and part B at middle of buffer at the same time, every individual timing also support their own cursor, voltage measurement, zoom factor .. etc.

Ck LA-213	2-512K					
<u>File V</u> iew	<u>T</u> iming	<u>R</u> eset Tr <u>igg</u> er	<u>W</u> indow	<u>H</u> elp		
😡 👳	TRIG	Status		ount 01	.34V 🛨	Normal
💷 Timing	view 2	time of last	data= On	18		
Cursor A	80	A-B -1.92uS	[(CursorT. zooi	m 🔽	
Cursor B	560	A-T -960.nS		Magnify 1	A	
Trigger	320	B-T 960.nS	9 .	.ink		
		Screen 0				
Hexdecimal	000	000000		010101		0202
Decimal	0 0 .0	0		65793		1315
ASCII	000			1		
Binary	000					
Chan D 0	000					
Chan D 1	001	<u>.</u>				
Chan D 2	010	2	<u> </u>			
Chan D 3	000	·	i			-
Chan D 4	000	-				
💷 Timing	view 1	time of last	data= On	15		
Cursor A	80	A-B -40.nS	Ī	CursorT, zooi	n 🔽	
Cursor B	90	A-T 80.nS	-	vlaonifu e 172	B	
Trigger	(60)	B-T 120.nS	24 1			
		Screen 0		<u> </u>	-	
Hexdecimal	000	000000	10101	020202	030303	0404
Decimal	000	0 6	5793	131586	197379	2631
ASCII	0 0 10					
Binary	000					
Chan D 0	000					
Chan D 1	000					

Another new function are let memory expand to 4 times by software, If memory size is 1 Mega size, this software can let it look like have 4 Mega size when user open 4 timing and set 4 timing by auto function. (it need 1024 Mega system memory or more). the method is software continue capture data to these 4 timing, every timing have 1 Mega individual buffer, so user can look almost 4 Mega memory.

it is better than any famous oscilloscope in the world. the third big function are it can show long timing when you have two monitor, the following show two monitor long timing, it can let user easy analyze timing, so the stand alone oscilloscope can not do it, because they only have one monitor.

📴 Timin	igiview 1	time of last data=0ms	
Cursor A	1000	A-B -3.6uS	
Cursor B	1180	A-T -7.6uS	Magnifu 1
Tiigger	1386	B·T -4.uS	
00	00000000	Screen 221	
B1 Ch	0 00		
B1 Ch	1 00	🛯 🚽 โกกการการรถการการการการการการการการการการการการการก	
B1 Ch	2 00	1 mmmmm	
ei ch	10	a mununur	
TH	4 0.0		

The fourth function is it can support two different timing at different monitor. the follow picture is left monitor show square waveform with magnify 1 and right monitor show the waveform with magnify 1/2. it easy compare last capture data and current data at different monitor. These function even famous oscilloscope have not support it.

IK LA-213	2-512K									
<u>File V</u> iew	Timing	<u>R</u> eset Tr <u>igg</u> er <u>W</u> ind	ow <u>H</u> elp							
<u>60</u> 🎯	TRIG	Status	Count 01.34V + Norr		250Mhz 🔶 🗴	xxxxxxx	xxxxxxxxx	XXxxxXXX	xxxxxx	XX1 🗛
	uion (time of last data-	0mc			vion 1	time of las	t data- Oma		
Cursor A	80	A-B -1.92uS	· OIIIS		Cursor A	80	A-B -40.nS			
	-	-	CursorT. zoom 💌					Curs	orT. zoom	-
Cursor B	560	A-T -960.nS	Magnify 1 🔍		Cursor B	90	A-1 80.nS	Mac	nify 1/2	-
Trigger	320	B-T 960.nS	11		Trigger	60	B-T 120.nS		1	Concerned St.
		Screen 340					Screen 0		.	
Hexdecimal	000	<mark>-</mark> 020202 030303	040404	050505	Hexdecimal	000	000000	010101 02	20202	030303
Decimal	000	197379	263172	328965	Decimal	000-	0	65793 13	31586	197379
ASCII	000				ASCII	000				
Binary	000				Binary	000				
Chan D 0	000				Chan D 0	000				
Chan D 1	001				Chan D 1	000				-
Chan D 2	010				Chan D 2	000	<u> </u>	4.0		
Chan D 3	000	•	i		Chan D 3	000.	<u>⊢ †ii</u>			
Chan D 5	000		1		Chan D 5	000	111			
Chan D 6	000				Chan D 6	000				
Chan D 7	000				Chan D 7	000	- 0 0-140			

Capture Mode

Set trigger acquisition mode.

- Single The LA looks for the trigger event. When it is found acquire a single buffer worth of data and stop.
- Normal The LA looks for the trigger event. When it is found acquire a buffer worth of data, re-arm and repeat until stop is hit.
- Auto Similar to Normal except that it will acquire regardless of the trigger event.

Trigger Mode Setup (Trigger Menu)

Trigger Levels Specifications of LA-2132 Series:

Model	 LA-2132- K2 (250 MHz, 256 K Memory, 2 Trigger levels) LA-2132- K8	 LA-2132- M2 (500 MHz, 1 Mega Memory, 2 Trigger levels) LA-2132- M8 (500 MHz, 1 Mega Memory, 8 Trigger levels) LA-2132- M512 (500 MHz, 1 Mega Memory, 512 Trigger levels) 	 7. LA-2132-G2 (1 GHz, 4 Mega Memory, 2 Trigger levels) 8. LA-2132-G8 (1 GHz, 4 Mega Memory, 8 Trigger levels) 9. LA-2132-G512 (1 GHz, 4 Mega Memory, 512 Trigger levels)
2 Trigger	with IF word xx happen yy times then next level else go to level 0 trigger structure . 1048576 event counter/every level 1 to1048576* (1 sec to 10nsec) delay time /every levels	with IF word xx happen yy times then next level else go to level 0 trigger structure. 1048576 event counter/every level 1 to 1048576* (1 sec to 10nsec) delay time /every levels	with IF word xx happen yy times then next level else go to level 0 trigger structure. 1048576 event counter/every level 1 to 1048576*(1 sec to 10nsec) delay time /every levels
Levels	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232) (NO) I ² C serial trigger (NO)	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232) (NO) I ² C serial trigger (NO)	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232) (NO) I ² C serial trigger (NO)

8	with IF word xx happen yy times	with IF word xx happen yy times	with IF word xx happen yy times
	then next level else go to level 0	then next level else go to level 0	then next level else go to level 0
	trigger structure.	trigger structure.	trigger structure.
	1048576 event counter/every	1048576 event counter/every	1048576 event counter/every
	level 1048576*(1 sec to	level 1048576*(1 sec to	level 1048576*(1 sec to
	10nsec) delay time /every	10nsec) delay time /every	10nsec) delay time /every
	levels	levels	levels
8 Trigger Levels	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232.)(difficulty) can work for 3 bit serial stream only I ² C serial trigger (NO)	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232.)(difficulty) can work for 3 bit serial stream only I ² C serial trigger (NO)	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232.)(difficulty) can work for 3 bit serial stream only I ² C serial trigger (NO)
512	with IF word xx happen yy times	with IF word xx happen yy times	with IF word xx happen yy times
	then next level else go to level 0	then next level else go to level 0	then next level else go to level 0
	trigger structure 1048576 event	trigger structure 1048576 event	trigger structure 1048576 event
	counter / every level 1048576*	counter / every level 1048576*	counter / every level 1048576*
	(1 sec to 10nsec) delay time /	(1 sec to 10nsec) delay time /	(1 sec to 10nsec) delay time /
	every levels.	every levels.	every levels.
Trigger Levels	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232) (YES) I ² C serial trigger (YES) all kind of trigger (YES) it is universal trigger structure	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232) (YES) I ² C serial trigger (YES) all kind of trigger (YES) it is universal trigger structure	detect width pulse in narrow stream detect narrow pulse in width stream trigger before delay (YES) serial trigger (RS232) (YES) I ² C serial trigger (YES) all kind of trigger (YES) it is universal trigger structure

A trigger word is the pattern that the Logic Analyzers needs to see before it will start to

acquire data. The trigger word is made of a series of "1", "0" and "x" (don't care) bits.

AND mode need 32 channels all match trigger condition.

OR mode need one of 32 channels match trigger condition.

It can set at toolbar or parameters form.



🗟 Paran	neters	
Trig Word	XXXXXXXX XXXXXXXX	XXXXXXXX XXX
Source	Internal	-
Voltage	01.34V 🚟	
Acquire	Normal	
Memory	8K 💽	
Rate	250MSa(4ns) 💌	
Mode	32 channels 🚽	

Ch31..24 Edit pattern for channels 31 to 24 Ch23..16 Edit pattern for channels 23 to 16 Ch15..8 Edit pattern for channels 15 to 8 Ch7..0 Edit pattern for channels 7 to 0 Logic Trigger if condition is true or false.

True logic need trigger condition from false to true.

False logic need trigger condition from true to false.

How to Set Trigger Word

- You can edit all 32 channels at a time.
 Edit the pattern: The LSB is to the right. Each bit can be set to "0", "1" or "x" (don't care, true, false).
- 2) You can set the trigger logic to "True" (trigger when pattern matches) or "False" (trigger when pattern stops matching).

Trigger Position

The trigger position defines how much data is captured prior to the trigger event and how much data stored after it. You set the Trigger position by moving the trigger cursor. This feature allows you to see the data that led up to the trigger as well as what happened after the trigger.

80
560
320

Trigger Word Setup

A sequence of up to 512 trigger words can be set. A trigger word is the pattern that the Logic Analyzers needs to see before it will start to acquire data. The trigger word is made of a series of "1", "0" and "x" (don't care) bits.

It can set trigger word at toolbar or parameter form or trigger form.



💐 Paran	ieters		
Trig Word	XXXXXXXX	XXXXXXXX	XXxxxXXX XXX
Source	Internal		-
Voltage	01.34V 📑		
Acquire	Normal	-	
Memory	8K	-	
Rate	250MSa(4ns)	•	
Mode	32 channels	-	

🖻 tri	gg	er													
				CH31-2-	4	CH2	23-16	CH1	5-8	CH7-0					
				*****	XXX	<u> </u>	XXXX	XXxx	×XXX	*******	Word	0 🔹		Update	
Level 0	IF	AND	▼ Ever	nt 🗖	· ·	•	Word0	•	1	then nex	t level		-	Ţ	Group edit
Level 1	IF	AND	- Ever	nt 🗖	-	•		•	1	then nex	t level	-	•		Trigger group
Level 2	IF	AND	- Ever	nt 🗖		•		•	1	then nex	t level		•		Serial Trigger
Level 3	IF	AND	- Ever	nt 🗖	• •	•		-	1	then nex	t level		•		
Level 4	IF	AND	▼ Ever	nt 🗖	•	•		-	1	then nex	t level	-	•		
Level 5	IF	AND	- Ever	nt 🗖		•		-	1	then nex	t level		•		
Level 6	IF	AND	- Ever	nt 🗖		•		-	1	then nex	t level	-	•		
Level 7	IF	AND	- Ever	nt 🗖		-		-	1	then nex	t level		•		
	nt – C	iggered ∙ Widi ⊂ Widi	dit in serial- th bit th bit with ti	ming	1	C Width C Width	n bit by ris n bit by fa	ing cloc	k sk	○ 1 bit Data by i ○ 1 bit Data by i	ising clo alling cl	ock ock	C 12C	 	

This logic analyzer support 2,8,512 trigger levels. Depend on which model user bought it, Because logic word now is very complex, like RS232, I²C.... need a lot of trigger level to complete it. Every trigger level support " if xx happen xx times then next level else go to 0". AND mode need 32 channels all match trigger condition.

OR mode need one of 32 channels match trigger condition.

Event : allow trigger happen after match trigger condition max 1048576 times.

Delay : wait 1 to 1048576* (1 sec to 10nsec).

You can set the trigger logic to "Enter" (trigger when pattern matches) or "Exit" (trigger when pattern stops matching).

Two trigger check be selected "trigger group" and serial trigger.

Trigger group check : Select which base you want to edit in.

Serial trigger : 7 kind of serial trigger can be selected as following:

Width Bit

Tradition logic analyzer only support 1 trigger level.

Advance logic analyzer can let this trigger word pass n time.

n =1 to 1048576.

In the following example, it will trigger if condition trigger word 55 happen 10 times. like as $77,44,22,55,66,55,66,55,66,55,66,55,44,55,33,55,22,55,22,55,77,55 \leftarrow$ trigger here.

• trigger							
	CH31-24	CH23-	16 CH15	5-8 CH7-0			
	XXXXXX	XXX XXXXXX	XXX XXXXX	XXXX 01010101	Word0 💌		Update
						-	
Level O IF AND 💌	Event 💌	Enter 🗾 👻	Word0 💌	10 then ne	ext level .	•	Group edit
Level 1 IF AND 👻	Event 💌	Enter 💌	• 💌	1 then ne	ext level .		C Trigger group
Level 2 IF AND 👻	Event 💌	Enter 💌	•	1 then ne	ext level .	-	Serial Trigger
Level 3 IF AND 👻	Event 💌	Enter 💌	•	1 then ne	ext level .		
Level 4 IF AND 👻	Event 💌	Enter 💌	•	1 then ne	ext level .	-	
Level 5 IF AND -	Event 💌	Enter 💌	•	1 then ne	ext level .	-	
Level 6 IF AND 👻	Event 💌	Enter 💌	•	1 then ne	ext level .	-	
Level 7 IF AND 👻	Event 💌	Enter 💌	•	1 then ne	ext level .	-	
Trigger edit in s	erial						
Width bit	with timing	C Width bit by	rising clock	C 1 bit Data by risin	g clock 🤇 🤇	° 12C	
< WIGHT DRV	warannig	· · · · · · · · · · · · · · · · · · ·			IG CIOCK		
0 1		0.02		Clear tri			
ľ –	155	8 Bit 💌					
		8Bit 💌		Go to le	vel 0		
<u> </u>]	8Bit 💌		i	i		
		8 Bit 🔽			-		
	I Decimal ↓ Hex						

It also can set delay n time, n =1 to 1048576. time delay unit from 10nsec to 1 sec.

Some time we call this function as **TRIGGER BEFORE DELAY**.

It is useful when we need to look data after reset signal a long period.

In next diagram, it trigger after 10 times trigger word 55 with 10nsec*100 time delay

like as 77,44,22,55,66,55,66,55,66,55,66,55,44,55,33,55,22,55,22,55,77,55 -----1 μ sec delay \leftarrow trigger here.

• trigge	Т							_ 🗆 🗙
		CH31-24	CH23-16	CH15-8	CH7-0			
		******	******	******	01010101	√ord0 🔻		Update
Level 0 IF	AND 💌 Eve	ent 💌 Enter	r 💽 Word	0 🔽 10	then next l	level .	•	Group edit
Level 1 IF	Del	ay 🔻 10ns	•	100	then next l	level		C Trigger group
Level 2 IF	AND 💌 Eve	ent 🗾 Enter		• 1	then next l	level .		Serial Trigger

At this time all LA-2132 model can work well because it only use two trigger levels to complete. LA-2132 has 2,8,512 trigger level model.

It need more than 2 trigger levels to complete next diagram example.

The following model can work for it

LA-2132-K8 (8 Trigger levels), LA-2132-K512 (512 Trigger levels).

LA-2132-M8 (8 Trigger levels), LA-2132-M512 (512 Trigger levels).

LA-2132-G8 (8 Trigger levels), LA-2132-G512 (512 Trigger levels).

A serial of width bit stream like 33 follow 55 follow 77.

it will not trigger if data stream is 33,66,55,77.





The dead time of trigger level to next level is 7 clocks in 32 channels mode. The dead time of trigger level to next level is 14 clocks in 16 channels mode. The dead time of trigger level to next level is 28 clocks in 16 channels mode.

Width Bit With Timing

🖣 trigger				
	CH31-24 CH23	-16 CH15-8	CH7-0	
	XXXXXXXX XXXXX	XXX XXXXXXX	00110011 Word0	•
				-
Level 0 IF AND 👻 Eve	ent 👻 Enter 👻	Word0 👻 1	then next level	· • •
Level 1 IF Del	lay 👻 10ns 👻	26	then next level	
Level 2 IF AND VEVE	ent 👻 Match 👻	Word1 👻 1	then next level	else go to level 0 👻
Level 3 IF Del	lay 👻 10ns 👻	16	then next level	
Level 4 IF AND VEVE	ent 💌 Match 💌	Word2 💌 1	then next level	else go to level 0 💌
Level 5 IF AND VEVE	ent 💌 Enter 💌	1	then next level	· •
Level 6 IF AND VEVE	ent 💌 Enter 💌	1	then next level	
Level 7 IF AND 👻 Eve	ent 💌 Enter 💌	· • 1	then next level	-
Trigger edit in serial				
C Width bit	C Width bit b	yrising clock C 1 t	bit Data by rising clock	C 12C
(RS232=1 bit Width	n bit with timing)		Dic Data by failing clock	
= 💌 1ns	▼ 200			
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		1	Charling 1	
	8 Bit	1	Llear trigger	
55	8 Bit 💌		Go to level 0	<u> </u>
▼ 77	8 Bit 💌			
	8 Bit 👻			-
	Decimal Use			
V I	Hex			

A serial of width bit stream like 33 follow 55 follow 77 by some timing .

It is 200nsec interval in this case.

Trigger commend wait 300nsec after detect trigger word 33 then check it in 200sec every time. 300nsec mean cross trigger word 33 200nsec plus trigger word 55 200nsec/2, equal 300nsec. but system need 7 clock dead time to turn level to level, so it set 260nsec and 160nsec instead. RS232 can be set in this mode, need set to 1 bit width.

The following model can work for it.

LA-2132-K8 (8 Trigger levels), LA-2132-K512 (512 Trigger levels). LA-2132-M8 (8 Trigger levels), LA-2132-M512 (512 Trigger levels). LA-2132-G8 (8 Trigger levels), LA-2132-G512 (512 Trigger levels).



in this mode, also can detect width pulse in narrow stream.

It has width pulse 55 55 55 55 in the following stream.

like as 55 aa 55 aa 55 55 55 55 aa 55 aa 55 aa 55.....

LH31-24 LH23-16 LH15-8 LH7-0 EXXXXXXXX XXXXX XXXXXX 01010101 Word • Level 0 IF AND • Event • Enter • Word0 • 1 then next level • Level 2 IF AND • Event • Match • Word0 • 1 then next level else go to level 0 Level 3 IF AND • Event • Enter • • • 1 then next level • Level 4 IF AND • Event • Enter • • • 1 then next level • Level 5 IF AND • Event • Enter • • • 1 then next level • Level 6 IF AND • Event • Enter • • • 1 then next level • Level 7 IF AND • Event • Enter • • • 1 then next level • Trigger edit in serial	🖣 trigg	er				01.01		100	10	CLIM		0112.0	
avel 0 IF AND Event Enter Word0 1 then next level . avel 1 IF Delay 10ns 27 then next level . avel 2 IF AND Event Match Word0 1 then next level . avel 3 IF AND Event Enter . 1 then next level . avel 4 IF AND Event Enter . 1 then next level . avel 5 IF AND Event Enter . 1 then next level . avel 6 IF AND Event Enter . 1 then next level . avel 7 IF AND Event Enter . 1 then next level . avel 7 IF AND Event Enter . 1 then next level . avel 7 IF AND Event Enter . 1 then next level . . avel 7					LH	31-24		H23-	-16 	CHIS)-8	CH7-0	
vvel 0 IF AND Event Enter Word0 1 then next level . vvel 1 IF Delay 10ns 27 then next level else go to level 0 vvel 2 IF AND Event Match Word0 1 then next level else go to level 0 vvel 3 IF AND Event Enter . 1 then next level . vvel 4 IF AND Event Enter . 1 then next level . vvel 5 IF AND Event Enter . 1 then next level . vvel 6 IF AND Event Enter . 1 then next level . vvel 7 IF AND Event Enter . 1 then next level . vvel 7 IF AND Event Enter . 1 then next level . vvel 7 IF AND Event Enter . 1 then next level . .					Xexe	(XX)		exexe	Xexex DXe	XXXX	OXOXOX		ord0 🗾
evel 0 IF AND Event Enter Word0 1 then next level . evel 1 IF Delay 10ns 27 then next level else go to level 0 evel 2 IF AND Event Match Word0 1 then next level else go to level 0 evel 3 IF AND Event Enter . 1 then next level . evel 4 IF AND Event Enter . 1 then next level . evel 5 IF AND Event Enter . 1 then next level . evel 6 IF AND Event Enter . 1 then next level . evel 6 IF AND Event Enter . 1 then next level . evel 6 IF AND Event Enter . 1 then next level . evel 7 IF AND Event Enter . 1 then next level . .													
evel 1 IF Delay 10ns 27 then next level evel 2 IF AND Event Match Word0 1 then next level evel 3 IF AND Event Enter 1 then next level evel 4 IF AND Event Enter 1 then next level evel 5 IF AND Event Enter 1 then next level evel 6 IF AND Event Enter 1 then next level evel 7 IF AND Event Enter 1 then next level rigger edit in serial Width bit by rising clock 1 bit Data by rising clock 12C Width bit Width bit by falling clock 1 bit Data by falling clock 12C Width bit with timing Width bit by falling clock 1 bit Data by falling clock 12C Width bit with timing Width bit by falling clock 1 bit Data by falling clock 12C Width bit with timing Width bit with timing Go to level 0 I	evel 0	IF	AND	•	Event	•	Enter	•	Word0	•	1	then next lev	vel .
avel 2 IF AND Event Match Word0 1 then next level else go to level 0 avel 3 IF AND Event Enter - 1 then next level - avel 4 IF AND Event Enter - 1 then next level - avel 5 IF AND Event Enter - 1 then next level - avel 6 IF AND Event Enter - 1 then next level - avel 6 IF AND Event Enter - 1 then next level - avel 6 IF AND Event Enter - 1 then next level - avel 7 IF AND Event Enter - 1 then next level - avel 7 IF AND Event Enter - 1 then next level - avel 7 IF AND Event Enter - 1 then next level -	vel 1	IF		_	Delay	-	10ns 👻			_	27	then next lev	/el
avel 3 IF AND Event Enter • 1 then next level . avel 4 IF AND Event Enter • 1 then next level . avel 5 IF AND Event Enter • 1 then next level . avel 6 IF AND Event Enter • 1 then next level . avel 6 IF AND Event Enter • 1 then next level . avel 6 IF AND Event Enter • 1 then next level . avel 7 IF AND Event Enter • 1 then next level . avel 7 IF AND Event Enter • 1 then next level . avel 7 IF AND Event Enter • 1 then next level . Vidth bit © Width bit by rising clock 1 1 then next level . •	evel 2	IF	AND	•	Event	-	Match	-	Word0	-	1	then next lev	vel else go to level 0
avel 4 IF AND Event Enter I then next level avel 5 IF AND Event Enter I then next level avel 6 IF AND Event Enter I then next level avel 7 IF AND Event Enter I then next level avel 7 IF AND Event Enter I then next level avel 7 IF AND Event Enter I then next level avel 7 IF AND Event Enter I I avel 8 If I I I I avel 9 If If If If I avel 9 <t< td=""><td>evel 3</td><td>IF</td><td>AND</td><td>•</td><td>Event</td><td>-</td><td>Enter</td><td>•</td><td></td><td>-</td><td>1</td><td>then next lev</td><td>vel .</td></t<>	evel 3	IF	AND	•	Event	-	Enter	•		-	1	then next lev	vel .
evel 5 IF AND Event Enter I then next level evel 6 IF AND Event Enter I then next level evel 7 IF AND Event Enter I then next level Trigger edit in serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Width bit Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the serial Image: Strategy of the series Image: Strategy of the serial Image: Strategy of the series Image: Strategy of the series Image: Strategy of the series Image: Strategy of the series Image: Strategy of the series Image: Strategy of the series Image: Strategy of the series Image: Strategy of the series </td <td>evel 4</td> <td>IF</td> <td>AND</td> <td>•</td> <td>Event</td> <td>-</td> <td>Enter</td> <td>•</td> <td></td> <td>-</td> <td>1</td> <td>then next lev</td> <td>vel .</td>	evel 4	IF	AND	•	Event	-	Enter	•		-	1	then next lev	vel .
evel 6 IF AND Event Enter · 1 then next level . evel 7 IF AND Event Enter · 1 then next level . Trigger edit in serial Width bit C Width bit by rising clock C 1 bit Data by rising clock C 12C Width bit with timing Width bit by falling clock C 1 bit Data by falling clock C 12C Width bit with timing) Ins 300 Ch0 as data Ch1 as clock Clear trigger B Bit B Bit B Bit Control to level 0	evel 5	IF	AND	•	Event	-	Enter	-		-	1	then next lev	/el .
ivel 7 IF AND Event Enter 1 then next level Trigger edit in serial Width bit Width bit by rising clock 1 bit Data by rising clock 12C Width bit with timing Width bit by falling clock 1 bit Data by falling clock 12C Width bit with timing Width bit by falling clock 1 bit Data by falling clock 12C Width bit with timing Width bit by falling clock 1 bit Data by falling clock 12C Width bit with timing Width bit with timing) Cho as data ch1 as clock Clear trigger Ch0 as data Bit Go to level 0 Go to level 0	evel 6	IF	AND	•	Event	-	Enter	-		-	1	then next lev	/el .
Trigger edit in serial C Width bit by rising clock C 1 bit Data by rising clock C 12C Width bit with timing C Width bit by falling clock C 1 bit Data by rising clock C 12C Width bit with timing C Width bit by falling clock C 1 bit Data by falling clock C 12C Ins 300 Ch0 as data , Ch1 as clock Clear trigger Go to level 0 8 Bit 8 Bit Go to level 0 Image: State of the set of	evel 7	IF	AND	•	Event	-	Enter	-		-	1	then next lev	/el .
8 Bit		Trigg (R:) 0	ger edit i Width I Width I \$232=1	n se pit pit w bit V 1n	rial ith timing /idth bit wi s _ Ch0 as c 55	th tim Jata ,	C Width (Width (00) Ch1 as clock (8 Bit (8 Bit (8 Bit (8 Bit) (8 Bit)	bit b bit b	y rising clo y falling clo	ck ock	C 1 C 1	bit Data by rising clo bit Data by falling clo Clear trigger Go to level 0	ck C I2C

The same is true for detecting narrow pulse in width stream when set < nn time.

All LA-2132 can work for it because it need two trigger level only.

But need adjust properly time delay.

Width Bit By Rising (Falling) Clock

A serial of width bit stream synchronous with clock. channel 31 default as clock. channel 0-30 as data.

Data flow 77,00,55 synchronous with ch31 clock rising edge as following diagram.

Word 3 set to 1xxxxxxxxx.....

It detect data 77 after ch31 clock rising edge else go to trigger level 0 to judge continuously. it also can select LSB out first or MSB out first

for example a stream 001111, LSB out first mean data flow is 111100.

MSB out first mean data flow is 001111.





The same is true for falling clock. The following model can work for it LA-2132-K8 (8 Trigger levels), LA-2132-K512 (512 Trigger levels). LA-2132-M8 (8 Trigger levels), LA-2132-M512 (512 Trigger levels). LA-2132-G8 (8 Trigger levels), LA-2132-G512 (512 Trigger levels).

1 Bit Data By Rising Clock

A serial of bit stream synchronous with clock.

Channel 0 default as data, channel 1 default as clock.

It is same as "width bit by rising clock".

but it detect one bit only when clock is rising.

to avoid unnecessary start bit. leve0-2 let clock can work at first bit.

trigge	ег							
		CH3	31-24 C	H23-16	CH15-8	CH7-0		
		XXX	XXXXX XX	XXXXXX	XXXXXXX	XXXXXXX1 Word0	•	
vel 0 IF	AND -	Event	▼ No Match	▼ Word1	• 1	then next level	else go to level 0	
vel 1 IF		Delay	▼ 10ns ▼	1	10	then next level		
vel 2 IF	AND -	Event	▼ No Match	Word1	• 1	then next level	else go to level 0	•
vel 3 IF	AND -	Event	✓ Enter	▼ Word1	- 1	then next level	-	
vel 4 IF	AND -	Event	▼ Match	▼ Word0	• 1	then next level	else go to level 0	•
vel 5 IF	AND -	Event	✓ Enter	▼ Word1	▼ 1	then next level	-	•
vel 6 IF	AND -	Event	✓ Match	▼ Word0	• 1	then next level	else go to level 0	•
vel 7 IF	AND -	Event	✓ Enter	▼ Word1	▼ 1	then next level	-	-
_ Trigg	geredit in s	erial					-	
0	Width bit		C Width	bit by rising cl	ock 💽 1 b	it Data by rising clock	C 12C	
C	Width bit (with timing	(Width	bit by falling c		it Data by falling clock		
		Ch0 As D	ata, Ch1 As clo	ck				
0	<u> </u>	33	8 Bit	-		Clear trigger		
			8 Bit	•		Ga ta laval 0		
			8 Bit	•		Gotolevero	7	
			8 Bit	•				
			al 🔽 LS	B sensor first			_	
		🔽 Hex	E MS	6B sensor first				

The same is true for falling clock. The following model can work for it LA-2132-K512 (512 Trigger levels). LA-2132-M512 (512 Trigger levels). LA-2132-G512 (512 Trigger levels).

l²C

It is same as "one bit by rising clock"

a serial of bit stream synchronous with clock. channel 0 default as data,

channel 1 default as clock in I²C format.

Level 0 -1 is I²C start format.

• tri	gge	er									
			СН	31-24	CH23-16	CH1	5-8	CH7-0			
			XXX	XXXXX	XXXXXXXX	X XXXX	XXXX	XXXXXX11 Word	0 💌		
Level 0	IF	AND	✓ Event	👻 Exit	- W	ord0 🖉 👻	1	then next level		•	•
_evel 1	IF	AND	✓ Event	▼ Match	- W	ord1 👻	1	then next level	else go to level 0		_
evel 2	IF	AND	✓ Event	✓ Enter	- W	ord3 👻	1	then next level		-	
Level 3	IF	AND	▼ Event	▼ Match	- W	ord2 🔻	1	then next level	else go to level 0	ĒĿ	•
Level 4	IF	AND	▼ Event	- Enter	- W	'ord3 👻	1	then next level		-	
Level 5	IF	AND	▼ Event	▼ Match	• W	ord2 🔻	1	then next level	else go to level 0	-	
Level 6	IF	AND	▼ Event	- Enter	• W	ord3 🗸	1	then next level	i j.	Ŧ	
evel 7	IF	AND	✓ Event	- Match	- W	ord2 👻	1	then next level	else go to level 0	Ţ	
Г	Trigg	ger edit in	n serial								
	0	Width b	it is union stanting	e w	idth bit by ris	ing clock	21	I bit Data by rising clock	○ 12C		
		width b	it with timing	v w	idth bit by fa	lling clock		i bit Data by failing cloci	< .		
			Ch0 As [)ata, Ch1 As	clock						
	4		55	7 Bit	• M	ISB 8 bit D	ata	Clear trigger]		
		2022	0	2 Bit	• 1	bit ack		Ge te level 0			
		-	f0	8 Bit	- L	SB 8 bit Da	ta				
		1000	0	1 Bit	• 1	bit ack					
			☐ Decim I Hex	al					_		

I²C need 73 trigger levels to complete trigger. That is why LA-2132 need design 512 trigger levels. The following model can work for it LA-2132-K512 (512 Trigger levels). LA-2132-M512 (512 Trigger levels). LA-2132-G512 (512 Trigger levels).

Threshold Voltage Setup

it can set threshold voltage at toolbar or parameter form. The range of threshold voltage is from -3.7V to 1.9V in 35mV step. In general, 5V TTL need set 1.4V. ECL (-1.3V) LVC1.5V (0.75V) LVC1.8V (0.9V) LVC2.5V (1.2V) LVC3.3V (1.4V) SSTL2|| 2.5V (1.25V) SSTL3|| 3.3V (1.4V) Adjust threshold voltage can remove unnecessary signal like noise sometime. LA-2164 support two sets threshold voltage.

Clock Menu

Select an internal clock rate or an external clock for sampling. It can set clock rate at toolbar or parameter form. 1 GHz (1 ns) when select 8 channel mode only. 500 MHz (2 ns) when select 8 channel or 16 channel mode only. 250 MHz (4 ns) below 250mhz can be used for all clock mode. 100 MHz (10 ns) 50 MHz (20 ns) 20 MHz (50 ns) 10 MHz (100 us) 5 MHz (200 us) 2 MHz (500 us) 1 MHz (1 us) 500 KHz (2 us) 200 KHz (2 us) 200 KHz (5 us) 100 KHz (10 us)

50 KHz (20 us) 20 KHz (50 us) 10 KHz (100 us) 5 KHz (200 us) 2 KHz (500 us) 1 KHz (1 ms) 500 Hz (2 ms) 200 Hz (5 ms) 100 Hz (10 ms) 50 Hz (20 ms) 20 Hz (50 ms) 10 Hz (100 ms) 5 Hz (200 ms) 2 Hz (500 ms) 1 Hz (1 s) LA-2164 can support all kind of clock rate as above except only support 1 GHz and 400 MHz At 16 channels mode.

External Clock

4 kind of external clock can be selected.

Channel 31 external clock rising.

Channel 31 external clock falling .

Channel 31 both of external clock rising and falling. it let external clock frequency double. LVDS0 is external clock in LVDS signal.

The software only transfers data to the PC when the buffer is full. If you are using a slow clock it might take a long time to fill the buffer. Recording time/Acquisition time/Capture time/Buffer Length.

The Logic analyzer will acquire data for time equal to Buffer length * clock rate.

Example:

If buffer length = 512K and sample rate = 100KHz. The LA will record for (512K * 10 us)

Magnify (Timing)

Select a zoom ratio for the timing window. You can display the timing data in a compressed or expanded format. Zooming in lets you see great detail. Zooming out lets you see large abundant of data. Zoom can be changed in the following ways:

- 1. A clicking on the combo brings up a magnify factor list.
- 2. Select what you want.

Zoom Combo



In the timing window you can do the following:

Zoom

Zoom in or out by selecting	zoom factor combo
Window to cursor A :	Zoom around cursor A
Window to cursor B :	Zoom around cursor B
Window to cursor T :	Zoom around cursor T (trigger cursor)
cursor A to Window :	shift cursor A to window
cursor B to Window :	shift cursor B to window
cursor T to Window :	shift cursor T to window
cursor A, B, T to Window :	shift cursor A, B, T to window

Timing Window

This window shows the data in a timing waveform style display. The channel names will be on the left edge with the data going horizontally. To the right of the channel names are the values of data at each cursor (it is color coded to match the cursors). The vertical scrollbar moves the window up and down to display more channels. The horizontal scrollbar moves the data forward and backward in time.

The channel order can be changed by the color form. The size of the window can be changed by grabbing an edge of the window and dragging it.

When the Timing window is selected (title says "active window") Left and right arrows scroll data with respect to time, or grabbing timing to shift data. Up and down arrows scroll data with respect to channels.

Window to cursor A :	Zoom around cursor A
Window to cursor B :	Zoom around cursor B
Window to cursor T :	Zoom around cursor T (trigger cursor)
cursor A to Window :	shift cursor A to window
cursor B to Window :	shift cursor B to window
cursor T to Window :	shift cursor T to window
cursor A, B, T to Window :	shift cursor A, B, T to window

Note:

This only works on the selected window. Click on the window to select it.

Cursor using

Cursors are used to mark points of interest in the data, to measure time between events and to define pre/post trigger position.



Moving a cursor:

- 1. In the timing you can select a cursor by using the arrow buttons in the timing move it.
- 2. You can also "grab" the cursor by left clicking on it in the timing and then move it by "dragging" it to a new location.
- 3. The timing cursor A, B, T have selections that allow you to bring the cursors onto their views.

Setting Up Group

set following after select group edit.

CER L.	A-2132	-G512 (1	GHz,	4 Mega	Memo	ory,5	12 le	vels)
Eile	View	Timing	<u>R</u> eset	Tr <u>igg</u> er	<u>W</u> in	dow	Help	e.
<u>60</u>	Cole	ors				Co	unt	01
CR 1	Para	ameters wi	ndow		ta= (Oms		
Curso Curso	✓ Too Stat	l <u>b</u> ar us Bar			ursor	T. zoc	m	• •
Triqq	Sam	nples or tim	ne	•		1		
Hex3	Sear	rch D63-D	0 data					
Dec3	Gro	up edit						
ASCI Bine	Cha Stat	nnel/State e of logic	/Timing analyzei	setup				

- 1. Select which group to display. Groups can be in different bases.
- 2. Set Base.
- 3. Set channel combination.

🖿 Gro	oup Setup			
Group	Name	Base	Number	
Group	0 Hex31-0	HEX 💌	32 •	
	Channel combi	nation		
Bit 0	Chan D 0 💌	Bit 8 Chan D 8	➡ Bit 16 Chan D 16 Bit 24 Chan D 24	1
Bit 1	Chan D 1 💌	Bit 9 Chan D 9	➡ Bit 17 Chan D 17 Bit 25 Chan D 25	OK
Bit 2	Chan D 2 💌	Bit 10 Chan D 10	Bit 18 Chan D 18 Bit 26 Chan D 26	Refresh
Bit 3	Chan D 3 💌	Bit 11 Chan D 11	➡ Bit 19 Chan D 19 Bit 27 Chan D 27	screen
Bit 4	Chan D 4 💌	Bit 12 Chan D 12	▼ Bit 20 Chan D 20 ▼ Bit 28 Chan D 28 ▼	
Bit 5	Chan D 5 💌	Bit 13 Chan D 13	▼ Bit 21 Chan D 21 ▼ Bit 29 Chan D 29 ▼	
Bit 6	Chan D 6 💌	Bit 14 Chan D 14	Bit 22 Chan D 22 Bit 30 Chan D 30	
Bit 7	Chan D 7 💌	Bit 15 Chan D 15	▼ Bit 23 Chan D 23 ▼ Bit 31 Chan D 31 ▼	
	Position	bit23	bit0 Mnemonic	
USEF		XXXXXXXXX	XXXXXXXX XXXXXXX /read	

atoup		Nar	ne		Ba	ase		- 1	lumb	er					
itoup	0	He	xde	cimal	H	ΕX		•	24	100		+			
	Cha	nnel	con	nbina	tion										
lit O	B1	Ch	0	•	Bit 8	B1	Ch	8	•	Bit 16	B1	Ch	16	•	
it 1	B1	Ch	1	•	Bit 9	Bl	Ch	9	•	Bit 17	B1	Ch	17	•	í
lit 2	B1	Ch	2	•	Bit 10	Bl	Ch	10	•	Bit 18	Bl	Ch	18	•	OK
lit 3	B1	Ch	з	•	Bit 11	B1	Ch	11	•	Bit 19	Bl	Ch	19	•	
lit 4	B1	Ch	4	•	Bit 12	B1	Ch	12	•	Bit 20	Bl	Ch	20	•	Refresh
lit 5	Bl	Ch	5	•	Bit 13	Bl	Ch	13	•	Bit 21	B1	Ch	21	•	Screen
lit 6	Bl	Ch	6	•	Bit 14	B1	Ch	14	•	Bit 22	B1	Ch	22	•	
lit 7	B1	Ch	7	•	Bit 15	B1	Ch	15	•	Bit 23	Bl	Ch	23	•	
	8	Cor	nditio	m	ы	23								bitO	Mnemonic
JSE	R0 -	-	0	-	XXX	XXX	XX	x	XXX	XXXX	x	XXX	XXX	0	/READ

Setting Up The State/Timing Window

(IK L.	A-2132	-G512 (GHz,	4 Mega	Memo	r y, 512 le	vels)
Eile	View	Timing	Reset	Trigger	Wind	ow <u>H</u> ely	>
ĢQ	<u>C</u> ole	ors				Count	01.
	🕽 🤉 Parameters window				ta= 0	ms	
Curso	🖌 Too	l <u>b</u> ar			ursorT	. zoom	-
Curso	<u>S</u> tatus Bar			lagnify	/1	•	
Trigg	Samples or time						
Hex3	Search D63-D0 data						
Dec3	Group edit						
ASCI	Cha	nnel/State	/Timing	setup			
Bins	Stat	e of logic	analyzer				

🖷 Channel / State / Timing Edit 👘			. D ×
Channel Edit B*	Ch0 B1Ch0	Group Edit	fresh 1
- Timing View 1			reen
⊥ State 0			
Timing Track 0	B1 Ch 0 💽 B1 Ch 0	Turn On 💌 Height 16 💌	

Setting up the state/timing display.

- 1. Set group.
- 2. Select which group to display. Groups can be in different bases.
- 3. Select display channel on or off. Timing display also can define timing height.

Setting Channel Names And Colors

Channel names can edit at timing window directly. Channel names should be edited at color form. Color form also can set all cursor color.



Search By Cursor

Select one of cursor A, B, T and specific word.

or edit search word directly.

It will search all memory and channel after Push forward or backward.

D31D0	- Search data
• XXXXXXXXXXXXXXXXXXXXXXXX11111111	Search by 📀 Cursor A
C XXXXXXXXXXXXXXX11111111XXXXXXXX	C Cursor B
C XXXXXXXXXXXXXXXXXXXXXX0000000	C Trigger cursor
C XXXXXXXXXXXXXX0000000XXXXXXXX	D31D0
C Cursor A data	=> XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
C Cursor B data	
🗅 Trigger bar data	Backward Forward

Search By Group

The same is true for search by group after selecting search group check item. It use group definition to quickly edit search word.

Search data		
Search edit by group Hex 31-24 • Hex 23-16 • Hex 15-8 Decimal • Hex	Image: Search data Image: Search data Search by Image: Search data Search by Image: Search data Image: Search data<	XXXXXXXXXXXXX Search group Group edit

Export (File Menu)

Use this to output data to other programs.

🖣 Data Outp	ut Option			
 ✓ D7-D0 ✓ Decimal ✓ HexDecimal ✓ Ascii 	 ✓ D15-D8 ✓ Decimal ✓ HexDecimal ✓ Ascii 	D23-D16 Decimal HexDecimal Ascii	D31-D24 Decimal HexDecimal Ascii	
From 0 to		.bort OK		

How to use:

- 1) Data: Select which data to output: Individual group or all channels Select base to output data in.
- 2) Start and End: Select data address range.
- 3) Click OK to save data.

File Menu Commands

Eile	⊻iew	Timing	Reset	Trigg	
Lo	oad Data		Ctrl	+L	
Lo	oad data	option		•	
Sa	ve Data			۲	
Tr	ansfer d	ata to <u>E</u> xc	el		
Sa	Save Data(text format)				
Lo	ad <u>S</u> etti	ng			
Lo	oad <u>D</u> ef	ault Settin	g		
Sa	ve Set <u>t</u> i:	ng As			
A	ito Save	Setting			
Print				•	
Pr	int Setu	p			
E2	cit				

The File menu offers the following commands: Load : Opens an existing file (data or settings). Save : Save a file to a specified file name. Save settings or data files. Save data after capture: it save to hard disk from 10-1000 times. if you need records mass data. but you need check your hard disk free capacity.

Eile	<u>V</u> iew <u>T</u> im	ing <u>R</u> ese	t Tr <u>igg</u> en	: <u>W</u> indow	Help				
Lo. Lo:	ad Data ad data opti	C	trl+L ⊧	nt -03.72V		8k 🛨	250Mhz 🛨	x0000000X	xxxxxxxxx x
Sat	re Data	511	•	<mark>st_data= (</mark> Save Data)ms a As				
Transfer data to Excel Save Data(text format)		•	Save Data after capture			10 times(savedata(0-9).dso) 100 times(savedata(0-99).dso) 1000 times(savedata(0.990).dso)			
						1(JUU times(sa	avedata(0-9	99).dso)

Export: Export data to excell programs format, or text format.

Auto save setting: If checked settings will be saved when you exit the program.

then loaded when you load the program.

Print: Prints data in Timing format.

Print Setup: Selects a print mode, printer and printer connection.

Exit: Exit.

The following is source code of LA-2132 save and load data visual c program.

Sometime user want to analyze data by themselves. it is useful for user to understand how program write and read data.

Every binary code describe 1 channel. For example 00110001 data mean channel 0 is high, channel 1 is low...etc at first record.

_declspec (dllexport)void _stdcall vc_savedata (uchar *buflogic0, int length, LPSTR sfile,uchar *model,unsigned char *LAPorts8)

```
{
int result,ii,II;
FILE *fp;
fp = fopen ( sfile, "w+b" );
if (model[0]== clk2132_1m){
II=1025;
}
if (model[0]== clk2132){
II=513;
}
if (model[0]== clk2132_256K){
II=257;
```

```
}
if (LAPorts8[channelmode]==0){
for(ii=0;ii<3;ii++) {
result = fwrite ( &buflogic0[1024*ll*ii], length, 1, fp );
}
}
if (LAPorts8[channelmode]==1){
for (ii=0;ii<1;ii++) {
result = fwrite ( &buflogic0[1024*II*ii*2], length, 1, fp );
}
}
if (LAPorts8[channelmode]==2){
result = fwrite ( &buflogic0[0], length, 1, fp );
}
fclose (fp);
}
_declspec (dllexport) void _stdcall vc_loaddata (uchar *buflogic0, int length ,LPSTR sfile,int position)
{
int result;
FILE *fp;
fp = fopen ( sfile, "r+b" );
result = fseek (fp, length*position,0);
result = fread ( &buflogic0[0], length, 1, fp );
fclose (fp);
}
```

Hardware Specifications

There are two Models is available for LA-2132 LVDS:

LA-2132 LVDS: (32 channels only, can't expand to 64 channels).

- K2 (250MHz, 256K Memory, 2 Trigger Levels, support LVDS).
- G512 (1GHz, 4Mega Memory, 512 Trigger Levels, support LVDS).

There are nine Models is available for LA-2132 Series:

LA-2132K Series: (Expand to 64 channels is available, without support LVDS).

- K2 (250MHz, 256K Memory, 2 Trigger Levels).
- K8 (250MHz, 256K Memory, 8 Trigger Levels).
- K512 (250MHz, 256K Memory, 512 Trigger Levels).
- LA-2132G Series: (Expand to 64 channels is available, without support LVDS).
- ☐ M2 (500MHz, 1Mega Memory, 2 Trigger Levels).
- M8 (500MHz, 1Mega Memory, 8 Trigger Levels).
- ☐ M512 (500MHz, 1Mega Memory, 512 Trigger Levels).

LA-2132G Series: (Expand to 64 channels is available, without support LVDS).

- G2 (1GHz, 4Mega Memory, 2 Trigger Levels).
- G8 (1GHz, 4Mega Memory, 8 Trigger Levels).
- G512 (1GHz, 4Mega Memory, 512 Trigger Levels).

Expand to 64 Channels Is Available

When use 20 pin flat cable connect two LA-2132 Series, it can expand to 64 channels. Please see page 6 (Expand to 64 channels) diagram.

LA-2132 LVDS Series Hardware Specifications

Model	LA-2132 LVDS (K2)	LA-2132 LVDS (G512)			
	250MHz, 256K Memory	1GHz, 4Mb Memory			
	32 channels from 1Sa/s to	32 channels from 1Sa/s to 250MSa/s			
	250MSa/s 256 K memory	1 Mega memory			
Internal Sampling		16 channels from 1Sa/s to 500MSa/s			
Rate		2 Mega memory			
Number of Channel		8 channels from 1Sa/s to			
Record Length	2 channels hi direction LVDS	2 channels bi direction LVDS			
	2 channels input IVDS	2 channels input LVDS			
	Expand to 64 Channels is not available	Expand to 64 Channels is not available			
External Clock Pate	Lin to 125 MSa/s DC	to 200 MHz for LVDS			
L/O Bandwidth	$CH 0 \sim 31 DC to 125 M$	Hz DC to 200 MHz for LVDS			
Input Impedance	200 KO // 2r	of (Tip to around)			
	Max _110 V to +	-110 V for CH 0 ~ 31			
Input Voltage	0 to 5V only for a	all LVDS signals			
input voltage	(it will burn out if input vo	bltage is exceed this range)			
	-2V to 1.9V	by 25mV step			
	ECL (-1.3V)	5			
	LVC1.5V (Ó	.75V)			
Threshold Voltage	LVC1.8V (0	.9V)			
Theshold voltage	LVC2.5V (1.2V)				
	LVC3.3V (1	.4V)			
	SSTL2 2.5	5V (1.25V)			
	SSTL3 II 3.3V (1.4V)				
Channel Skew	Iypica	ii < 200 ps			
I rigger position	Any position	tor user defined			
Max. Trigger Speed		HZ (4NS)			
Trigger Quality	U, 1, X (don't care) settings for all Dig	Ital channels, 2, 8, 512 Trigger Levels			
Dower Cumply	No External Do	war Course Deguire			
Power Suppry	NO EXternal PO	Cromo			
Net Weight Size (Dimonsion)	120 107mm x 7	Gidilis Zmm v 16mm			
	Harness Color Wires 32 Pin x 2 pos	LISB 2 0 Two Head Cable			
A	Harness Color Wires 32 Pin x 2 pcs. USB 2.0 Two Head Cable.				

LA-2132 Series Hardware Specifications

Model	LA-2132 K Series	LA-2132 M Series	LA-2132 G Series			
MOUEI	250MHz, 256K Memory	500MHz, 1Mb Memory	1GHz, 4Mb Memory			
	32 channels from 1Sa/s	32 channels from 1Sa/s	32 channels from 1Sa/s			
	to 250MSa/s 256 K	to 250MSa/s 512 K	to 250MSa/s 1 Mega			
	memory	memory	memory			
Internal Sampling		16 channels from 1Sa/s	16 channels from 1Sa/s			
Dete		to 500MSa/s 1 Mega	to 500MSa/s 2 Mega			
Rale		memory	memory			
Number of Channel			8 channels from 1Sa/s to			
Record Length			1 GSa/s 4 Mega memory			
l teeera _erigtii	Not support LVDS	Not support LVDS	Not support LVDS			
	Two LA-2132 connect by a	Two LA-2132 connect by a	Two LA-2132 connect by a			
	20Pin flat cable, it can be	20Pin flat cable, it can be	20Pin flat cable, it can be			
External Clask Data	expand to 64 channels.	expand to 64 channels.	expand to 64 channels.			
UO Randwidth			7			
Input Impedance 200 Kohm // 2nf (Tin to ground)						
Input Voltage	Zo Max	-110 V to +110 V for CI	1 0-31			
	Max					
		-2V to 1.9V by 25mV step				
	ECL (-1.3V)					
	LVC1.5V (0.75V)					
Threshold Voltage	LVC1.8V (0.9V)					
Theorem Voltage	LVC2.5V (1.2V)					
	LVC3.3V (1.4V)					
	SSTL2 II 2.3V (1.25V) SSTL3 II 3 3V/ (1.4V/)					
Channel Skew		10012011000000000000000000000000000000				
Trigger position	Ar	v position for user defined	ł			
Max Trigger Speed	250 MHz (Ang)					
Trigger Quality	0, 1, x (don't care) setting	is for all Digital channels.	2. 8. 512 Trigger Levels			
			_, c, c : ggo: _ c : c : c			
Power Supply	No	External Power Source R	equire			
Net Weight		120 Grams	-			
Size (Dimension)		107mm x 77mm x 16mm	1			
	Harness Color Wires 32 Pin x 2 pcs. USB 2.0 Two Head Cable.					
Accessories	Harness Color Wires 32 I	Pin x 2 pcs. USB 2.0 Two	Head Cable.			

LA-2164 Series Hardware Specifications

Model	LA-2164 K Series 250MHz, 256KMemory	LA-2164 M Series 500MHz, 1Mb Memory	LA-2164 G Series 1GHz, 4Mb Memory		
Internal Sampling	64 channels from 1Sa/s to 250MSa/s 256 K memory	64 channels from 1Sa/s to 250MSa/s 512 K memory	64 channels from 1Sa/s to 250MSa/s 1 Mega memory		
Rate Number of Channels Record		32 channels from 1Sa/s to 500MSa/s 1 Mega memory	32 channels from 1Sa/s to 500MSa/s 2 Mega memory		
Length			16 channels from 1Sa/s to 1 GSa/s 4 Mega memory		
	Not Support LVDS	Not Support LVDS	Not Support LVDS		
External Clock Rate		Up to 125MSa/s			
I/O Bandwidth	CH 0 ~ 63 DC to 125MHz				
Input Impedance 250Konm // 2pt (Tip to ground)					
input voltage	Iviax.		10~63		
Threshold Voltage	-2V to 1.9V by 35mV step ECL (-1.3V) LVC1.5V (0.75V) LVC1.8V (0.9V) LVC2.5V (1.2V) LVC3.3V (1.4V) SSTL2 II 2.5V (1.25V) SSTL3 II 3.3V (1.4V)				
Channel Skew		I ypical < 200ps			
Max Trigger Speed	A		eu		
Trigger Quality	0 1 x (dop't care) settin	as for all Digital channels	2 8 512 Trigger Levels		
Thyger Quality					
Power Supply	No E	External Power Source Re	quire		
Net Weight		120 Grams			
Size (Dimension)		107mm x 77mm x 16m	n		
Accessories	Harness Color Wires 32 Easy Hook 100 pcs, Soft	Pin x 4 pcs. USB 2.0 Two ware CD, User's Manual,	Head Cable. 20 Pin Flat Cable 1 pcs.		

Window USB Driver Install

Windows 98/ME USB driver install

When USB2.0 control interface be connected to computer, screen will display



Click Next to continue



Edit or browse path to ...\USB20driver\win98_ME\gene.inf (here D: is CD location, dso25216A may be dso29xx or la5000b or la2124a)



Click Next to continue



Completing install

Windows 2000 USB driver install

When USB2.0 control interface be connected to computer, screen will display

Found New Hardware Wizard	
	Welcome to the Found New Hardware Wizard This wizard helps you install a device driver for a hardware device.
HI HINA PROPERTY	To continue, click Next.
	KBack Next > Cancel

Found New Hardware Wizard	
Install Hardware Device Drivers A device driver is a software program that an operating system.	enables a hardware device to work with
This wizard will complete the installation for	or this device:
USB2.0 Device	
A device driver is a software program that needs driver files for your new device. To installation click Next.	makes a hardware device work. Windows locate driver files and complete the
What do you want the wizard to do?	
Search for a suitable driver for my	device (recommended)
 Display a list of the known drivers I driver 	ior this device so that I can choose a specific
	< Back Next > Cancel

Click Next to continue

Locate [Priver Files		50
When	a do you want Windows to searc	h for driver files?	
Searc	h for driver files for the following	hardware device:	
- P	USB2.0 Device		
The v any o	izard searches for suitable driver the following optional search lor	s in its driver database on y ations that you specify.	vour computer and in
To sta insert	irt the search, click Next. If you a the floppy disk or CD before click	are searching on a floppy di king Next.	sk or CD-ROM drive,
Optic	nal search locations:		
Г	Floppy disk drives		
Г	CD-ROM drives		
1	Specify a location		
Г	Microsoft Windows Update		



Edit or browse path to ...\USB20driver\win2000_XP\gene.inf (here F: is CD location, dso25216A may be dso29xx or la5000b or la2124a) Press OK





Click Yes to continue

Found New Hardware Wizard	
	Completing the Found New Hardware Wizard Usb2.0 Controller 5 Windows has finished installing the software for this device.
	To close this wizard, click Finish.
	K Back Finish Cancel

Completing install

Windows XP USB driver install

When USB2.0 control interface be connected to computer, screen will display

Found New Hardware Wizard	
	Welcome to the Found New Hardware Wizard
	This wizard helps you install software for:
	USB2.0 Device If your hardware came with an installation CD or floppy disk, insert it now.
	What do you want the wizard to do?
	 Install the software automatically (Recommended) Install from a list or specific location (Advanced)
	Click Next to continue.
	< Back Next > Cancel

Click Next to continue

lease cho	ose your search and installation options.
💿 Sean	ch for the best driver in these locations.
Use t paths	he check boxes below to limit or expand the default search, which includes local and removable media. The best driver found will be installed.
	Search removable media (floppy, CD-ROM)
	Include this location in the search:
	E:\dso25216\Usb20Driver\Win2000_XP Browse
◯ Don'i	search. I will choose the driver to install.
Choo the d	se this option to select the device driver from a list. Windows does not guarantee t iver you choose will be the best match for your hardware.
	<pre>< Back Next > Cancel</pre>

Edit or browse path to ...\USB20driver\win2000_XP\gene.inf (here E: is CD location, dso25216A may be dso29xx or la5000b or la2124a) Click Next to continue



Press Continue Anyway



Completing install

Windows Vista USB driver install

When USB2.0 control interface be connected to computer, screen will display as following:

Found New Hardware
Windows needs to install driver software for your USB2.0 Device
Locate and install driver software (recommended) Windows will guide you through the process of installing driver software for your device.
Ask me again later Windows will ask again the next time you plug in your device or log on.
Don't show this message again for this device Your device will not function until you install driver software.
Cancel

Press Locate and install driver software (recommended) Continue Anyway



Press Continue Anyway

G	Found New Hardware - USB2.0 Device	×
	Insert the disc that came with your USB2.0 Device If you have the disc that came with your device, insert it now. Windows will automatically search the disc for driver software.	
	✤ I don't have the disc. Show me other options.	
4	Next C	Cancel

Press Insert the disc that came with your USB2.0 Device

Click Next to continue

Don't install this driver software
You should check your manufacturer's website for updated driver software for your device.
Install this driver software anyway
Only install driver software obtained from your manufacturer's website or disc. Unsigned software from other sources may harm your computer or steal information.
tails

Press Install this driver software anyway to Continue

Found New Hardware - USB2.0 Device	×
The software for this device has been successfully installed	
Windows has finished installing the driver software for this device:	
USB2.0 Device	
	Close

Completing install

Threshold Voltage Calibration

Signal Generator



Let signal generator output a square wave from -5V to 5V. Set threshold from -4.8 to 4.8V, it should get square waveform. Set threshold to 5.2V, it should get low signal.

Set threshold to -4.8V, it should get high signal.

Trigger Word and Position Calibration

LA-55160 Pattern Generator



LA-55xx use software let trigger position always lock in 100% accuracy position, even you zoom in the waveform, still lock in 100 % accuracy position.

then set trigger word. it should get trigger word at proper position.

it should test more than ten sets trigger word.

Trigger Sequential Calibration

LA-55160 Pattern Generator PG-32400



then set trigger word from 1 to 15 sequential. it should get trigger word at proper position. it should test more than ten sets trigger word.

Clock Source Calibration



It has two clock source, one is internal clock, another is external clock .

Use LA-55160 arbitrary pattern generator to output some 1/2 1/4 ... etc pattern .

the LA-55160 output sample rate is 1 to 100 MHz, for 1/2 pattern, it can get 1/2 Hz to 50

MHz square wave form. then set logic analyzer internal clock to proper sample rate to get data, measure the data frequency should be 1/2 to 50 MHz. the same is true for external clock.

Technical Support

Technical Support can be reached at



CLOCK COMPUTER CORP.

克拉克電腦股份有限公司 7F., No: 5. Lane 236, Section 5. Roosevelt Road. Taipei, Taiwan. <u>11678</u> Phone: 886-2-29321685. 29340273. 29335954. Fax: 886-2-29331687. Email: <u>ufclockc@ms9.hinet.net</u>

Software Updates

Software can be downloaded from our website. Web: <u>www.clock-link.com.tw</u> Software @copyright Clock Computer Corp. 7F., No: 5. Lane 236, Section 5. Roosevelt Road. Taipei, Taiwan. <u>11678</u> All Right Reserved Phone: 886-2-29321685. 29340273. 29335954. Fax: 886-2-29331687. Email: <u>ufclockc@ms9.hinet.net</u>