

Trenz Electronic GmbH info@trenz-electronic.de www.trenz-electronic.de Spartan-3E FPGA Industrial Micromodule

User Manual

Features

- High-density plug-in Xilinx Spartan-3E module
- **USB 2.0** interface with high speed (480 Mbit/s) data rate
- Large SPI flash for configuration and user storage accessible via USB or SPI connector
- Large **DDR-SDRAM**
- FPGA configuration is implemented via JTAG, SPI Flash or USB
- 3 on-board high-power, high-efficiency, switch-mode DC-DC converters (1 A for each voltage rail: 1.2 V, 2.5 V, 3.3 V)
- Power supply via USB or B2B (carrier board)
- Flexible expansion via high-density shockproof B2B (board-to-board) connectors
- Most I/O's on the B2B connectors are routed as LVDS pairs
- Evenly spread supply pins for good signal integrity



Figure 1: TE0300: top view.

- Industrial temperature grade available on request
- Low-cost, versatile and ruggedized design

Specifications

- FPGA: Xilinx Spartan-3E XC3S500E XC3S1600E
- USB controller: Cypress EZ-USB FX2 USB 2.0 microcontroller CY7C68013A-56LFX
- Non volatile memory: 16 MBit 64 Mbit SPI Flash for FPGA-configuration and user data
- Volatile memory: 512 Mbit x 16 DDR SDRAM with up to 666 Mbyte/s
- Up to 110 FPGA user I/Os
- Supply voltage range: 4.0 V 5.5 V
- 1 push-button
- 1 LED
- Small size (only 40.5 mm x 47.5 mm)



Figure 2: TE0300: bottom view.

Applications

- IP (intellectual property) development
- Digital signal processing
- Image processing
- Cryptography
- Industrial control
- Low-power design
- General-purpose prototyping platform

Description

The FPGA industrial micromodule integrates a leading edge Xilinx Spartan-3E FPGA, an USB 2.0 microcontroller, configuration Flash, DDR SDRAM and power supplies on a tiny footprint. A large number of configurable I/Os are provided via B2B mini-connectors.

The module is intended to be used as an OEM board, or to be combined with our carrier boards. It is a powerful system widely used for educational and research activities.

Boards with other configurations, larger FPGA's or equipped with industrial temperature grade parts are available on request.

Software for SPI flash programming over USB as well as reference designs for high speed data transfer over USB are included.

Physical Features

Board Dimensions

The module measures 40.50 mm by 47.50 mm.



Figure 3: module dimensions in mm (top view).

Board-to-Board Connectors



Figure 4: connector receptacles J4 and J5 (bottom view).

The module has two B2B (board-toboard) receptacle connectors (J4 and J5) for a total of 160 contacts (Figure 5).



Figure 5: micromodule receptacle.

The ordering numbers of the connector receptacles are given in Table 1.

supplier	header	
Digikey	H2373CT-ND	
Hirose	DF17(3.0)-080DS-0.5V(51)	
Trenz Electronic	22684	

Table 1: equivalent part numbers ofthe receptacle connectors J4 and J5.

The on-board receptacles mate with their corresponding headers on the carrier board (Figure 6).



Figure 6: mating header.

The ordering number of the headers is given in Table 2.

supplier	header	
Digikey	H2407CT-ND	
Hirose	DF17(4.0)-80DP-0.5V(51)	
Trenz Electronic	22938	

Table 2: equivalent part numbers ofthe mating connectors.

Figure 7 shows the definition of stacking height featured by the combination of the TE0300 receptacle with its corresponding header.



Figure 7: stacking height (h).

The stacking height of the TE0300 B2B connectors is 7 (seven) mm. The stacking height does not include the solder paste thickness.

USB Connector

The micromodule uses a mini-USB (B type) receptacle connector.



Figure 8: mini-USB (B type) receptacle connector.

Power Supply

The module can be powered by the B2B connector or the USB connector. If both power supplies are available, the B2B connector power supply takes precedence, disabling the USB power supply automatically.

B2B Connector Power Supply

The B2B connector power supply requires a single nominal 5 V DC power supply. The power is usually supplied to the module through the 5 V contacts (5Vb2b) of the B2B connectors J5 (see Appendix). The recommended minimum supply voltage is 4 V. The maximum supply voltage is 5.5 V.The recommended maximum continuous supply current is 1.5 A.

USB Power Supply

The module is powered by the USB connector if the following conditions are met:

- the module is equipped with an USB connector,
- the module is connected to a USB bus,
- no power supply is provided by the B2B connectors.

In this case, other components (e.g. extension or carrier boards) may also be powered by the corresponding 5 Volt line (5V) of the B2B connector J5.

On-board Power Rails

Three on-board voltage regulators provide the following power supply rails needed by the components on the micromodule:

- 1.2 V, 1 A max
- 2.5 V, 1 A max
- 3.3 V, 1 A max

The power rails are available for the FPGA and can be shared with a baseboard by the **corresponding** lines of the B2B connectors J4 and J5. Please note that the **power consumption of the FPGA is highly dependent on the design** actually loaded. So please use a tool like Xilinx Xpower to determine the expected power consumption.

Even if the provided voltages of the module are not used on the baseboard, it is recommended to bypass them to ground with 10 nF - 100 nF capacitors.

I/O Banks Power Supply

The Spartan-3E architecture organizes I/Os into four I/O banks (see Table 3).

Bank	Supply Voltage (V)	Min (V)	Max (V)
B0	VccIO	1.2	3.3
B1	2,5	-	-
B2	3,3	-	-
B3	3,3	-	-

Table 3: I/O banks power supply.

Voltage for banks B1, B2 and B3 is fixed respectively to 2,5 V, 3,3 V and 3,3 V.

Voltage VccIO for bank B0 shall span from 1.2 V to 3.3 V. VccIO can be supplied either externally or internally to the micromodule.

Warning! Spartan-3 I/Os are not 5 V tolerant. Applying more than the recommended operating voltages at any pin, results in a damaged FPGA (see Xilinx Answer AR#19146).

Externally Supplied VccIO

VccIO can be externally supplied over the B2B connector J4. If bank B0 is not used, then VccIO can be left open.

Internally Supplied VccIO

If VccIO is **not** externally supplied, it can be internally supplied by **one** of the internal power rails of 2.5 V and 3.3 V. This is possible by short-circuiting **one** of the two pad pairs placed on the right of connector J4 at the top right corner of the bottom side of the micromodule.

Figure 9 shows how to short-circuit VccIO to internal 3.3 V power rail.

Figure 10 shows how to short-circuit VccIO to internal 2.5 V power rail.



Figure 9: R102 pad pair (blue highlight) for 3.3 V internal supply.



Figure 10: R103 pad pair (blue highlight) for 2.5 V internal supply.

Two suitable ways of shirt-circuiting the paid pair are by means of a zero-ohm 0603 (1608 metric) chip resistor or a solder blob.

FPGA User I/Os

A total of 110 FPGA user I/Os are available on corresponding contacts of B2B connectors J4 and J5 (see Appedix).

- 37 differential digital I/O pairs: each pair is configurable as 2 singleended digital I/Os, corresponding to a maximum of 74 single-ended digital I/Os;
- 4 differential clock input pairs: each pair is configurable as differential digital I/O pair or 2 single-ended clock inputs or 2 single-ended digital I/Os (or combination thereof), corresponding to from a maximum of 8 independent clock inputs to a maximum of 8 independent digital I/Os;
- 1 differential clock input pair: the pair is configurable as differential digital input pair or as 2 single-ended clock inputs or 2 single-ended digital inputs (or combination thereof), corresponding to from a maximum of 2 independent clock inputs to a maximum of 2 independent digital inputs;
- 21 single-ended digital I/Os;
- 5 single-ended inputs.

Table 4 summarizes the maximum available FPGA user I/Os divided by supply voltage.

type	VccIO	3.3 V
diff. I/O pairs	≤ 18	≤ 23
diff inputs	≤ 1	none
diff. clocks	≤ 4	≤ 1
s. e. I/Os	≤ 46	≤ 58
s. e. inputs	≤ 2	≤ 4
s. e. cloks	≤ 8	≤ 3

Table 4: maximum FPGA user I/Os bysupply voltage.

Differential Pairs

The micromodule has a total of 42 differential signal pairs routed pairwise with a differential impedance of 100 ohm to adjacent connector pins. These lines can be used for high speed signaling up to 666 Mbit/s per differential pair (see Xilinx Application Note XAPP485).

User Button and LED

LED

The LED is lit when the U_LED line (pin R10) is set high as detailed in the following table.

Signal	FPGA pin	FPGA ball
U_LED	IO_L15P_2 (bank 2)	R10

Tabelle 5: user led signal details.

Push Button

The push button is connected to the PB input (pin V16). as detailed in the following table.

Signal	FPGA pin	FPGA ball
PB	IP (bank 2)	V16

Tabelle 6: user button signal details.

The input is normally low. The input is pulled up when pressed.

Configuration Switches

The micromodule hosts 4 DIP switches on the top side: S1; S2, S3 and S4.

For customers requesting a sufficient amount of units, the micromodules can be manufactured replacing the switches by fixed connections.

DIP Switch S1

S1 enables / disables the communication between the Cypress EZ-USB FX2 micro-controller and the I2C CMOS Serial EEP-ROM.

Turn S1 off when programming the USB EEPROM storing the USB vendor ID and device ID. This will force the USB microcontroller to provide its default vendor ID and device ID.

S1	position	
EEPROM (on)*	EEPROM <u>en</u> abled	
Off (off)	EEPROM <u>dis</u> abled	

Table 7: S1 (* default: EEPROM).

For further information, please read paragraph "Software Configuration".

DIP Switch S2

S2 enables / disables the reset line. The reset line (available also on 2 contacts of the B2B connector) resets the USB micro-controller and the FPGA.

S2 has to be turned off (*Reset*) if the user wants to program the SPI Flash memory in direct mode. For programming the SPI Flash memory in indirect mode over JTAG, S2 has to be turned on (*Run*).

S2	position	
Run (on)*	system running	
Reset (off)	system reset	

Table 8: S2 (*default: Run).

For further information, please read paragraph "Software Configuration".

DIP Switch S3

S3 conditionally / unconditionally enables the 1.2 V and 2.5 V power rails.

When S3 is turned on, the 1.2 V and 2.5 V power rails are controlled by the USB microcontroller. At start-up, the USB mi-

crocontroller switches off the 1.2 V and 2.5 V power rails and starts up the module in low-power mode. After enumeration, the USB microcontroller firmware switches the 1.2 V and 2.5 V power rails on, if enough current is available from the USB bus.

When S3 is turned off, the 1.2 V and 2.5 V power rails are always enabled.

S3	position	
FX2 PON (on)*	rails controlled by FX2	
PON (off)	rails always enabled	

Table 9: S3 (* default: FX2 PON).

Warning! When S3 is turned on (*FX2 PON*), make sure that no signals are applied to the input pins when power-rails are disabled by the USB microcontroller.

The 3.3 V power-rail though is out of the control of the USB-microcontroller and is supplied down-converting the 5 V power supply provided by either the USB-bus or the B2B receptacle connector. In this case, signals that are applied to the 3.3 V I/O banks do not need to be disconnected when power-rails are disabled by the USB microcontroller.

DIP Switch S4

S4 enables / disables the FPGA configuration through the SPI interface. The FPGA configuration through the JTAG interface cannot be disabled.

When S4 is turned on, the FPGA tries to configure from the SPI Flash memory. The FPGA can be configured by the JTAG interface at any time.

When S4 is turned off, the FPGA waits to be configured by the JTAG interface.

For further information about direct (pure SPI) / indirect (SPI over JTAG) in-system programming of SPI flash memories, please see Xilinx Application Notes XAP-P951 "Configuring Xilinx FPGAs with SPI

Serial Flash" and XAPP974 "Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs".

S4	position	
SPI (on)*	FPGA configuration: JTAG + SPI	
JTAG (off)	FPGA configuration: JTAG	

Table 10: S4 (* default: SPI).

Warning! When downloading via parallel JTAG programmer to FPGA, it can happen that programming fails with Error: "'1' : Programming terminated. DONE did not go high." Try setting DIP switch S4 to JTAG-only. A bug in certain Xilinx iMPACT versions can cause this.

DIP Switches Overview

Figure 11 summarizes functions and location of the four DIP switches.



Figure 11: DIP switches overview.

JTAG and SPI

JTAG Header

JTAG signals are available on the dedicated header J2 through a JTAG programmer with flying leads as described in Table 11.



Table 11: JTAG header (J2).

SPI Header

SPI signals are routed to / from bank 2 of the FPGA as detailed in Table 12 and made available on the dedicated header J3 accessible through an SPI programmer with flying leads as described in Table 13.

Signal	FPGA pin	FPGA ball
SPI /S	IO_L01P_2	U3
SPI D	IO_L03N_2	T4
SPI Q	IO_L16N_2	N10
SPI /C	IO_L26N_2	U16

Table 12: SPI signal details (bank 2).





Clock Networks

24 MHz Clock Oscillator

The module has a 24 MHz SMD clock oscillator providing a clock source for both the USB microcontroller and the FPGA as detailed in Table 14.

Signal	FPGA pin	FPGA ball
24MHZ1	IO_L12P_2 (bank 2)	N9

Table 14: 24 MHz clock signal details.

Main Clock Oscillator

The module has a main SMD clock oscillator providing a clock source for the FPGA as detailed in Table 15.

Signal	FPGA pin	FPGA ball
100MHZ 125MHZ	GCLK0 (bank 2)	U10

Table 15: main clock signal details.

Standard frequencies are 100 MHz and 125 MHz (please visit Trenz Electronic website for current ordering information). The lower the main clock frequency, the lower the module power consumption. Moreover, as the main clock is preferably used as DDR SDRAM clock, a lower clock frequency makes easier for the development tools to meet the timing requirements (particularly for DDR SDRAM). For customized boards, this clock can be changed according to user requirements.

Interface Clock (IFCLK)

The IFCLK line synchronizes the communication between the USB microcontroller and bank3 of the FPGA as detailed in Table 16.

Signal	FPGA pin	FPGA ball
IFCLK	LHCLK5 (bank 3)	K4

Table 16: interface clock signal details (bank 3).

Digital Clock Manager (DCM)

The DCMs of the FPGA can be used to synthesize arbitrary clock frequencies from any on-board clock network, differential clock input pair or single-ended clock input. For further reference, please read Xilinx data sheet DS485 "Digital Clock Manager (DCM) Module" (dcm_module.pdf) and Xilinx application note XAPP462 "Using Digital Clock Managers (DCMs) in Spartan-3 FPGAs" (xapp462.pdf).

On-board Memories

The TE0300 has three on-board memories:

- DDR SDRAM
- SPI Flash
- serial EEPROM

DDR SDRAM

TE0300 modules have a 512Mb DDR SDRAM component for operation (code and data) accessible through the FPGA.

Commercial-grade modules mount the following component:

Micron Technology MT46V32M16BN-6

Industrial-grade modules mount the following component:

Micron Technology MT46V32M16BN-6 IT

You can get the exact part number of the component mounted on your module from the Micron FBGA decoder:

http://www.micron.com/support/part_inf o/fbga/decoder When developing DDR SDRAM designs with Xilinx tools (e.g. MIG, MPMC, ...), you should select the following product type:

MT46V32M16-6.

Should it be not available, you can use one of the following product types:

- MT46V32M16-5
- MT46V32M16XX-5B
- MT46V32M16BN-5B
- MT46V32M16FN-5B
- MT46V32M16P-5B
- MT46V32M16TG-5B

 $\mathsf{TE0300}\xspace$ modules with the following part numbers

- TE0300-00
- TE0300-00-4I5C
- TE0300-00B
- TE0300-01
- TE0300-01B
- TE0300-01BLP

were assembled with

Qimonda HYB25DC512160CF-6

512Mb DDR SDRAM components. When developing DDR SDRAM designs with Xilinx tools, you should select the following product type:

HYB25D512160BF-6.

SPI Flah

TE0300 modules have a

STMicroelectronics M25P32

32-Mbit, low voltage, serial Flash memory with 75 MHz SPI bus interface for configuration and operating storage accessible through USB or SPI.

Serial EEPROM

TE0300 modules have a

Micron Technology 24LC128

128K I2C CMOS Serial EEPROM for EZ-USB FX2 firmware, vendor ID and device ID storage accessible through the EZ-USB FX2 microcontroller.

Module Configuration

This section describes how to configure the TE0300 module and access some of its resources.

The JTAG interface allows a fast, frequent but volatile configuration of the TE0300 module. However, only through the JTAG interface it is possible to develop and debug with Xilinx tools (e.g. Xilinx Chip-Scope, Xilinx Microprocessor Debugger.

The SPI interface allows a fast, frequent and non-volatile configuration of the TE0300 module.

Configuration of the TE0300 module through a USB host is recommended for occasional, non-volatile on-site operations such as firmware upgrade.

System Requirements

TE0300 modules can be configured through a host computer with the follow-ing system requirements:

- Operating system: Microsoft Windows 2000, Microsoft Windows XP, Microsoft Vista;
- Xilinx ISE 10.1 or later for indirect SPI in-system programming (see Xilinx Answer AR #25377);
- Xilinx EDK for some reference designs;
- Interface: USB host;
- JTAG/SPI USB cable with flying leads.

EZ-USB FX2 Microcontroller Firmware

If the EEPROM has never been programmed before (virgin board), S1 can be switched to **EEPROM**. The USB microcontroller will detect an empty EEPROM and will provide its default vendor ID and device ID to the USB host.

DIP switch	on (left)	off (right)
S1	EEPROM	-
S2	Run	-
S3	Х	Х
S4	х	х

If the EEPROM has been programmed before (EEPROM not empty), S1 must be switched to **Off**. The USB microcontroller will detect a missing EEPROM and will provide its default vendor ID and device ID to the USB host.

DIP switch	on (left)	off (right)
S1	-	Off
S2	Run	-
S3	Х	Х
S4	Х	Х

Generic USB Microcontroller Driver installation

If the USB microcontroller (Cypress EZ-ESB FX2) driver is not installed on the host computer, then the easiest way to do it is the following:

- disconnect the micromobule or leave the micromodule unconnected;
- configure the micromodule such that the USB microcontroller will provide its default vendor ID and device ID to the USB host (i.e. S1 = OFF -- see paragraph "EZ-USB FX2 Microcontroller Firmware");
- connect the micromodule to the host computer through the USB interface;

- wait until the operating system detects new hardware and starts the hardware assistant;
- if S1 is not already switched to EEP-ROM, do it now;
- answer the hardware assistant questions as shown in the following example.

Assistent für das Suchen r	neuer Hardware
	Willkommen
	Mit diesem Assistenten können Sie Software für die folgende Hardwarekomponente installieren:
	USB Device
	jetzt ein.
	Software <u>a</u> utomatisch installieren (empfohlen) Software von einer Liste oder bestimmten Quelle
	installieren (rur rorrgeschrittene behutzer) Klicken Sie auf "Weiter", um den Vorgang fortzusetzen.
	< <u>Zurück</u> <u>W</u> eiter > Abbrechen







Check that in the "Device Manager" under "USB-Controller" the "Cypress Generic USB Device" has been added.



Now the USB microcontroller can be accessed from the host computer through dedicated software.

EZ-USB FX2 EEPROM Programming

First of all, check that S1 is actually switched to EEPROM.

The USB EEPROM can be programmed by opening the dedicated software "Cypress USB Console" (double click the "CyConsole.exe" file in the "1st_program\CyConsole" folder).

🐨 Cypress USB Co	onsole				
Eile Options Help					
èv 🗉 🖸 🖨 [Selected Script:		ж	8 🕻	7
Select Device					
USB Address Devic	ce Name	Name in Wir	dows Device Mgr	(from .inf	
4 USB	Device	Cypress Gen	eric USB Device		
1					
Device Properties C	ontrol Endpt ×fers 0	Ither Endpt Xfers M	isc.		
VendorID 0)x04B4	Class	0xFF		
ProductID 0)x8613	Subcl	assOxFF		
Manufacturer		Protoc	ol UXFF		
Serial Number		DCuDe	SMCE UXAUUT		
o ondiritambor					
Device Configuration	s (1)				
Value	Attributes	Max Power			
0x01	0x80	0x32 (100 mA)			
Configuration Interfac	es (4)				
Intfc Alt Setting	Class	Subclass	Protocol		~
0 0	0xFF (Vendor)	0xFF	0xFF		
0 1	0xFF (Vendor)	0xFF	0xFF		
JU 2	uxhr (vendor)	UXFF	UXFF		
Interface Endpoints ((0)				
Address	Attributes	Max Pkt Size	e Interval		
,					

Click "Options > EZ-USB Interface" to Open EZ-USB Interface window.

☞ EZ-USB Interface	
Device USB Device Clear Load Mon S EEPROM Select Mon	
Get Dev Get Conf Get Pipes Get Strings Download Re-Load Get Pipes URB Stat H	IOLD RUN
Vend Req Req 0x00 Value 0x0000 Index 0x0000 Length 0 Dir 0 0UT - Hex Byt	es CO B4 04 81 00 01 00 💌
Iso Trans Pipe Length 128 Packet Size Packets	
Bulk Trans Pipe Length 64 Hex Bytes 5	
Reset Pipe Abort Pipe File Trans Pipe	
Set IFace Interface 0 AltSetting 0	
	~

"S EEPROM" button refers to the small EEPROM (256 bytes) whereas the "Lg EE-PROM" refers to the large EEPROM (64 kB). Press the "Lg_EEPROM" button, select the "USB.iic" file and press the "Open" button to start writing to EEPROM.

Large (512 - 64	IK byte) EEPRC	OM Download				? 🛛
<u>S</u> uchen in:	🛅 TE0300		•	(=	🔺 💷 •	
Zuletzt verwendete D	i driver CyConsole dusb.iic					
Desktop Eigene Dateien						
Arbeitsplatz						
Netzwerkumgeb ung	Datei <u>n</u> ame: Dateityp:	usb.iic i2c EEPROM File Schreibgeschi	es (".iic) ültzt öffnen		•	<u>Üf</u> fnen Abbrechen

Upgrade progress is displayed in status window and is completed when "Down-load Successful" text is displayed.

→ EZ-USB Interface	. 🗆 🗙
Device USB Device Clear Load Mon S EEPROM Select Mon	
Oet Dev Get Conf Get Pipes Get Strings Download Re-Load La EEPROM URB Stat HOLD RUN	
Vend Reg Reg 0x00 Value 0x084E Index 0x0000 Length 0 Dir 0 OUT - Hex Bytes C0 84 04 81 00	01 00 💌
Iso Trans Pipe Length 128 Packet Size Packets	
Bulk Trans Pipe Length 64 Hex Bytes 5	
Reset Pipe Abort Pipe File Trans Pipe	
Set IFace AtSetting 0	
000 02 0D 91	^
ownload 12 bytes: addr=d91	
1000 /8 /F #4 F6 D8 FD /5 81 38 02 05 #6	
ovnijaa 26 pytes: augr-ove NNN DD NI NE 80 02 90 BE 02 BE 02 BE 02 BN 22 EN	
010 06 K9 25 82 K8 K8 22 K8 K8 06 K9 25 82 K8 K2 22	
020 E5 82 29 F5 82 E5 83 3A F5 83 E4 93 22 F8 BB 01	
030 OD E5 82 29 F5 82 E5 83 3A F5 83 E8 F0 22 50 06	
040 89 25 82 C8 F6 22 BB FE 05 89 25 82 C8 F2 22 8B	
050 9F F5 F0 EA 9E 42 F0 E9 9D 42 F0 E8 9C 45 F0 22	
oggle 8051 Reset (00)	
ownloading file: C:\TE0300\usb.iic	
ownloading 1221 bytes to addr=0	
ownload Successful: 547 buts downloaded	
	_
	~

Disconnect the USB cable.

Dedicated USB Firmware Driver Installation

Check the configuration switches against the following table:

DIP switch	on (left)	off (right)
S1	EEPROM	-
S2	Run	-
S3	FX2 PON	-
S4	Х	Х

Reconnect the USB cable to run the newly uploaded firmware in the USB microcontroller. Under the default switch configuration, the USB microcontroller is now ready to provide dedicated vendor ID and device ID. Wait until the operating system detects new hardware and starts the hardware assistant and answer the hardware assistant questions as shown in the following example.





Check that in the "Device Manager" under "USB-Controller" the "DEWESoft USB Device 0" has been added.





🚇 Geräte-Manager	
Datei Aktion Ansicht ?	
🗄 🏶 Prozessoren	~
Systemgerde	
🗄 🚔 USB-Controller	
්දී CA-200	
DEWESoft USB Device 0	
Intel(R) ICH8 Family USB Universal Host Controller - 2830 Intel(R) ICH8 Family USB Universal Host Controller - 2830	
Intel(R) ICH6 Family USB Universal Host Controller - 2831	
The Intel(R) ICH8 Family USB Universal Host Controller - 2834	
Intel(R) ICH8 Family USB Universal Host Controller - 2835	
Intel(R) ICH8 Eamly LISB2 Enhanced Host Controller - 2836	
- 🕰 Intel(R) ICH8 Family USB2 Enhanced Host Controller - 283A	
USB-Root-Hub	8
🕰 USB-Root-Hub	
- 🙀 USB-Root-Hub	
😴 USB-Root-Hub	
ංඥ USB-Root-Hub	~

FWU File Generation

The TE0300 micromodule can be configured by means of a firmware-upgrade (FWU) file (see next section "Micromodule Configuration" for further reference). The first step in generating the FWU file is to generate the *fpga.bin* file corresponding to a given FPGA design. The TE0300 reference projects provide a way to generate the *fpga.bin* file in an automatic way, i.e. by executing the following batch file:

#XilinxEdkReferenceProject#\ PREPARE_FW\TE0300_usb_fw.bat

where *#XilinxEdkReferenceProject#* is the base directory of the corresponding reference project.

Alternatively you can use Xilinx IMPACT from Start / Programs / Xilinx ISE / Accessories / Impact

Select "create new project".

<u>×</u>

Select "prepare PROM file".

🐉 iMPACT - Welcome to iMPACT	_ 🗆 🗙
Please select an action from the list below	
C Configure devices using Boundary-Scan (JTAG)	
Automatically connect to a cable and identify Boundary-Scan chain 💌	
Prepare a PROM File	
C Prepare a System ACE File	
C. Prepare a Boundary-Scan File	
SVF 💌	
C Configure devices	
using Slave Serial mode	
< Back. Next >	Cancel

Select "BIN" as output.

🐉 iMPACT - Prepare PROM Files		_ 🗆 🗙
I want to target a		
 Xilinx PROM 		
C Generic Parallel PROM		
C 3rd-Party SPI PROM		
C PROM Supporting Multiple Design Versions:	Spartan3E MultiBoot	$\overline{\gamma}$
PROM File Format		
C MCS C TEK C UFP ("C" format)		
C EXO C BIN C ISC		
C HEX 🗖 Swap Bits		
Checksum Fill Value (2 Hex Digits): FF		
PROM File Name: fpga		
Location: C:Willinx\		Browse
	< Back Next >	Cancel

Set "PROM File Name" to "fpga" and change "Location" to a suitable name and location.

🕵 iMPACT - Specify Xilinx PROM Device	- I X
Auto Select PROM	
Enable Revisioning	
Number of Revisions: 1	
Enable Compression	
Select a PROM (bits): Unspecifier	Add
Position Part Name	
Delete All	
< <u>B</u> ack <u>N</u> ext >	Cancel

Add Device				<u>? ×</u>
Look in:	implementation	T	🗢 🗈 💣 🎟	•
Recent Desktop My Documents My Computer	cache chipscope_cop_bla_0_wrapper chipscope_opb_bla_0_wrapper dcm_0_wrapper dcm_0_wrapper debug_module_wrapper dmb_cntr_wrapper dmb_cntr_wrapper imb_cntr_wrapper imb_cht_wrapper imb_cb_wrapper imb_cb_wrapper imb_cb_wrapper imb_cb_wrapper imb_cb_wrapper imb_cb_wrapper imb_cb_wrapper imb_cb_wrapper	Copb_rtc_0_wag	oper per per pper mp.bit	
My Network Places	File name: download.bit	(* bit)	• •	<u>O</u> pen Cancel
		· ·		/

The following warning is normal :).

🐉 Warn	ing X
⚠	WARNING:IMPACT:2257 - Startup Clock has been changed to 'Cclk' in the bitstream stored in memory, but the original bitstream file remains unchanged.
	OK

Check "Auto Select PROM".

퉳 Add D	evice 🔀
٩	Start adding device file to Data Stream: 0
	ОК

Navigate to your project's IMPLEMENTA-TION folder and select "download.bit". This is probably the one and only file with your design.

퉳 Add D	evice	×
?	Would you like to add another device file to	
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	Data Stream: 0	
	Yes No	

Congratulations!



Click GENERATE FILE or select from menu Operations / Generate file.

🐉 iMPACT - C:\Xilinx\default.ipf - [PROM File Formatter]
😵 Eile Edit View Operations Window Help
] 沙 🖥 🖇 🔓 🗶 🖶 ※ 井井 🛱 🗉 ( 井井 ひ 😺 🕅
×
Boundary Scan
SelectMAP
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SuptemACE
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Modes
x
Available Operations are:
👄 Generate File
Derations
Bendidina Bendidi Bendidina Bendidina Bendidina Bendidina Bendidina Bendidia
INFO: iMPACT: 501 - '1': Added Device xc3s400 successfully.
i <b>-</b>
<b>_</b>
Output & Error & Warning
PROM File Generation   Target Xilinx PROM   1,699,136 Bits used   File: fpga in Location: C:\Xilinx\/

You are done.

🐉 iMPACT - C:\Xilinx\default.i	pf - [PROM File Formatter]	_ 🗆 🗵
🎯 Elle Edit View Operations :	Window Help	_ 8 ×
📝 🗟 🗶 🖻 🖉 🗶 🛤	× 🗄 🖽 🗇 E 🛛 🗱 O 😺 😽	
Available Operations ere	Example of the second s	
Operations	PROM File Formatter	
Writing file "C:\ Writing file "C:\ 4 Output / Error / Warning	Xilinx\//fpga.prm". Xilinx\//fpga.sig".	•
Ready	PROM File Generation Target Xlinx PROM 1,699,136 Bits used File: fpga in Location:	C:\Xilinx\/

Don't forget to save your project for further use

🐉 Exit iMPACT	×
Do you want to save pr	oject file before exiting?
Yes No	Cancel

Once you have got your *fpga.in* file, you can proceed and generate your FWU file. The FWU file is a ZIP file containing 3 files:

- Bootload.ini booting settings
- *fpga.bin* FPGA programming file
- usb.bin FX2 firmware

To create your FWU file, you need to

- replace the existing USBFWUTool\FWUs\fpga.bin with the latest fpga.bin (Bootload.ini and usb.bin are always unchanged)
- zip the 3 files
- change the *.zip* file extension to *.fwu*
- upload the file as explained in the next section (Micromodule Configuration).

# Warning! file and path names are given and must NOT be changed!

#### Micromodule Configuration

The micromodule can now be programmed with its dedicated firmware upload tool. Turn S1, S2, S3 and S4 on. Open the dedicated firmware upgrade tool "USB Firmware Upgrade Tool" (double click the "USBFirmwareUpgrade-Tool.exe" file in the "USBFWUTool" folder).

😫) USB Firn	nware Upgrade Tool 🛛 🔀
Device:	JSB Device
File name:	Upload
	Version: 2.6

Press the "..." button corresponding to the "File name" field and select for instance the sample firmware upload file "TE0300_v1012.fwu" in the "USB-FWUTool\FWUs" folder.



🗟 ) USB Firn	nware Upgrade Tool	
Device:	USB Device	
File name:	C:\TE0300\USBFWUTool\FWUs\TE0300_v1012.	Upload
	 Ve	rsion: 2.6

Press the "Upload" button to upload the micromodule firmware and check the "FPGA uploading..." progress bar.

a) USB Firmware Upgrade Tool	X
Device: USB Device	
File name: C:\TE0300\USBFWUTool\FWUs\TE0300_v1012.	Upload
FPGA uploading (22%)	Version: 2.6

After successful completion of the firmware upload procedure, the following message should pop up.

USB Firmware Upgrade Tool 🛛		
Firmware upgrade successful!		
(OK]		

Reboot the micromodule with the new firmware by disconnecting and reconnecting the USB cable. You may want to test the sample application "TE0300_API_Example.exe" in the "TE0300 API Example\Debug" folder.

To generate your own firmware upload file, please read the document "Generating_FWU_file.doc" in the "USBFWUTool" folder.

#### SPI Direct In-System Programming (ISP)

Make sure S2 is switched to "Reset" (off) during programming.

Connect the host computer to the micromodule through both the SPI flying leads cable and the USB cable.

Start Xilinx ISE iMPACT. The following example shows the case of iMPACT 9.2. If the "iMPACT Project" window pops up, press the "Cancel" button.

😻 iMPACT Project			
I want to			
Ioad most recent project	default.ipf	~	Browse
		Load most recent project file when iMPA	CT starts
🔵 create a new project (.ipf)	default.ipf		Browse
	<u>0</u> K	Cancel	

Double click the "Direct SPI Configuration" option in the "Modes" panel.

💱 ІМРАСТ	
Ble Edit Yew Operations Options Output Debug Window Help	
2     2	
Tree         X         MALT homeon         X           Tablands 2-45 mill         Tablands 2-45 mill         Tablands 2-45 mill         X           Tablands 2-45 mill         Tablands 2-45 mill         Tablands 2-45 mill         X           Tablands 2-45 mill         Tablands 2-45 mill         Tablands 2-45 mill         X           Tablands 2-45 mill         Tablands 2-45 mill         Tablands 2-45 mill         X           Tablands 2-45 mill         Tablands 2-45 mill         Tablands 2-45 mill         X           Tablands 2-45 mill         Tablands 2-45 mill         Tablands 2-45 mill         X           Tablands 2-45 mill         Tablands 2-45 mill         Tablands 2-45 mill         X	
Nodes Openations	http://www.stiinx.com
<ul> <li>Feldine to 1996/T</li> </ul>	
Danit Dros Warring	8
	III.e

Right click the "Direct SPI Configuration" panel to add a device and select "Add SPI Device".

<ul> <li>WPACT - [Direct SPI Configuration</li> <li>Bo Edit Zow Operations Optime Quint</li> <li>P 田 美 印 正 美 印 金 部 第二</li> </ul>	n] npt Debug Window Help 副 前: 音音 〇 华 紀	
Fixe         X           ************************************	Arola-It Operator X	Ale Briteman, Dir-O Gele Laug, . Fight dak Li Ald Direks or Bould Direks
Notes	Operations	Se Elen: SP Configuration
Fileson 20 IFACI (7) *** BACC (0D) restor (7) *** BACC (0D) restor (	da -api da -api	
Deput Dros Warning		8

You can now select the file corresponding to your device. In the following example, we will show how to select the micromodule reference device "blinking.mcs" in the "TE0300" folder.

Add Device					? 🛛
<u>S</u> uchen in:	C TE0300		•	🗢 🗈 💣 📰 •	
Zuletzt verwendete D	blinkin.mcs blink1600.mcs				
Eigene Dateien					
Arbeitsplatz					
Netzwerkumgeb ung	Datei <u>n</u> ame: Datei <u>t</u> yp:	blinkin.mcs All Design Files (*.mcs *.exc	2)	<b>•</b>	Ü <u>f</u> fnen Abbrechen

Select the part name corresponding to the SPI flash present on the module (STMicroelectronics M25P32, a 32 Mbit (4M x 8) Serial Flash memory).

🐉 Select Device Par	t Name 🔀
Select PROM	
Part Name:	M25P32
<u>o</u> k	<u>Cancel</u> Help

iMPACT should now look like this.

👺 IMPACT - [Direct SPI Configuration]	
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fine X MPACI Incense X	
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Drast Two Waving	8
	No Cable Connection

Right click the SPI PROM device and select the "Program" operation.

😺 IMPACT - [Direct SPI Configurati	in]			
😼 Bie Edit Ziew Ogerations Opjions (	Quiput Debug ∭rdov Help			
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4				× 1
Deput Dires Warning				No Cable Competition

In the "Programming Properties" window, just leave the default settings and press the "OK" button.



iMPACT will first erase the memory (notice the mismatch between the two progress indicators)

😵 Progress Dialog [61%]	? 🔀
Executing command	
0%	
	Cancel

and then write it (notice the match between the two progress indicators).

🐉 Progress Dialog [10%]	? 🗙
Executing command	
10%	
	Cancel

After successful programming, you should read the message "Program Succeeded" popping up for a few seconds in the "Direct SPI Configuration" panel.



Switch S2 back to the "Run" position. In case you uploaded the test design, you should see the on-board led blinking at 0.5 Hz.

For further information about direct (pure SPI) in-system programming of SPI Flash memories, please see Xilinx Application Note XAPP951 "Configuring Xilinx FPGAs with SPI Serial Flash".

#### SPI Indirect In-System Programming (ISP)

Check the configuration switches against the following table:

DIP switch	on (left)	off (right)
S1	Х	Х
S2	Run	
S3	-	PON
S4	Х	Х

Connect the host computer to the micromodule through both the SPI flying leads cable and the USB cable.

Start Xilinx ISE iMPACT. The following example shows the case of iMPACT 10.1. If the "iMPACT Project" window pops up, press the "Cancel" button.

🔯 iMPACT Project					×
I want to					
Ioad most recent project	default.ipf			~	Browse
		🔲 Load most recer	it project file when iM	IPACT	starts
🔘 create a new project (.ipf)	default.ipf				Browse
	<u>o</u> k	Cance	91		

Double click the "Boundary Scan" option in the "Modes" panel.

🐉 ІМРАСТ		
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Nores	Opersions	nito www.critic.com
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impact Version: 10.1		
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Right click the "Boundary Scan" to initialize the chain and select "Initialize Chain".

💱 IMPACT - [Boundary Scan]			
😼 Bie Edit View Operations Options (	Quaput Debug Window Help		L B X
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Door         X           Statution Scar         Statution           Statution Final         Statution           Statution         Statution	NPACT * costor X Available Operations are:	Add Booline Groups         CH-1           Add Booline Groups         CH-1           Call Acad Callocat         CH-1           Call Acad Callocat         CALL Direct reliability 1160 chase           Chipter Singer         Image: Chipter Singer	
<pre>meme bicket to 100ACT stDect Version to.t // inv Acct cost and // i</pre>	1	i konderfyten	
CApe Ena Waning		No Cable Correction   No File	e Oper     .

An "Assign New Configuration File" dialog window should pop up automatically. You can now select the file corresponding to your design. In the following example, we will show how to select the micromodule reference design "blinking.bit" in the "TE0300" folder. Do not forget to select the "Enable Programming of SPI Flash Device Attached to this FPGA" option in the same window.

San New Configuration File	? 🔀
Look jn: 🔄 E:/TE0300/ 💌 🗢 🖸	È 💣 🖩 🖩
C blinkin.bit	
blinkin1600.bit	
File name: blinkin.bit	<u>O</u> pen
File type: All Design Files (*.bit *.nky *.isc *.bsd)	Cancel
Cancel <u>A</u> ll	<u>B</u> ypass
O None	
<ul> <li>Enable Programming of SPI Flash Device Attached to this FPGA</li> </ul>	
C Enable Programming of BPI Flash Device Attached to this FPGA	

An "Add PROM File" dialog window should pop up automatically. You can now select the file corresponding to your design. In the following example, we will show how to select the micromodule reference design "blinking.mcs" in the "TE0300" folder.

Add PROM File					? 🔀
<u>S</u> uchen in:	bemp_TE030	0	•	+ 🗈 💣 🎟	•
Zuletzt verwendete D	blinkin.mcs				
Eigene Dateien					
Arbeitsplatz					
Netzwerkumgeb ung	Datei <u>n</u> ame: Datei <u>t</u> yp:	blinkin.mcs MCS Files (*.mcs	)	•	Ü <u>f</u> fnen Abbrechen

Select now the SPI Flash corresponding to the one present on the module (STMicroelectronics M25P32 in the example, a 32 Mbit (4M x 8) Serial Flash memory).

💱 FPGA SPI Flash Association 🛛 🔀			
Select SPI Flash FPGA xc3s1200e	SPI Flash M25P32		
<u><u> </u></u>	Cancel		

iMPACT should now look like this.

We may not a simplement A second		
File Edit View Cperations Output	Debug Window Help	000
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dche. PROGRESS END - End Cp Elapoid time - C // *** EATCH CED : 10	ara:icn. Joo. RaildyWFM	

Right click the "Flash" device and select the "Program" operation.

SiNPACT - [Direct SPI Configuration]	
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Caper Env Waning	<u>&gt;</u>
	No Caste Connection

In the "Device Programming Properties" window, just leave the default settings and press the "OK" button.



iMPACT will first erase the memory

😵 Progress Dialog [1%]	? 🛛
Executing command	
1%	
	Cancel

and then write it.

😵 Progress Dialog [10%]	? 🔀
Executing command	
10%	
	Cancel

After successful programming, you should read the message "Program Succeeded" popping up for a few seconds in the "Boundary Scan" panel.

🖗 INPACT - [Boundary Scan]					
🖗 Ble Edit Yew Operations Quiput	Debug Window Help				
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flost	K NPACT PLUESES X	· · · · ·			
P Pellourden Scar	Available Deceations are:	Right click d	evere to ever to presture	*	
The second second	mb Exercision		FLASH		
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		100-		110grain baccecaea	
Norm	Operators	Sh Fants	mit can		
Decryptor security se	t		0		
DCN Indited			-		
DC1 matched			-		
legacy imput error					
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status ci oji					
value of NODE rin MD					
velue of HODE rin H1			ō		
value of BOOK T'D BZ					
value of CFG PDY (INI	7 81		1		
DONEIN input from DON	2 pin				
ILCODE not validated	while trying to write YDSI		0		
write FDRI issued bef	ore or after decrypt operat	1001	0		
Decryptor keys not us	id in proper sequence	•	0		
INFO:1MFACT:2219 - SC	icus regiscer values:				
INPO: INFACT - COII OI	1: 10:1 10:00 0000 C000 0:00	0.00L			
INFOLINE ACTINIC 11	a completes covalocally file	LIIC CO C	JCV100.		
11: Programmed survey	estally				
PLOCRESS END End Cr	ration.				
Elapsed tipe - 01	sec.				
¢					
0.4pu Enu Waning					
				Configuration Patrio	ann Ceble USD   C Milts   usb-h

Switch S3 back to the "FX PON" position. In case you uploaded the reference design, you should see the on-board led blinking at 0.5 Hz.

For further information about indirect (SPI over JTAG) in-system programming of SPI Flash memories, please see Xilinx Application Note XAPP974 "Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs".

# Changes from TE0300-00 to TE0300-01

#### Clocks

TE0300-00 has a 50MHz secondary clock, whereas TE0300-01 has a 125MHz secondary clock.

#### **Volatile Memory Interface**

TE0300-00 could access the DDR SDRAM *only* with Xilinx OPB (on-chip peripheral bus) cores.

TE0300-01 can *also* access the DDR SDRAM through the dedicated Xilinx MIG (memory interface generator) memory interface.

#### **B2B Connectors**

Contact 14 of connector J5 has been extended from an input in TE0300-00 to an I/O in TE0300-01. Therefore hardware designs developed for the TE0300-00 are compatible with the TE0300-01 whereas those developed for the TE0300-01 are compatible with the TE0300-00 if that contact is configured as input.

Contact 76 of connector J5 has mistakenly been described as I/O in TE0300-00, but it has always been an input-only contact as documented for TE0300-01.

Connector J4 has not been changed.

#### LED

With TE0300-00, the LED is lit when the U_LED line on pin T15 is set high whereas with TE0300-01 the LED is lit when the U_LED line on pin R10 is set high.

## **Ordering Information**

For the latest product details and available options, please visit:

www.trenz-electronic.de

shop.trenz-electronic.de

# **Revision History**

Rev	Date	Who	Description
0.1	2008-04-24	FDR	created
1.0	2008-08-01	FDR	completed
1.01	2008-08-08	Π	50MHz to 125MHz clock
1.02	2008-10-17	FDR	U_LED for TE0300-00
1.03	2008-10-17	FDR	updated FUT from 1.9 to 2.6
1.04	2008-10-27	FDR	DIP switches overview
1.05	2008-10-29	FDR	stacking height

Rev	Date	Who	Description
1.06	2008-12-08	FDR	DIP switches revised
1.07	2009-02-16	FDR	fixed DIP switches overview picture
1.08	2009-03-09	FDR	clarified warning regarding 3.3 V power-rail
1.09	2009-03-16	FDR	fixed and improved switch settings
1.10	2009-06-03	FDR	added "FWU File Generation" sec- tion
1.11	2009-07-23	FDR	clarified changes/LED section
1.12	2009-08-24	FDR	added FPGA signal details for main user signals
1.13	2009-09-01	FDR	improved "On- board Memories" chapter
1.14	2009-09-03	FDR	improved clock, memory and con- figuration chapters

Table 17: revision history.

### **Appendix**

The following tables reports pin-out information of B2B (board-to-board) receptacle connectors J4 and J5 respectively.

mim	B2B	<b>FPGA</b>	FPGA	ba	d :	sup	di	di	sup	di	ba	FPGA	FPGA	B2B	
pin	name	pin	name	nk	air	ply	ff	ff	ply	аг	nk	name	pin	name	pin
1	VccIO	-	VccO	0	Ι	-	-	-	-	Ι	0	VccO		VccIO	2
3	VccIO	-	VccO	0	Ι	-	-	-	-	Ι	0	VccO	-	VccIO	4
5	B3_L01_P	C1	IO_L01P	3	IO	3.3 V	Υ	Υ	3.3 V	IO	3	IO_L07P	G6	B3_L07_P	6
7	B3_L01_N	C2	IO_L01N	3	IO	3.3 V	Υ	Υ	3.3 V	IO	3	IO_L07N	G5	B3_L07_N	8
9	B3_L02_P	D1	IO_L02P	3	IO	3.3 V	Υ	Υ	3.3 V	IO	3	IO_L03N	E1	B3_L03_N	10
11	B3_L02_N	D2	IO_L02N / VREF	3	IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L03P	E2	B3_L03_P	12
13	GND													GND	14
15	B0 IO C3	C3	IO L25P	0	IO	VccIO	Ν	Υ	VccIO	IO	0	IO L19 P	F7	B0 L19 P	16
17	B0_L24_N	B4	IO_L24_N	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L19N / VREF	E7	B0_L19_N	18
19	B0 L24 P	A4	IO L24P	0	IO	VccIO	Y	Υ	VccIO	IO	0	IO L21N	E6	B0 L21 N	20
21	B0_IO_C4	C4	ĪO	0	IO	VccIO	Ν	Υ	VccIO	IO	0	IO_L21P	D6	B0_L21_P	22
23	GND													GND	24
25	B0_L23_N	D5	IO_L23N / VREF	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L18N / VREF	D7	B0_L18_N	26
27	B0_L23_P	C5	IO_L23P	0	IO	VccIO	Υ	Υ	VccIO	IO	0	IO_L18P	C7	B0_L18_P	28
29	B0_L20_P	B6	IO_L20P	0	ΙΟ	VccIO	Υ	Υ	VccIO	IO	0	IO_L17N	F8	B0_L17_N	30
31	B0_L20_N	A6	IO_L20N	0	ΙΟ	VccIO	Υ	Υ	VccIO	IO	0	IO_L17P	E8	B0_L17_P	32
33	3.3 V													3.3 V	34
35	B0_IO_A7	A7	IO	0	IO	VccIO	Ν	Ν	VccIO	IO	0	IO	A8	B0_IO_A8	36
37	B0_IO_G9	G9	IO	0	IO	VccIO	Ν	Y	VccIO	IO	0	IO_L14N / GCLK11	D9	GCLK_L14_N	38
39	GCLK_L13_P	B8	IP_L13P / GCLK8	0	Ι	VccIO	Y	Y	VccIO	IO	0	IO_L14P / GCLK10	C9	GCLK_L14_P	40
41	GCLK_L13_N	B9	IP_L13N / GCLK9	0	Ι	VccIO	Y	Y	VccIO	IO	0	IO_L11N / GCLK5	E10	GCLK_L11_N	42
43	GND							Y	VccIO	IO	0	IO_L11P / GCLK4	D10	GCLK_L11_P	44
45	GCLK_L12_P	B10	IO_L12P / GCLK6	0	IO	VccIO	Y							GND	46
47	GCLK_L12_N	A10	IO_L12N / GCLK7	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L09N	D11	B0_L09_N	48
49	B0_L15_P	E9	IO_L15P	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L09P	C11	B0_L09_P	50
51	B0_L15_N	F9	IO_L15N	0	IO	VccIO	Y	Ν	VccIO	IO	0	IO	A11	B0_I0_A11	52
53	2.5 V													2.5 V	54
55	B0_L08_P	E11	IO_L08P	0	IO	VccIO	Y	Ν	VccIO	IO	0	IO/VREF	B11	B0_IO_B11	56
57	B0_L08_N	F11	IO_L08P	0	IO	VccIO	Y	Ν	VccIO	IO	0	IO	A12	B0_IO_A12	58
59	B0_L05_P	A13	IO_L05P	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L06P	F12	B0_L06_P	60
61	B0_L05_N	B13	IO_L05N / VREF	0	IO	VccIO	Y	Y	VccIO	IO	0	IO_L06N	E12	B0_L06_N	62
63	GND													GND	64
65	B0_L04_N	A14	IO_L04N	0	IO	VccIO	Y	Ν	VccIO	IO	0	IO	D13	B0_I0_D13	66
67	B0_L04_P	B14	IO_L04P	0	IO	VccIO	Y	Ν	VccIO	IO	0	IO	E13	B0_I0_E13	68
69	B0_L03_N	C14	IO_L03N / VREF	0	IO	VccIO	Y		3.3 V	Ι	2	TDI	A2	TDI	70
71	B0_L03_P	D14	IO_L03P	0	IO	VccIO	Υ		3.3 V	0	2	TDO	C16	TDO	72
73	1.2 V													1.2 V	74
75	B0_L01_N	A16	IO_L01N	0	IO	VccIO	Υ		3.3 V	Ι	2	TCK	A17	TCK	76
77	B0_L01_P	B16	IO_L01P	0	IO	VccIO	Υ		3.3 V	Ι	2	TMS	D15	TMS	78
79	GND													GND	80

receptacle connector J4 pinout information

mim	B2B	FPGA	FPGA	ba	d :	sup	di	di	sup	din	ba	FPGA	FPGA	B2B	
pin	name	pin	name	nk	air	ply	ff	ff	ply	air	nk	name	pin	name	pin
1	5Vb2b				Ι					Ι				5Vb2b	2
3	5Vb2b				Ι					Ι				5Vb2b	4
5	5V				0					Ι				/MR	6
7	B2B D P				IO		Υ			0				/RESET	8
9	B2B D N				IO		Υ			0				RESET	10
11	GND													GND	12
13	B3 L22 P	P3	IO L22P	3	IO	3.3 V	Y	Ν	3.3 V	IO	3	IO L24P	T2	B3 IO T2	14
15	B3 L22 N	P4	IO L22N	3	IO	3.3 V	Υ	Y	3.3 V	IO	3	IO L21N	P1	B3 L21 N	16
17	B2 IP V4	V4	IP LO2P	2	Ι	3.3 V	Ν	Y	3.3 V	IO	3	IO L21P	P2	B3 L21 P	18
19	B3 L20 P	N4	IO L20P	3	IO	3.3 V	Y	Ý	3.3 V	IO	3	IO L23N	R2	B3 L23 N	20
21	B3 L20 N	N5	IO L20N	3	IO	3.3 V	Υ	Y	3.3 V	IO	3	IO L23P	R3	B3 L23 P	22
23	GND													GND	24
25	B2 L04 N	T5	IO L04N	2	IO	3.3 V	Y	Ν	3.3 V	IO	3	IO L18N	M3	B3 IO L18N	26
												IO LO3P			
27	B2 L04 P	R5	IO LO4P	2	IO	3.3 V	Y	Ν	3.3 V	IO	2	/ DOUT /	U4	B2 IO L03	28
		_										BUSY			
20		DC		2	10	2 2 4	v		2 2 4	10	2	IO			20
29	B2_L05_P	ко	10_L05P	2	10	3.3 V	Ŷ	IN	3.3 V	10	2	/ VREF	05	B2_I0_05	30
31	B2_L05_N	P6	IO_L05N	2	IO	3.3 V	Υ	Υ	3.3 V	IO	2	IO_L06P	V5	B2_L06_P	32
22			το	h	τO	2 2 1	N	v	2 2 1/	τO	2	IO_L06N	NG		24
55	DZ_IO_V7	V /	10	2	10	5.5 V	IN	T	5.5 V	10	2	/ VREF	vo	DZ_LUO_N	54
35	3.3 V													3.3 V	36
37	B2_L07_N	P7	IO_L07N	2	IO	3.3 V	Y	Ν	3.3 V	IO	2	IO	U6	B2_IO_U6	38
30		NZ		2	τO	2 2 V	v	v	2 2 1/	τO	2	IO_L17N	15	B3 117 N	10
55	D2_L07_F	117	10_1071	2	10	5.5 V	'	'	5.5 V	10	5	/ VREF	LJ	DJ_L1/_N	40
			IO_L12N												
41	B2_GCLK12	M9	/ D6 /	2	Ι	3.3 V	Ν	Y	3.3 V	IO	3	IO_L17P	L6	B3_L17_P	42
			GCLK12												
43	GND													GND	44
45	B2_L10_N	T8	IO_L10N	2	IO	3.3 V	Y	Ν	3.3 V	I	2	IP_L08P	T7	B2_IP_T7	46
47	B2_L10_P	R8	IO_L10P	2	IO	3.3 V	Y	Ν	3.3 V	I	2	IP_L11P	U8	B2_IP_U8	48
			IO_L13N												
49	B2_GCLK_L13_N	V9	/ D3 /	2	IO	3.3 V	Y	Y	3.3 V	IO	3	IO_L19P	M5	B3_L19_P	50
			GCLK15												
			IO_L13P	_							_				
51	B2_GCLK_L13_P	09	/ D4 /	2	10	3.3 V	Y	Y	3.3 V	10	3	10_L19N	M6	B3_L19_N	52
50	2 5 1		GCLK14			2 2 1								2 5 1	<b>F</b> 4
53	2.5 V			2	10	3.3 V	V	V	2 2 4	10	~		DO	2.5 V	54
55	B2_L18_N	NII	10_L18N	2	10	3.3 V	Y	Y	3.3 V	10	2	10_L09P	P8	B2_L09_P	56
5/	B2_L18_P	P11	10_L18P	2	10	3.3 V	Y	Y	3.3 V	10	2	10_L09N	N8	B2_L09_N	58
59	B2_L20_N	R12	10_L20N	2	10	3.3 V	Y	N	3.3 V	10	2	10	P9	B2_IO_P9	60
61	B2_L20_P	112	10_L20P	2	10	3.3 V	Y	N	3.3 V	10	2	10	R11	B2_I0_R11	62
63	GND													GND	64
65			IO L19N	~	10						_	10_L15N	54.0		~ ~
65	B2_L19_N	V13	/ VREF	2	10	3.3 V	Y	N	3.3 V	10	2	/ D1 /	P10	B2_IO_P10	66
												GCLK3			
67	B2 L19 P	V12	IO L19P	2	IO	3.3 V	Y	Ν	3.3 V	IO	2		R9	B2 IO R9	68
												/ D5			
69	B2_L22_N	R13	10_L22N	2	IO	3.3 V	Υ	Υ	3.3 V	IO	2	IO_L21N	P12	B2_L21_N	70
															-
71	B2_L22_P	P13	10_L22P	2	IO	3.3 V	Υ	Υ	3.3 V	IO	2	IO_L21P	N12	B2_L21_P	72
70	1 2 1/		/ AZ3									_		1 2 1/	74
/3	1.2 V				<u> </u>									1.2 V	/4
75	B2_L24_P	T14	10_L24P	2	IO	3.3 V	Y	Ν	3.3 V	Ι	2	IP_L23P	V14	B2_IP_V14	76
															-
77	B2_L24_N	R14	/ A20	2	IO	3.3 V	Y	Ν	3.3 V	IO	2	IO	U13	B2_IO_U13	78
70	GND		/ 720								-			CND	80
13	GND	1	1	1	1	1			1	1	1		1		00

receptacle connector J5 pinout information