Start Here Guide For FPGA Advantage

Software Version 8.2

October 28, 2008

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FPGA Advantage 8.2

FPGA Advantage 8.2 integrates the following tools:

- Design entry and management: HDL Designer Series 2008.1

- HDL simulation: Model*Sim* 6.4a

- HDL synthesis: LeonardoSpectrum 2008a and/or Precision Synthesis 2008a.

Refer to the separate HDL Designer Series, Model*Sim*, LeonardoSpectrum and Precision Synthesis release notes for information about problems fixed in the latest versions of these tools.

FPGA Advantage 8.1

FPGA Advantage 8.1 integrates the following tools:

- Design entry and management: HDL Designer Series 2007.1

- HDL simulation: Model*Sim* 6.3a

- HDL synthesis: LeonardoSpectrum 2007a and/or Precision Synthesis 2006a Update 2.

Refer to the separate HDL Designer Series, Model*Sim*, LeonardoSpectrum and Precision Synthesis release notes for information about problems fixed in the latest versions of these tools.

FPGA Advantage 7.3

FPGA Advantage 7.3 integrates the following tools:

- Design entry and management: HDL Designer Series 2006.1

- HDL simulation: Model*Sim* 6.2d

- HDL synthesis: LeonardoSpectrum 2006a and/or Precision Synthesis 2006a Update 1.

Refer to the separate HDL Designer Series, Model*Sim*, LeonardoSpectrum and Precision Synthesis release notes for information about problems fixed in the latest versions of these tools.

FPGA Advantage 7.2

FPGA Advantage 7.2 integrates the following tools:

- Design entry and management: HDL Designer Series 2005.3

- HDL simulation: Model*Sim* 6.1c

- HDL synthesis: LeonardoSpectrum 2005b and/or Precision Synthesis 2005b Update 1.

Refer to the separate HDL Designer Series, Model*Sim*, LeonardoSpectrum and Precision Synthesis release notes for information about problems fixed in the latest versions of these tools.

FPGA Advantage 7.1

FPGA Advantage 7.1 integrates the following tools:

- Design entry and management: HDL Designer Series 2005.1b

- HDL simulation: Model*Sim* 6.1a

- HDL synthesis: LeonardoSpectrum 2005a Update1 and/or Precision Synthesis 2005a Update2.

Refer to the separate HDL Designer Series, Model*Sim*, LeonardoSpectrum and Precision Synthesis release notes for information about problems fixed in the latest versions of these tools.

FPGA Advantage 7.0

FPGA Advantage 7.0 integrates the following tools:

- Design entry and management: HDL Designer Series 2004.1b

- HDL simulation: Model*Sim* 6.0c

- HDL synthesis: LeonardoSpectrum 2004b Update1 and/or Precision Synthesis 2004c Update1.

FPGA Advantage 6.3

FPGA Advantage 6.3 integrates the following tools:

- Design entry and management: HDL Designer Series 2004.1

- HDL simulation: Model*Sim* 5.8c

- HDL synthesis: LeonardoSpectrum 2004a Update1 and/or Precision Synthesis 2003c Update1.

The following defect reported against FPGA Advantage has been fixed in this release:

CQ**168924** Link to the Quick Reference Index was missing for FPGA Advantage

For clarity, the prefix *CQ* represents the ClearQuest database prefix *dts01* and other leading zeros are omitted.

FPGA Advantage 6.2

FPGA Advantage 6.2 integrated the following tools:

- Design entry and management: HDL Designer Series 2003.2

- HDL simulation: Model*Sim* 5.7f

- HDL synthesis: LeonardoSpectrum 2003b and/or Precision Synthesis 2003b Update1.

The following defects reported against FPGA Advantage were fixed in this release:

CQ**087694** Install instructions for Netscape users added to HTML page

CQ**129079** Icon in the Add/Remove Programs dialog appeared randomly

CQ**129142** Change install to include new configurations

FPGA Advantage 6.1

The FPGA Advantage 6.1 release included configurations containing either or both of the Precision Synthesis and LeonardoSpectrum synthesis tools.

FPGA Advantage 6.1 comprised:

- Design entry and management: HDL Designer Series 2003.1

- HDL simulation: Model*Sim* 5.7d PE or SE

- HDL synthesis: LeonardoSpectrum 2003a and/or Precision Synthesis 2003a

The following defects were fixed in the FPGA Advantage 6.1 release.

SC**327452** Run Place & Route button should be added to the Precision setup

SC**338781** Inappropriate shortcuts in start menu

SC**338355** Internal assertion on bus move

SC**340011** Provide shortcuts to FLEXlm and MTI license manager

The defects in the above list refer to the Scopus defect tracking system. Scopus defects can also be accessed in the ClearQuest system by using the Prompt Old Defect public query. For example, entering Scopus defect SC340011 returns the ClearQuest defect dts0100106837.

FPGA Advantage 6.0

The FPGA Advantage 6.0 release included the new Precision Synthesis tool in place of the LeonardoSpectrum synthesis tool which was included in previous releases of the software.

FPGA Advantage 6.0 comprised:

- Design entry and management: HDL Designer Series 2002.1b

- HDL simulation: Model*Sim* 5.6d

- HDL synthesis: Precision Synthesis 2002b

The following defects were fixed in FPGA Advantage 6.0.

SC**308980** VHDL code example added to the tutorial flow

SC**309786** Note added about unsetting MODEL_TECH to resolve licensing issues

SC**329401** ModelSim evaluation files not deleted when full product is installed

Chapter 1
Introduction

This chapter is an introduction to the FPGA Advantage products including content, configuration and licensing information.

Product Configurations

FPGA Advantage is an integrated set of tools supporting VHDL or Verilog design flows including design capture and design management, through simulation to synthesis.

All FPGA Advantage products are based on a HDL Designer Series design capture and management tool integrated with a Model*Sim* simulator and Precision Synthesis or LeonardoSpectrum synthesis tools.

UNIX and Linux Platforms' Configurations

When you install FPGA Advantage 8.2 on Unix or Linux platforms, you are prompted to choose the HDL Designer Series licensed configuration to be either HDL Designer or HDL Author. Depending on your platform you are then prompted to choose one of the following configurations:

Solaris & Linux

   o   FPGA Advantage with Model*Sim* SE & Precision RTL Synthesis

   o   FPGA Advantage with Model*Sim* SE & Precision Physical Synthesis

Linux Only

- o FPGA Advantage with Model*S*im LE & Precision RTL Synthesis

- o FPGA Advantage with Model*S*im LE & Precision Physical Synthesis

Solaris Only

- o FPGA Advantage with Model*S*im SE, LeonardoSpectrum & Precision RTL Synthesis

- o FPGA Advantage with Model*S*im SE, LeonardoSpectrum & Precision Physical Synthesis

- o FPGA Advantage with Model*S*im SE & LeonardoSpectrum

The UNIX invoke scripts can be accessed in the *<install_path>/Fpgadv/bin/* directory. For example:

```
<install_path>/Fpgadv/bin/fa_with_ps
```

Windows Platform Configurations

The installation process of FPGA Advantage 8.2 on a Windows platform allows you to specify the licensed configuration of HDL Designer Series as either HDL Designer or HDL Author.

You then specify your simulation tool by choosing to install either Model*S*im SE or Model*S*im PE.

The last step is to specify your synthesis tool. You can choose to install one or more of the following tools:

- Precision RTL Synthesis

- Precision Physical Synthesis

- Leonardo Spectrum

Invoke shortcuts for the Windows configurations are available in the Windows **Start** menu and from shortcuts created on your desktop.

Refer to the *Start Here Guide for the HDL Designer Series* for more information about the HDL Designer and HDL Author tools.

System Requirements

All tools can be run on Microsoft Windows XP and Red Hat Enterprise Linux 4 except Leonardo.

All tools can run on Solaris 9 - Leonardo is not officially supported on 9 but it still can run on it.

UNIX

The table below shows the system requirements for installing FPGA Advantage on UNIX workstations:

Operating System	Sun UltraSPARC or Blade workstation running Solaris 8.
Memory (minimum)	512MByte of RAM; large designs will require more memory.
Disk space	Program files require approximately 1800MByte of disk space (HDS, 500MByte; Model*Sim*, 350MByte; Precision Synthesis, 600MByte; LeonardoSpectrum, 300MByte; Docs 3MByte).

It is recommended that the latest operating system patches should be installed.

Solaris workstations should also have the latest recommended J2SE patch bundle for the Java Runtime Environment (JRE).

Information about Solaris patches is available from Sun customer support or from the SunSolve Online Public Patch Access web site at:

http://sunsolve.sun.com/pubpatch/

Linux

The table below shows the system requirements for installing FPGA Advantage on Linux workstations:

Operating System	Red Hat Enterprise Linux 3
Memory (minimum)	512MByte of RAM; large designs may require more memory.
Disk space	Program files require approximately 1450MByte of disk space (HDS, 450MByte; Model*Sim,* 350MByte; Precision Synthesis, 600MByte; Docs 3MByte).

Windows

The table below shows the system requirements for installing FPGA Advantage on Windows workstations:

Operating system	Microsoft Windows 2000 or XP.
Memory (minimum)	512MByte of RAM and 8MByte of VRAM; large designs may require more memory.
Monitor	A 17-inch monitor is recommended and should be set to 64K colors at resolution 1024x768 or 1280x1024.
Disk space	Program files require approximately 1600MByte of disk space (HDS, 500MByte; Model*Sim*, 300MByte; Precision Synthesis, 450MByte; LeonardoSpectrum, 300MByte; Docs, 3MByte).

TCP/IP networking must be enabled in the Windows control panel and you should set your monitor display properties to use the maximum number of colors. You are advised to use small fonts and the maximum desktop area.

Licensing FPGA Advantage

FPGA Advantage licensing is based on the Macrovision FLEXlm license manager and supports the PCLS and MGLS versions of FLEXlm normally used for Mentor Graphics Corporation (MGC) products.

The licensing software is installed automatically when you install FPGA Advantage. Users upgrading from a previous release and using server based licensing should upgrade their server license to FLEXIm 10.8.

If you have floating licenses on an existing server, you may need to add new license keys to the license file on the server, and then re-read the license file.

If you have new nodelocked uncounted licenses, you will need to add them to your local license file.

License File Location

The LM_LICENSE_FILE environment variable is used to specify the location of the license file.

Thus, LM_LICENSE_FILE can be used by applications that use standard FLEXlm licensing.

These settings are search paths and can be set to multiple locations by entering multiple pathnames or port specifications (separated by a colon on UNIX and Linux or by a semi-colon on Windows). For example:

1700@mylichost:/usr/opt/license.dat (UNIX or Linux)
1700@mylichost;C:\license.dat;C:\hds\license.dat (Windows).

You can check the variable and registry settings on Windows by using the **PCLS_OK** utility which can be accessed from the **Licensing** cascade for **FPGA Advantage** in the **Programs** section of your Windows **Start** menu.

Using a Hardware Security Key

Licensing can be locked to a hardware identifier provided by a FLEXid hardware security key.

It can be used for nodelocked licenses, or to identify a license server for floating licenses.

The driver for the hardware key is normally loaded during installation. It can be checked using the **LMTOOLS** utility which can be accessed from the **Licensing** cascade for **FPGA Advantage** in the **Programs** section of your Windows **Start** menu.

Further Licensing Information

Detailed information about the Mentor Graphics Licensing System (MGLS) is given in the *Licensing Mentor Graphics Software* manual which is available in the Precision Synthesis or LeonardoSpectrum bookcases. These bookcases also include a copy of the *FLEXlm End Users Guide*.

Both manuals are also available in the *release_documents* directory on the FPGA Advantage CD-ROM or from the Mentor Graphics SupportNet web site:

http://www.mentor.com/supportnet

For more information about *FLEXlm*, visit the Macrovision Corporation web site at:

http://www.macrovision.com

Migrating from pre-6.1 FPGA Advantage

The FPGA Advantage install program provides eight install options on Windows, four on UNIX and two on Linux.

These options support the various combinations of HDL Designer, HDL Author, ModelSim SE, ModelSim PE, LeonardoSpectrum, Precision RTL Synthesis and Precision Physical Synthesis.

If you are migrating from a pre-6.1 version of FPGA Advantage (or from a pre-2003.1 HDL Designer Series tool), your existing license may enable old HDL Designer Series configurations that have been superseded in the latest versions:

Old HDL Designer Configuration	License	New Configuration
HDL Author - Text	hdlauthortxt	N/A
HDL Author - Graphics	hdlauthorgfx	N/A
HDL Author - Pro	hdlauthorpro	HDL Author
HDL Designer - Text	hdldesignertxt	N/A
HDL Designer - Graphics	hdldesignergfx	N/A
HDL Designer - Pro	hdldesignerpro	HDL Designer

The Text and Graphics configurations have been discontinued from the 2003.1 release of HDL Designer Series. Users who have previously installed FPGA Advantage which included either the Text or Graphics configuration must select the corresponding pre-2003.1 install option to ensure that they can continue using the existing licenses.

Note that the HDL Designer - Pro configuration was renamed HDL Designer and similarly, HDL Author - Pro was renamed HDL Author. There are no changes to the license features for these configurations.

The install program will then create the correct shortcuts on Windows or invocation scripts on UNIX and Linux.

For example, if you have a *hdldesignergfx* license, select **HDL Designer - Graphics** in the license selection page during installation. This will add a **-graphics** switch in the shortcut or invoke script.

The following table shows which switch will be added when the HDL Designer configuration is selected:

HDL Designer Configuration	License	Invocation Argument
HDL Author - Text	hdlauthortxt	-authortext
HDL Author - Graphics	hdlauthorgfx	-authorgraphics
HDL Author - Pro	hdlauthorpro	-authorpro
HDL Designer - Text	hdldesignertxt	-text
HDL Designer - Graphics	hdldesignergfx	-graphics
HDL Designer - Pro	hdldesignerpro	none

Preferences and Design Migration

If you are updating from a previous version of FPGA Advantage, your HDL Designer Series preferences, library mapping and design libraries will be migrated for use with this release.

However, if you have used Model*Sim*, LeonardoSpectrum or Precision Synthesis downstream tools in a previous HDL Designer Series or FPGA Advantage installation, the old downstream tool locations are preserved in your preferences and will need to be manually updated.

The table below shows the default paths to the executables for each of the downstream tools used with FPGA Advantage:

Tool	Default Path
Model*Sim* SE	$HDS_HOME/../Modeltech/win32
Model*Sim* PE	$HDS_HOME/../Modeltech/win32pe
LeonardoSpectrum	$HDS_HOME/../Exemplar/bin/win32
Precision RTL or Physical Synthesis	$HDS_HOME/../Precision/Mgc_home/bin

Note that the paths for Precision RTL Synthesis and Precision Physical Synthesis are identical. The required synthesis tool is determined automatically from the license features available when it is invoked.

Please refer to the "Updating from a Previous Release" section in the *Transition Guide for the HDL Designer Series* for more information about migrating designs.

Inventra Intellectual Property

FPGA Advantage users can download Inventra Intellectual Property (IP) models for free evaluation. For more information, see the Inventra web site at:

http://www.mentor.com/inventra

Chapter 2
Documentation

This chapter provides information about the documentation available for FPGA Advantage and its constituent tools.

Locating Documentation

Documentation for HDL Designer Series, Model*Sim*, LeonardoSpectrum and Precision Synthesis is available from the **Help** menu within each application.

All documents are provided in Adobe Acrobat portable document format (PDF). No hardcopy documentation is provided. However, any Acrobat PDF document can be printed out for your own personal use if a printer is available.

Note

In case of HDL Designer Series, documents are provided in PDF and HTML format as well. The documents can be accessed through the HDS InfoHub which is opened by clicking **Help and Manuals** from the **Help** menu.

This also applies to Model*Sim* which has an InfoHub including both PDF and HTML versions of documents, in addition to a separate bookcase including PDF versions only of documents. Both the Model*Sim* InfoHub and Bookcase can be accessed through the **Help** menu of Model*Sim*.

In addition, you can access this Start Here Guide and the *FPGA Advantage Tutorial* from the *FPGA Advantage Bookcase* in the HDL Designer Series **Help** menu.

Windows users can also access this bookcase by choosing **Bookcase** from the **FPGA Advantage** cascade in the **Programs** section of the Windows **Start** menu.

UNIX users can access the FPGA Advantage Bookcase by using the Adobe Acrobat reader to open the file: *<install_dir>/Doc/docindex.pdf*

Release Notes

Detailed information about the tools comprising this FPGA Advantage release is given in the release notes for each tool. The release notes are available in the documentation bookcase for each tool - or in the InfoHub in case of HDL Designer Series and Model*Sim* - or from the **Design**, **Simulation** and **Synthesis** cascades from the Windows **Start** menu.

For example, to view release notes for HDL Designer Series, choose:
Start > Programs > FPGA Advantage 8.2 > Design > Release Notes

UNIX users can locate the release notes for each tool by exploring the install directory structure.

The location of documentation in this structure is shown below:
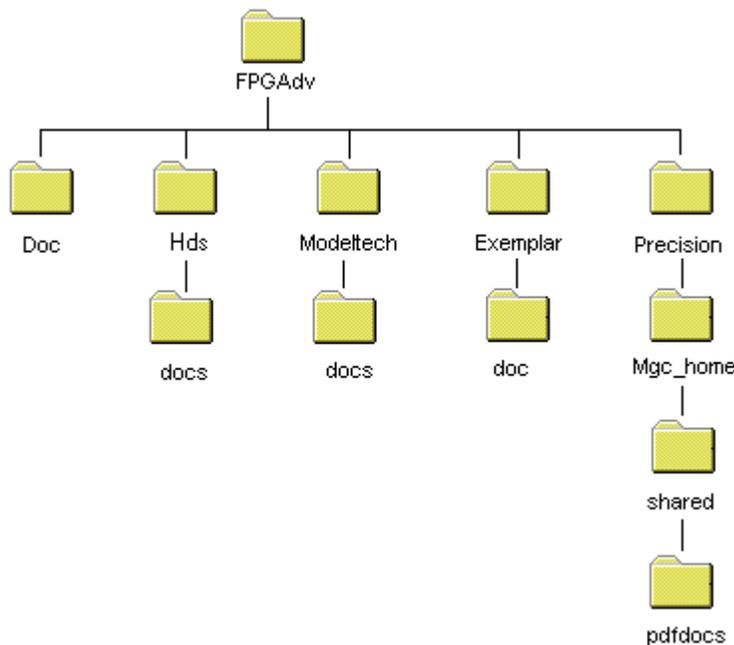
The documents specific to FPGA Advantage are in the top level *Doc* subdirectory. Documents for HDS, LeonardoSpectrum (Exemplar) and Precision are in the *docs*, *doc* and *pdfdocs* subdirectories respectively. The current Model*Sim* release notes (in HTML and plain text format) are in the *Modeltech* subdirectory with all other Model*Sim* documents (including an archive of previous release notes) in a *docs* subdirectory.

Tutorials

All users should perform the *FPGA Advantage Tutorial* which is available from the *FPGA Advantage Bookcase*.

The following HDL Designer Series tutorials are also available:

- The *Interface-Based Design Tutorial* is an introduction to interface-based design (IBD) which uses HDL import, tabular IO, an IBD view and ModuleWare parts to capture a VHDL or Verilog text design. Simulation and synthesis design flows are illustrated using the Model*Sim* and LeonardoSpectrum tools.

- The *Design Exploration Tutorial* is an introduction to the **HDL Detective** tool. This tutorial shows how this tool can be used to import an existing VHDL or Verilog text design, visualize the design using graphical views and export these views in HTML format.

- The *DesignChecker Tutorial* is an introduction to the **DesignChecker** tool. This tutorial shows how to configure DesignChecker settings, analyze a design, and investigate the analysis results.

- The *SystemVerilog for AVM 2.0 and QuestaSim 6.2g* and *SystemVerilog for AVM 3.0 and QuestaSim 6.3*.

You can learn more about using Model*Sim* by performing the *ModelSim SE Tutorial* or the *ModelSim LE/PE Tutorial*.

> **Note**
>
> The *ModelSim PE Tutorial* is available if you have installed one of the FPGA Advantage Personal configurations. The *ModelSim SE Tutorial* is available in all other configurations.

User Manuals

General user procedures for using the HDL Designer Series are described in the *HDL Designer Series User Manual*.

Additional procedures for using the symbol, tabular IO, block diagram, IBD view, flow chart and truth table editors are described in the *HDL Designer Series Graphical Editors User Manual*.

Procedures for using the state diagram and algorithmic state machine editors are described in the *State Machine Editors User Manual*.

Procedures for using the integrated **DesignPad** HDL text editor are described in the *DesignPad Text Editor User Guide.*

Procedures for using Model*Sim* are given in the *ModelSim SE User's Manual* or *ModelSim LE/PE User's Manual*.

Procedures for using LeonardoSpectrum are given in the *LeonardoSpectrum User's Manual*.

Procedures for using Precision RTL Synthesis are given in the *Precision RTL Synthesis User's Manual*.

Procedures for using Precision Physical Synthesis are given in the *Precision Physical Synthesis User's Manual*.

Using the Bookcase Search

The FPGA Advantage Bookcase allows you to attach document indexes which allow you to perform a full text search through all of the available documentation.

This facility is available if you have installed the Adobe Acrobat Reader with search capabilities. The latest version of the Acrobat Reader can be obtained from the Adobe web site at:

http://www.adobe.com/products/acrobat/readstep2.html

Attaching Document Indexes

The following indexes should be available in the *<install_path>/Doc* directory of the FPGA Advantage installation:

fpga_index.pdx   FPGA Advantage documents

ls_index.pdx   LeonardoSpectrum documents

ps_index.pdx   Precision Synthesis documents

> **Note**
>
> For information on how to search the HDL Designer Series and Model*Sim* documentation, refer to "Using the InfoHub Search" on page 24.

Some of these indexes may already be available in the dialog box. However, you may need to add or remove indexes for the FPGA Advantage configuration you wish to use. For example, you will typically want only one of the LeonardoSpectrum and Precision Synthesis indexes.

If you are using Acrobat 6.0, you can attach a document index by choosing **Search** from the **Edit** menu to display the Search PDF window and selecting **Use Advanced Search Options**.
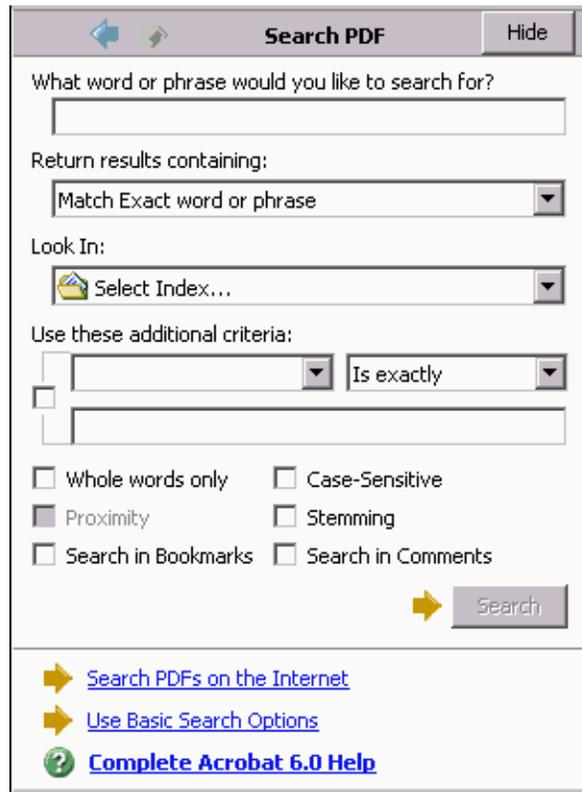
Choose *Select Index* from the Look In dropdown list to display the Index Selection dialog box.

If you are using Acrobat 5.0, you can display the **Index Selection** dialog box directly by choosing **Select Indexes** from the **Search** cascade in the Acrobat Reader **Edit** menu. You can use the **Add** button to browse for additional indexes or the **Remove** button to remove an index. The attached indexes are automatically loaded the next time that you use the Acrobat Reader.
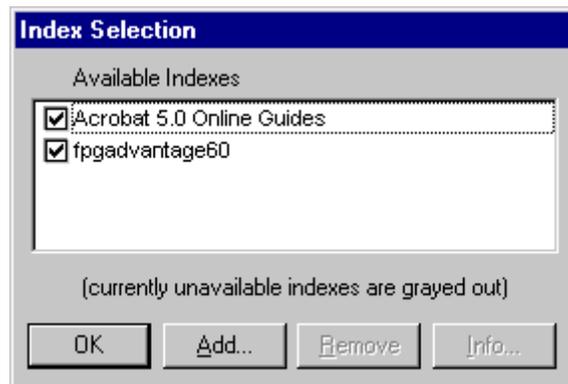
Search Tips

If you are using Acrobat 6.0, you can perform a bookcase search by selecting *Currently Selected Indexes* from the Look In dropdown list of the Search PDF window. Then, enter a search string, select one or more options and use the [Search] button.

The search results are displayed in the Search PDF window which also provides options to sort by relevance ranking, date modified, filename or location. You can double-click on a search result to display the corresponding document.

If you are using Acrobat 5.0, you can search the attached indexes by clicking **Search** in the FPGA Advantage Documentation Bookcase (or by choosing **Query** from the **Search** cascade of the Acrobat Reader **Edit** menu) to display the Adobe Acrobat Search dialog box:
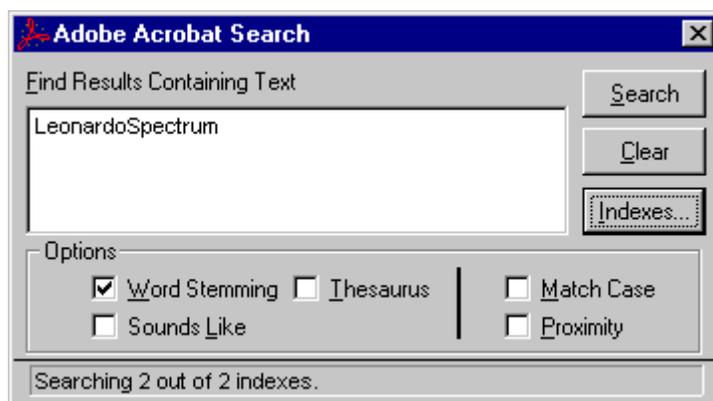
Enter a search string, select one or more options and use the [Search] button.

The Search Results dialog box displays the results of the search with an indication of their relevance:
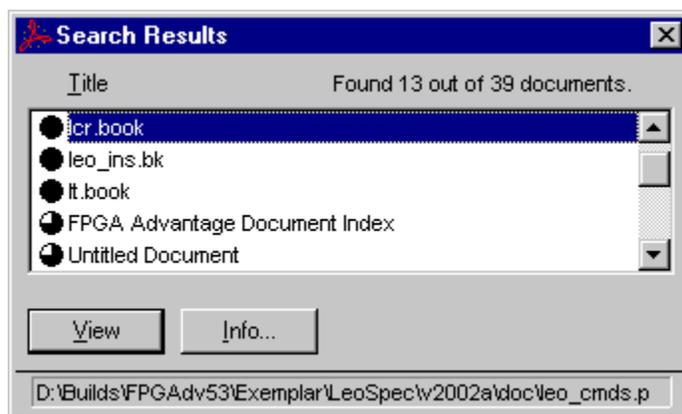
You can double-click on a search result or use the [View] button to display the document or use the [Info...] button to display information about the corresponding document.

For information about search options, search relevance and refining searches, refer to the online help for your version of the Acrobat Reader.

Using the InfoHub Search

HDL Designer Series and Model*Sim* have an InfoHub which provides documentation in both HTML and PDF versions. A documentation search can be run through the InfoHub itself. To open the InfoHub, select **Help and Manuals** from the **Help** menu.
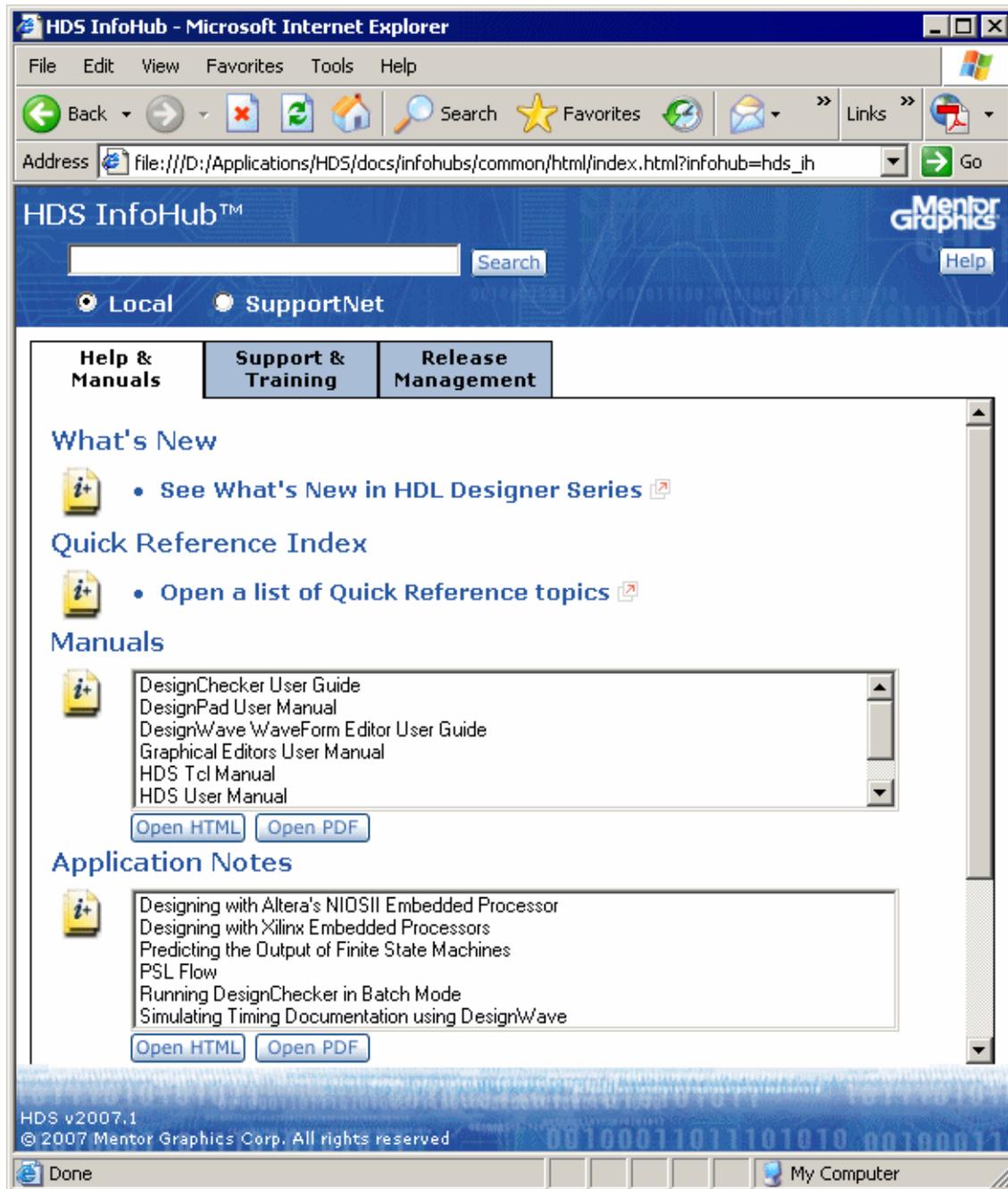
There are two search tools embedded in the InfoHub:

- A keyword search of locally installed HTML content.

- A comprehensive, natural language search of SupportNet that includes all documentation, release notes, technical notes, and application notes.

The following search methods can be performed through the InfoHub:

- **Searching a Single HTML Document** — this takes place by opening a specific HTML document and running a search through the Search tab in the navigation pane.

- **Searching a Single PDF Document** — this takes place by opening a specific PDF document and running a search through the Acrobat Reader.

- **Searching the Entire HTML Library from a Document** — this takes place by opening any HTML document, selecting the HDS/ModelSim Online Library option in the Search tab and then running a search.

- **Searching the Entire HTML Library from the InfoHub** — this takes place by opening the InfoHub and running a local search in the banner text box.

- **Searching SupportNet** — the SupportNet can be searched through the InfoHub banner text box, through the Support and Training tab in the InfoHub, or through the Search tab of an opened HTML document while setting the SupportNet option.

The **Help** button on the right most side of the InfoHub opens an HTML page that provides more details on the above search methods.

Further Information

For the latest information about FPGA Advantage, see the FPGA Advantage web site at:

http://www.mentor.com/fpga-advantage

To go directly to the contacts page visit:

http://www.mentor.com/fpga-advantage/contact_us.html

End-User License Agreement

The latest version of the End-User License Agreement is available on-line at:
www.mentor.com/terms_conditions/enduser.cfm

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15. **CONTROLLING LAW, JURISDICTION AND DISPUTE RESOLUTION.** THIS AGREEMENT SHALL BE GOVERNED BY AND CONSTRUED UNDER THE LAWS OF THE STATE OF OREGON, USA, IF YOU ARE LOCATED IN NORTH OR SOUTH AMERICA, AND THE LAWS OF IRELAND IF YOU ARE LOCATED OUTSIDE OF NORTH OR SOUTH AMERICA. All disputes arising out of or in relation to this Agreement shall be submitted to the exclusive jurisdiction of Portland, Oregon when the laws of Oregon apply, or Dublin, Ireland when the laws of Ireland apply. Notwithstanding the foregoing, all disputes in Asia (except for Japan) arising out of or in relation to this Agreement shall be resolved by arbitration in Singapore before a single arbitrator to be appointed by the Chairman of the Singapore International Arbitration Centre ("SIAC") to be conducted in the English language, in accordance with the Arbitration Rules of the SIAC in effect at the time of the dispute, which rules are deemed to be incorporated by reference in this section 15. This section shall not restrict Mentor Graphics' right to bring an action against you in the jurisdiction where your place of business is located. The United Nations Convention on Contracts for the International Sale of Goods does not apply to this Agreement.

16. **SEVERABILITY.** If any provision of this Agreement is held by a court of competent jurisdiction to be void, invalid, unenforceable or illegal, such provision shall be severed from this Agreement and the remaining provisions will remain in full force and effect.

17. **PAYMENT TERMS AND MISCELLANEOUS.** You will pay amounts invoiced, in the currency specified on the applicable invoice, within 30 days from the date of such invoice. Any past due invoices will be subject to the imposition of interest charges in the amount of one and one-half percent per month or the applicable legal rate currently in effect, whichever is lower. Some Software may contain code distributed under a third party license agreement that may provide additional rights to you. Please see the applicable Software documentation for details. This Agreement may only be modified in writing by authorized representatives of the parties. Waiver of terms or excuse of breach must be in writing and shall not constitute subsequent consent, waiver or excuse.

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