

輕鬆上手Andes 開發板一 ADP-XC7KFF676 使用介紹

Driving Innovations



陳昭伸 台灣晶心科技公司技術經理 Email: jchen@andestech.com

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Agenda



- Product information
- Board introduction
- Program FPGA netlist and system program
- Quick boot up





Product information

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Product Information



- Product Name
 ADP-XC7KFF676
- Release bitmap
 - Support all of Andes core and AG101,AE210 platform IP
 - CPU/AHB/APB clock rate: 30/30/15MHz (N7,N8)

60/30/15 MHz(N9,N10,N12,N13) (N13 CPU clock up to 144MHz)



Product Document



ITEM	Document Number	Revision
Release Note	RN-086	V1.0
Product Brief	RN-081	V1.0
Production Guide	PB-082	V1.0
User Manual	UM-098	V1.0
Quick Start Guide	UM-099	V1.0





Product information

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Function and location







Board of the Feature



- Xilinx Kintex-7 FPGA XC7K160T (L/C :162240, Package:676 speed grade :-1M)
- ✤ 1 GB on-board DDR3 SDRAM (800MHz)
- 128MB on-board NOR flash; 64MB for FPGA configuration, and 64MB for system storage
- ✤ 10/100 Ethernet compatible RJ45 (MII interface)
- DB9 UART port (Null modem cable)
- SD memory card slot
- IDE/GPIOs connector for extension



Board of the Feature



- Support 2W/5W/7W JTAG pins on AICE ports
- ✤ 8 user defined push buttons
- ✤ 3"/7" LCD module connector with RGB interface
- MIC-in, Line-in, and Line-out with AC97 audio codec
- Two 7-segment LED displays
- ✤ SPI Flash ROM (16Mb)
- ✤ I2C EEPROM (128Kb)



Optional device



USB 2.0 OTG port

- ✤ USB 1.1 device port
- ✤ 10/100/1000 Ethernet
- ✤ PCI-E x8 I/F



Leopard vs. Orca



	ADP-XC5FF676 Leopard	ADP-XC7KFF676 Orca
FPAG Capacity/ Logic Cell	110K	160K 💥
FPGA PROM	4MB	64MB 💥
DRAM Size/ Speed	128MB/SDRAM 40MHz	1GB/DDR3 800M 💥
On-board Flash	32MB	64MB 💥
Board to Board Connection	AHB	PCI-E 🔆
AICE Port	1/Fixed Voltage (3.3V)	1/Fixed Voltage+ 1/Multi-Voltage (3.3V, 2.5V, 1.8V) 🦄
Giga Ethernet	No	Yes 🔆
USB 2.0 OTG	No	Yes 💥
USB 1.1 Device	No	Yes 🔆
Push Buttons	5	8 🔆
Adaptive	5V/3A, 2.0mm	12V/5A, 1.7mm





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Xilinx Configuration File Format

File Extension	Xilinx Software Tool	Description
BIT	BitGen (generated by default)	BIT file is a raw storage of the programming bits for the FPGA and can be loaded directly to the FPGA via JTAG using iMPACT.
MCS	PROMGen or iMPACT	.MCS file is what you load into a PROM (non-volatile memory) which stores the programming information.
BIN	BitGen (generated if -g binary:yes option is set) or PROMGen	Binary configuration data file with no header information. Can be used for custom configuration solutions (for example, microprocessors), or in some cases to program third-party PROMs.



PFLASH 128MB









Programing FPGA by Andes Burner



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Programing FPGA by Andes Burner





Programming Tools

✤ Xilinx iMPACT 14.5 以上版本

◆ 安裝 AndeSight[™] STD, AndeSight[™] MCU, or BSP

ADP-XC7KFF676 programming package

- orca.bat (script file)
- orca.cmd (script file for config file)
- isp_ag101p.exe (burner tool)
- burn_fpga.encrypt.bit (FPGA config file)
- ag101_chip.bin (FPGA netlist file)
- Xilinx Platform Cable USB

Andes AICE MCU







- 1. Copy all files in ADP-XC7KFF676 programming package to \Xilinx\14.5\LabTools.
- 2. 連接 Xilinx download Cable to ADP-XC7KFF676 and host PC.
- 3. 開啟ADP-XC7KFF676 的電源並按"PWR_SW1"開關. 電源 LEDs (LED12 to LED17) 需要亮起來.
- 4. 確認Xilinx cable 上的綠燈有亮.



5. 開啟 "ISE Design Suit Command Prompt "from Start → Program → Xilinx Design Tools/Lab Tools 14.5→Accessories.







6. 執行Orca.bat

ex ISE Design Suite Command Prompt	- 🗆 ×
d:\Xilinx\14.5\LabTools>orca.bat_	<u> </u>
	_
I I I I I I I I I I I I I I I I I I I	





7.當出現下圖畫面,表示FPGA config file 燒錄成功.

📾 ISE Design Suite Command Prompt - orca.bat	- 🗆 🗙		
Reading: 43.98 C	_		
1: UCCINT Supply: Current Reading: 1.049 V, Min. Reading: 1.040 V, Max.			
Reading: 1.052 V			
1: VCCAUX Supply: Current Reading: 1.869 V, Min. Reading: 1.860 V, Max.			
Reading: 1.872 V			
INFO:iMPACT - Creating XC7K160T device.			
'1': Programming device			
$Match_cycle = 2.$			
LCK_cycle = NoWait.			
LCK cycle: NoWait			
done.			
INFO:Cse — Status register values:			
INFO:Cse - 0011 1111 0101 1110 0000 1000 0100 0010			
INFO:Cse - '1': Completed downloading bit file to device.			
INFO:Cse - '1': Programming completed successfully.			
$Match_cycle = 2.$			
LCK_cycle = NoWait.			
LCK cycle: NoWait			
INFO <mark>:iMPACT - '1': Checking don</mark> e pindone.			
'1': Programmed successfully.			
Elapsed time = 17 sec.			
FPGA DONE			
1. Unplug and plug the USB cable of AICE-MCU.			
2. Wait DONE LED on AICE-MCU lights up.			
請按任意鍵繼續---	-		

8. 連接 AICE-MCU to your host PC.





9. 等待Done LED亮起.





10. 按任意鍵並且繼續. 11. FPGA netlist file燒錄成功後顯示如下圖畫面.

📾 ISE Design Suite Command Prompt	- 🗆 >
0×00480000	
0x004a0000	
0x004c0000	
0x004e0000	
0x00500000	
0x00520000	
0x00540000	
0x00560000	
0x00580000	
0x005a0000	
0x005c0000	
0x005e0000	
0×00600000	
0×00620000	
0×00640000	
0×00660000	
programming done. elapsed time = 53 seconds	
verifyingdone verifying. elapsed time = 54 seconds	
d:\Xilinx\14.5\LabTools>	
4	•





Programing FPGA by Xilinx Burner



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Programing FPGA by iMPACT

1. Check控制台/系統/硬體/裝置管理員







Programing FPGA by iMPACT

1.程式集開啟Xilinx Design Tools → Lab Tools14.6 → iMPACT







2.Automatic Project File Load 選擇 "No"



3.Automatically create and save a project選擇 "No"







4.選擇"create new project (.ipf)" 後,按 "OK".

🗋 🎓 🗄 🌠 🗄 🖻 🗄 🖉 🥙 🚱	
4PACT Flows ↔ □ ₽ × Boundary Scan SystemACE Create PROM File (PROM File Formatter) Web Talk Data	
	New iMPACT Project
	I want to
	 load most recent project default.ipf Load most recent project file when iMPACT starts
dPACT Processes ↔ □ 륨 ×	Create a new project (ipf) default.ipf
1-	



ISE iMPACT (P.68d)	
<u>File Edit View Operations Output</u> Debug <u>W</u> indov	w <u>H</u> elp
i 🗋 🤌 i 🦗 - i 🖻 🖬 i 🥕 😪	
iMPACT Flows ↔ □ ₽ × Boundary Scan SystemACE Create PROM File (PROM File Formatter) Web Talk Data	 Welcome to iMPACT Please select an action from the list below Configure devices using Boundary-Scan (ITAG) Automatically connect to a cable and identify Boundary-Scan chain Prepare a PROM File Prepare a System ACE File Prepare a Boundary-Scan File SVF
iMPACT Processes ↔ □ ₽ ×	OK Cancel
Console	
Welcome to iMPACT iMPACT Version: 14.6	





◆6.Auto Assign Configuration Files Query Dialog選擇 "No"

🐉 Auto Assign Configuration Files Query Dialog 🛛 🛛 🔀
Do you want to continue and assign configuration files(s)?
<u>Y</u> es <u>N</u> o



7.Right click device to select operations /Add SPI/BPI



8.Add PROM File \rightarrow n13c0_ag101c43.mcs





9.選擇 PROM參數設定

- BPI PROM
- 28F00AM29EW
- Data Width : 16
- Select RS[1:0]b Pin Address Bits : NOT USED

設定完成後選擇 "OK"

₽	🐉 Select Attached SPI/BPI			
Select the PROM attached to FPGA:				
	BPI PROM 🔽	28F00AM29EW	~	
	Data Width:	16	~	
	Select RS[1:0]b Pin Address Bits:	NOT USED	~	
	ОК	Cancel		

32







10.選擇Flash元件後,按滑鼠右鍵,選擇"Program"



11.依照圖示選擇後,按 "OK"

😻 Device Programming Properties - Device	1 Programming Properties		
Category			
Boundary-Scan			
Device 1 (FPGA xc7k160t)	Property Name	Value	
Device I (Attached PLASH, 26P007	Verify		
	General CPLD And PROM Properties		
	Design-Specific Erase Before Programming		
	FPGA Device Specific Programming Properties		
	After programming Flash	automatically load FPGA with Flash contents <default></default>	~
8	Configuration Bank Voltage	Based on CFGBVS pin	~
<			
		OK Cancel Apply	7 He





12.開始燒錄

🐉 Progress Dialog [3%]	? 🔀
Executing command	
0%	
	Cancel



Program Succeeded



Burn System program by AndeSigh

開啟 Flash Burner 在 AndeSight.(Andesight需Patch





Burn System program by AndeSigh

Flash programming 設定項目.

- 1.選擇 burner tool 2.選擇 flash image file 3.選擇 Target board
- AG101P_4G Burner tool: IntelJ3 Target board: XC5
- AG101P_16M Burner tool: IntelJ3 Target board:ag101p_16mb

✤ AE210

Burner tool: SPI Target board: None



Flashing Driver User specify corresponding information and press Burn' to start					
User specify corresponding information and press Burn' to start					
<u>_</u>					
Flashing Driver Intell3.exe Browse					
Image file setting					
Flashing Image T.\Production\ADP-XC7KFF676\bitmap\AG101P\boot code\rominit_32 Browse					
Programming Start Address:					
Driver Arguments					
Target board: xx5 💽 Flash Controller Address:					
Unlock Lock after Programming					
Verification Erase All					
Misc Arguments:					
Logging					
(?) I Bum Close					



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Quick Boot Up



- 電腦超級終端機設定:
- ✤ Baud Rate: 38400
- Data: 8 bits
- Parity: none
- ✤Stop: 1 bit
- Flow control: none



Quick Boot Up (cont'd)







Quick Boot Up



1. 按System_Enable 按鈕 (PWR_SW1), 七段顯示器LEDs 顯示 *99". 並且console 會顯示下面的畫面:

Ba	Bank 1: size;0x4000000+	
Ba	Bank 2: size;0x40000004	
SE SE	cpu id : d revision: 1.04	
	Check SD Card+	
SI	SD Card is not Exist on Card Slot.4	
ų	له	
Pl	Please press a GPIO Button for booting:+	
_	لې	
G	<u>GPIQ1 (</u> SW1): Run Setup & Diagnosis#	
G	<u>GPIO2 (</u> SW2): <u>Burnin</u> Test+	



Quick Boot Up



2. 按GPIO1 按鈕 (SW1), 系統將開啟Diagnosis program. 七段顯示 器將顯示"b7" 並且console 顯示Diagnosis Menu如下:

Andes Development Platform Diagnosis Menu for ADR32 environment, Built@Jul 12 2013 (v1.81)+ This is Engineering Board ([PMU_BASE+0x8c]=0x20130710)+ (2) Timer Test (1) SDRAM Test (3) DMA Test≁ (...5) UART Loopback Test (6) UART DMA Test 🔰 (9) Watchdog Test+ (10) Watchdog Reset Test(11) MAC Loopback Test (12) Flash Test+ (14) SDRAM(bnk1,2) (17) AC97 Test (18) AC97 DMA Test≁ (21) LCD Test (22) LCD Menu (23) Query RTC₽ (24) RTC Alarm Test (25) GPIO Test (35) SD. Test≁ (38) USB 1.1 Test (39) USB 2.2 Test (40) USB-OTG Test+ (41) USB-Host Test (53) Enable Cache (54) Disable Cache₽ (55) CLI (67) Set Console's UART (75) Burn-in Test+ (95) Production (96) NDS BOOT (97) CopyImageFromCard+ (98) Linux test from SD card(99) Setup+ Command>>+

3. Then, the system is ready to use.



Boot Up to Linux

In Diagnosis Menu

- ✤ Command>>55
- ✤ CLI>go 0x80400000 <Enter</p>
- Into Linux command line

🖳 COM1:38400baud - Tera Term VI					
<u>File E</u> dit <u>S</u> etup C <u>o</u> ntrol	<u>W</u> indow <u>H</u> elp				
/ # / # ls bin dev elf_core_checking etc home / #	lib lib64 linuxrc lost+found mnt	proc root sbin sys tmp	usr var		









創新.前瞻.國際化

Thank You

