» Kontron User's Guide «

microETXexpress®-PC

Document Revision 0.1

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1 User Information

1.1 About This Document

This document provides information about products from Kontron Embedded Modules GmbH and/or its subsidiaries. No warranty of suitability, purpose, or fitness is implied. While every attempt has been made to ensure that the information in this document is accurate, the information contained within is supplied “as-is” and is subject to change without notice.

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

1.2 Copyright Notice

1.3 Trademarks

The following lists the trademarks of components used in this board.

- IBM, XT, AT, PS/2 and Personal System/2 are trademarks of International Business Machines Corp.
- Microsoft is a registered trademark of Microsoft Corp.
- Intel is a registered trademark of Intel Corp.
- All other products and trademarks mentioned in this manual are trademarks of their respective owners.

1.4 Standards

Kontron Embedded Modules GmbH is certified to ISO 9000 standards.

1.5 Warranty

This Kontron Embedded Modules GmbH product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules GmbH will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Embedded Modules GmbH will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules GmbH that are caused by a faulty Kontron Embedded Modules GmbH product.

1.6 Technical Support

Technicians and engineers from Kontron Embedded Modules GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Please consult our Web site at http://www.kontron.com/support for the latest product documentation, utilities, drivers and support contacts. Consult our customer section http://emdcustomersection.kontron.com for the latest BIOS downloads, Product Change Notifications and additional tools and software. In any case you can always contact your board supplier for technical support.

2 Introduction

2.1 microETXexpress®-PC

Based on the COM Express standard, Kontron's microETXexpress®-PC, powered by a variety of Intel®'s Core2Duo® and CeleronM® processors, is a next-generation embedded module that brings advanced technology to tomorrow's applications, as well as continuing today's legacy devices. Built around serial differential signaling technologies, microETXexpress®-PC modules incorporate the following interfaces into 95 x 125 small form factor embedded module:

- PCI Express, which provides a high performance I/O infrastructure with transfer rates starting at 2.5 Giga transfers per second over a x1 PCI Express lane
- PCI
- Serial ATA (SATA II)
- USB 2.0
- LVDS
- Azalia High Definition Audio
- Advanced Configuration and Power Interface (ACPI) for optimized power management

The microETXexpress®-PC is built around the Intel® Core2Duo® and CeleronM® processor and the Intel® GS45 chipset. These modules feature the most current desktop features such as USB 2.0, SATA, and PCI Express buses.

The microETXexpress®-PC delivers up to 4GB DDR3 RAM. For applications that require advanced real-time video capabilities, the microETXexpress®-PC has integrated graphics with 2D, 3D and Motion Video Acceleration and also supports PCI Express graphics, two SDVO ports or two HDMI capable DVI ports.

Fast communications are possible courtesy of a Gigabit Ethernet port.

The microETXexpress®-PC supports up to 6 PCI Express x1 Lanes and PCI Express cards (only when 10/100MB Ethernet is equipped) as well as established hardware solutions based on current buses such as 32-bit PCI. A Gigabit Ethernet port provides fast connectivity to LAN/WAN and 8 USB 2.0 ports provide fast and sufficient interfaces for external peripherals.

microETXexpress®-PC modules also provide the following interfaces that are always located in the same physical position on each board:

PCI-express, PCI32, USB, serial ATA (SATA), parallel ATA (PATA), LVDS Multi Media ports, as well as an ACPI (Advanced Configuration and Power Interface) for optimized power management. Mounting holes on the board provide secure mounting to allow the module increased shock and vibration resistance.

2.2 Naming clarification

COMexpress™ defines a Computer-On-Module, or COM, with all components necessary for a bootable host computer, packaged as a super component. Interfaces will provide a smooth transition path from legacy parallel interfaces to LVDS (Low Voltage Differential Signaling) interfaces. These include the PCI bus and parallel ATA and PCI Express and Serial ATA.

» ETXexpress® modules are Kontron's COMexpress™ modules in basic form factor (125mm x 95mm)

» microETXexpress® modules are Kontron's COMexpress™ modules in compact form factor (95mm x 95mm)

» nanoETXexpress® modules are Kontron's COMexpress™ modules in the future ultra form factor (55mm x 84mm)

2.3 Understanding microETXexpress®-PC functionality

All Kontron ETXexpress® and microETXexpress® modules contain two connectors; each of it has two rows. The primary connector has two rows called Row A and Row B. The secondary connector has two rows called Row C and Row D.

The primary connector (Row A and Row B) feature the following legacy-free functionality:

» Ethernet

» Serial ATA (SATA)

» USB 2.0

» LVDS/VGA and dual display video

» Intel High Definition Audio (Azalia)

» LPC (low pin count) Bus

The secondary connector (Row C and Row D) provides support for the following buses and I/O:

» PCI Express

» PCI

» IDE

2.4 COMexpress™ Documentation

This product manual serves as one of three principal references for a COMexpress™ design. It documents the specifications and features of microETXexpress®-DC. The other two references, which are available from your Kontron Support or from PICMG®, include:

» The COMexpress Specification defines the COMexpress™ module form factor, pinout, and signals. This document ist available from the PIGMG website by filling out the order form.

» The COMExpress™ Design Guide by PICMG serves as a general guide for baseboard design, with a focus on maximum flexibility to accommodate a wide range of COMexpress™ modules.

Note:	Some of the information contained within this product manual applies only to certain product revisions (CE: xxx). If certain information applies to specific product revisions (CE: xxx) it will be stated. Please check the product revision of your module to see if this information is applicable.

2.5 COMexpress™ Benefits

Computer on modules express (COMexpress) modules in compact formfactor are very compact (95 x 95 mm, 12mm thick), highly integrated computers. All (micro)ETXexpress® modules feature a standardized form factor and a standardized connector layout that carry a specified set of signals. Each microETXexpress® module is based on

connector type 2 of the COMexpress specification. This standardization allows designers to create a single-system baseboard that can accept present and future (micro)ETXexpress® modules.

microETXexpress® modules include common personal computer (PC) peripheral functions such as:

- Graphics
- USB ports
- Ethernet
- Sound
- IDE (and SATA)

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

A peripheral PCI bus can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard using the computer as one plug-in component simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design can use a range of ETXexpress®, microETXexpress® and nanoETXexpress modules. This flexibility can differentiate products at various price/performance points, or to design future proof systems that have a built-in upgrade path. The modularity of a COMexpress™ solution also ensures against obsolescence as computer technology evolves. A properly designed COMexpress™ baseboard can work with several successive generations of COMexpress® modules.

A COMexpress™ baseboard design has many advantages of a custom, computer-board design but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

3 Specification

3.1 Functional Specification

Processor: Intel® Core2Duo (Penryn)

- CPU: 45nm Penryn SL9400, SU9300 or CM722
- Cache: 3MB (CM722) or 6MB

Chipset Northbridge:Intel® GS45

- Speed: 667 / 800 / 1066 MHz FSB
- RAM: single channel up 4GB DDR3-667/800/1066 on SODIMM socket
- PEG: One x16 PCIe port for PCI Express based graphic cards

Chipset Southbridge: Intel® ICH-9M

- USB: 8 x USB 1.1/2.0
- Audio: Intel® High Definition Audio (24 bit / 96 kHz)
- PCI Express: 5 x PCI Express x1 (x4 possible)
- PCI bus: 32bit / 33MHz

Integrated graphics: Intel® GMAX4500

- Graphics Memory: up to 1024 MByte
- Features: HDTV/HD capable, Decoder for MPEG2(HD) / H.264, DirectX®10.0, OpenGL 2.0, Pixelshader 4.0

Display Interfaces

- CRT: maximum resolution up to QXGA (2048x1536)
- Flat Panel: dual channel 18bit and 24bit (with dithering) up to UXGA (1600x1200)
- Digital Display: 2 SDVO channels (muxed with PEG) supporting external SDVO components (HDMI, DVI, LVDS, TV-out)
- HDMI
- DisplayPort

Storage

- » SATA: 3 SATA ports up to 300 MB/S supporting NCQ, Hotplug, Staggered Spinup, eSATA, PortMultiplier, RAID 0, RAID1, Matrix-RAID
- » IDE: One Channel over JMD330 SATA2PATA Bridge

Onboard Devices:

- » Ethernet: Intel® 82567 10/100/1000 Phy
- » TPM: TPM 1.2, integrated in Southbridge
- » Watchdog: onboard CPLD with integrated Watchdog functionality

Additional Interfaces:

- » LPC: Yes
- » SMBus: Yes
- » I2C: Yes
- » GPIO: 8, Fixed to 4 GPI or 4 GPO via JIDA interface

Power Management & Misc

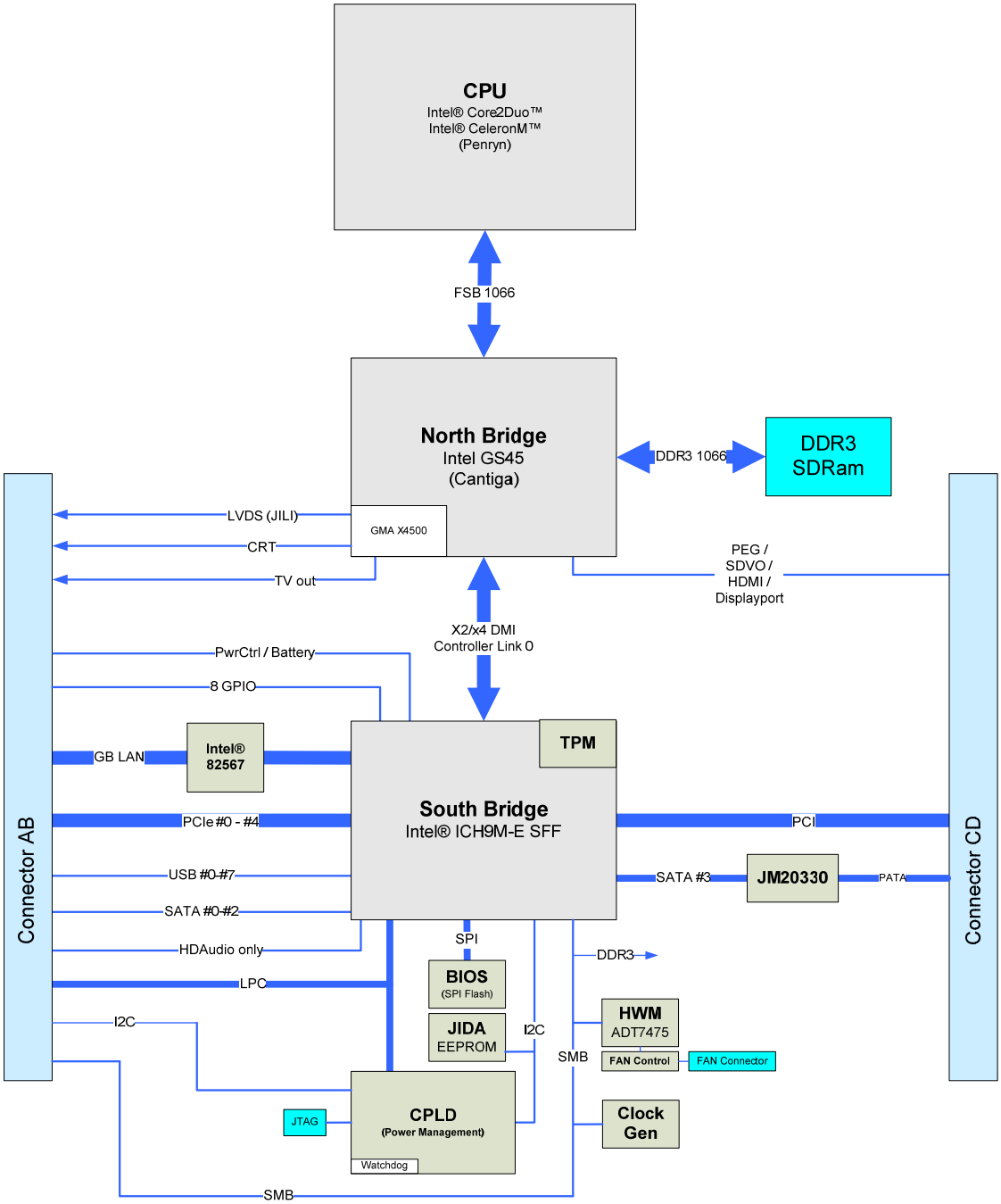
- » JIDA support: Yes
- » MARS support: Yes
- » HWM: Temperature Monitoring for CPU and Board Temperature
- » Passice Cooling: Passice and Critical Trip Point (with BIOS NOW1R112 or newer)
- » ACPI: ACPI 1.0 / 2.0 / 3.0
- » S-States: S0, S3, S4, S5
- » Input Voltage: Single supply support with wide range input 8.5 V - 18 V

3.2 Available modules

Part No	Intel® CPU
36004-0000-19-2	SL9400
36004-0000-12-2	SU9300
36004-0000-12-1	722

3.3 Block Diagram

microETXexpress®-PC



3.4 Meachnical Specification

Dimensions

- 95.0 mm x 114.0 mm (3.75" x 4.5")
- Height approx. 12 mm (0.4")

3.5 Electical Specification

3.5.1 Supply Voltage

- VCC: 12V DC +/- 5% or
- 8.5V DC to 18V DC wide range input
- 5V_Stb: 5V DC +/- 5% but always equal or lower VCC

Note:	It is not possible to use E2 rated boards with wide range input!

Note:	It is recommended to follow the ATX specification for voltage rise times which claims: "The output voltage shall rise from ≤ 10% of nominal to within the regulation ranges ... within 0.1ms to 20ms".

3.5.2 Supply Voltage Ripple

- Maximum 100 mV peak to peak 0 – 20 MHz

3.5.3 Supply Current 5V_STB

- Typical 50 mA, peak up to 350 mA (S3)

3.5.4 Supply Current (Windows XP SP3)

The tested boards were mounted on a Kontron Evaluation Board (Article number: 38100-0000-00-0), a mouse and a keyboard were connected. The Power-consumption tests were executed during Windows XP SP2 by using a tool to stress the CPU (100 % load). The power measurements values were acquired after 15 min full load and a stable CPU die temperature. To ensure a stable die temperature a corresponding heatsink was used to hold the temperature under the critical trip point.

All boards were equipped with TBD of memory. The Modules were tested using maximum CPU frequency.

Mode	[A] 5V	[A] 5VSB	[W]
Full Load	TBD	TBD	TBD
Idle	TBD	TBD	TBD
Idle with C1E/EIST	TBD	TBD	TBD

Standby S1	TBD	TBD	TBD
Standby S3	TBD	TBD	TBD
Soft Off S5	TBD	TBD	TBD

3.5.5 CMOS Battery Power Consumption

CMOS battery power consumption was measured with a microETXexpress®-DC module on a standard Kontron ETX® evaluation board. The system was turned off and the battery was removed from the evaluation board. The 2.5 V or 3.0 V of power was supplied from a DC power supply. Do not use these values to calculate the CMOS battery lifetime.

TBD

3.6 Environmental Specification

Temperature

Operating: (with Kontron Embedded Modules GmbH heat-spreader plate assembly):

- Ambient temperature: 0 to +60 °C
- Maximum heatspreader-plate temperature: 0 to +60 °C (*)
- Non-operating: -30 to +85 °C

Note: *The maximum operating temperature with the heatspreader plate is the maximum measurable temperature on any spot on the heatspreader's surface. You must maintain the temperature according to the above specification.

Operating (without Kontron Embedded Modules GmbH heat-spreader plate assembly):

- Maximum operating temperature: 0 to +60 °C (**)
- Non operating: -30 to +85 °C

Note: **The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.

Humidity

- Operating: 10% to 90% (non condensing)
- Non operating: 5% to 95% (non condensing)

3.7 MTBF

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts.

The Bellcore calculation used is “Method 1 Case 1”. In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer’s data has been used wherever possible. The manufacturer’s data, when used, is specified at 50° C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40° C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

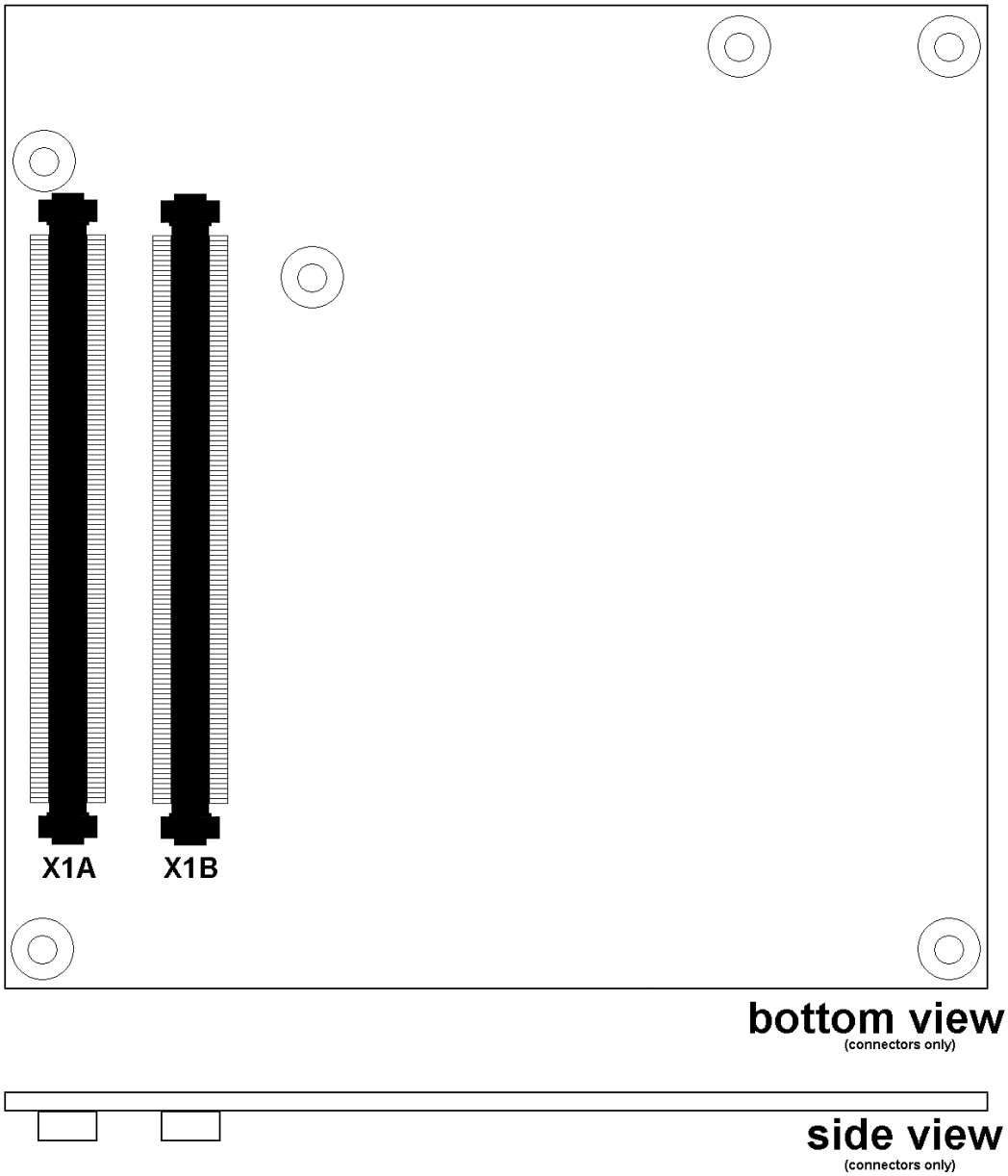
System MTBF (hours): TBD

Notes:	Fans usually shipped with Kontron Embedded Modules GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.

4 microETXexpress®-PC Connectors

The pinouts for microETXexpress® Interface Connectors X1A and X1B are documented for convenient reference. Please see the COMexpress™ Specification and COMexpress™ Design Guide for detailed, design-level information.

4.1 Connector Locations



4.2 Pinout List

4.2.1 General Signal Description

Type	Description
I/O-3,3	Bi-directional 3,3 V IO-Signal
I/O-5T	Bi-dir. 3,3V I/O (5V Tolerance)
I/O-5	Bi-directional 5V I/O-Signal
I-3,3	3,3V Input
I/OD	Bi-directional Input/Output Open Drain
I-5T	3,3V Input (5V Tolerance)
OA	Output Analog
OD	Output Open Drain
O-1,8	1,8V Output
O-3,3	3,3V Output
O-5	5V Output
DP-I/O	Differential Pair Input/Output
DP-I	Differential Pair Input
DP-O	Differential Pair Output
PU	Pull-Up Resistor
PD	Pull-Down Resistor
PWR	Power Connection

Notes: To protect external power lines of peripheral devices, make sure that: the wires have the right diameter to withstand the maximum available current the enclosure of the peripheral device fulfils the fire-protection requirements of IEC/EN60950

4.2.2 Connector X1A (A1 - A55)

Pin	Signal	Description	Type	Termination	Comment
A1	GND	Power Ground	PWR	-	-
A2	GBE0_MDI3-	GBE0_MDI3_N | Ethernet Receive	DP-I	-	-
A3	GBE0_MDI3+	GBE0_MDI3_P | Ethernet Receive	DP-I	-	-
A4	GBE0_LINK1	GBE0_LINK100# | Ethernet Speed	O-3,3	-	-
A5	GBE0_LINK1	GBE0_LINK1000# | Ethernet Speed	O-3,3	-	-
A6	GBE0_MDI2-	GBE0_MDI2_N | Ethernet Receive	DP-I	-	-
A7	GBE0_MDI2+	GBE0_MDI2_P | Ethernet Receive	DP-I	-	-
A8	GBE0_LINK#	GBE0_LINK# | LAN Link LED	OD	-	-
A9	GBE0_MDI1-	GBE0_MDI1_N | Ethernet Receive	DP-I	-	-
A10	GBE0_MDI1+	GBE0_MDI1_P | Ethernet Receive	DP-I	-	-
A11	GND	Power Ground	PWR	-	-
A12	GBE0_MDI0-	GBE0_MDI0_N | Ethernet Transmit	DP-O	-	-
A13	GBE0_MDI0+	GBE0_MDI0_P | Ethernet Transmit	DP-O	-	-
A14	GBE0_CTREF	GBE0_CTREF	O-1,8	-	is on a power rail controlled by Intels
A15	SUS_S3#	PM_SLP_S3_EXT#	O-3,3	PU 10k 3,3V	-
A16	SATA0_TX+	opt. SATA_TX0_P | SATA 0 Transmit	Nc	-	- just available if
A17	SATA0_TX-	opt. SATA_TX0_N | SATA 0 Transmit	Nc	-	- just available if
A18	SUS_S4#	PM_SLP_S4_EXT#	O-3,3	-	-
A19	SATA0_RX+	opt. SATA_RX0_P | SATA 0 Receive	Nc	-	- just available if
A20	SATA0_RX-	opt. SATA_RX0_N | SATA 0 Receive	Nc	-	- just available if
A21	GND	Power Ground	PWR	-	-
A22	SATA2_TX+	SATA_TX2_P | SATA 2 Transmit Data	DP-O	-	-
A23	SATA2_TX-	SATA_TX2_N | SATA 2 Transmit Data	DP-O	-	-
A24	SUS_S5#	PM_SLP_S#5	O-3,3	-	-
A25	SATA2_RX+	SATA_RX2_P | SATA 2 Receive Data	DP-I	-	-
A26	SATA2_RX-	SATA_RX2_N | SATA 2 Receive Data	DP-I	-	-
A27	BATLOW#	PM_BATLOW# | Battery Low	I-3,3	PU 8k25 3,3V	-
A28	ATA_ACT#	ATA_LED# | SATA LED	O-3,3	PU 10k 3,3V	int. PU 15k in ICH9 only active if
A29	AC_SYNC	HDA_SYNC | HD Audio Sync	O-3,3	-	opt. for x4: PU 1k 3,3V(S0)
A30	AC_RST#	HDA_RST# | HD Audio Reset	O-3,3	-	int. PD 20k in ICH9
A31	GND	Power Ground	PWR	-	-
A32	AC_BITCLK	HDA_BITCLK | HD Audio Clock	O-3,3	-	int. PD 20k in ICH9 active only in S3
A33	AC_SDOUT	HDA_SDOUT | HD Audio Data	O-3,3	-	int. PD 20k in ICH9– x4 => PU 1k
A34	BIOS_DISABL	BIOS_DISABLE#	I-3,3	-	-
A35	THRMTRIP#	EXT_THRMTRIP#	I/O-	PU 10k 3,3V	-
A36	USB6-	USB6_N | USB Data – Port6	DP-	-	int. PD 15k in ICH9 | 5V tolerant
A37	USB6+	USB6_P | USB Data + Port6	DP-	-	int. PD 15k in ICH9 | 5V tolerant
A38	USB_6_7_OC	USB_67_OC# | USB OverCurrent	I-3,3	PU 10k 3,3V	-
A39	USB4-	USB4_N | USB Data - Port4	DP-	-	int. PD 15k in ICH9 | 5V tolerant
A40	USB4+	USB4_P | USB Data + Port4	DP-	-	int. PD 15k in ICH9 | 5V tolerant
A41	GND	Power Ground	PWR	-	-
A42	USB2-	USB2_N | USB Data - Port2	DP-	-	int. PD 15k in ICH9 | 5V tolerant
A43	USB2+	USB2_P | USB Data + Port2	DP-	-	int. PD 15k in ICH9 | 5V tolerant
A44	USB_2_3_OC	USB_23_OC# | USB OverCurrent	I-3,3	PU 10k 3,3V	-
A45	USB0-	USB0_N | USB Data - Port0	DP-	-	int. PD 15k in ICH9 | 5V tolerant
A46	USB0+	USB0_P | USB Data + Port0	DP-	-	int. PD 15k in ICH9 | 5V tolerant
A47	VCC_RTC	V_BAT	PWR	-	-
A48	EXCD0_PERST	EXCD0_PERST# | Express card reset	O-3,3	-	-
A49	EXCD0_CPPE#	EXCD0_CPPE# | capable c. request	I-3,3	PU 10k 3,3V	-
A50	LPC_SERIRQ	LPC_SERIRQ | Serial Interrupt	IO-3,3	PU 10k 3,3V	-
A51	GND	Power Ground	PWR	-	-
A52	PCIE_TX5+	opt. PCI Express lane 5 + Transmit	Nc	-	just available if no GbEthernet PHY is
A53	PCIE_TX5-	opt. PCI Express lane 5 - Transmit	Nc	-	just available if no GbEthernet PHY is
A54	GPI0	EXT_GPI0 | General Purpose Input 0	I-3,3	PU 10k 3,3V	-
A55	PCIE_TX4+	PCI Express lane 4 + Transmit	DP-O	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

4.2.3 Connector X1A (A56-A110)

Pin	Signal	Description	Type	Termination	Comment
A56	PCIE_TX4-	PCI Express lane 4 - Transmit	DP-O	-	-
A57	GND	Power Ground	PWR	-	-
A58	PCIE_TX3+	PCI Express lane 3 + Transmit	DP-O	-	-
A59	PCIE_TX3-	PCI Express lane 3 - Transmit	DP-O	-	-
A60	GND	Power Ground	PWR	-	-
A61	PCIE_TX2+	PCI Express lane 2 + Transmit	DP-O	-	-
A62	PCIE_TX2-	PCI Express lane 2 - Transmit	DP-O	-	-
A63	GPI1	EXT_GPI1 | General Purpose Input 1	I-3,3	PU 10k 3,3V (S0)	-
A64	PCIE_TX1+	PCI Express lane 1 + Transmit	DP-O	-	-
A65	PCIE_TX1-	PCI Express lane 1 - Transmit	DP-O	-	-
A66	GND	Power Ground	PWR	-	-
A67	GPI2	EXT_GPI2 | General Purpose Input 2	I-3,3	PU 10k 3,3V (S0)	-
A68	PCIE_TX0+	PCI Express lane 0 + Transmit	DP-O	-	-
A69	PCIE_TX0-	PCI Express lane 0 - Transmit	DP-O	-	-
A70	GND	Power Ground	PWR	-	-
A71	LVDS_A0+	LVDS_A_DATA0_P | LVDS Channel A	DP-O	-	-
A72	LVDS_A0-	LVDS_A_DATA0_N | LVDS Channel A	DP-O	-	-
A73	LVDS_A1+	LVDS_A_DATA1_P | LVDS Channel A	DP-O	-	-
A74	LVDS_A1-	LVDS_A_DATA1_N | LVDS Channel A	DP-O	-	-
A75	LVDS_A2+	LVDS_A_DATA2_P| LVDS Channel A	DP-O	-	-
A76	LVDS_A2-	LVDS_A_DATA2_N | LVDS Channel A	DP-O	-	-
A77	LVDS_VDD_EN	LVDS_VDD_EN | LVDS Panel Power	O-3,3	PD 100k	-
A78	LVDS_A3+	LVDS_A_DATA3_P | LVDS Channel A	DP-O	-	-
A79	LVDS_A3-	LVDS_A_DATA3_N | LVDS Channel A	DP-O	-	-
A80	GND	Power Ground	PWR	-	-
A81	LVDS_A_CK+	LVDS_A_CLK_P | LVDS Channel A	DP-O	-	-
A82	LVDS_A_CK-	LVDS_A_CLK_N | LVDS Channel A	DP-O	-	-
A83	LVDS_I2C_CK	LVDS_DDC_CLK | JILI I2C Clock	I/O-	PU 2k21 3,3V (s0)	-
A84	LVDS_I2C_DAT	LVDS_DDC_DATA | JILI I2C Data	I/O-	PU 2k21 3,3V (s0)	-
A85	GPI3	EXT_GPI3 | General Purpose Input 3	I-3,3	PU 10k 3,3V (S0)	-
A86	KBD_RST#	KBD_RST# | Keyboard Reset	I-3,3	PU 10k 3,3V (S0)	-
A87	KBD_A20GATE	KBD_A20GATE	I-3,3	PU 10k 3,3V (S0)	-
A88	PCIE0_CK_REF+	CLK_PCIE_CON_P	DP-O	-	-
A89	PCIE0_CK_REF-	CLK_PCIE_CON_N	DP-O	-	-
A90	GND	Power Ground	PWR	-	-
A91	RSVD	n.c.	Nc	-	-
A92	RSVD	n.c.	Nc	-	-
A93	GPO0	EXT_GPO0 | General Purpose Output 0	O-3,3	PD 10k	-
A94	RSVD	n.c.	Nc	-	-
A95	RSVD	n.c.	Nc	-	
A96	GND	Power Ground	PWR	-	-
A97	VCC_12V	12V VCC	PWR	-	-
A98	VCC_12V	12V VCC	PWR	-	-
A99	VCC_12V	12V VCC	PWR	-	-
A100	GND	Power Ground	PWR	-	-
A101	VCC_12V	12V VCC	PWR	-	-
A102	VCC_12V	12V VCC	PWR	-	-
A103	VCC_12V	12V VCC	PWR	-	-
A104	VCC_12V	12V VCC	PWR	-	-
A105	VCC_12V	12V VCC	PWR	-	-
A106	VCC_12V	12V VCC	PWR	-	-
A107	VCC_12V	12V VCC	PWR	-	-
A108	VCC_12V	12V VCC	PWR	-	-
A109	VCC_12V	12V VCC	PWR	-	-
A110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

4.2.4 Connector X1A (B1 - B55)

Pin	Signal	Description	Type	Termination	Comment
B1	GND	Power Ground	PWR	-	-
B2	GBE0_ACT	GBE0_ACT# | Ethernet Activity LED	OD	-	-
B3	LPC_FRAME#	LPC_FRAME# | LPC Frame Indicator	I-3,3	-	-
B4	LPC_AD0	LPC_AD0 | LPC Adress & DATA Bus	I/O-	-	int. PU 20k in ICH9
B5	LPC_AD1	LPC_AD1 | LPC Adress & DATA Bus	I/O-	-	int. PU 20k in ICH9
B6	LPC_AD2	LPC_AD2 | LPC Adress & DATA Bus	I/O-	-	int. PU 20k in ICH9
B7	LPC_AD3	LPC_AD3 | LPC Adress & DATA Bus	I/O-	-	int. PU 20k in ICH9
B8	LPC_DRQ0#	LPC_DRQ#0 | LPC Request 0	I-3,3	PU 10k 3,3V	int. PU 20k in ICH9
B9	LPC_DRQ1#	LPC_DRQ#1 | LPC Request 1	I-3,3	PU 10k 3,3V	int. PU 20k in ICH10
B10	LPC_CLK	CLK_LPC_33M_EXT |33MHz LPC clock	O-3,3	-	-
B11	GND	Power Ground	PWR	-	-
B12	PWRBTN#	EXT_PWRBTN# | Power Button	I-3,3	PU 20k 3,3V	-
B13	SMB_CK	SMB_CLK_EXT | SMBUS Clock	O-3,3	PU 2k2 3,3V	-
B14	SMB_DAT	SMB_DATA_EXT | SMBUS Data	IO-3,3	PU 2k2 3,3V	-
B15	SMB_ALERT#	SMB_ALERT# | SMBUS Interrupt	IO-3,3	PU 1k0 3,3V	-
B16	SATA1_TX+	SATA_TX1_P | SATA 1 Transmit Data +	DP-O	-	-
B17	SATA1_TX-	SATA_TX1_N | SATA 1 Transmit Data -	DP-O	-	-
B18	SUS_STAT#	PM_SUS_STAT#	O-3,3	-	-
B19	SATA1_RX+	SATA_RX1_P | SATA 1 Receive Data +	DP-I	-	-
B20	SATA1_RX-	SATA_RX1_N | SATA 1 Receive Data -	DP-I	-	-
B21	GND	Power Ground	PWR	-	-
B22	SATA3_TX+	SATA_TX3_P | SATA 3 Transmit Data +	DP-O	-	-
B23	SATA3_TX-	SATA_TX3_N | SATA 3 Transmit Data -	DP-O	-	-
B24	PWR_OK	EXT_PWR_OK | Power OK	I-3,3	-	-
B25	SATA3_RX+	SATA_RX3_P | SATA 3 Receive Data +	DP-I	-	-
B26	SATA3_RX-	SATA_RX3_N | SATA 3 Receive Data -	DP-I	-	-
B27	WDT	WDT | Watch Dog Timer	O-3,3	-	-
B28	AC_SDIN2	HDA_SDIN2_ICH| HD Audio Serial	I-3,3	-	int. PD 20k in ICH9
B29	AC_SDIN1	HDA_SDIN1_ICH| HD Audio Serial	I-3,3	-	int. PD 20k in ICH9
B30	AC_SDIN0	HDA_SDIN0_ICH| HD Audio Serial	I-3,3	-	int. PD 20k in ICH9
B31	GND	Power Ground	PWR	-	-
B32	SPKR	HDA_SPKR | Speaker	O-3,3	-	int. PD 20k in ICH9
B33	I2C_CK	I2C_CLK_EXT | I2C clock	O-3,3	PU 2k21 3,3V	-
B34	I2C_DAT	I2C_DATA_EXT | I2C data	I/O-	PU 2k21 3,3V	-
B35	THRM#	PM_THRM# | Over Temperature	O-3,3	PU 8k25 3,3V	-
B36	USB7-	USB7_N | USB Data – Port7	DP-I/O	-	int. PD 15k in ICH9 | 5V
B37	USB7+	USB7_P | USB Data + Port7	DP-I/O	-	int. PD 15k in ICH9 | 5V
B38	USB_4_5_OC#	USB_45_OC# | USB OverCurrent Port	I-3,3	PU 10k 3,3V	-
B39	USB5-	USB5_N | USB Data – Port5	DP-I/O	-	int. PD 15k in ICH9 | 5V
B40	USB5+	USB5_P | USB Data + Port5	DP-I/O	-	int. PD 15k in ICH9 | 5V
B41	GND	Power Ground	PWR	-	-
B42	USB3-	USB3_N | USB Data – Port3	DP-I/O	-	int. PD 15k in ICH9 | 5V
B43	USB3+	USB3_P | USB Data + Port3	DP-I/O	-	int. PD 15k in ICH9 | 5V
B44	USB_0_1_OC#	USB_01_OC# | USB OverCurrent Port	I-3,3	PU 10k 3,3V	-
B45	USB1-	USB1_N | USB Data – Port1	DP-I/O	-	int. PD 15k in ICH9 | 5V
B46	USB1+	USB1_P | USB Data + Port1	DP-I/O	-	int. PD 15k in ICH9 | 5V
B47	EXCD1_PERST#	EXCD1_PERST# | Express card reset	O-3,3	-	-
B48	EXCD1_CPPE#	EXCD1_CPPE# | capable c. request	I-3,3	PU 10k 3,3V	-
B49	SYS_RESET#	EXT_SYS_RESET# | Reset Input	I-3,3	PU 10k 3,3V	-
B50	CB_RESET#	CB_RESET# | Carrier board Reset	O-3,3	-	-
B51	GND	Power Ground	PWR	-	-
B52	PCIE_RX5+	opt. PCI Express lane 5 + Recieve	Nc	-	just available if no
B53	PCIE_RX5-	opt. PCI Express lane 5 - Recieve	Nc	-	just available if no
B54	GPO1	EXT_GPO1 | General Purpose Output 1	O-3,3	PD 10k	-
B55	PCIE_RX4+	PCI Express lane 4 + Recieve	DP-I	-	availlable when ICH9-MDH

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

4.2.5 Connector X1B (C1 - C55)

Pin	Signal	Description	Type	Termination	Comment
C1	GND	Power Ground	PWR	-	-
C2	IDE_D7	IDE Data Bus	I/O-5T	PD 10k	-
C3	IDE_D6	IDE Data Bus	I/O-5T	-	-
C4	IDE_D3	IDE Data Bus	I/O-5T	-	-
C5	IDE_D15	IDE Data Bus	I/O-5T	-	-
C6	IDE_D8	IDE Data Bus	I/O-5T	-	-
C7	IDE_D9	IDE Data Bus	I/O-5T	-	-
C8	IDE_D2	IDE Data Bus	I/O-5T	-	-
C9	IDE_D13	IDE Data Bus	I/O-5T	-	-
C10	IDE_D1	IDE Data Bus	I/O-5T	-	-
C11	GND	Power Ground	PWR	-	-
C12	IDE_D14	IDE Data Bus	I/O-5T	-	-
C13	IDE_IORDY	IDE I/O Ready	I/O-5T	PU 4k7 3,3V (S0)	-
C14	IDE_IOR#	IDE I/O Read	I/O-	-	-
C15	PCI_PME#	PCI Power Management Event	I/O-	-	int. PU 20k in ICH9
C16	PCI_GNT2#	PCI Bus Grant 2	O-3,3	-	int. PU 20k in ICH9 (if
C17	PCI_REQ2#	PCI Bus Request 2	I-5T	PU 8k2 3,3V (S0)	-
C18	PCI_GNT1#	PCI Bus Grant 1	O-3,3	-	int. PU 20k in ICH9 (if
C19	PCI_REQ1#	PCI Bus Request 1	I-5T	PU 8k2 3,3V (S0)	-
C20	PCI_GNT0#	PCI Bus Grant 0	O-3,3	PD 1k0	int. PU 20k in ICH9 (if
C21	GND	Power Ground	PWR	-	-
C22	PCI_REQ0#	PCI Bus Reqest 0	I-5T	PU 8k2 3,3V (S0)	-
C23	PCI_RST#	PCI Bus Reset	O-3,3	-	-
C24	PCI_AD0	PCI Adress & Data Bus line	I/O-5T	-	-
C25	PCI_AD2	PCI Adress & Data Bus line	I/O-5T	-	-
C26	PCI_AD4	PCI Adress & Data Bus line	I/O-5T	-	-
C27	PCI_AD6	PCI Adress & Data Bus line	I/O-5T	-	-
C28	PCI_AD8	PCI Adress & Data Bus line	I/O-5T	-	-
C29	PCI_AD10	PCI Adress & Data Bus line	I/O-5T	-	-
C30	PCI_AD12	PCI Adress & Data Bus line	I/O-5T	-	-
C31	GND	Power Ground	PWR	-	-
C32	PCI_AD14	PCI Adress & Data Bus line	I/O-5T	-	-
C33	PCI_C/BE1#	PCI Bus Command and Byte enables 1	I/O-5T	-	-
C34	PCI_PERR#	PCI Bus Grant Error	I/O-5T	PU 8k2 3,3V (S0)	-
C35	PCI_LOCK#	PCI Bus Lock	I/O-5T	PU 8k2 3,3V (S0)	-
C36	PCI_DEVSEL#	PCI Bus Device Select	I/O-5T	PU 8k2 3,3V (S0)	-
C37	PCI_IRDY#	PCI Bus Bus Initiator Ready	I/O-5T	PU 8k2 3,3V (S0)	-
C38	PCI_C/BE2#	PCI Bus Command and Byte enables 2	I/O-5T	-	-
C39	PCI_AD17	PCI Adress & Data Bus line	I/O-5T	-	-
C40	PCI_AD19	PCI Adress & Data Bus line	I/O-5T	-	-
C41	GND	Power Ground	PWR	-	-
C42	PCI_AD21	PCI Adress & Data Bus line	I/O-5T	-	-
C43	PCI_AD23	PCI Adress & Data Bus line	I/O-5T	-	-
C44	PCI_C/BE3#	PCI Bus Command and Byte enables 3	I/O-5T	-	-
C45	PCI_AD25	PCI Adress & Data Bus line	I/O-5T	-	-
C46	PCI_AD27	PCI Adress & Data Bus line	I/O-5T	-	-
C47	PCI_AD29	PCI Adress & Data Bus line	I/O-5T	-	-
C48	PCI_AD31	PCI Adress & Data Bus line	I/O-5T	-	-
C49	PCI_IRQA#	PCI Bus Interrupt Request A	I-5T	PU 8k2 3,3V (S0)	-
C50	PCI_IRQB#	PCI Bus Interrupt Request B	I-5T	PU 8k2 3,3V (S0)	-
C51	GND	Power Ground	PWR	-	-
C52	PEG_RX0+	PCIexpress Graphics Recieve + (0)	DP-I	-	-
C53	PEG_RX0-	PCIexpress Graphics Recieve - (0)	DP-I	-	-
C54	TYPE0#	n.c. for type 2 module	nc	-	-
C55	PEG_RX1+	PCIexpress Graphics Recieve + (1)	DP-I	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

4.2.6 Connector X1B (C56 - C110)

Pin	Signal	Description	Type	Termination	Comment
C56	PEG_RX1-	PCIexpress Graphics Recieve - (1)	DP-I	-	-
C57	TYPE1#	n.c. for type 2 module	nc	-	-
C58	PEG_RX2+	PCIexpress Graphics Recieve + (2)	DP-I	-	-
C59	PEG_RX2-	PCIexpress Graphics Recieve - (2)	DP-I	-	-
C60	GND	Power Ground	PWR	-	-
C61	PEG_RX3+	PCIexpress Graphics Recieve + (3)	DP-I	-	-
C62	PEG_RX3-	PCIexpress Graphics Recieve - (3)	DP-I	-	-
C63	RSVD	n.c.	nc	-	-
C64	RSVD	n.c.	nc	-	-
C65	PEG_RX4+	PCIexpress Graphics Recieve + (4)	DP-I	-	-
C66	PEG_RX4-	PCIexpress Graphics Recieve - (4)	DP-I	-	-
C67	RSVD	n.c.	nc	-	-
C68	PEG_RX5+	PCIexpress Graphics Recieve + (5)	DP-I	-	-
C69	PEG_RX5-	PCIexpress Graphics Recieve - (5)	DP-I	-	-
C70	GND	Power Ground	PWR	-	-
C71	PEG_RX6+	PCIexpress Graphics Recieve + (6)	DP-I	-	-
C72	PEG_RX6-	PCIexpress Graphics Recieve - (6)	DP-I	-	-
C73	SDVO_DATA	SDVO_CTRLDATA	I/O-	-	opt. PU 2k21 3,3V (S0) =
C74	PEG_RX7+	PCIexpress Graphics Recieve + (7)	DP-I	-	-
C75	PEG_RX7-	PCIexpress Graphics Recieve - (7)	DP-I	-	-
C76	GND	Power Ground	PWR	-	-
C77	RSVD	n.c.	nc	-	-
C78	PEG_RX8+	PCIexpress Graphics Recieve + (8)	DP-I	-	-
C79	PEG_RX8-	PCIexpress Graphics Recieve - (8)	DP-I	-	-
C80	GND	Power Ground	PWR	-	-
C81	PEG_RX9+	PCIexpress Graphics Recieve + (9)	DP-I	-	-
C82	PEG_RX9-	PCIexpress Graphics Recieve - (9)	DP-I	-	-
C83	RSVD	n.c.	nc	-	-
C84	GND	Power Ground	PWR	-	-
C85	PEG_RX10+	PCIexpress Graphics Recieve + (10)	DP-I	-	-
C86	PEG_RX10-	PCIexpress Graphics Recieve - (10)	DP-I	-	-
C87	GND	Power Ground	PWR	-	-
C88	PEG_RX11+	PCIexpress Graphics Recieve + (11)	DP-I	-	-
C89	PEG_RX11-	PCIexpress Graphics Recieve – (11)	DP-I	-	-
C90	GND	Power Ground	PWR	-	-
C91	PEG_RX12+	PCIexpress Graphics Recieve + (12)	DP-I	-	-
C92	PEG_RX12-	PCIexpress Graphics Recieve - (12)	DP-I	-	-
C93	GND	Power Ground	PWR	-	-
C94	PEG_RX13+	PCIexpress Graphics Recieve + (13)	DP-I	-	-
C95	PEG_RX13-	PCIexpress Graphics Recieve - (13)	DP-I	-	-
C96	GND	Power Ground	PWR	-	-
C97	RSVD	n.c.	nc	-	-
C98	PEG_RX14+	PCIexpress Graphics Recieve + (14)	DP-I	-	-
C99	PEG_RX14-	PCIexpress Graphics Recieve - (14)	DP-I	-	-
C100	GND	Power Ground	PWR	-	-
C101	PEG_RX15+	PCIexpress Graphics Recieve + (15)	DP-I	-	-
C102	PEG_RX15-	PCIexpress Graphics Recieve - (15)	DP-I	-	-
C103	GND	Power Ground	PWR	-	-
C104	VCC_12V	12V VCC	PWR	-	-
C105	VCC_12V	12V VCC	PWR	-	-
C106	VCC_12V	12V VCC	PWR	-	-
C107	VCC_12V	12V VCC	PWR	-	-
C108	VCC_12V	12V VCC	PWR	-	-
C109	VCC_12V	12V VCC	PWR	-	-
C110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

4.2.7 Connector X1B (D1 - D55)

Pin	Signal	Description	Type	Termination	Comment
D1	GND	Power Ground	PWR	-	-
D2	IDE_D5	IDE Data Bus	I/O-5T	-	-
D3	IDE_D10	IDE Data Bus	I/O-5T	-	-
D4	IDE_D11	IDE Data Bus	I/O-5T	-	-
D5	IDE_D12	IDE Data Bus	I/O-5T	-	-
D6	IDE_D4	IDE Data Bus	I/O-5T	-	-
D7	IDE_D0	IDE Data Bus	I/O-5T	-	-
D8	IDE_REQ	IDE Data Bus	I/O-5T	PD 5k62	-
D9	IDE_IOW#	IDE IO Write	O-3,3	-	-
D10	IDE_ACK#	IDE DMA Acknowledge	O-3,3	-	-
D11	GND	Power Ground	PWR	-	-
D12	IDE_IRQ	IDE Interrupt Request	I-5T	PD 10k	-
D13	IDE_A0	IDE Adress Bus	O-3,3	-	-
D14	IDE_A1	IDE Adress Bus	O-3,3	-	-
D15	IDE_A2	IDE Adress Bus	O-3,3	-	-
D16	IDE_CS1#	IDE Chip Select Channel 0	O-3,3	-	-
D17	IDE_CS3#	IDE Chip Select Channel 1	O-3,3	-	-
D18	IDE_RESET#	IDE Hard Drive Reset	O-3,3	-	int. PU 31k in PATA bridge
D19	PCI_GNT3#	PCI Bus Grant 3	O-3,3	-	int. PU 20k in ICH9 (if
D20	PCI_REQ3#	PCI Bus Reqest 0	I-5T	PU 8k2 3,3V	-
D21	GND	Power Ground	PWR	-	-
D22	PCI_AD1	PCI Adress & Data Bus line	I/O-5T	-	-
D23	PCI_AD3	PCI Adress & Data Bus line	I/O-5T	-	-
D24	PCI_AD5	PCI Adress & Data Bus line	I/O-5T	-	-
D25	PCI_AD7	PCI Adress & Data Bus line	I/O-5T	-	-
D26	PCI_C/BE0#	PCI Bus Command and Byte enables 0	I/O-5T	-	-
D27	PCI_AD9	PCI Adress & Data Bus line	I/O-5T	-	-
D28	PCI_AD11	PCI Adress & Data Bus line	I/O-5T	-	-
D29	PCI_AD13	PCI Adress & Data Bus line	I/O-5T	-	-
D30	PCI_AD15	PCI Adress & Data Bus line	I/O-5T	-	-
D31	GND	Power Ground	PWR	-	-
D32	PCI_PAR	PCI Bus Parity	I/O-5T	-	-
D33	PCI_SERR#	PCI Bus System Error	I/O-5T	PU 8k2 3,3V	-
D34	PCI_STOP#	PCI Bus Stop	I/O-5T	PU 8k2 3,3V	-
D35	PCI_TRDY#	PCI Bus Target Ready	I/O-5T	PU 8k2 3,3V	-
D36	PCI_FRAME#	PCI Bus Cycle Frame	I/O-5T	PU 8k2 3,3V	-
D37	PCI_AD16	PCI Adress & Data Bus line	I/O-5T	-	-
D38	PCI_AD18	PCI Adress & Data Bus line	I/O-5T	-	-
D39	PCI_AD20	PCI Adress & Data Bus line	I/O-5T	-	-
D40	PCI_AD22	PCI Adress & Data Bus line	I/O-5T	-	-
D41	GND	Power Ground	PWR	-	-
D42	PCI_AD24	PCI Adress & Data Bus line	I/O-5T	-	-
D43	PCI_AD26	PCI Adress & Data Bus line	I/O-5T	-	-
D44	PCI_AD28	PCI Adress & Data Bus line	I/O-5T	-	-
D45	PCI_AD30	PCI Adress & Data Bus line	I/O-5T	-	-
D46	PCI_IRQC#	PCI Bus Interrupt Request C	I-5T	PU 8k2 3,3V	-
D47	PCI_IRQD#	PCI Bus Interrupt Request D	I-5T	PU 8k2 3,3V	-
D48	PCI_CLKRUN#	PCI Clock Run	I-5T	PU 8k25 3,3V	-
D49	PCI_M66EN	n.c.	nc	-	-
D50	PCI_CLK	CLK_PCI_33M_EXT | PCI Clock 33MHz	O-3,3	-	-
D51	GND	Power Ground	PWR	-	-
D52	PEG_TX0+	PCIexpress Graphics Transmit + (0)	DP-O	-	-
D53	PEG_TX0-	PCIexpress Graphics Transmit - (0)	DP-O	-	-
D54	PEG_LANE_RV#	PCIexpress Graphics Lane Reversal	I-3,3	-	-
D55	PEG_TX1+	PCIexpress Graphics Transmit + (1)	DP-O	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

4.2.8 Connector X1B (D56 - D110)

Pin	Signal	Description	Type	Termination	Comment
D56	PEG_TX1-	PCIexpress Graphics Transmit - (1)	DP-O	-	-
D57	TYPE2#	n.c. for type 2 module	nc	-	-
D58	PEG_TX2+	PCIexpress Graphics Transmit + (2)	DP-O	-	-
D59	PEG_TX2-	PCIexpress Graphics Transmit - (2)	DP-O	-	-
D60	GND	Power Ground	PWR	-	-
D61	PEG_TX3+	PCIexpress Graphics Transmit + (3)	DP-O	-	-
D62	PEG_TX3-	PCIexpress Graphics Transmit - (3)	DP-O	-	-
D63	RSVD	-	nc	-	
D64	RSVD	-	nc	-	
D65	PEG_TX4+	PCIexpress Graphics Transmit + (4)	DP-O	-	-
D66	PEG_TX4-	PCIexpress Graphics Transmit - (4)	DP-O	-	-
D67	GND	Power Ground	PWR	-	-
D68	PEG_TX5+	PCIexpress Graphics Transmit + (5)	DP-O	-	-
D69	PEG_TX5-	PCIexpress Graphics Transmit - (5)	DP-O	-	-
D70	GND	Power Ground	PWR	-	-
D71	PEG_TX6+	PCIexpress Graphics Transmit + (6)	DP-O	-	-
D72	PEG_TX6-	PCIexpress Graphics Transmit - (6)	DP-O	-	-
D73	SDVO_CLK	SDVO_CTRLCLK	IO-3,3	-	-
D74	PEG_TX7+	PCIexpress Graphics Transmit + (7)	DP-O	-	-
D75	PEG_TX7-	PCIexpress Graphics Transmit - (7)	DP-O	-	-
D76	GND	Power Ground	PWR	-	-
D77	IDE_CBLID	IDE_CBLID# | IDE cable type detect	I/O-	-	opt. int. PU in IDE flash
D78	PEG_TX8+	PCIexpress Graphics Transmit + (8)	DP-O	-	-
D79	PEG_TX8-	PCIexpress Graphics Transmit - (8)	DP-O	-	-
D80	GND	Power Ground	PWR	-	-
D81	PEG_TX9+	PCIexpress Graphics Transmit + (9)	DP-O	-	-
D82	PEG_TX9-	PCIexpress Graphics Transmit - (9)	DP-O	-	-
D83	RSVD	n.c.	nc	-	-
D84	GND	Power Ground	PWR	-	-
D85	PEG_TX10+	PCIexpress Graphics Transmit + (10)	DP-O	-	-
D86	PEG_TX10-	PCIexpress Graphics Transmit - (10)	DP-O	-	-
D87	GND	Power Ground	PWR	-	-
D88	PEG_TX11+	PCIexpress Graphics Transmit + (11)	DP-O	-	-
D89	PEG_TX11-	PCIexpress Graphics Transmit - (11)	DP-O	-	-
D90	GND	Power Ground	PWR	-	-
D91	PEG_TX12+	PCIexpress Graphics Transmit + (12)	DP-O	-	-
D92	PEG_TX12-	PCIexpress Graphics Transmit - (12)	DP-O	-	-
D93	GND	Power Ground	PWR	-	-
D94	PEG_TX13+	PCIexpress Graphics Transmit + (13)	DP-O	-	-
D95	PEG_TX13-	PCIexpress Graphics Transmit - (13)	DP-O	-	-
D96	GND	Power Ground	PWR	-	-
D97	PEG_ENABLE#	PCIexpress Graphics Enable	I-3,3	PU 10k 3,3V	-
D98	PEG_TX14+	PCIexpress Graphics Transmit + (14)	DP-O	-	-
D99	PEG_TX14-	PCIexpress Graphics Transmit - (14)	DP-O	-	-
D100	GND	Power Ground	PWR	-	-
D101	PEG_TX15+	PCIexpress Graphics Transmit + (15)	DP-O	-	-
D102	PEG_TX15-	PCIexpress Graphics Transmit - (15)	DP-O	-	-
D103	GND	Power Ground	PWR	-	-
D104	VCC_12V	12V VCC	PWR	-	-
D105	VCC_12V	12V VCC	PWR	-	-
D106	VCC_12V	12V VCC	PWR	-	-
D107	VCC_12V	12V VCC	PWR	-	-
D108	VCC_12V	12V VCC	PWR	-	-
D109	VCC_12V	12V VCC	PWR	-	-
D110	GND	Power Ground	PWR	-	-

Note: The termination resistors in this table are already mounted on the ETXexpress® board. Refer to the design guide for information about additional termination resistors.

4.2.9 Alternative Pinout of HDMI

Pin Nr.	Pin Name PCIexpress	Pin Name HDMI	HDMI Pin Description
D61	PCIexpress Graphics Transmit + 3	TMDS_B_CLK	HDMI Port B Clock
D62	PCIexpress Graphics Transmit - 3	TMDS_B_CLK#	HDMI port B Clock complement
D58	PCIexpress Graphics Transmit + 2	TMDS_B_DATA0	HDMI port B Data0
D59	PCIexpress Graphics Transmit - 2	TMDS_B_DATA0#	HDMI port B Data0 complement
D55	PCIexpress Graphics Transmit + 1	TMDS_B_DATA1	HDMI port B Data1
D56	PCIexpress Graphics Transmit - 1	TMDS_B_DATA1#	HDMI port B Data1 complement
D52	PCIexpress Graphics Transmit + 0	TMDS_B_DATA2	HDMI port B Data2
D53	PCIexpress Graphics Transmit - 0	TMDS_B_DATA2#	HDMI port B Data2 complement
C61	PCIexpress Graphics Receive + 3	TMDS_B_HPD#	HDMI port B Hot-plug detect
D74	PCIexpress Graphics Transmit + 7	TMDS_C_CLK	HDMI port C Clock
D75	PCIexpress Graphics Transmit – 7	TMDS_C_CLK#	HDMI port C Clock complement
D71	PCIexpress Graphics Transmit + 6	TMDS_C_DATA0	HDMI port C Data0
D72	PCIexpress Graphics Transmit – 6	TMDS_C_DATA0#	HDMI port C Data0 complement
D68	PCIexpress Graphics Transmit + 5	TMDS_C_DATA1	HDMI port C Data1
D69	PCIexpress Graphics Transmit – 5	TMDS_C_DATA1#	HDMI port C Data1 complement
D65	PCIexpress Graphics Transmit + 4	TMDS_C_DATA2	HDMI port C Data2
D66	PCIexpress Graphics Transmit – 4	TMDS_C_DATA2#	HDMI port C Data2 complement
C74	PCIexpress Graphics Receive + 7	TMDS_C_HDP#	HDMI port C Hot-plug detect

4.2.10 Alternative Pinout of Display Port

Pin Nr.	Pin Name PCIexpress	Pin Name HDMI	HDMI Pin Description
D61	PCIexpress Graphics Transmit + 3	DPB_LANE3	Displayport B Lane3
D62	PCIexpress Graphics Transmit – 3	DPB_LANE3#	Displayport B Lane3 complement
D58	PCIexpress Graphics Transmit + 2	DPB_LANE2	Displayport B Lane2
D59	PCIexpress Graphics Transmit – 2	DPB_LANE2#	Displayport B Lane2 complement
D55	PCIexpress Graphics Transmit + 1	DPB_LANE1	Displayport B Lane1
D56	PCIexpress Graphics Transmit - 1	DPB_LANE1#	Displayport B Lane1 complement
D52	PCIexpress Graphics Transmit + 0	DPB_LANE0	Displayport B Lane0
D53	PCIexpress Graphics Transmit – 0	DPB_LANE0#	Displayport B Lane0 complement
C61	PCIexpress Graphics Receive + 3	DPB_HPD#	Displayport B Hot-plug detect
C58	PCIexpress Graphics Receive + 2	DPB_AUX	Displayport B Aux
C59	PCIexpress Graphics Receive – 2	DPB_AUX#	Displayport B Aux complement
D74	PCIexpress Graphics Transmit + 7	DPC_LANE3	Displayport C Lane3
D75	PCIexpress Graphics Transmit – 7	DPC_LANE3#	Displayport C Lane3 complement
D71	PCIexpress Graphics Transmit + 6	DPC_LANE2	Displayport C Lane2
D72	PCIexpress Graphics Transmit – 6	DPC_LANE2#	Displayport C Lane2 complement
D68	PCIexpress Graphics Transmit + 5	DPC_LANE1	Displayport C Lane1
D69	PCIexpress Graphics Transmit – 5	DPC_LANE1#	Displayport C Lane1 complement
D65	PCIexpress Graphics Transmit + 4	DPC_LANE0	Displayport C Lane0
D66	PCIexpress Graphics Transmit – 4	DPC_LANE0#	Displayport C Lane0 complement
C74	PCIexpress Graphics Receive + 7	DPC_HPD#	Displayport C Hot-plug detect
C71	PCIexpress Graphics Receive + 6	DPC_AUX	Displayport C Aux
C72	PCIexpress Graphics Receive – 6	DPC_AUX#	Displayport C Aus complement
D88	PCIexpress Graphics Transmit + 11	DPD_LANE3	Displayport D Lane3
D89	PCIexpress Graphics Transmit – 11	DPD_LANE3#	Displayport D Lane3 complement

D85	PCIexpress Graphics Transmit + 10	DPD_LANE2	Displayport D Lane2
D86	PCIexpress Graphics Transmit – 10	DPD_LANE2#	Displayport D Lane2 complement
D81	PCIexpress Graphics Transmit + 9	DPD_LANE1	Displayport D Lane1
D82	PCIexpress Graphics Transmit – 9	DPD_LANE1#	Displayport D Lane1 complement
D78	PCIexpress Graphics Transmit + 8	DPD_LANE0	Displayport D Lane0
D77	PCIexpress Graphics Transmit – 8	DPD_LANE0#	Displayport D Lane0 complement
C88	PCIexpress Graphics Receive + 11	DPD_HPD#	Displayport D Hot-plug detect
C85	PCIexpress Graphics Receive + 10	DPD_AUX	Displayport D Aux
C86	PCIexpress Graphics Receive – 10	DPD_AUX#	Displayport D Aus complement

4.3 Signal Description

4.3.1 PCIexpress x1 lanes

The PCI express x1 lanes is a fast connection interface for many different system devices, such as network controllers, I/O controllers or express card devices. The implementation of this subsystem complies with the ETXexpress® / COMexpress™ Specification. Implementation information is provided in the COMexpress™ Design Guide. Refer to the documentation for additional information.

The microETXexpress®-PC has 5 PCIexpress x1 Lanes.

4.3.2 USB

Eight USB ports (EHCI high-speed 2.0 controller) are connected to the module connector. The USB controllers comply with both versions 1.1 and 2.0 of the USB standard and are backward compatible.

Configuration

The USB controllers are PCI bus devices. The BIOS allocates required system resources during configuration of the PCI bus.

4.3.3 SATA

The Intel® ICH-9M south bridge device offers the possibility to connect 4 SATA Harddisks. One of it is used to provide a parallel ATA interface and therefore 3 SATA ports are routed to the module connector. The SATA port provide 300 MB/s per channel and offers NCQ, HotPlug, Staggered Spinup, eSATA and PortMultiplier in AHCI mode.

Configuration

The SATA controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI bus.

4.3.4 Audio

The microETXexpress®-PC HD audio controller is integrated in the Intel® ICH-9M Southbridge.

Warning:	Baseboards with AC'97 codec only are not supported.

Configuration

The audio controller is a PCI bus device. The BIOS allocates required system resources during configuration of the PCI device.

4.3.5 Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine is in "Continuous Mode"

4.3.6 VGA Output

The microETXexpress®-PC graphics subsystem is integrated in the Intel® GS45 northbridge.

Configuration

The graphics controller requires the following resources:

- An IRQ
- Several I/O addresses
- Memory-address blocks in high memory

The BIOS allocates the resources during AGP configuration. Many resources are set for compatibility with industry-standard settings.

4.3.7 LVDS Flat Panel Interface (JILI)

The user interface for flat panels is the JUMPtec Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the ETXexpress® Specification. Implementation information is provided in the COMexpress™ Design Guide. Refer to the documentation for additional information.

4.3.8 PCIexpress Graphics

The PCI express Graphics interface allows the connection of high performace graphics chips on a high bandwidth interface.

The implementation of this subsystem complies with the COMexpress Specification. Implementation information is provided in the COMexpress™ Design Guide. Refer to the documentation for additional information.

4.3.9 SDVO

The microETXexpress®-PC Serial Digital Video Output port is integrated in the Intel® GS45 northbridge. It has the following features:

- Share its pins with the PEG interface
- Serial Digital Video Out Port (DVOB & DVOC) support
- Two 12-bit channels
- The SDVO B/C ports can drive a variety of SDVO devices (TV-Out Encoders, TMDS and LVDS transmitters, etc.)

The implementation of this subsystem complies with the COMexpress™ Specification. Implementation information is provided in the COMexpress™ Design Guide. Refer to the documentation for additional information.

4.3.10 HDMI

There is one HDMI port available shared together with PCIexpress Graphics, SDVO and Displayport.

4.3.11 Displayport

The display port is available shared together with PCIexpress Graphics, SDVO and HDMI.

4.3.12 Ethernet

The Ethernet interface offers 10 Mbit, 100Mbit or 1Gbit connection and is driven by the Intel® 82567 PCIexpress Gbit Ethernet controller.

Configuration

The Ethernet controller is a PCIexpress bus device. The BIOS allocates required system resources during configuration of the PCIexpress device.

4.3.13 Power Control

Power Good / Reset Input

The microETXexpress®-PC provides an external input for a power-good signal or a manual- reset pushbutton. The implementation of this subsystem complies with the COMexpress™ Specification. Implementation information is provided in the COMexpress™ Design Guide. Refer to the documentation for additional information.

4.3.14 Power Management

ATX PS Control

The microETXexpress®-PC can control the main power output of an ATX-style power supply. The implementation of this subsystem complies with the COMexpress™ Specification. Implementation information is provided in the COMexpress™ Design Guide. Refer to the documentation for additional information.

External SMI Interrupt

Contact Kontron Embedded Modules technical support for information on this feature.

4.3.15 Miscellaneous Circuits

Speaker

The implementation of the speaker output complies with the COMexpress™ Specification. Implementation information is provided in the COMexpress™ Design Guide. Refer to the documentation for additional information.

Battery

The implementation of the battery input complies with the COMexpress™ Specification. Implementation information is provided in the COMexpress™ Design Guide. Refer to the documentation for additional information.

In compliance with EN60950, there are at least two current-limiting devices (resistor and diode) between the battery and the consuming component.

4.3.16 I2C Bus

The I2C Bus is implemented by using the onboard CPLD which offers fast speed a multimaster capability.

You also can access the I2C Bus via JUMPtec's Intelligent Device Architecture (JIDA) BIOS functions.

For additional information, refer to the COMexpress™ Design Guide, I2C application notes and JIDA specifications which are available at the Kontron Web site.

SM Bus

System Management (SM) bus signals are connected to the SM bus controller, which is located in the Intel® ICH-9M device. For more information about the SM bus, please see the System Management (SM) Bus section in the System Resources chapter.

LPC Bus

The Low Pin Count Interface signals are connected to the LPC Bus bridge, which is located in the Intel® ICH-9M. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller, which typically combine legacy-device support into a single IC. The implementation of this subsystem complies with the COMexpress™ Specification. Implementation information is provided in the COMexpress™ Design Guide. Refer to the documentation for additional information.

PCI Bus

The implementation of this subsystem complies with the COMexpress™ Specification. Implementation information is provided in the COMexpress™ Design Guide. Refer to the documentation for additional information.

IDE Port

The IDE host adapter is PIO mode 0 - 4 and UDMA mode 0 - 7.

Configuration

The IDE host adapter is a SATA to IDE converter. It is configured by the BIOS during PCI device configuration. You can disable it in setup. Resources used by the host adapter are compatible with the PC/AT.

Warning:	It is not possible to use 2 IDE devices on the IDE port. Only master operation is possible. The SATA port where the IDE converter is connected to relies on the mode setting in the BIOS and therefore a SATA driver on IDE might be necessary when switched to AHCI or RAID mode.

5 Special Features

5.1 Watchdog Timer

This feature is implemented in a watchdog PIC. You can configure the Watchdog Timer (WDT) in BIOS setup to start after a set amount of time after power-on boot. The WDT can also be controlled by the JIDA32 Library API (Refer to Appendix F: JIDA Standard). The application software should strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

Configuration

You can program the timeout period for the watchdog timer in two ranges:

- 1-second increments from 1 to 255 seconds
- 1-minute increments from 1 to 255 minutes

The watchdog can be programmed via the JIDA API and via the BIOS setup. Triggering is possible via JIDA API.

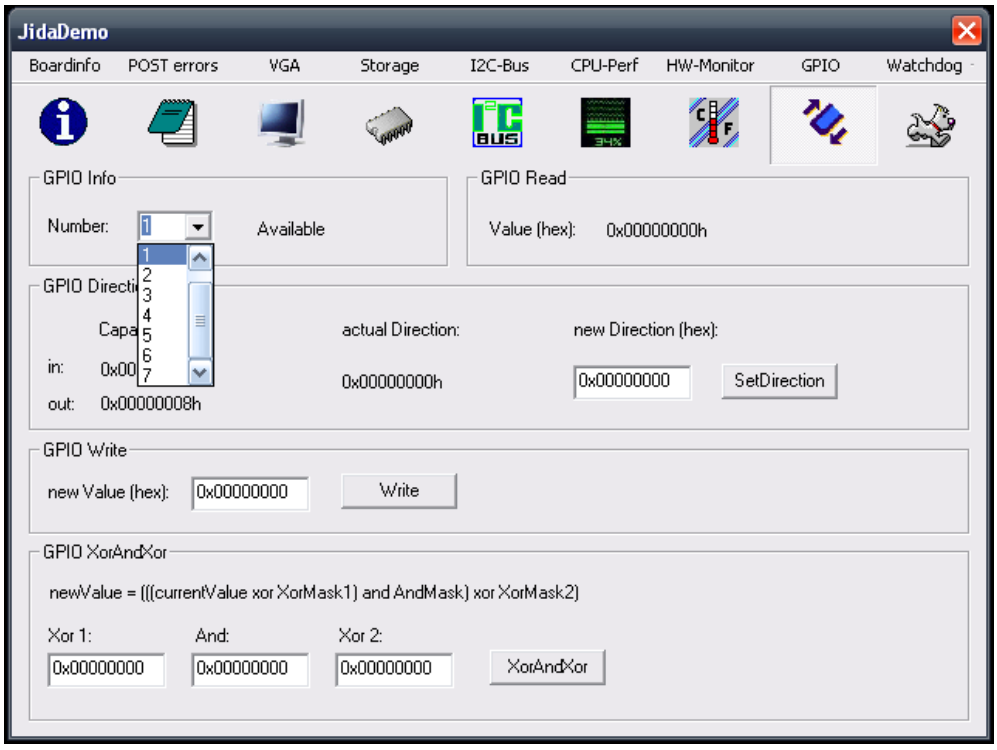
5.2 GPIO - General Purpose Input and Output

microETXexpress®-PC offers 4 General Purpose Input (GPI) pins and 4 General Purpose Output (GPO) pins. On a 3.3V level digital in- and outputs are available.

Signal	Pin	Description
GPI0	A54	General Purpose Input 0
GPI1	A63	General Purpose Input 1
GPI2	A67	General Purpose Input 2
GPI3	A85	General Purpose Input 3
GPO0	A93	General Purpose Output 0
GPO1	B54	General Purpose Output 1
GPO2	B57	General Purpose Output 2
GPO3	B63	General Purpose Output 3

Configuration

The GPI and GPO pins can be configured via JIDA32. Please refer to the JIDA32 manual in the driver download packet on our website.

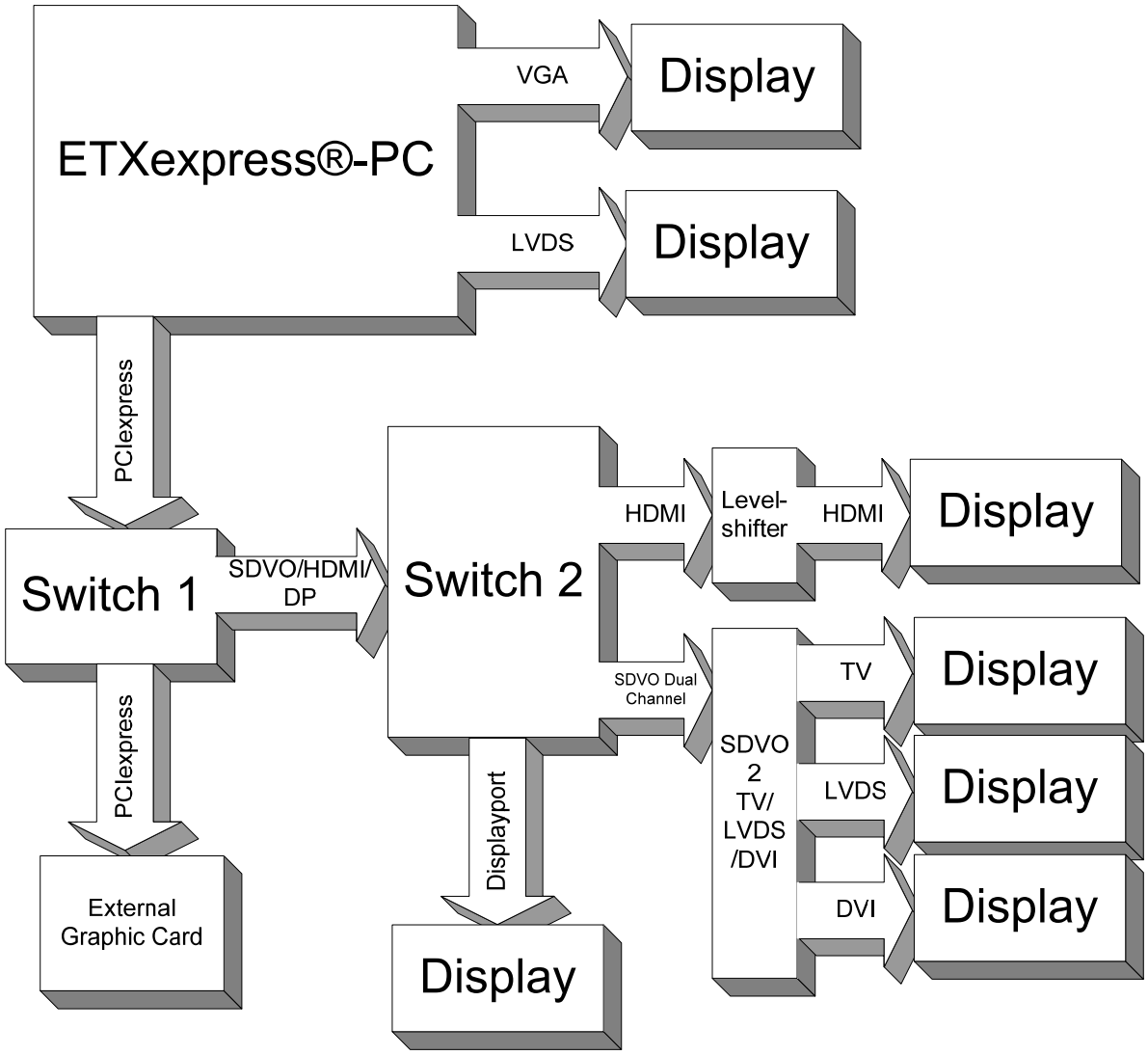


5.3 Usage of Different Graphic interfaces

5.4 Available Graphic interfaces

The microETXexpress®-PC offers VGA, PCIexpress, LVDS, HDMI, SDVO and Displayport interfaces to connect graphical user interfaces. The usage of VGA, PCIexpress and SDVO complies with the current COMexpress™ Specification.

The principle of using them is shown in the next drawing.



VGA and LVDS interface is always available and can be used. The pins of PCIexpress Graphics either are used as PCIexpress Graphics or as HDMI/SDVO/DP, which is controlled by switch1.

Switch1 is the SDVO_SDA# line (C73). When this signal is high (2.5V) the SDVO/HDMI/DP output is enabled. Otherwise the lines can be used as PCIexpressGraphic.

The switch 2 to select HDMI, SDVO or Displayport consists of the devices detected on the regarding sense circuits. When there is an SDVO 2 TV/LVDS/DVI converter found on the SDVO_DATA and _CLK lines (C73; D73) then the output

is switched to SDVO. When there is Displayport device found on the Displayport AUX lines (C71; C72) then it is Display port and in any other case the output is switched to HDMI.

6 Design Consideration

6.1 Thermal Management

A heat-spreader plate assembly is available from Kontron Embedded Modules for the microETXexpress®-PC. The heat-spreader plate on top of this assembly is NOT a heat sink. It works as a COMexpress™-standard thermal interface to use with a heat sink or other cooling device.

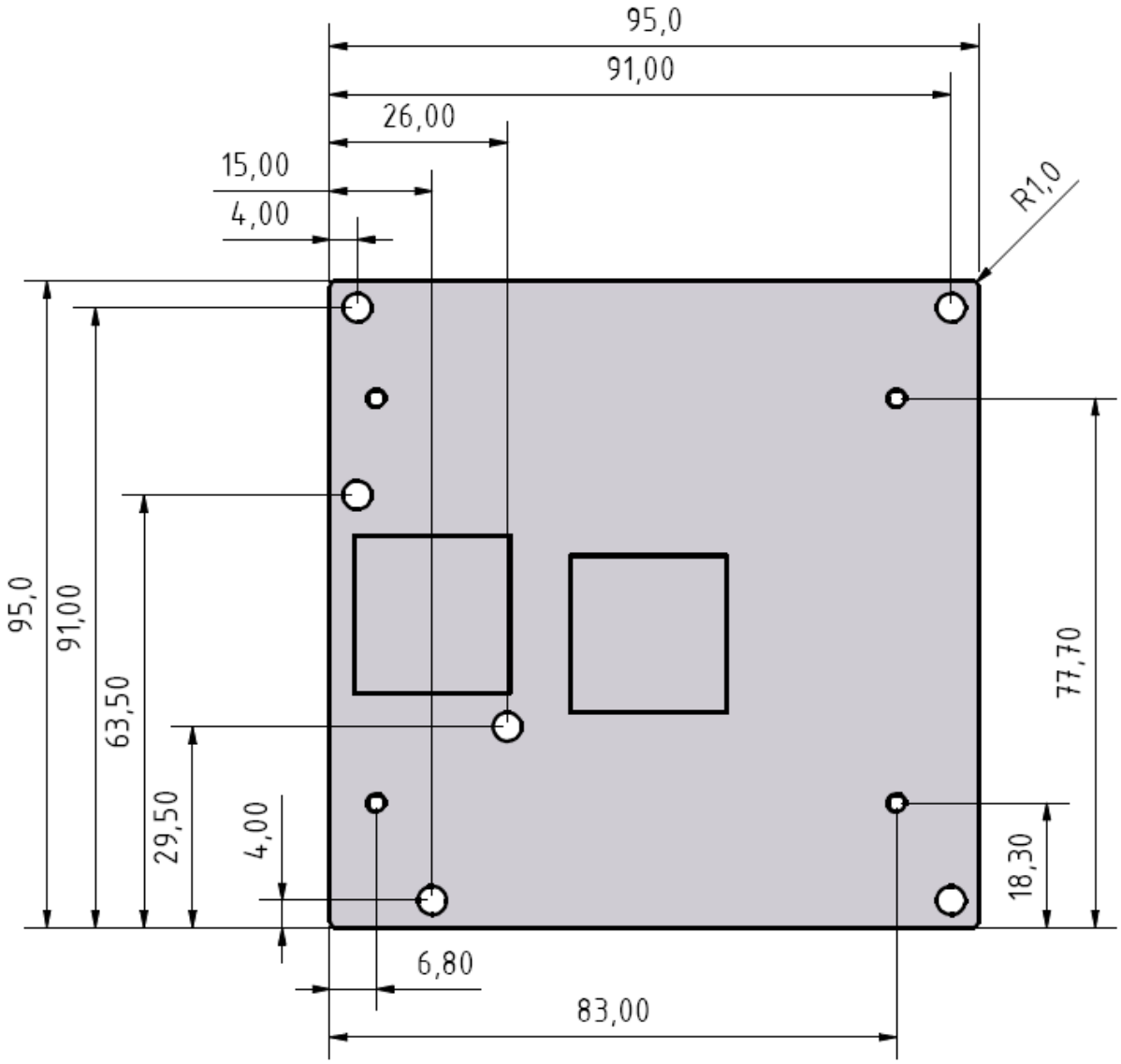
External cooling must be provided to maintain the heat-spreader plate at proper operating temperatures. Under worst-case conditions, the cooling mechanism must maintain an ambient air and heat-spreader plate temperature of 60° C or less.

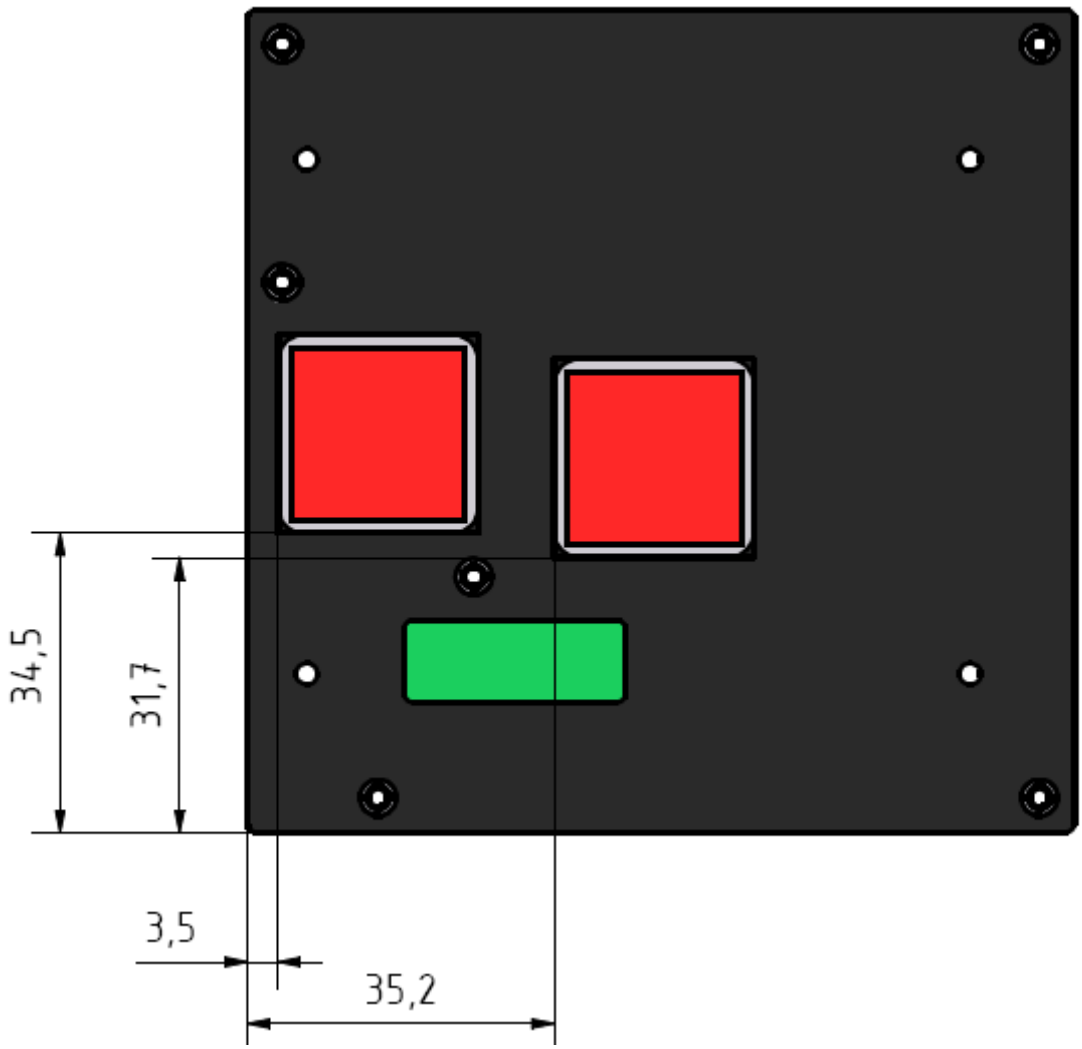
The aluminum slugs and thermal pads on the underside of the heat-spreader assembly implement thermal interfaces between the heat spreader plate and the major heat-generating components on the microETXexpress®-DC. About 80 percent of the power dissipated within the module is conducted to the heat-spreader plate and can be removed by the cooling solution.

You can use many thermal-management solutions with the heat-spreader plates, including active and passive approaches. The optimum cooling solution varies, depending on the COMexpress™ application and environmental conditions. Please see the COMexpress™ Design Guide for further information on thermal management.

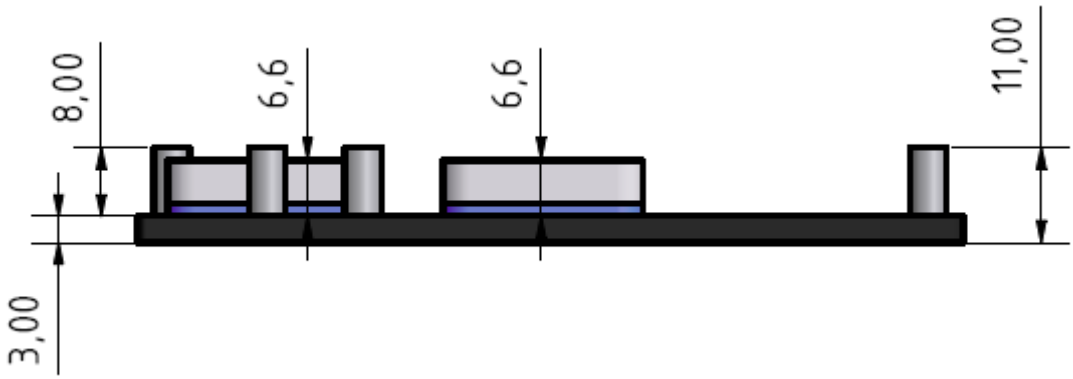
6.2 Heatspreader Dimension

This is the backside view of the heatspreader plat with pads marked for the heat generating components for microETXexpress®-PC Modules.





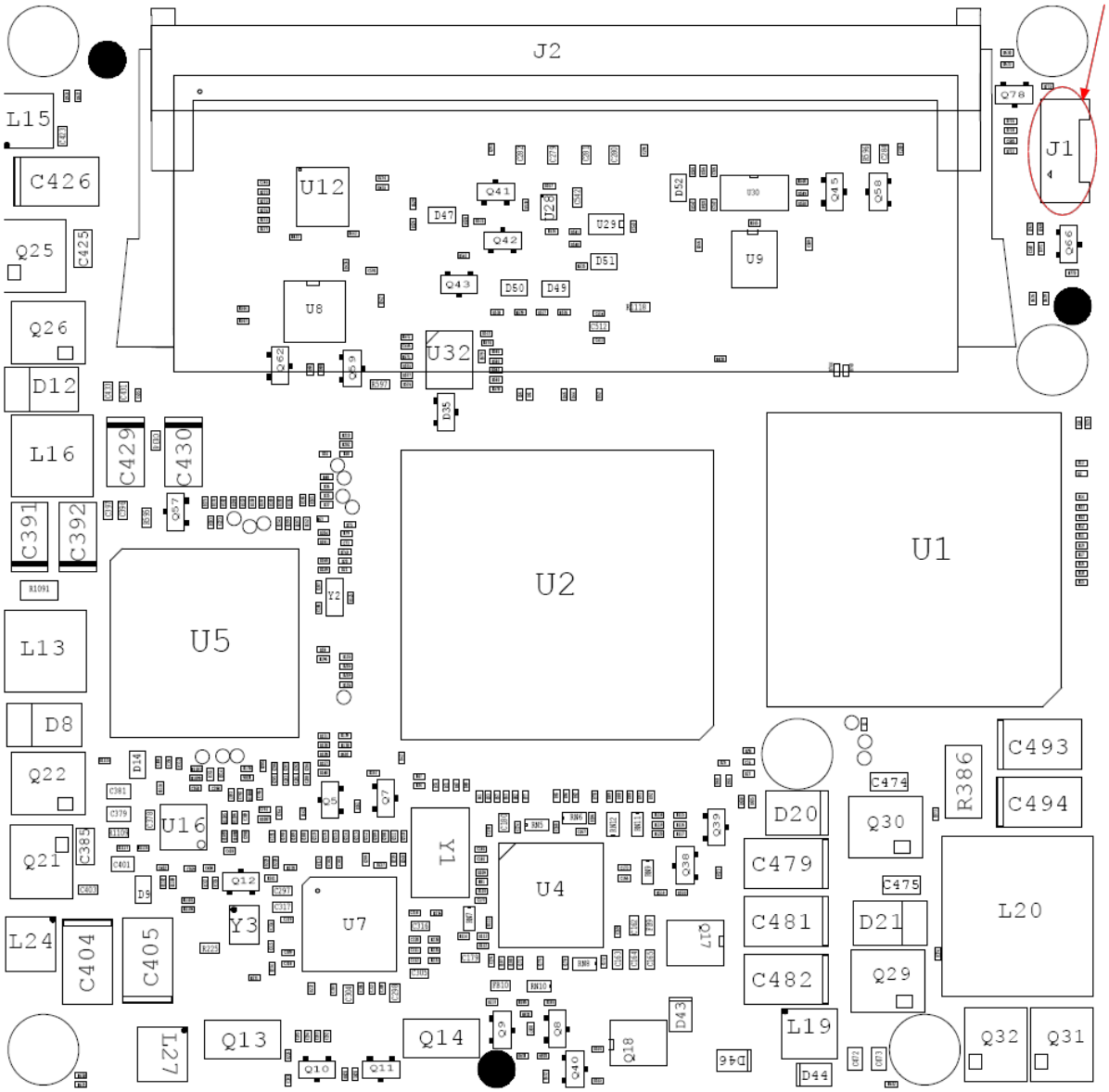
Sideview of the heat spreader:



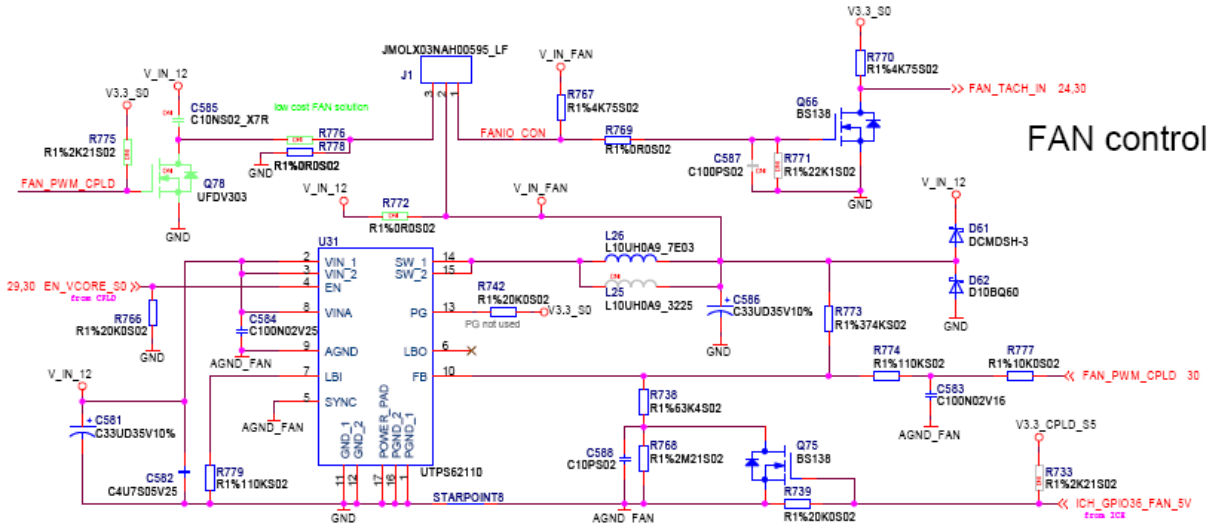
6.3 microETXexpress®-PC onboard fan connector

This section describes how to connect a fan to the connector located directly on the microETXexpress®-PC. With certain BIOS-settings it is possible to control the fan depending on the Active Trip Point temperature. The fan switches on/off depending on the adjusted Active Trip Point temperature. In order for this feature to function properly an ACPI compliant OS is necessary.

6.3.1 Location and pinout of fan connector



The onboard fan connector (J1) can be found at the right side nearby the DRAM socket and it is connected onboard according to the following schematic:



Connector J1 has following specification:

- Part number (Molex) J8: 53261-0390
- Mates with: 51021-0300
- Crimp terminals: 50079-8100

6.3.2 BIOS Settings for fan control

6.3.3 Electrical Characteristics

- VCC in FANCON: VCC of board, limited to 12V max
- Imax: 0,40 A

Note:	The VCC_in_FANCON output is not short circuit proof. If necessary the user has to ensure that the circuit is protected externally, for example by a fuse on the backplane.

7 System Ressources

8 BIOS Operation

The module is equipped with AMI® BIOS, which is located in an onboard SPI serial flash memory. You can update the BIOS using a Flash utility.

8.1 Determining the BIOS Version

To determine the AMI® BIOS version, immediately press the Pause key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

- AMIBIOS © 2006 American Megatrends, Inc.
- BIOS Date: 06/16/08 10:52:49 Ver: 08.00.14
- Kontron® BIOS Version <UNTGRXXX>
- © Copyright 2002-2008 Kontron Embedded Modules GmbH

8.2 Setup Guide

The AMIBIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

Note:	Selecting incorrect values may cause system boot failure. Load setup default values to recover by pressing <F9>.

8.2.1 Start AMI® BIOS Setup Utility

To start the AMI® BIOS setup utility, press <DEL> when the following string appears during bootup.

Press <DEL> to enter Setup

The Info Menu then appears.

The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Right side Bottom	Lists setup navigation keys.
Item Specific Help Window	Right side Top	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and – keys to select a value for that field. The Save Value commands in the Exit menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▸) marks all submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> or <Alt-F1> on a menu brings up the General Help window that describes the legend keys and their alternates. Press <Esc> to exit the General Help window.

8.3 BIOS Setup

9 Appendix A: JIDA Standard

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jumptec Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

- AH=Eah
- AL=function number
- DX=4648h (security word)
- CL=board number (starting with 1)

The interrupt returns a CL□0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

9.1 JIDA Information

To obtain information about boards that follow the JIDA standard, use the following procedure.

- Call Get BIOS ID with CL=1. The name of the first device installed will be returned. If you see the result Board exists (CL=0), increment CL, and call Get BIOS ID again.
- Repeat until you see Board not present (CL□0). You now know the names of all boards within your system that follow the JIDA standard.
- You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

Note:	Association between board and board number may change because of configuration changes. Do not rely on any association between board and board number. Always use the procedure described above to determine the association between board and board number.

Refer to the JIDA manual in the jidai1xx.zip folder, which is available from the Kontron Embedded Modules GmbH Web site, for further information on implementing and using JIDA calls with C sample code.

10 Appendix B: Architecture Information

The following sources of information can help you better understand PC architecture.

10.1 Buses

10.1.1 ISA, Standard PS/2 – Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

10.1.2 PCI/104

- Embedded PC 104 Consortium
- The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
- The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- PCI & PCI-X Hardware and Software Architecture & Design, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- PCI System Architecture, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

10.2 General PC Architecture

- Embedded PCs, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- Hardware Bible, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- Interfacing to the IBM Personal Computer, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- The Indispensable PC Hardware Book, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

10.3 Ports

10.3.1 RS-232 Serial

» EIA-232-E standard

» The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.

» RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3

» National Semiconductor: The Interface Data Book includes application notes. Type “232” as search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

10.3.2 Serial ATA

Serial AT Attachment (ATA) Working Group. This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web. We recommend you also search the Web for information on 4.2 I/O cable, if you use hard disks in a DMA3 or PIO4 mode.

10.3.3 USB

USB Specification

USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

10.4 Programming

» C Programmer’s Guide to Serial Communications, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0

» Programmer’s Guide to the EGA, VGA, and Super VGA Cards, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4

» The Programmer’s PC Sourcebook, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X

» Undocumented PC, A Programmer’s Guide to I/O, CPUs, and Fixed Memory Areas, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

11 Appendix C: Document Revision History

Revision	Date	Edited by	Changes
001	22.06.09	UMA	Preliminary release

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