QSFP+

Active Optical Cable Assembly

USER'S MANUAL

COVERING:

QSFPO Series

JANUARY 2014

COPYRIGHTS, TRADEMARKS AND PATENTS

Product names used herein are trademarks of their respective owners. All information and material in this publication are property of Samtec, Inc. All related rights are reserved. Samtec, Inc. does not authorize customers to make copies of the content for any use.

Terms of Use

Use of this publication is limited to viewing the pages for evaluation or purchase. No permission is granted to the user to copy, print, distribute, transmit, display in public, or modify the contents of this document in any way.

Disclaimer

The information in this publication may change without notice. All materials published here are "As Is" and without implied or express warranties. Samtec, Inc. does not warrant that this publication will be without error, or that defects will be corrected. Samtec, Inc. makes every effort to present our customers an excellent and useful publication, but we do not warrant or represent the use of the material here in terms of their accuracy, reliability or otherwise. Therefore, you agree that all access and use of this publication's content is at your own risk.

Patents

Patents pending on technologies used within this product.

NEITHER SAMTEC, INC. NOR ANY PARTY INVOLVED IN CREATING, PRODUCING, OR DELIVERING THIS PUBLICATION SHALL BE LIABLE FOR ANY DIRECT, INCIDENTAL, CONSEQUENTIAL, INDIRECT, OR PUNITIVE DAMAGES ARISING OUT OF YOUR ACCESS, USE OR INABILITY TO ACCESS OR USE THIS PUBLICATION, OR ANY ERRORS OR OMISSIONS IN ITS CONTENT.

TABLE OF CONTENTS

c UL us LISTED
FILE NO. E357212 I.T.E.

INTRODUCTION

Product Features

QSFPO Series Active Optical Cables (AOCs) are 4-channel bidirectional optical assemblies for QSFP+ applications and are designed to meet the requirements of modern optical based interconnects. Each AOC offers 4 independent transmit and receive channels carrying 850 nm signals across standard multi-mode fibers. Two different series are available providing an aggregate bandwidth of up to 40 Gbps (QSFPO-40G Series) or 56 Gbps (QSFPO-56G Series).

The electrical interface is a standard QSFP+ 38 contact edge type connector and is electrically compliant with the SFI+ and PPI interface supporting InfiniBand™, Ethernet, Fibre Channel and other protocols. The connector is hot pluggable and provides I^2C serial access via an on-board microcontroller.

Figure 1:
QSFP+ Active Optical Cable Assembly

INTRODUCTION

Applications

The QSFP+ AOC comes pre-tested and can be used as a direct replacement for traditional copper cables but with the added benefit of a lighter weight and smaller diameter solution for cable lengths from 1 to 100 m. It can also be used to replace a pair of transceivers proving equivalent performance at a lower cost.

The QSFPO-40G Series AOC complies with the standard for InfiniBand™ QDR and Ethernet 40 GbE (40 Gigabit Ethernet) applications and is listed on the InfiniBand™ Trade Association's Approved Integrator's List for lengths from 1 to 100 m.

The QSFPO-56G Series AOC provides the same capabilities as the QSFPO-40G Series, but provides a higher data rate and the ability to reconfigure the output voltage amplitude. It complies with the InfiniBand™ FDR standard and is listed on the InfiniBand™ Trade Association's Approved Integrator's List for lengths from 1 to 100 m.

FUNCTIONAL DESCRIPTION

The QSFP+ AOC has a miniature optical engine embedded into each end of the cable assembly. The engines interconnect 4 independent transmit / receive lanes. An on-board microcontroller provides control, diagnostic and monitoring for the cable functions, as well as the external I²C serial communication interface.

A functional block diagram of the engine is shown in Figure 2. The transmitter section consists of a 4-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 4-channel input buffer and laser driver. The receiver section consists of a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4-channel output buffer.

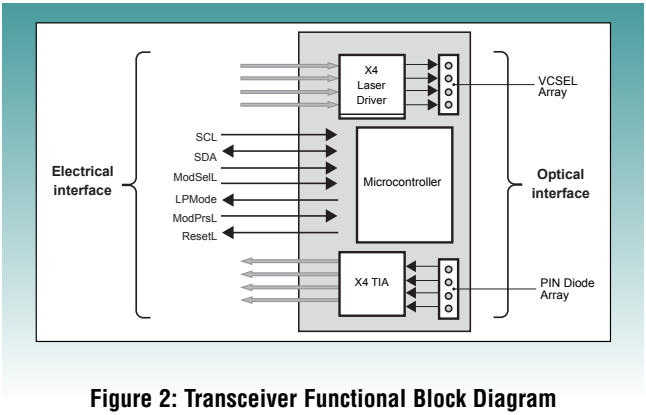


Figure 2: Transceiver Functional Block Diagram

Transmitter Block

The optical transmit portion of the engine incorporates a 4-channel VCSEL array, a 4-channel input buffer and laser driver, diagnostic monitors, control and bias blocks. The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100Ω. AC coupling capacitors are located on the optical engine board and therefore are not required on the host board. An LVTTL compatible Two-Wire Serial (or I²C) interface is provided for module control and diagnostics. Status, alarm and fault information are available via the TWS interface. To reduce the need for polling, a hardware interrupt signal is provided to inform hosts of an assertion of an alarm, Loss of Signal (LOS) and Transmitter (Tx) fault.

FUNCTIONAL DESCRIPTION

Receiver Block

The optical receiver portion of the engine incorporates a 4-channel PIN photodiode array, a 4-channel TIA array, a 4-channel output buffer, diagnostic monitors, control, and bias blocks. The Receiver Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50Ω to AC ground and 100Ω differentially that should be differentially terminated with 100Ω. Again, AC coupling capacitors are located on the optical engine and are therefore not required on the host board.

Management Interface

The internal optical engine provides digital diagnostics and control/monitor functions, as specified in SFF-8436. A microcontroller, which can be accessed through the Two-Wire interface, monitors and reports this information. The functionality of the Two-Wire interface is specified in the SFF-8436 specification.

The following module and channel digital diagnostic parameters are provided for monitoring:

- Transceiver Temperature
- Transceiver Supply Voltage

The microcontroller will generate an Interrupt Flag, by asserting the IntL signal, when an operational fault occurs. The host can identify the source of the interrupt by reading the appropriate registers through the Two-Wire interface. The following Interrupt Flags are provided:

- Rx LOS - Provided for each channel, which indicates that the optical power input into the receiver has dropped below a minimum allowed value
- Tx Fault - Provided for each channel, which indicates that a fault condition relating to either the laser or one of the optical modulators has occurred
- Transceiver Temperature High and Low Alarm, and, High and Low Warning
- Transceiver Supply Voltage High and Low Alarm, and, High and Low Warning

SPECIFICATIONS

Common Electrical Characteristics

The maximum operating and storage conditions are shown in Table 1. Any stress beyond these maximum ratings may result in permanent damage to the device.

Table 1: Absolute Maximum Rating

Specifications	Symbol	Unit	Min	Max	Notes
Storage Temperature Range	T_{sto}	°C	-40	85	
Powered Case Temperature	T_{case}	°C	0	70	Heat sink temperature
Operating Humidity	RH	%	5	90	Noncondensing
Supply Voltage Range	V_{CC1}	V	0.5	4.0	

Specifications listed in this documentation are only guaranteed when the QSFP+ AOC is operated under the recommended operating conditions listed in Table 2.

Table 2: Recommended Operating Conditions

Specifications	Symbol	Unit	Min	Max	Notes
Operating Case Temperature	T_{case}	°C	0	70	Heat sink temperature
Power Supply Voltage	V_{CC1}	V	3.15	3.45	
DC Common Mode Voltage	V_{CM}	V	0	3.6	
Per Channel Data Rate (40G series)		Gbps	1	10.5	
Per Channel Data Rate (56G series)		Gbps	1	14.1	

In addition to the recommended operating conditions, the power supply requirements are shown in Table 3.

Table 3: Power Supply Requirements

Specifications	Symbol	Unit	Min	Max	Notes
Power Supply Voltage	V_{CC1}	V	3.15	3.45	
Power Supply Current	I_{CC1}	mA	240 typical		
Power Consumption		W		1.0	0.8 W typical
Power Supply Noise including Ripple		mV		50	1 kHz to frequency of operation measured at Vcc host

The QSFP+ specification recommends the use of a host board power supply filter to reduce power supply noise. The recommended power supply filter is shown in Figure 3.

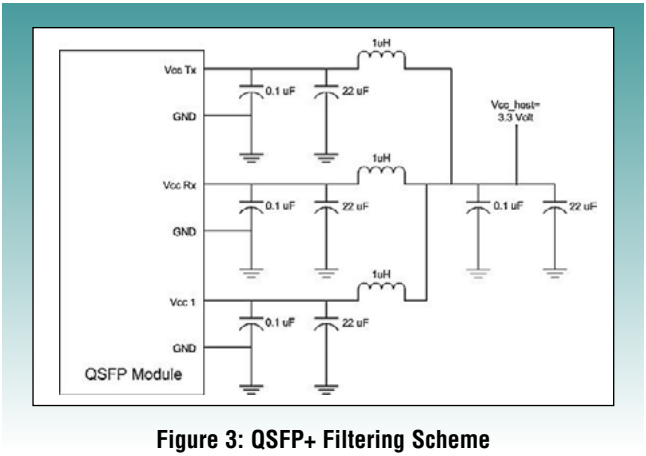


Figure 3: QSFP+ Filtering Scheme

SPECIFICATIONS

High Speed Electrical Characteristics: QSFPO-40G Series

The electrical requirements for input signal into the QSFPO-40G Series are defined for the transmit side in Table 4. With inputs into the AOC that meet these requirements, the output parameters shown in Table 5 are guaranteed.

Table 4: QSFPO-40G Series Electrical Input Requirements

Specifications	Symbol	Unit	Min	Max	Notes
Data Rate per Channel		Gbps	1	10.5	
Differential Input Amplitude	V_{DI}	mV	150	1600	Peak-to-peak differential
Single-ended Voltage Tolerance		V	-0.3	3.8	
AC Common Mode Voltage		mV	15		RMS
Differential Input S-Parameter	S_{DD11}	dB	See Note 1		10 MHz to 11.1 GHz
Reflected Differential to Common Mode Conversion	S_{CD11}	dB		-10	10 MHz to 11.1 GHz
Total Jitter	TJ	UI_{p-p}		0.28	
Data Dependent Jitter	DDJ	UI_{p-p}		0.1	
Data Dependent Pulse Width Shrinkage	DDPWS	UI_{p-p}		0.055	
Uncorrelated Jitter	UJ	UI_{RMS}		0.023	
J2 Jitter Tolerance	J2	UI	0.17		
J9 Jitter Tolerance	J9	UI	0.29		
Eye Mask			See Note 2		Hit ratio = 5×10^{-5}

Notes for Table 4:

1. Maximum S_{DD11} is defined by the formulas:

$0.1 < f < 4.11$ $\quad -12 + 2\sqrt{f}$

$4.11 \leq f < 11.1$ $\quad -6.3 + 13\log_{10}\left(\frac{5.5}{f}\right)$

2. The worst case electrical input is defined by the eye mask:

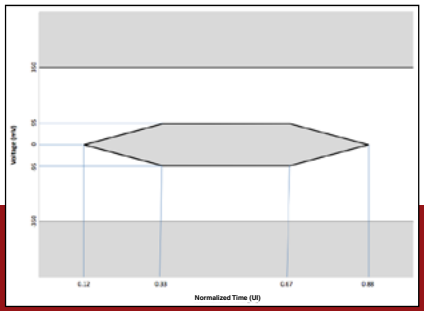


Table 5: QSFPO-40G Series Electrical Output Specification

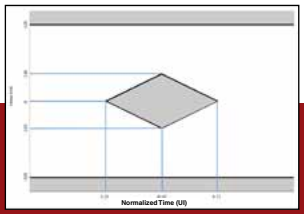
Specifications	Symbol	Unit	Min	Max	Notes
Data Rate per Channel		Gbps	1	10.5	
Termination Mismatch at 1 MHz	ΔZ_M	%		15	
Output AC Common Mode Voltage		mV		7.5	RMS
Single-ended Output Voltage Tolerance		V	-0.3	3.8	
Differential Output Amplitude	V_{DO}	mV	310	750	Peak-to-peak differential
Differential Output Amplitude in Squelched State		mV		50	Peak-to-peak differential
Differential Unsigned Amplitude	V_{diffc}		0.1	0.6	
Common Mode Output Reflection Coefficient	S_{CC22}	dB	See Note 1		10 MHz to 11.1 GHz
Differential Output S-Parameter	S_{DD22}	dB	See Note 2		10 MHz to 11.1 GHz
Output Transition Time	Tr, Tf	ps	28		20% to 80%
Total Jitter	TJ	UI_{p-p}		0.7	
Deterministic Jitter	DJ	UI		0.4	
J2 Jitter		UI_{p-p}		0.42	
J9 Jitter		UI_{p-p}		0.65	
Eye Mask			See Note 3		Hit ratio = 5×10^{-5}
Eye Mask			See Note 3		Hit ratio = 1×10^{-12}

Notes for Table 5:

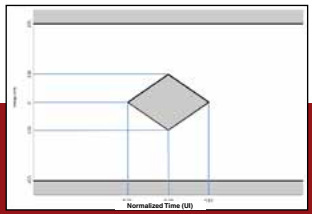
1. Maximum S_{CC22} is defined by the formulas:
   $0.1 < f < 2.5$ $\quad -7 + 1.6f$
   $2.5 \leq f < 11.1$ $\quad -3$

2. Maximum S_{DD22} is defined by the formulas:
   $0.1 < f < 4.11$ $\quad -12 + 2\sqrt{f}$
   $4.11 \leq f < 11.1$ $\quad -6.3 + 13\log_{10}\left(\frac{5.5}{f}\right)$

3. Two eye masks are specified, but are considered to be identical due to the differences in the hit ratio:



Eye Mask for Hot Ratio = 1×10^{-5}



Eye Mask for Hot Ratio = 1×10^{-12}

SPECIFICATIONS

High Speed Electrical Characteristics: QSFPO-56G Series

The electrical requirements for input signal into the QSFPO-56G Series are defined for the transmit side in Table 6. With inputs into the AOC that meet these requirements, the output parameters shown in Table 7 are guaranteed.

Table 6: QSFPO-56G Series Electrical Input Requirements

Specifications	Symbol	Unit	Min	Max	Notes
Data Rate per Channel		Gbps	1	14.2	
Differential Input Amplitude	V_{DI}	mV	250	1600	Peak-to-peak differential
Single-ended Voltage Tolerance		V	-0.3	3.8	
AC Common Mode Voltage		mV	15		RMS
Differential Input Return Loss	S_{DD11}	dB	See Note 1		50 MHz to 14.1 GHz
Common Mode Input Return Loss	S_{CC11}	dB		-2	
Common Mode to Differential Reflection	S_{DC11}		See Note 2		
Reflected Differential to Common Mode Conversion	S_{CD11}	dB		-10	
Total Jitter	TJ	UI_{p-p}		0.28	
Data Dependent Jitter	DDJ	UI_{p-p}		0.1	
Data Dependent Pulse Width Shrinkage	DDPWS	UI_{p-p}		0.11	
J2 Jitter Tolerance	J2	UI	0.19		
J9 Jitter Tolerance	J9	UI	0.34		
Eye Mask			See Note 3		Hit ratio = 5×10^{-5}

Notes for Table 6:

1. Maximum S_{DDxx} is defined by the formula:

   $0.05 < f < 5.6 \qquad -12 + 1.71\sqrt{f}$

2. Maximum S_{DC11} is defined by the formula: $-16 + \frac{2}{3}f$

3. The worst case electrical input is defined by the eye mask:

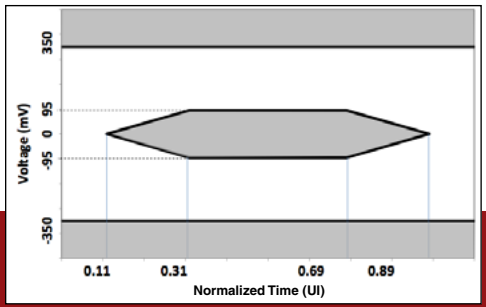


Table 7: QSFPO-56G Series Electrical Output Specification

Specifications	Symbol	Unit	Min	Max	Notes
Data Rate per Channel		Gbps	1	14.2	
Termination Mismatch at 1MHz	ΔZ_M	%		15	
Output AC Common Mode Voltage		mV		20	RMS
Single-ended Output Voltage Tolerance		V	-0.3	3.8	
Differential Output Amplitude in Squelched State		mV		50	Peak-to-peak differential
Differential Unsigned Output Voltage		mV	50, 225		Range 0
			100, 350		Range 1
			150, 450		Range 2
Common Mode Output Reflection Coefficient	S_{CC22}	dB	See Note 1		50 MHz to 15 GHz
Differential Output S-Parameter	S_{DD22}	dB	See Table 6, Note 2		
Common Mode to Differential Reflection	S_{DC22}		See Table 6, Note 2		
Output Transition Time	Tr, Tf	ps	17		20% to 80%
Total Jitter	TJ	UI_{p-p}		0.7	
J2 Jitter		UI_{p-p}		0.44	
J9 Jitter		UI_{p-p}		0.69	
Eye Mask			See Note 2		Hit ratio = 5 x 10^{-5}

Notes for Table 7:

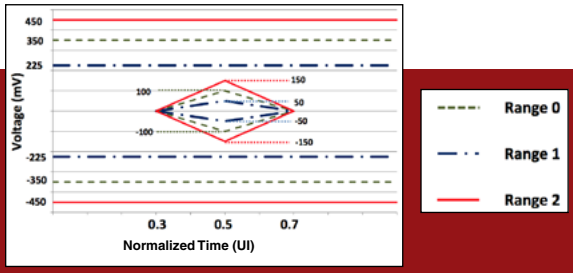
1. Maximum S_{CC22} is defined by the formulas:

   $0.01 < f < 4.1 \qquad -12 + 2\sqrt{f}$

   $11.1 \leq f < 15 \qquad -2$

2. The "InfiniBand™ Architecture Release 1.3" introduces the concept of user selectable output voltage to enable interworking with linear and limiting PHYs. By default, a QSFPO-56G Series cable will power up with a voltage output range of 1. This can be changed to produce a higher or lower output voltage swing by changing Bytes 238 and 239 within Page 03 of the memory map. For further information, please refer to the aforementioned standard.

   The voltage mask is dependent on the Selected Voltage Range:



SPECIFICATIONS

Optical Characteristics

QSFP+ Active Optical Cables are also available as half cable assemblies. Half cables with MTP connectors are available for applications that require connection to existing infrastructure. Breakout cables with four Duplex LC connectors are available for connecting a QSFP+ port to SFP+ or XFP transceivers.

Table 8: QSFPO-40G Series Optical Performance

Specifications	Unit	Min	Max	Notes
Center Wavelength	nm	840	860	
RMS Spectral Width	nm		0.65	Defined as the standard deviation of the spectrum
RIN OMA	dB/Hz		-128	
Encircled Flux			≥86% ≥30%	At 19 µm At 4.5 µm
Average Power of an Off Transmitter	dBm		-30	
Fiber Length	m	0.1	100	Electrical connector to optical connector
Average Launch Power per Lane	dBm	-5.0	-1.2	
Extinction Ratio	dB	3		
Average Receive Power	dBm	-9.9	-1	
Receiver Sensitivity in OMA	dBm		-11.1	

Table 9: QSFPO-56G Series Optical Performance

Specifications	Unit	Min	Max	Notes
Center Wavelength	nm	840	860	
RMS Spectral Width	nm		0.65	Defined as the standard deviation of the spectrum
RIN OMA	dB/Hz		-128	
Encircled Flux			≥86% ≥30%	At 19 µm At 4.5 µm
Average Power of an Off Transmitter	dBm		-30	
Fiber Length	m	0.1	100	Electrical connector to optical connector
Average Launch Power per Lane	dBm	-5.0	-1.2	
Extinction Ratio	dB	3		
Average Receive Power	dBm	-9.9	-1	
Receiver Sensitivity in OMA	dBm		-10.5	

Interfaces

Control Interface

As described in the QSFP+ standard, the electrical interface has the following low speed signals for control and status: ModSelL, LPMode, ResetL, ModPrsL, IntL. Their operation is described below:

- **ModSelL**
  The ModSelL signal allows multiple QSFP+ modules to be on a standard I^2C Serial control bus. By default, this pin is held low by the host. In this state, the module will respond to the I^2C interface. When the ModSelL pin is pulled high by the host, the module will not respond to or acknowledge any I^2C query or command.

  Care must be taken to ensure that the ModSelL pin is used to toggle control of different modules, the assert and de-assert times must be taken into account to prevent communication conflicts.
- **LPMode**
  The LPMode pin is used by the host to set the maximum power consumption by the module. This is intended to protect hosts that are not designed to cool higher power modules that draw more than 1.5 W.

  Since the power consumption of a QSFP+ AOC is 0.8 W maximum, this pin is not used and the module is always in a low power state.
- **ResetL**
  The AOC can be reset to its default settings by pulling this control pin to a low level for a period longer than the minimum pulse length of the Two-Wire serial interface. While in this reset state, the host should disregard all status bits.
- **ModPrsL**
  ModPrsL is used to indicate to the host that the connector is populated by the AOC. In the absence of an AOC, this is pulled up to the host Vcc. When the AOC is inserted, it completes the path to ground through a resistor on the host and pulls ModPrsL to a low state.
- **IntL**
  This control pin is used to indicate a possible module operation fault or a status critical to the host system. The IntL pin is an open collector output and must be pulled to the host Vcc voltage on the host board. When pulled “low” by the AOC, the alarm is active and the AOC will identify the source of the interrupt using the Two-Wire serial interface.

SPECIFICATIONS

In addition, there is an industry standard Two-Wire serial interface scaled for 3.3 volt LVTTL. It is implemented as a slave device. Signal and timing characteristics are further defined below:

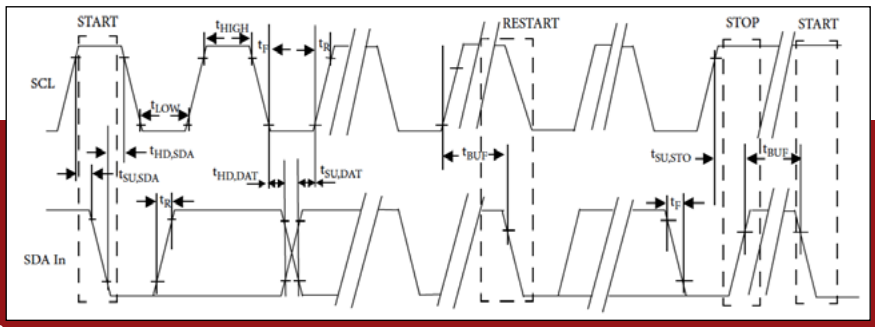
Two-Wire Serial Interface

Table 10 and Figure 4 show the Two-Wire timing specifications as defined by SFF-8436.

Table 10: Optical Engine Two-Wire Timing Specifications

Parameter	Symbol	Unit	Min	Typ	Max	Conditions
Clock Frequency	f_{SCL}	KHz	0	400	400	
Clock Pulse Width Low	t_{LOW}	µs	1.3			
Clock Pulse Width High	t_{HIGH}	µs	0.6			
Time Bus Free Before New Transmission Can Start	t_{BUF}	µs	20			Between STOP and START
START Hold Time	$t_{HD,STA}$	µs	0.6			
START Setup Time	$t_{SU,STA}$	µs	0.6			
Data in Hold Time	$t_{HD,DAT}$	us	0			
Data in Setup Time	$t_{SU,DAT}$	µs	0.1			
Input Rise Time (400 kHz)	$t_{R,400}$	ns			300	From $V_{IL,MAX}$-0.15 to $V_{IH,MIN}$ + 0.15
Input Fall Time (400 kHz)	$t_{F,400}$	ns			300	From $V_{IL,MAX}$-0.15 to $V_{IH,MIN}$ + 0.15
STOP Setup Time	$t_{SU,STO}$	µs	0.6			
ModSelL Setup Time	HOST_select_setup	ms	2			Setup time on the select lines before start of a host initiated serial bus sequence
ModSelL Hold Time	Host_select_hold	µs	10			Delay from completion of a serial bus sequence to changes of module select status
Abort Sequence – Bus Release	Deselect_abort	ms	2			Delay from a host de-asserting ModSelL (at any point in a bus sequence), to the module releasing SCL and SDA

Figure 4: Two-Wire Timing Diagram (per SFF-8436)



Control, Status and Monitor Interface

Table 11 and Table 12 provide the specifications of the control, status and monitoring interface.

Table 11: I/O Timing for Control, Status and Monitoring

Specifications	Symbol	Unit	Min	Max	Notes
Initialization Time	t_{INIT}	ms		2000	Time from power on, hot plug or rising edge of reset until the module is fully functional
Reset init Assert Time	t_{RESET_INIT}	µs		2.5	A reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin
Serial Bus Hardware Ready	t_{SERIAL}	ms		2000	Time from power on until module responds to data transmission over the Two-Wire serial bus
Monitor Data Ready Time	t_{DATA}	ms		2000	Time from power on to data not ready, bit 0 of Byte 2, de-asserted and IntL asserted
Reset Assert Time	t_{RESET}	ms		2000	Time from rising edge on the ResetL pin until the module is fully functional[3]
IntL Assert Time	t_{ON_INTL}	ms		200	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL De-assert Time	t_{OFF_INTL}	µs		500	Time from operation[4] of associated flag until Vout:IntL = Voh. This includes de-assert times for Rx LOS, Tx Fault and other flag bits
Rx LOS Assert Time	t_{ON_LOS}	ms		100	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted
Tx Fault Assert Time	$t_{ON\_TXFAULT}$	ms		200	Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted
Flag Assert Time	t_{ON_FLAG}	ms		200	Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and IntL asserted
Mask Assert Time	t_{ON_MASK}	ms		100	Time from mask bit set (value = 1b)[1] until associated IntL assertion is inhibited
Mask De-assert Time	t_{OFF_MASK}	ms		100	Time from mask bit cleared (value = 0b)[1] until associated IntlL operation resumes
Application or Rate Select Change Time	t_{RATE_SEL}	ms		100	Time from change of state of Application or Rate Select bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification
Power Over-ride or Power Set Assert Time	t_{ON_PDOWN}	ms		100	Time from P_Down bit set (value = 1b)[1] until module power consumption enters Power Level[1]
Power Over-ride or Power Set De-assert Time	t_{OFF_PDOWN}	ms		300	Time from P_Down bit cleared (value = 0b)[1] until the module is fully functional[3]

Note 1. Measured from falling clock edge after stop bit of write transaction.
Note 2. Power is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 3.
Note 3. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 Byte 2 de-asserted. The module should also meet electrical specifications.
Note 4. Measured from falling edge after stop bit of read transaction.

Table 12: I/O Timing for Squelch

Specifications	Symbol	Unit	Min	Max	Notes
Rx Squelch Assert Time	tON_RXSQ	µs		80	Time from loss of Rx input signal until the squelched output condition is reached
Rx Squelch De-assert Time	tOFF_RXSQ	µs		80	Time from resumption of Rx input signals until normal Rx output condition is reached

INITIALIZATION PROCEDURE

Memory Map

Introduction – EEPROM Virtual Addressing

The SFF-8436 specification calls for a list of cable parameters to be readable through an I²C interface, commonly referred as the "EEPROM" parameters. When the first standard revision was written, all the parameters were static and were stored in an on-board EEPROM. As revisions evolved, some of the fields became dynamic (such as temperature or optical power readings), while others (such as interrupts and alarms) became Read/Write (R/W). As a result, an EEPROM based implementation does not suffice anymore, although the term is still used to refer to the Memory Map. We will refer to this as the "SFF Memory Map."

Consequently, the Samtec current implementation, although referred to as an "EEPROM map," does not use an actual direct EEPROM read or write. Instead, each I²C read or write request is interpreted by the embedded microprocessor in the optical engine. The microprocessor then reads or stores data which could come from, or go to, different sources:

- The processor's own internal EEPROM
- The processor's static, dynamic RAM or register memory
- Sensors or internal chipset readings
- Internal processor calculations or registers

An important consequence is that EEPROM byte addresses used in I²C requests are virtual – they will not always correspond to the physical address in the processor internal EEPROM, or might not have a physical EEPROM location at all.

This is invisible to the end user, who just reads and writes to the I²C as if it were an actual EEPROM according to the standard SFF Memory Map. The processor will take care of fetching and writing the data internally from/to the correct physical location.

Instructions for modifying the EEPROM map can be found at www.samtec.com.

SFF Memory Map

The structure of the SFF Memory Map as defined by SFF-8436 rev. 3.8 is shown in Figure 3.

For historical reasons, the SFF Memory Map is somewhat contrived. It is divided into lower and upper memory:

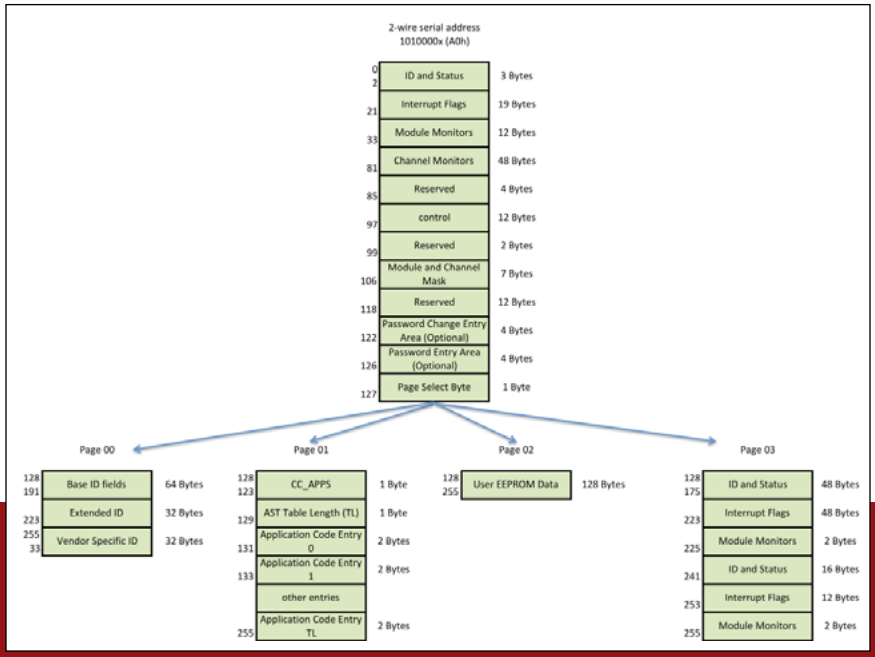
The lower memory is a block or “page” of 128 bytes, and its bytes address are numbered 0 to 127.

The upper memory is itself divided in four pages, numbered page 0 to page 3. Each page is also 128 bytes long block, but with byte addresses numbered 128-255 for each page.

All QSFP+ AOCs are hard-wired at I^2C device address A0h. The lower page is accessed by using the A0h address as the device address, and the 0 to 127 address as the byte address.

Upper pages are accessed by first writing the desired page number at byte in address 127 (Page Select Byte). Any subsequent byte read or write request in the address range 128-255 will be done from/to the page that has been specified in the Page Select Byte. Samtec AOCs do not use Page 02.

Figure 5: Structure of the SFF Memory Map (from the SFF specification)



INITIALIZATION PROCEDURE

Below is a summary description of the memory pages. For more details, see pages 18-19 of this product specification:

- Lower memory, Page 00, bytes 0-127: contains status, interrupt and monitoring information.
- Page 00, bytes 128-255: contains standardized Read-Only information for the end-user. The data is physically mapped to the microprocessor internal EEPROM bytes 128-255.
- Page 01, bytes 128-255 is optional and not supported in the Samtec AOC.
- Page 02, bytes 128-255 is available for the user to store and read his own data.
- Page 03, bytes 128-255 contains module thresholds, channel thresholds and masks, and optional channel controls.

Page 00, Lower Memory

Many of the lower memory bytes are optional or not applicable to an AOC implementation. Table 13 lists the bytes and corresponding features supported in our implementation. Full details about the bit fields and usage can be found in the SFF-8436 specification.

Table 13: Supported Page 00 Lower Memory Fields

Page 00 Byte #	Description	Default Value	Read-Only / Read-Write	Notes
0	Identifier	0D	RO	
2	Status – Flat or Paged Memory	0	RO	
3	Interrupt Flags – LOS		R0	1
4	Interrupt Flags – Tx Fault		RO	
6	Interrupt Flags – Temp Alarm		RO	
7	Interrupt Flags – Voltage Alarm		RO	
22	Module Monitors – Temperature MSB		RO	
23	Module Monitors – Temperature LSB		RO	
26	Module Monitors – Supply Voltage MSB		RO	
27	Module Monitors – Supply Voltage LSB		RO	
86	Control – Transmitter Disable		R/W	
93	Low Power Control		R/W	2
100	Interrupt Masks – Tx LOS Mask	0	R/W	
101	Interrupt Masks – Tx Fault Mask	0	R/W	
103	Interrupt Masks – Temperature Fault Mask	0	R/W	
104	Interrupt Masks – Voltage Fault Mask	0	R/W	
119	Password Change Entry Data		R/W	3
120	Password Change Entry Data		R/W	3
121	Password Change Entry Data		R/W	3
122	Password Change Entry Data		R/W	3
123	Password Entry Area		R/W	3
124	Password Entry Area		R/W	3
125	Password Entry Area		R/W	3
126	Password Entry Area		R/W	3
127	Page Select Byte		R/W	

[1] Rx only. Tx LOS not supported
[2] The engine always runs in low power mode, writing to this register has no effect
[3] User settable password protection of page 02 not supported

Page 00, Upper Memory

The values for the Page 00 Upper Memory bytes are shown in Table 14. Default factory-programmed values for InfiniBand™ are shown. Some of the fields will need to be adjusted by the customer at manufacturing time. Values can be uploaded using our software tool. For details, please contact optics@samtec.com. Please contact Samtec for alternate default configurations.

Table 14: Page 00 Upper Memory Fields (factory default, InfiniBand™)

Byte #	Bit/s	Description	Value	Meaning
128	7:0	Identifier	0Dh	
129	7:6	Extended Identifier Values, Power Class	0	Power Class 1 Module
130	7:0	Connector	23h	AOC has no optical connector
140	7:0	Nominal BR	Part Specific	
142	7:0	Cable Length (SM fiber), in km	0	
143	7:0	Cable Length (OM3 fiber), in 2 m Increments	0	
144	7:0	Cable Length (OM2 fiber), in 1 m Increments	0	
145	7:0	Cable Length (OM1 fiber), in 1 m Increments	0	
146	7:0	Link Length Units of 1 m	Part Specific	
147	7:4	Transmitter Technology	0	Pass: 850 nm VCSEL
148-163		Vendor Name	Samtec, Inc.	
164	3:0	Extended Module Codes (InfiniBand™ Data Rates)	Part Specific	
165-167		Vendor OUI	04C880h	
168-183		Vendor Part Number	Part Specific	
184-185		Vendor Revision	0	
186	7:0	Wavelength (fiber)	42h	Wavelength = 850 nm
187	7:0	Wavelength (fiber)	68h	Wavelength = 850 nm
188	7:0	Wavelength Tolerance	0Fh	Wavelength Tolerance = 20 nm
189	7:0	Wavelength Tolerance	A0h	Wavelength Tolerance = 20 nm
190	7:0	Max Case Temp	70	Max Temp Case = 70ºC
191	7:0	Check Sum	Part Specific	
193	0	RX Output Amplitude Programming	0	Not Implemented
194	3	RX Squelch Disable Implemented	0	Not Implemented
194	2	RX Output Disable Capable	1	RX Output Disable Capable
194	1	TX Squelch Disable Implemented	0	Not Implemented
194	0	TX Squelch Implemented	0	Not Implemented
195	7	Memory Page 02 Provided	1	Memory Provided
195	6	Memory Page 01 Provided	0	Not Implemented
195	4	TX Disable Implemented (also disables serial output)	1	TX Disable Implemented
195	3	TX Fault Reporting Implemented	1	TX Fault Reporting Implemented
195	1	LOS and Reporting Implemented	0	Not Implemented
196-211	All	Vendor Serial Number	Part Specific	
212-217	All	Date Code	Part Specific	
218-219	All	Lot Code	0	Optional - Value = 00
223	7:0	Check Sum	Part Specific	
224-255	All	Vendor Specific Information	FF000110	

Notes to Page 00 Implementation

Please see Table 15 for further clarification of our implementation of Page 00 fields.

Table 14: Notes to the Memory Map Implementation

Type of Parameter	Address		Name	Notes
	Page	Byte		
Interrupt Flag	00	3	Tx_LOS	Not Provided
Interrupt Flag	00	9-10	L-Rx Power Alarm	Not Provided
Channel Monitoring	00	34-41	Rx Input Power	Rx Input Power is Not Supported
Channel Monitoring	00	42-49	Tx Bias	Tx Bias Monitoring is Not Supported
Channel Mask	00	100[7:4]	M-Tx LOS	Tx LOS is Not Supported
Optional Channel Controls	03	241[3:0]	Tx SQ Disable	Tx Squelch is Not Supported

Page 02

Page 02, bytes 128-255 are provided for end-customer's own use. The fields are initialized to 0 at the factory.

Page 03

Table 16: Supported Page 03 Fields

Page 03 Byte #	Description	Default Value	Read-Only / Read-Write
128	Temp High Alarm MSB	75ºC	RO
129	Temp High Alarm LSB		RO
130	Temp Low Alarm MSB	0ºC	RO
131	Temp Low Alarm LSB		RO
132	Temp High Warning MSB	70ºC	RO
133	Temp High Warning LSB		RO
134	Temp Low Warning MSB	5ºC	RO
135	Temp Low Warning LSB		RO
144	Vcc High Alarm MSB	3.465 V	RO
145	Vcc High Alarm LSB		RO
146	Vcc Low Alarm MSB	3.135 V	RO
147	Vcc Low Alarm LSB		RO
148	Vcc High Warning MSB	3.3825 V	RO
149	Vcc High Warning LSB		RO
150	Vcc Low Warning MSB	3.2175 V	RO
151	Vcc Low Warning LSB		RO
176	Rx Power High Alarm MSB		RO
177	Rx Power High Alarm LSB		RO
238	FDR Voltage Select	Range 1	R/W
239	FDR Voltage Select	Range 1	R/W
240	Squelch Disable		R/W
241	Rx Output Disable		R/W

Note: Bytes 238 and 239 are only writeable for QSFPO-56G Series variants.

Output Voltage and Pre-emphasis Settings

The Rx output amplitude swing and pre-emphasis settings are factory adjustable. Four output voltage amplitude settings are available.

- 0 mV (Rx channel permanently disabled)
- 317 mV
- 422 mV
- 739 mV (factory default)

Four pre-emphasis settings are available:

- 0 mV (factory default)
- 125 mV
- 175 mV
- 325 mV

These settings will change the quality of the electrical output. In addition, changing these settings also affect the power consumption of the optical engine as shown on Table 17. Reducing voltage and pre-emphasis results in the lowest power consumption available, while larger voltage and pre-emphasis might be used in special non-standard applications to overcome poor electrical traces or provide more design margin at the expense of power consumption.

All QSFP+ AOC cables will default on power up to the 739 mV, 0 mV settings. As per the InfiniBand™ FDR specification, the memory map can be used to change the output settings of the QSFPO-56G Series. Changing the output to Range 0 will result in a drop in power consumption, whereas changing to Range 2 will increase the power consumption.

Table 17: Typical Power Consumption vs. Rx Settings

Voltage Swing Setting (mV)	Pre-emphasis Setting (mV)	Typical Power Consumption (mW)	Notes
317	0	590	
317	125	740	
317	175	770	
317	325	850	
422	0	620	56G Range 0
422	125	770	
422	175	800	
422	325	890	
739	**0**	**710**	**Default Setting**
739	125	860	56G Range 2
739	175	890	
739	325	980	

INTERFACE

Electrical

Figure 5 shows the contact numbering for the assembly connector. The diagram shows the module from the bottom view. There are 38 pins intended for high speed low speed signals, power and ground connections. These pins are described in Table 18.

Table 18: Edge Connector Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence	Note
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTLL-I	ModSelL	Module Select	3	
9	LVTLL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3 V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	Two-Wire Serial Interface Clock	3	
12	LVCMOS-I/O	SDA	Two-Wire Serial Interface Data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTLL-O	ModPrsL	Module Present	3	
28	LVTLL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3 V Power Supply Transmitter	2	2
30		Vcc1	+3.3 V Power Supply	2	2
31	LVTLL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the optical engine. All are common within the optical engine and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 18. The connector pins are each rated for a maximum current of 500 mA.

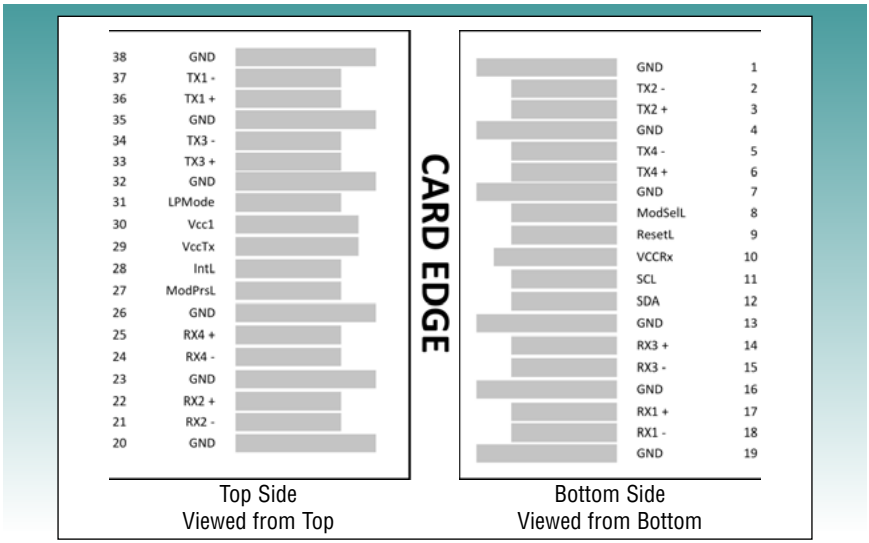


Figure 5: Edge Card Connector Pinout

MECHANICAL CHARACTERISTICS

Connector Dimensions

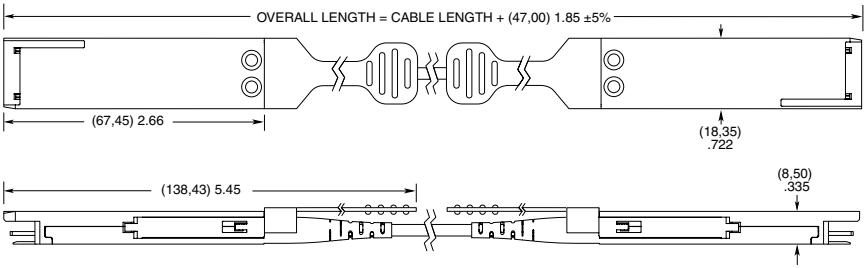


Figure 6: Connector Dimensions

TECHNICAL INFORMATION

Regulatory and Compliance

Table 19: Regulatory and Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Contact	JEDEC Human Body Model (HBM) (JESD22-A114-B) JEDEC Machine Model (MM) (JESD22-A115-A)	1 kV TBD
Electrostatic Discharge (ESD) to Module Case	Variation of IEC 61000-4-2	15 kV
Electromagnetic Interference (EMI)	FCC part 15 CENELEC EN55022 (CISPR 22A) VCCI class 1	TBD
EMI Immunity	Variation of IEC 61000-4-3	10 V/m, 80 – 1000 Mz
Laser Eye Safety	IEC 60825-1 amendment 2 CFR 21 section 1040	Class 1
RoHS Compliance	RoHS 6/6 directive 2002/95/EC amendment 4054 (2005/747/EC)	

Class 1 LASER PRODUCT
per IEC 60825-1 Ed. 2 (2007)

Complies with FDA performance standards for laser products except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007

Manufacturing Location: Samtec, 520 Park East Blvd., New Albany, IN 47150

Caution - Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

QSFP+ Active Optical Cable

QSFPO - XXX - XXX.X - 01

Product Category

Speed

4 x 10G lanes 40G
4 x 14G lanes 56G

Type

Length in meters = 0.5 to 100.0
(500 mm to 100 m. See www.samtec.com?QSFPO-40G, www.samtec.com?QSFPO-56G)

MTP or Duplex LC end terminations also available. Call Samtec.

Definitions

This document uses the following conditions:
All voltages are referred to GND unless otherwise specifically noted.
Currents are defined positive out of the pin.

Reference Documents

SFF-8436:	QSFP+ Specifications Document
SFF-8431:	SFP+ Specifications Document
InfiniBand™	Architecture Release 1.3
IEEE802.3ba	Amendment 4: Media Access Control Parameters, Physical Layers, and Management Parameters for 40 Gbps and 100 Gbps Operation

Notice

This document is made available subject to Samtec General Terms and Conditions available at www.samtec.com and contains information about a product which is currently under final development. The information contained in this document is based on design targets, simulation results or early prototype test results. Characteristics, data and other specifications are subject to change without notice. Therefore the reader is cautioned that this datasheet is preliminary. The reader is advised to obtain the most recent datasheet before considering any purchase or use for design considerations.

Warning

Samtec products are not intended for use in life support applications and any such use without written consent is therefore prohibited.

For more information visit www.samtec.com/active-optics or contact Samtec's Optical Group at optics@samtec.com

samtec
SUDDEN SERVICE

JANUARY 2014