XVME-542
6U 64/32-Channel Analog Input, 8-Channel Analog Output Module

USER'S MANUAL

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Chapter 1 – XVME-542 Overview

Product Features

The XVME-542 is a powerful VMEbus-compatible analog input/output (AIO) module. It is capable of performing analog-to-digital (A/D) conversions with a 16-bit resolution, and digital-to-analog (D/A) conversions with a 12-bit resolution. The module can be configured to provide 64 single-ended, 32 differential, or 64 pseudo-differential analog input channels, with three ranges of programmable gain and six modes of operation. The analog output can provide up to eight analog output channels, with two modes of operation.

XVME-542 analog input features include

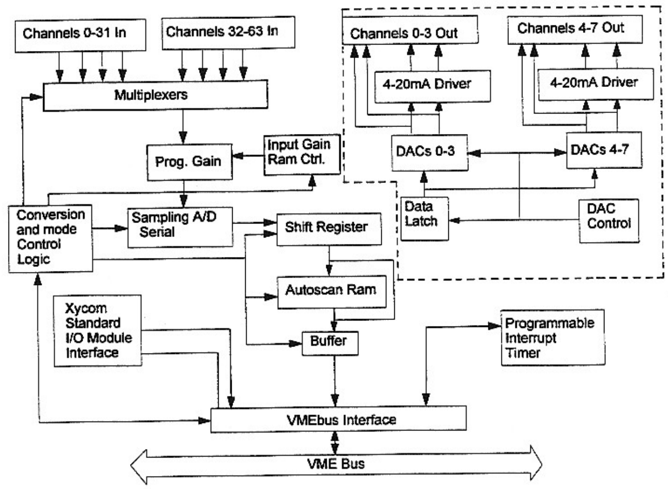
- 64 single-ended, 32 differential, or 64 pseudo-differential 16-bit analog input channels
- Unipolar 0-5 V, 0-10 V, or bipolar ±5 V, ±10 V operation
- Programmable gains of 1, 2, 5,10; 4, 8, 20, 40; or 10, 20, 50, 100
- 16-bit conversion
- 6 operating modes
    - Single channel conversion
    - Sequential channel conversion
    - Random channel conversion
    - External trigger conversion
    - Autoscanning conversion
    - Programming gain
- 10 µsec acquisition and conversion time
- 16 µsec settling time

Analog output features include

- 8 analog output channels with 12-bit resolution
- 4-20 mA, 0-5 V, 0-10 V, ±2.5 V, ±5 V, and ±10 V operation
- 5 mA output drive for voltage output
- Transparent and simultaneous update operating modes
- D/A latch readback capability
- Analog ground reference for current return

Operational Description

The following figure shows the operational diagram of the XVME-542 AIO module.



XVME-542 Operational Block Diagram

Xycom Standard I/O Architecture

All Xycom XVME I/O modules conform to the Xycom VMEbus Standard I/O Architecture. This architecture is intended to make the programming of all Xycom VMEbus I/O modules simple and consistent. The following features apply to the operation of the AIO module:

- Module Address Space – All XVME modules are controlled by writing to addresses within the 64 Kbyte short I/O address space (or the upper 64 Kbyte FFXXXXh of VMEbus standard address space). A module can be configured to occupy any one of 64 available 1 Kbyte blocks within the address space. The 1 Kbyte block occupied by the module (known as the I/O interface block) contains all of the module's programming registers, module identification data, and I/O registers. Within the I/O interface block, the address offsets are standardized so that users can find the same registers and data at the same address offsets across the entire Xycom XVME product line.
- Module Identification – The AIO has ID information which provides the module name, model number, manufacturer, and revision level information at a location that is consistent with other Xycom I/O modules.
- Status/Control Register – This register is always located at address module base + 81h, and the lower two bits are standard from module to module.

Specifications

Specifications for the XVME-542 are detailed in the following tables.

Characteristic	**Specification**
Number of channels	
Single-ended	64
Differential	32
Pseudo-differential	64
Accuracy	
Resolution	16 bits
Single-channel mode	.003% FSR
All other modes	.006% FSR
Speed	
Conversion time, 16 bits	10 µsec
Settling time	16 µsec
Throughput	
Single-channel mode	100 KHz
Autoscanning mode	62.5 KHz
All other modes	38.5 KHz
A/D full scale voltage ranges (G=1)	
Unipolar	0-5 V, 0-10 V
Bipolar	±5 V, ±10 V
Programmable Gain	
Range 1	1, 2, 5, or 10
Range 2	4, 8, 20, or 40
Range 3	10, 20, 50, or 100
Maximum input voltage	
Power on	44 V
Power off	30 V
Input impedance	18 M ohm, minimum
Bias current	±200 pA, maximum
Input capacitance	100 pF, maximum
Operating common mode voltage	-11 V, +13 V
External trigger to sample	26 µsec
Power requirements	
Voltage outputs	5 V ±5%, 1.8 A typical, with voltage outputs at full scale
Current Outputs	5 V ±5%, 2.75 A typical, with current outputs at full scale

Analog Input Specifications

Characteristic	Specification
Number of channels	8
Accuracy Resolution Overall error Differential linearity	 12 bits ±¼ LSB ±½ LSB
Voltage output characteristics Ranges Settling time Output current Offset temperature coefficient Gain temperature coefficient	 0-5 V, 0-10 V, ±2.5 V, ±5 V, ±10 V 4 µsec 5 mA maximum 10 ppm/°C 20 ppm/°C
Current Loop Characteristics Range Compliance voltage Settling time Load resistance range Offset temperature coefficient Gain temperature coefficient	 4-20 mA, non-isolated .2 V min.; 10.5 V max. 80 µsec 50-525 ohms 30 ppm/°C 50 ppm/°C
Digital Input Coding	OBN, CTC

Analog Output Specifications

Characteristic	Specification
Temperature Operating Non-operating	 0° to 65°C (32° to 149°F) -40 to 85°C (-40° to 185°F)
Humidity	5 to 95% RH, non-condensing
Altitude Operating Non-operating	 Sea level to 10,000 ft. (3048 m) Sea level to 50,000 ft. (15240 m)
Vibration Operating Non-operating	 5 to 2000 Hz .015" peak-to-peak displacement 2.5 g acceleration (maximum) 5 to 2000 Hz .030" peak-to-peak displacement 5.0 g acceleration (maximum)
Shock Operating Non-operating	 30 g peak acceleration, 11 msec duration 50 g peak acceleration 11 msec duration
VMEbus Compliance A24/16:D16 DTB slave AM CODES 29, 2D, 39, 3D BGXIN hardwired to BGXOUT Conforms to Xycom Standard I/O Architecture I(1) - I(7) (STAT) (Programmable Vector)	

Environmental Specifications

Chapter 2 – Installation

System Requirements

To operate correctly, the XVME-542 AIO must be properly installed in a VMEbus backplane. Following are the minimum system requirements for module operation:

- A host processor installed in the same backplane and a properly installed controller subsystem

  or

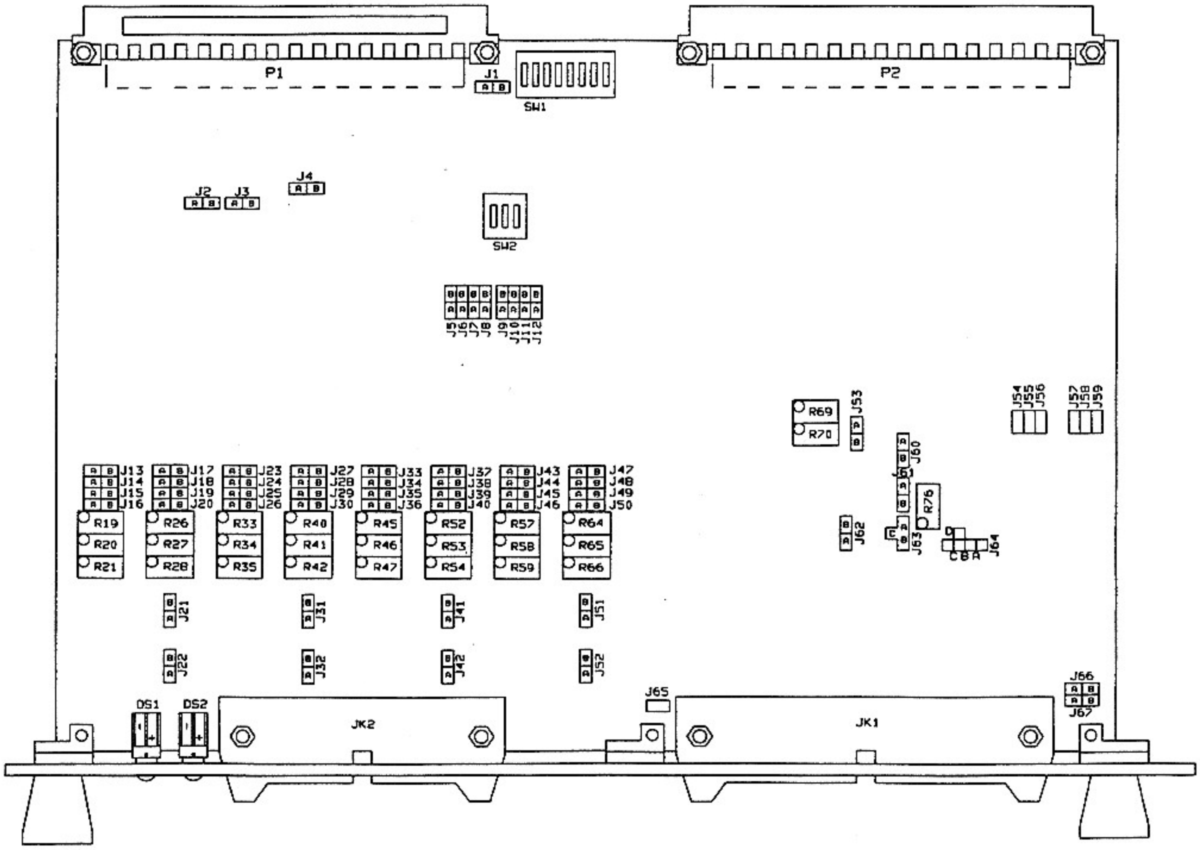
- A host processor module that incorporates an on-board controller subsystem

Relevant Components

Prior to installing the analog input/output module, you must configure several jumper/switch options. The configuration of the jumpers and switches is dependent upon which of the module operational capabilities are required for a given application. The switches are used to set VMEbus-related options. The jumper options can be divided into three categories:

- VMEbus-related options
- Analog-to-digital conversion options
- Digital-to-analog conversion options

The figure on the following page illustrates the jumpers, switches, connectors, and potentiometers located on the XVME-542.



XVME-542 Jumpers, Switches, Connectors, and Potentiometers

Switch Settings

The XVME-542 has two switches: an eight-position addressing switch and a three-position interrupt level select switch.

Switch SW-1

Addressing switch SW-1 is used to

- Select the address on a 1 Kbyte boundary in the VMEbus short I/O or FF*XXXX*h in the VMEbus standard address space
- Select supervisory only or both supervisory and non-privileged accesses
- Choose between the short I/O or FF*XXXX*h in the standard address space.

The table below describes the switch bits and their functions.

Position	**Function**	**Setting**
1	Address bit A10	Open = 1 Closed = 0
2	Address bit A11	Open = 1 Closed = 0
3	Address bit A12	Open = 1 Closed = 0
4	Address bit A13	Open = 1 Closed = 0
5	Address bit A14	Open = 1 Closed = 0
6	Address bit A15	Open = 1 Closed = 0
7	Supervisory/non-privileged	Open = supervisory Closed = supervisory & non-privileged
8	Standard/short I/O	Open = standard access Closed = short I/O access

Switch SW-1 Bit Settings

Interrupt Level Select Switch (SW-2)

This three-position switch selects which VMEbus interrupt level the XVME-542 uses to generate a periodic interrupt or an interrupt at the end of a conversion. The time period is determined by the interrupt timer register (base + 101h).

Position 1	Position 2	Position 3	VMEbus Interrupt Level
Open	Open	Open	7
Open	Open	Closed	6
Open	Closed	Open	5
Open	Closed	Closed	4
Closed	Open	Open	3
Closed	Open	Closed	2
Closed	Closed	Open	1
Closed	Closed	Closed	None

Interrupt Level Switch Settings

Jumper Settings

This section defines the XVME-542 jumper settings.

Note

J1 must always be set to A for proper operation.

SYSFAIL*

The position of jumper J3 determines whether the XVME-542 can assert a SYSFAIL*. When J3 is set to A, the SYSFAIL* driver is disabled; when it is set to B the SYSFAIL* driver is enabled and the module asserts SYSFAIL* when the red (fail) LED is on. J3A is the factory-shipped configuration.

Analog-to-Digital Conversion Options

Following are the jumper settings for analog-to-digital conversions.

Input Conversion Format Options

Jumper J62 sets the conversion of analog information to straight binary or two's complement binary format. J62A sets straight binary format; J62B sets two's complement binary format.

Differential/Single-ended Input Options

Use jumpers J2 and J64 to configure the analog input channels for 64 single-ended, 64 pseudo-differential, or 32 differential input channels.

Jumper	Single-ended	Pseudo-differential	Differential
J2	B	A	B
J64	A, C	A, D	B

Jumper Settings: Input Channels

Input Voltage Options

Jumpers J53, J60, J61, and J63 configure the module for one of four input voltage ranges.

Jumper	0-5 V	0-10 V	±5 V	±10 V
J53	B	B	B	A
J60	A	A	A	B
J61	A	B	B	A
J63	C	A	B	B

Jumper Settings: Input Voltage

Input Gain Range Options

You can program each analog input channel gain for one of three ranges, as shown below:

Jumper	1, 2, 5, 10	4, 8, 20, 40	10, 20, 50, 100
J54	In	Out	Out
J55	Out	In	Out
J56	Out	Out	In
J57	In	Out	Out
J58	Out	In	Out
J59	Out	Out	In

Jumper Settings: Input Gain Range

Input Calibration Grounding Options

Use jumpers J66 and J67 to ground channel 0 in single-ended or differential mode for programmable gain offset adjustment.

Jumper	Single-ended Ground	Differential Ground
J66	B	B
J67	A	B

Jumper Settings: Input Calibration Grounding

If you do not want to ground channel 0, jumpers J66 and J67 should be set to A.

In external trigger mode, set J65 IN to pick up digital ground for external trigger signals returned on JK1 top or bottom, pin 49. If external trigger mode is not used, remove J65.

Digital-to-Analog Conversion Options

The XVME-542 offers six jumper-configurable output configurations:

- 0-5 V
- 0-10 V
- ±2.5 V
- ±5 V
- ±10 V
- 4-20 mA

The table below indicates the jumper settings to achieve the desired configuration:

Channel #	0-5 V	0-10 V	±2.5 V	±5 V	±10 V	4-20 mA
0	J47B J48B J49A J50B J52A	J47A J48B J49B J50B J52A	J47B J48B J49A J50A J52A	J47A J48B J49B J50A J52A	J47A J48A J49B J50A J52A	J47A J48B J49B J50B J52B
1	J43B J44B J45A J46B J51A	J43A J44B J45B J46B J51A	J43B J44B J45A J46A J51A	J43A J44B J45B J46A J51A	J43A J44A J45B J46A J51A	J43A J44B J45B J46B J51B
2	J37B J38B J39A J40B J42A	J37A J38B J39B J40B J42A	J37B J38B J39A J40A J42A	J37A J38B J39B J40A J42A	J37A J38A J39B J40A J42A	J37A J38B J39B J40B J42B

Jumper Settings: D/A Output Configurations (continued)

Continued from previous page

Channel #	0-5 V	0-10 V	±2.5 V	±5 V	±10 V	4-20 mA
3	J33B J34B J35A J36B J41A	J33A J34B J35B J36B J41A	J33B J34B J35A J36A J41A	J33A J34B J35B J36A J41A	J33A J34A J35B J36A J41A	J33A J34B J35B J36B J41B
4	J27B J28B J29A J30B J32A	J27A J28B J29B J30B J32A	J27B J28B J29A J30A J32A	J27A J28B J29B J30A J32A	J27A J28A J29B J30A J32A	J27A J28B J29B J30B J32B
5	J23B J24B J25A J26B J31A	J23A J24B J25B J26B J31A	J23B J24B J25A J26A J31A	J23A J24B J25B J26A J31A	J23A J24A J25B J26A J31A	J23A J24B J25B J26B J31B
6	J17B J18B J19A J20B J22A	J17A J18B J19B J20B J22A	J17B J18B J19A J20A J22A	J17A J18B J19B J20A J22A	J17A J18A J19B J20A J22A	J17A J18B J19B J20B J22B
7	J13B J14B J15A J16B J21A	J13A J14B J15B J16B J21A	J13B J14B J15A J16A J21A	J13A J14B J15B J16A J21A	J13A J14A J15B J16A J21A	J13A J14B J15B J16B J21B

Once you've configured the module for unipolar or bipolar mode, you can configure the D/A format for complementary offset binary/complementary straight binary (COB) or complementary two's complement (CTC).

Channel #	COB	CTC
Channel 0	J12A	J12B
Channel 1	J11A	J11B
Channel 2	J10A	J10B
Channel 3	J9A	J9B
Channel 4	J8A	J8B
Channel 5	J7A	J7B
Channel 6	J6A	J6B
Channel 7	J5A	J5B

Jumper Settings: D/A Format

Jumper J4 resets the DAC. When J4A is set, the four digital-to-analog converters are loaded with 0s at reset or power up. When J4B is set, they are loaded with 1s.

External Connectors

The XVME-542 uses standard VMEbus connectors for P1 and P2 (96-pin DIN). P2 is used for extra +5 V and GND connections only.

JK1 Connector

A dual 50-pin ribbon connector with latches containing 100 pins is used for the analog input section. Pinouts are shown in the following tables.

JK1 Pinouts (bottom 50-pin connector)

Pin	Single-Ended Configuration	Differential Configuration	Pin	Single-Ended Configuration	Differential Configuration
1	Channel 0	Channel 0 low	26	Channel 24	Channel 8 high
2	Channel 8	Channel 0 high	27	Analog GND	Analog GND
3	Analog GND	Analog GND	28	Channel 25	Channel 9 high
4	Channel 9	Channel 1 high	29	Channel 17	Channel 9 low
5	Channel 1	Channel 1 low	30	Analog GND	Analog GND
6	Analog GND	Analog GND	31	Channel 18	Channel 10 low
7	Channel 2	Channel 2 low	32	Channel 26	Channel 10 high
8	Channel 10	Channel 2 high	33	Analog GND	Analog GND
9	Analog GND	Analog GND	34	Channel 27	Channel 11 high
10	Channel 11	Channel 3 high	35	Channel 19	Channel 11 low
11	Channel 3	Channel 3 low	36	Analog GND	Analog GND
12	Analog GND	Analog GND	37	Channel 20	Channel 12 low
13	Channel 4	Channel 4 low	38	Channel 28	Channel 12 high
14	Channel 12	Channel 4 high	39	Analog GND	Analog GND
15	Analog GND	Analog GND	40	Channel 29	Channel 13 high
16	Channel 13	Channel 5 high	41	Channel 21	Channel 13 low
17	Channel 5	Channel 5 low	42	Analog GND	Analog GND
18	Analog GND	Analog GND	43	Channel 22	Channel 14 low
19	Channel 6	Channel 6 low	44	Channel 30	Channel 14 high
20	Channel 14	Channel 6 high	45	Analog GND	Analog GND
21	Analog GND	Analog GND	46	Channel 31	Channel 15 high
22	Channel 15	Channel 7 high	47	Channel 23	Channel 15 low
23	Channel 7	Channel 7 low	48	Analog GND	Analog GND
24	Analog GND	Analog GND	49	Power GND	Power GND
25	Channel 16	Channel 8 low	50	External trigger	External trigger

JK1 Pinouts continued on following page

JK1 Pinouts continued from previous page (top 50-pin connector)

Pin	Single-Ended Configuration	Differential Configuration	Pin	Single-ended Configuration	Differential Configuration
1	Channel 32	Channel 16 low	26	Channel 56	Channel 24 high
2	Channel 40	Channel 16 high	27	Analog GND	Analog GND
3	Analog GND	Analog GND	28	Channel 57	Channel 25 high
4	Channel 41	Channel 17 high	29	Channel 49	Channel 25 low
5	Channel 33	Channel 17 low	30	Analog GND	Analog GND
6	Analog GND	Analog GND	31	Channel 50	Channel 26 low
7	Channel 34	Channel 18 low	32	Channel 58	Channel 26 high
8	Channel 42	Channel 18 high	33	Analog GND	Analog GND
9	Analog GND	Analog GND	34	Channel 59	Channel 27 high
10	Channel 43	Channel 19 high	35	Channel 51	Channel 27 low
11	Channel 35	Channel 19 low	36	Analog GND	Analog GND
12	Analog GND	Analog GND	37	Channel 52	Channel 28 low
13	Channel 36	Channel 20 low	38	Channel 60	Channel 28 high
14	Channel 44	Channel 20 high	39	Analog GND	Analog GND
15	Analog GND	Analog GND	40	Channel 61	Channel 29 high
16	Channel 45	Channel 21 high	41	Channel 53	Channel 29 low
17	Channel 37	Channel 21 low	42	Analog GND	Analog GND
18	Analog GND	Analog GND	43	Channel 54	Channel 30 low
19	Channel 38	Channel 22 low	44	Channel 62	Channel 30 high
20	Channel 46	Channel 22 high	45	Analog GND	Analog GND
21	Analog GND	Analog GND	46	Channel 63	Channel 31 high
22	Channel 47	Channel 23 high	47	Channel 55	Channel 31 low
23	Channel 39	Channel 23 low	48	Analog GND	Analog GND
24	Analog GND	Analog GND	49	Power GND	Power GND
25	Channel 48	Channel 24 low	50	External Trigger	External Trigger

JK2 Connector

A dual 34-pin ribbon connector with latches containing 68 pins is used for the analog output section. The pinouts for this connector are shown in the following table.

JK2 Pinouts (upper and lower)

Dual Connector–1st Half		**Dual Connector–2nd Half**	
Pin	**Definition**	**Pin**	**Definition**
1	Channel 0 Vout	1	Channel 4 Vout
2	NC	2	NC
3	Analog GND	3	Analog GND
4	NC	4	NC
5	Channel 1 Vout	5	Channel 5 Vout
6	Analog GND	6	Analog GND
7	Channel 2 Vout	7	Channel 6 Vout
8	NC	8	NC
9	Analog GND	9	Analog GND
10	NC	10	NC
11	Channel 3 Vout	11	Channel 7 Vout
12	Analog GND	12	Analog GND
13	NC	13	NC
14	NC	14	NC
15	Analog GND	15	Analog GND
16	NC	16	NC
17	NC	17	NC
18	Analog GND	18	Analog GND
19	NC	19	NC
20	NC	20	NC
21	Analog GND	21	Analog GND
22	NC	22	NC
23	NC	23	NC
24	Analog GND	24	Analog GND
25	NC	25	NC
26	NC	26	NC
27	Channel 0 IOUT+	27	Channel 4 IOUT+
28	Channel 0 IOUT-	28	Channel 4 IOUT-
29	Channel 1 IOUT-	29	Channel 5 IOUT-
30	Channel 1 IOUT+	30	Channel 5 IOUT+
31	Channel 2 IOUT+	31	Channel 6 IOUT+
32	Channel 2 IOUT-	32	Channel 6 IOUT-
33	Channel 3 IOUT-	33	Channel 7 IOUT-
34	Channel 3 IOUT+	34	Channel 7 IOUT+

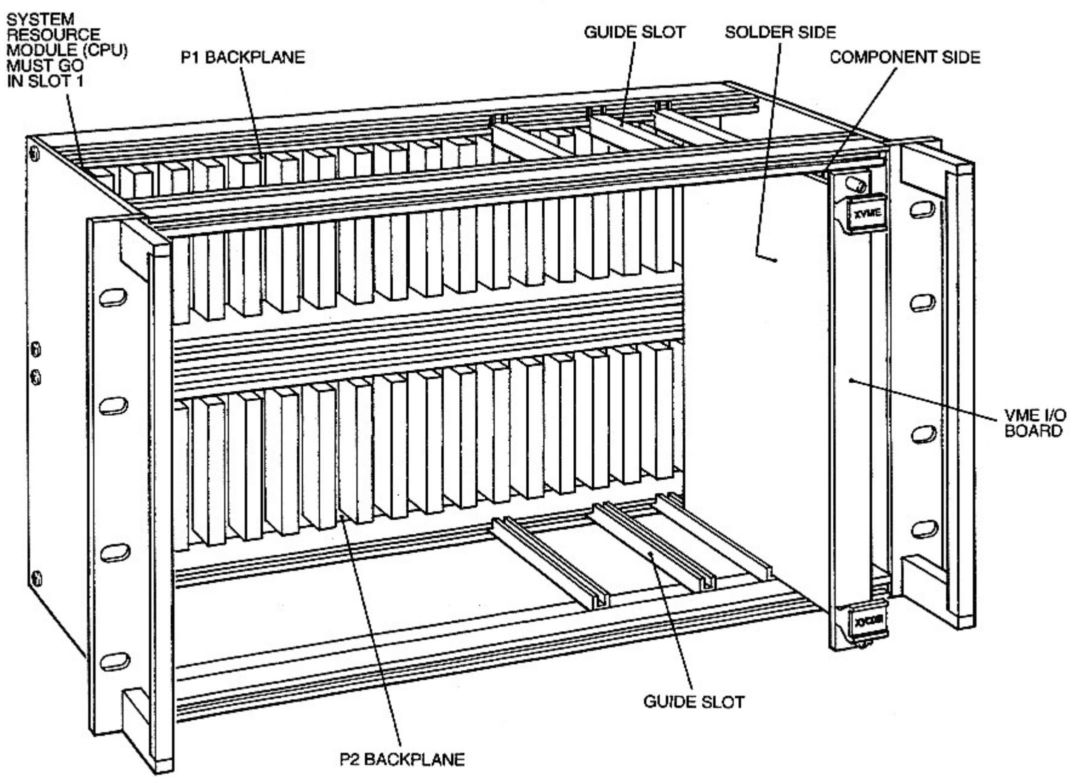
Card Cage Installation

Caution

Do not attempt to install or remove any boards without first turning off power to the bus and all related external power supplies.

Prior to installing a module, determine and verify all relevant jumper configurations. Check the jumper configuration with the diagram and lists in the manual.

Xycom VMEbus modules can accommodate typical VMEbus backplane construction. The following illustration depicts a standard VMEbus chassis and a typical backplane configuration. There are two rows of backplane connectors depicted (the P1 and the P2 backplane).



VMEbus Chassis

Perform the following steps to install a board in the card cage:

1. Make sure the card cage slot that you are going to use is clear and accessible.
2. Center the board on the plastic guides in the slot so that the handle on the front panel is toward the bottom of the card cage.
3. Push the card slowly toward the rear of the chassis until the connectors are fully engaged and properly seated.

Note

It should not be necessary to use excess force to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

4. Once the board is properly seated, tighten the two machine screws at the top and bottom of the front panel.

Chapter 3 – Programming

This chapter provides the information required to program the XVME-542 for analog input and output signal conversions. This information includes the following:

- Flow charts providing quick-start information
- Module address map showing programming locations
- Base addressing and the module I/O interface block
- A/D conversion modes
- D/A conversion principles

Flow Charts

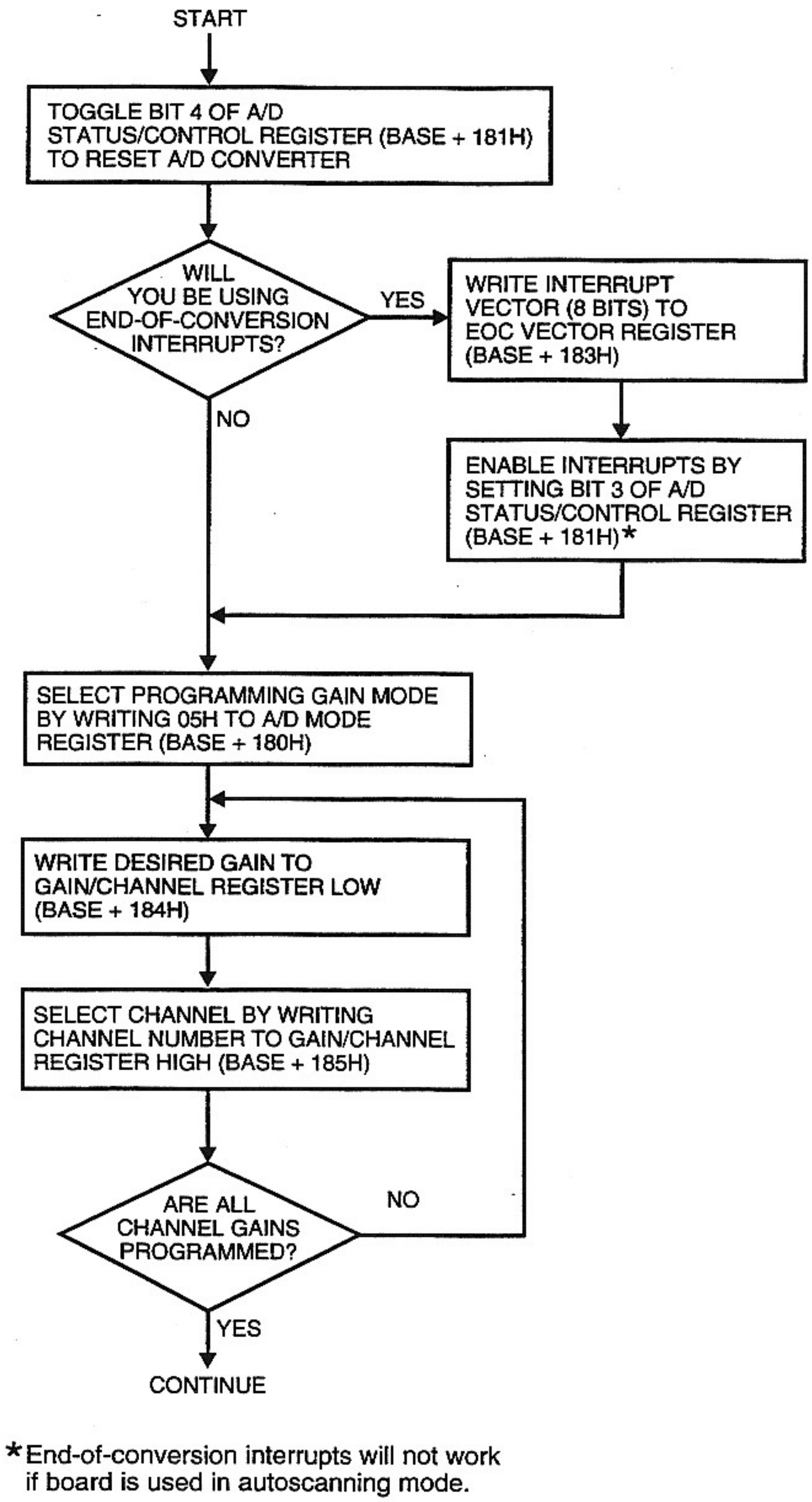
The following flow charts provide information on initializing the XVME-542 board, using A/D conversion modes and analog outputs, and detecting the end of a conversion. The flow charts assume that hardware jumpers have been set. See Chapter 2 for information on setting jumpers.

Note

Register information begins on page 3-14.

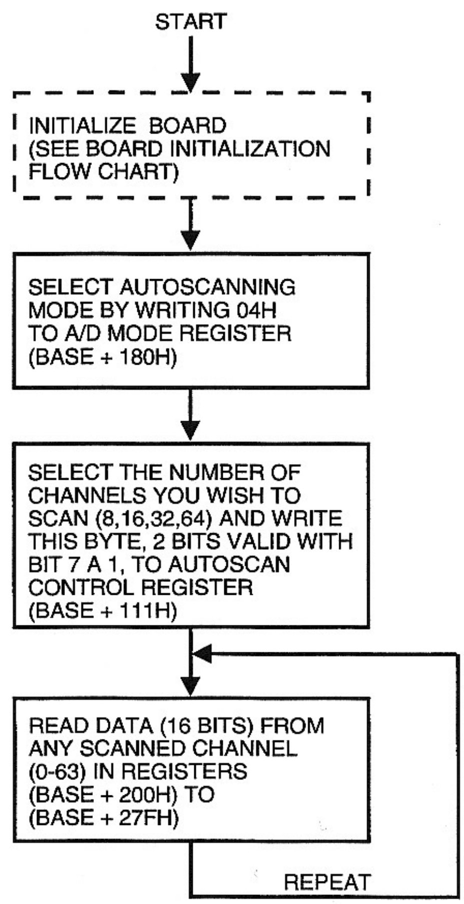
Board Initialization Flow Chart

This flow chart describes the steps necessary to initialize the XVME-542.



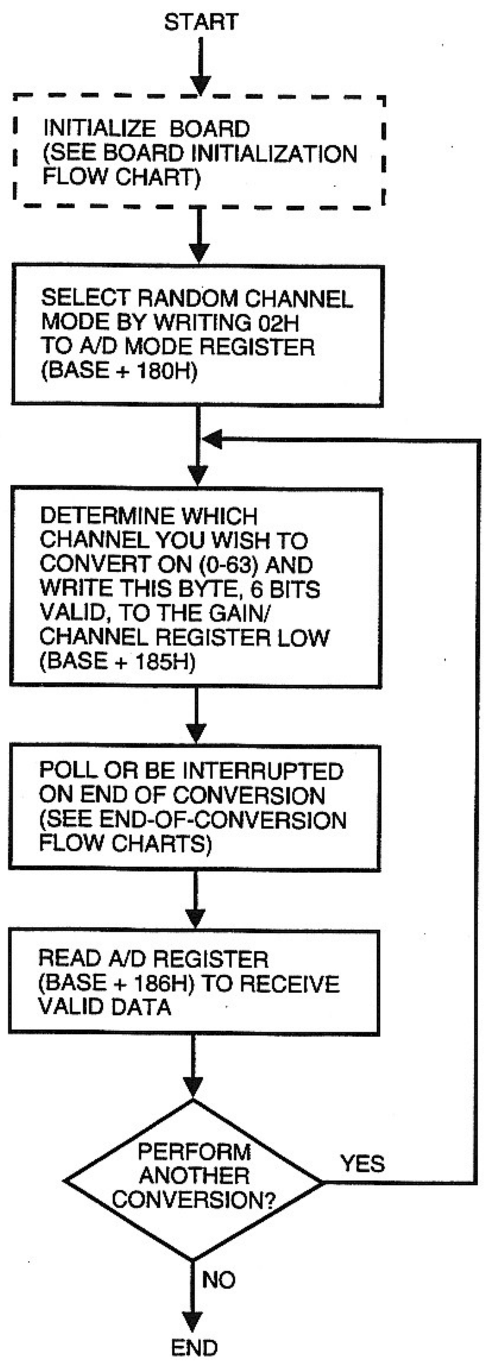
Autoscanning Mode Flow Chart

In autoscanning mode, continuous conversions are performed on 8, 16, 32, or 64 channels, and the results of each channel are stored in 16-bit registers, starting at offset base + 200h for channel 0 to base + 27Fh for channel 63.



Random Channel Mode Flow Chart

In random channel mode, a control byte written to the low byte of the gain/channel register that specifies a channel automatically starts a conversion on that channel.

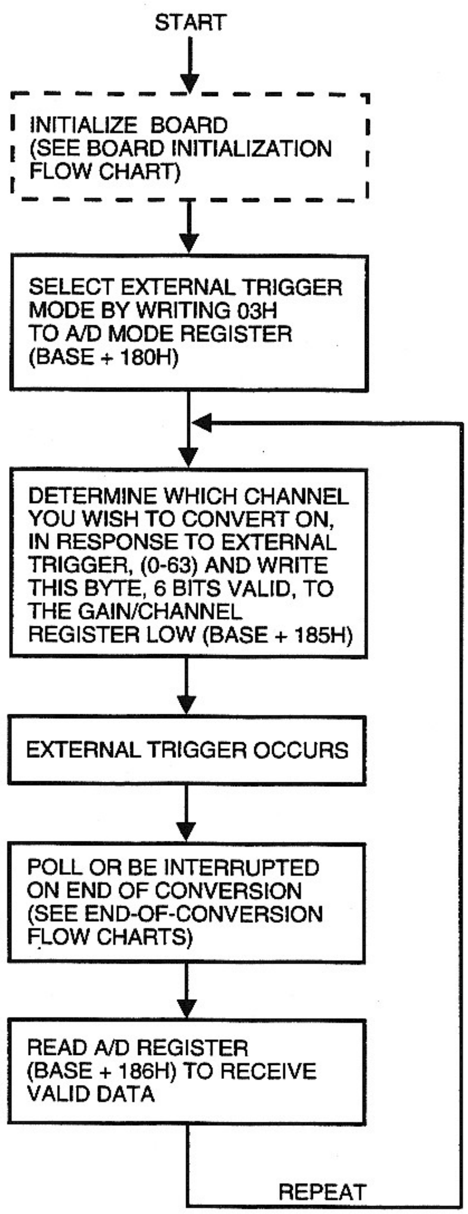


External Trigger Mode Flow Chart

In external trigger mode, the rising edge of a low-going, externally triggered pulse (on pin 50 of JK1)–referenced to power ground (pin 49 of JK1, J65IN)–initiates a conversion.

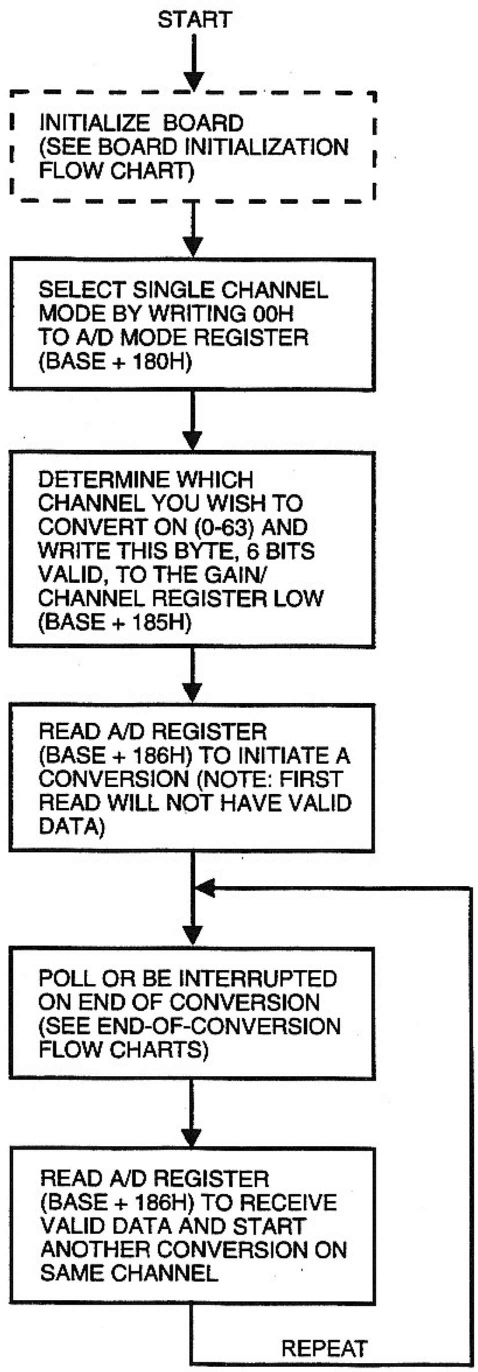
Note

J65 must be IN to use this mode. See Chapter 2 for information on jumper settings.



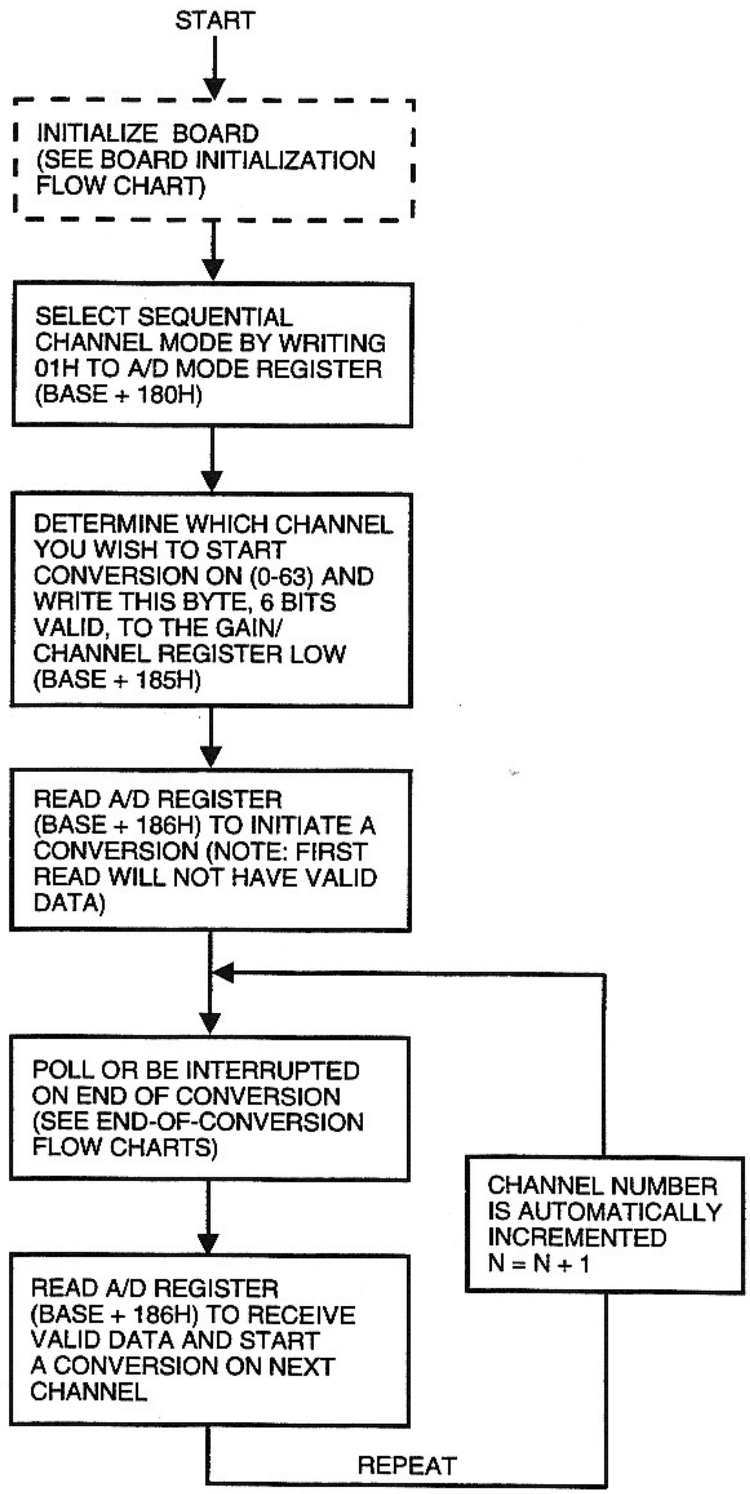
Single Channel Mode Flow Chart

In single channel mode, the module automatically starts another conversion on the specified channel after the low order A/D register (base + 187h) has been read.

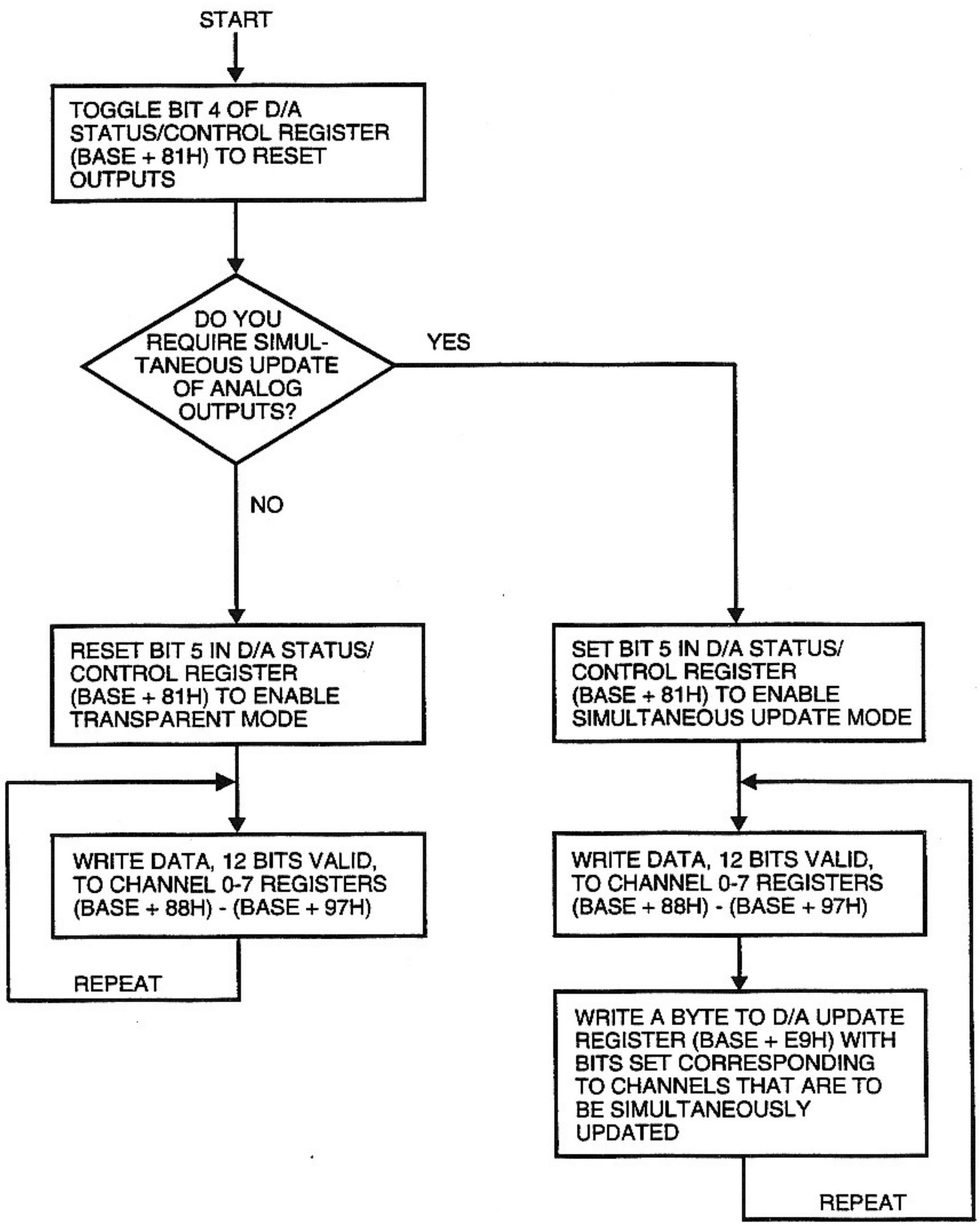


Sequential Channel Mode Flow Chart

In sequential channel mode, the module automatically increments the channel number by one and initiates a conversion on the next channel (previous channel + 1) after the low byte A/D register (base + 187h) has been read.

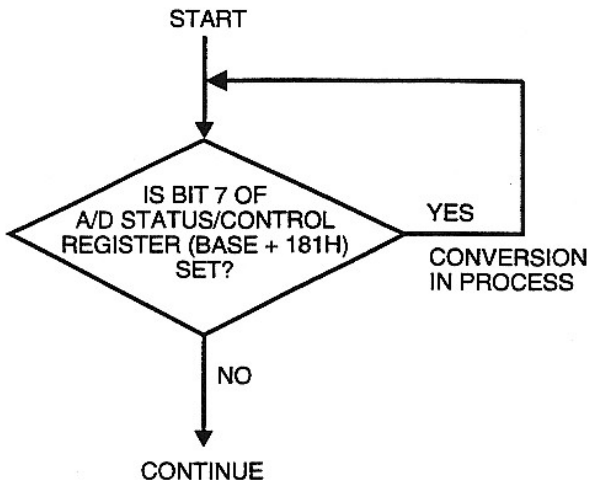


Analog Output Flow Chart

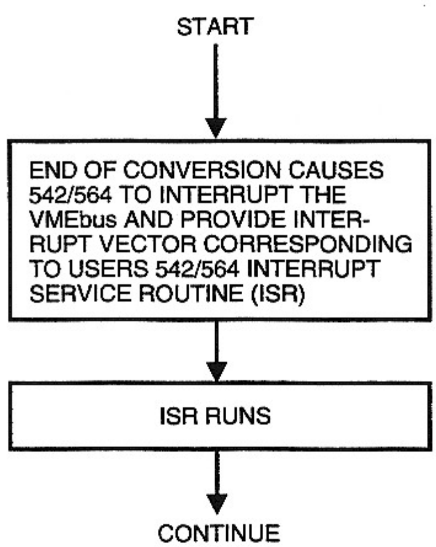


End-of-Conversion Flow Charts

1- Polling method



2 - Interrupt vector method



NOTE: INTERRUPT VECTOR MUST BE LOADED AND INTERRUPTS ENABLED (SEE BOARD INITIALIZATION FLOW CHART)

Module Base Addressing

The XVME-542 is designed to be addressed within either the VMEbus-defined 64 Kbyte short I/O address space or the upper 64 Kbytes of the standard address space (FF0000h-FFFC00h). Because each I/O module connected to the bus must have a unique base address, the addressing scheme for Xycom XVME I/O modules is configurable. When the XVME-542 is installed in a system, it will occupy a 1 Kbyte block of address space (also referred to as the I/O block)

The base address decoding scheme for the XVME-542 positions the starting address of each board on a 1 Kbyte boundary. Thus, there are 64 possible base addresses (1 Kbyte boundaries) for the XVME-542 within either the short I/O address space or the upper 64 Kbytes of standard address space. (Refer to Chapter 2 for a list of base addresses and their corresponding SW-1 bit locations.)

	Even	Odd	
Base +00h +3Eh	Undefined	Module Identification	01h 3Fh
+40h +7Eh	Reserved		41h 7Fh
+80h		D/A Status/Control Register	81h
+82h +86h	Undefined		83h 87h
+88h	Channel 0 D/A High Byte	Channel 0 D/A Low Byte	89h
+8Ah	Channel 1 D/A High Byte	Channel 1 D/A Low Byte	8Bh
+8Ch	Channel 2 D/A High Byte	Channel 2 D/A Low Byte	8Dh
+8Eh	Channel 3 D/A High Byte	Channel 3 D/A Low Byte	8Fh
+90h	Channel 4 D/A High Byte	Channel 4 D/A Low Byte	91h
+92h	Channel 5 D/A High Byte	Channel 5 D/A Low Byte	93h
+94h	Channel 6 High Byte	Channel 6 Low Byte	95h
+96h	Channel 7 High Byte	Channel 7 Low Byte	97h
+98h +E6h	Reserved		99h E7h
+E8h		D/A Update Register Channels 0-7	E9h
+EAh			EBh
+100h		Interrupt Timer Register	101h
+102h		Programmable Timer Interrupt Vector Register	103h
+104h +108h			105h 109h
+110h		Autoscan Control Register	111h
+112h +178h			113h 179h
+180h	A/D Mode Register	A/D Status/Control Register	181h
+182h		End of Conversion Vector Register	183h
+184h	Gain/Channel Register High	Gain/Channel Register Low	185h
+186h	A/D Register High	A/D Register Low	187h
+188h +198h			189h 199h
+200h	Channel 0 A/D Scan	Channel 0 A/D Scan	201h
+202h	Channel 1 A/D Scan	Channel 1 A/D Scan	203h
+204h +27Ch	Channels 2-62 A/D Scan	Channels 2-62 A/D Scan	205h 27Dh
+27Eh	Channel 63 A/D Scan	Channel 63 A/D Scan	27Fh

XVME-542 Memory Map

Any location within the XVME-542's 1 Kbyte I/O interface block can be accessed by adding the module base address to the address of the specific location within the I/O interface block (referred to as the I/O interface block offset). For example, the D/A status/control register is located at address 81h within the I/O interface block. If the module base address is set at 1000h, then the status/control register would be accessible at address 1081h.

Module Base Address		I/O Interface Block Offset		D/A Status/Control Register
1000h	+	081h	=	1081h

For memory-mapped CPU modules, the short I/O address space is memory mapped to begin at a specific address. For such modules, the I/O interface block offset is an offset from the start of this memory-mapped short I/O address space. For example, if the short I/O address space of a CPU module starts at F90000h and if the base address of the AIO is set at 1000h, the actual module base address would be F91000h.

I/O Interface Block

This section describes the programming locations in the XVME-542 I/O interface block.

Note

Reading from or writing to undefined I/O interface block locations may make application software incompatible with future XVME modules.

Module Identification Data

The Xycom module identification scheme provides a unique method of registering module-specific information in an ASCII-encoded format. ID data is provided as 32 ASCII encoded characters consisting of the board type, manufacturer identification, module model number, number of 1 Kbyte blocks occupied by the module, and module functional revision level. This information can be read by the system processor on power up to verify the system configuration and operational status. The table on the following page defines the identification information locations.

Offset Relative to a Module Base	Contents	ASCII Encoding (hexadecimal)	Description
1	V	56	ID PROM identifier; always VMEID (five characters)
3	M	4D	
5	E	45	
7	I	49	
9	D	44	
B	X	58	Manufacturer’s ID, always XYC for Xycom modules (three characters)
D	Y	59	
F	C	43	
11	5	35	Module Model Number (three characters, four trailing blanks)
13	4	34	
15	2	32	
17		20	
19		20	
1B		20	
1D		20	
1F	1	31	Number of 1 Kbyte blocks of I/O space occupied by this module (one character)
21		20	Major functional revision level with leading blank (if single digit)
23	1	31	
25	1	31	Minor functional revision level with trailing blank (if single digit)
27		20	
29	Reserved		Manufacturer-dependent information; reserved for future use
2B	Reserved		
2D	Reserved		
2F	Reserved		
31	Reserved		
33	Reserved		
35	Reserved		
37	Reserved		
39	Reserved		
3B	Reserved		
3D	Reserved		
3F	Reserved		

Identification Data

The module has been designed so that it is only necessary to use odd backplane addresses to access the ID data. Thus, each of the 32 bytes of ASCII data have been assigned to the first 32 odd I/O interface block bytes (that is, odd bytes 1h-3Fh).

ID information can be accessed by addressing the module base, offset by the specific address for the character(s) needed. For example, if the base address of the board is jumpered to 1000h, and if you wish to access the module model number (I/O interface block locations 11h, 13h, 15h, 17h, 19h, 1Bh, and 1Dh), individually add the offset addresses to the base addresses to read the hex-encoded ASCII value at each location. Thus, in this example, the ASCII values that make up the module model number are found sequentially at locations 1011h, 1013h, 1015h, 1017h, 1019h, 101Bh, and 101Dh.

D/A Status/Control Register (base + 81h)

This 8-bit register is used to

- Select the operating mode for the D/A channels
- Reset the module
- Control the red and green LEDs used on the module

Below is a description of the bits in this register:

Bit 7 (MSB)	Reserved
Bit 6	Reserved
Bit 5	This bit determines the mode in which the D/A converters are operating. 1 = Simultaneous update mode 0 = Transparent mode In transparent mode, each analog output channel or DAC is updated individually when the lower byte of the desired DAC is written to. Byte or word transfers are allowed. If all 12 bits are written at once, then that DAC's register, along with the output of the DAC, gets updated. Each channel has its own word location. In simultaneous channel update mode, the individual DAC registers are written to both high and low bytes with no update to the DAC output. Updating the channel or channels is accomplished by writing to location E9h with the desired channels to update. In simultaneous channel update mode any combination of the 8 channels may be updated at once.
Bit 4	This bit performs a software reset to the D/A section. A software reset occurs when this bit is toggled to 1, then 0. This resets all DAC outputs and clears the D/A update register.
Bits 3,2	Reserved
Bits 1, 0 (LSB)	These bits control the green and red LEDs. 1 = Turns on red LED 0 = Turns on green LED Refer to the table on the following page for more information on bits 1 and 0.

Status Bits		**LEDs**			
1	**0**	**Green**	**Red**	**SYSFAIL***	**Status**
0	0	Off	On	On	Module failed, or not yet tested
0	1	Off	Off	Off	Inactive module
1	0	On	On	Off	Module undergoing test
1	1	On	Off	Off	Module passed test

Note

Whenever bit 0 is 0, the VMEbus SYSFAIL* signal is asserted, and the red LED turns on. The power-up or reset state for status bits is 00.

D/A Channel Registers (base + 88h - 97h)

Each output channel (8 total) has its own word address, starting at locations 88h and 89h for channel 0 and ending at locations 96h and 97h for channel 7. Each channel can be written as a byte or word. The even byte contains data bits 8-11 and the odd byte contains data bits 0-7. The D/A converters are double buffered, which means the DAC register can be written to without affecting the output of the D/A converter.

When you write to a D/A channel, both RAM and the actual DAC register gets written. During a read, *only* the RAM is read.

Since the D/A RAMs (used for reading DAC registers) power up with unknown data, they must be initialized before they can be read correctly. This is also true for any reset conditions (SYSRESET* or a software reset) since the RAM data remains the same after the reset, while the DAC registers are reset.

Note

When reading a D/A channel, the information read contains the data in the D/A register and not necessarily the actual output of the D/A channel.

D/A Update Register–Channels 0-7 (base + E9h)

> **Note**
>
> When the module is in transparent mode, update registers serve no purpose. In this mode, individual channels are updated with a write to the lower byte of the D/A channel, and only the channel written to is updated.

The D/A channel update registers update up to 8 D/A channels simultaneously when the D/A status/control register is set to simultaneous mode (bit 5 is set to 1). Writing to the D/A channel latches the data into the D/A data register. To update the D/A channel's output, you must write a 1 to the channel update register(s) corresponding to the D/A channel register(s) you want to update. This starts the conversion process.

This register is cleared on power, SYSRESET*, or a D/A software reset.

For example, if you specify bipolar, unsigned (straight binary) mode with a jumper-selected output voltage range of ±10 and you want to set channel 0 to -10 V, channel 3 to 0 V, and channel 7 to +10 V, perform the following steps:

1. Set bit 5 in the D/A status/control register (base + 81h) to 1. This selects simultaneous update mode.
2. Write 0000h to the channel 0 D/A registers (base + 88h-89h).
3. Write 800h to the channel 3 D/A registers (base + 8Eh-8Fh).
4. Write 0FFFh to the channel 7 D/A registers (base + 96h-97h).
5. To update the outputs of channels 0, 3, and 7, write base + 89h to register base + E9h. This byte has a bit pattern corresponding to the channels to be updated. Channel 0 will then update to -10 V; channel 3 will update to 0 V; and channel 7 will update to +10 V.

Interrupt Timer Register (base + 101h)

The 8-bit interrupt timer register generates VMEbus interrupts with configurable delay times. It has the following bit definitions:

Bit 7 (MSB)	Depending on jumper and switch settings, this bit enables or disables periodic VMEbus interrupts.		
	1	=	Enables periodic interrupts
	0	=	Disables periodic interrupts
Bit 6	This period select bit selects the time interval for a one-bit change in delay bits.		
	1	=	Delay bit time interval is 131.072 msec
	0	=	Delay bit time interval is 8.192 msec
Bits 5-3	Reserved		
Bits 2-0 (LSB)	These period multiplier bits select a timeout period for the interrupt timer. The resolution for each bit is determined by the delay set bit.		

The table below defines the interrupt timeout periods.

Period Multiplier Bits	Period Select Bit	Interrupt Timeout Period
000	0	8.192 msec
001	0	16.384 msec
010	0	24.576 msec
011	0	32.768 msec
100	0	40.960 msec
101	0	49.152 msec
110	0	57.344 msec
111	0	65.536 msec
000	1	131.072 msec
001	1	262.144 msec
010	1	393.216 msec
011	1	524.288 msec
100	1	655.360 msec
101	1	786.432 msec
110	1	917.504 msec
111	1	1048.576 msec or 1.048 sec

Interrupt Timeout Periods

Programmable Timer Interrupt Vector Register (base + 103h)

This read/write register holds the vector to be driven on the VMEbus when the interrupt generated by the interrupt timer is acknowledged. This register clears on power up.

Autoscan Control Register (base + 111h)

Continuous conversions are performed on 8, 16, 32, or 64 channels when autoscanning mode is selected (that is, base + 180h is set to 4). The results of each channel are stored in a 16-bit register (using dual-ported RAM) starting at offset 200h (channel 0) and ending at 2Fh (channel 63).

In this mode, end of A/D conversion interrupts cannot be used; however, the programmable interrupt timer is still available.

This register clears on power up or sysreset. Bit 7 can also be cleared by an A/D section software reset.

The bits in this register are defined below:

Bit 7 (MSB) This bit enables or disables the autoscan control register. It is cleared on power up, SYSRESET*, or A/D software reset.

1 = Autoscanning enabled

0 = Autoscanning disabled

Bits 6-2 Reserved

Bits 1, 0 (LSB) These bits, defined in the table below, are used to select the channels to be scanned. These bits are cleared on power up or SYSRESET*.

Scan Select Bits		
Bit 1	**Bit 0**	**Channels Scanned**
0	0	0-7
0	1	0-15
1	0	0-31
1	1	0-64

A/D Mode Register (base + 180h)

This 8-bit register determines the operating mode for the analog inputs used on the module. The bits are defined below:

Bits 15 (MSB) -11 Reserved

Bit 10 Mode bit 2

Bit 9 Mode bit 1

Bit 8 (LSB) Mode bit 0

The mode bits determine the operating mode for analog inputs. One of six modes can be selected, as defined in the table below:

Mode Bits			
Bit 2	**Bit 1**	**Bit 0**	**A/D Conversion Mode**
0	0	0	Single channel
0	0	1	Sequential channel
0	1	0	Random channel
0	1	1	External trigger
1	0	0	Autoscanning
1	0	1	Programming gain

The A/D conversion modes are described below.

Single Channel Mode

In single channel mode, the module automatically starts another conversion on the specified channel after the low byte of the A/D register (base + 187h) has been read. An added feature of the single channel mode is that it offers faster conversions than the other modes (10 µsec as opposed to 26 µsec in sequential, random channel, and external trigger modes, and 18 µsec in autoscanning mode).

Sequential Channel Mode

In sequential channel mode, the module automatically increments the channel number by one and initiates a conversion on the next channel (previous channel + 1), after the low byte of the A/D register (base + 187h) has been read. You can force a conversion in this mode without incrementing the channel number by writing a 1 to bit 7 of the status/control register (base + 181h).

Random Channel Mode

In random channel mode, a control byte written to the low byte of the gain/channel register (base + 184h) that specifies a channel number automatically starts a conversion on the specified channel.

External Trigger Mode

External trigger mode allows the rising edge of a low-going, externally triggered pulse (on pin 50 of JK1)–referenced to power ground (pin 49 of JK1, J65IN)–to initiate a conversion.

Autoscanning Mode

Autoscanning mode performs continuous conversions on 8, 16, 32, or 64 channels, and stores the results of each channel in its own 16-bit register starting at offset base + 200h for channel 0 to base + 27Fh for channel 63. When autoscanning mode is selected, and bit 7 of the autoscan control register is set to 1, conversions are initiated and stored. End of A/D conversion interrupts cannot be used with this mode and will not generate interrupts. However, the programmable interrupt timer is available.

Programming Gain Mode

After power up or system reset, use this mode to initialize the XVME-542's on-board gain RAM to provide each input channel with an associated gain factor from the jumper-selectable range set at installation. Once an input channel is initialized, the associated gain factor is automatically applied when an A/D conversion occurs on that channel.

To program the gain RAM, first select programming gain mode. Once this mode is set, you can write the gain for each channel to the high byte of the gain/channel register (base + 184h). Refer to the A/D Gain/Channel Register section later in this chapter for more information on programming the gain RAM.

A/D Status/Control Register (base + 181h)

This 8-bit register is used to monitor the status of A/D channels, enable and disable interrupts, and reset the module. The bits in this register are defined below:

Bit 7 (MSB) — This bit acts as a busy flag to show when an A/D conversion is in progress.

1	=	A/D conversion in process
0	=	No conversion in process

Bit 6 — This bit initiates a conversion. The length of the conversion is dependent upon which of the six A/D modes the board is operating.

1	=	Conversion initiated
0	=	No conversion initiated

Bit 5 — Reserved

Bit 4 — This bit is used to perform an analog input section software reset. A software reset stops a conversion in process and clears any end-of-conversion interrupts. It also clears the interrupt pending flag (bit 2), resets the gain/channel register (base + 184h), and disables scanning by clearing the scan control bit (bit 7 of base + 111h).

1	=	Starts the software reset process
0	=	Stops the reset

Bit 3 — When the associated jumpers and switches are set, this bit generates end of A/D conversion VMEbus interrupts.

1	=	Enables end of A/D conversion VMEbus interrupts
0	=	Disables end of A/D conversion VMEbus interrupts

Bit 2 — This bit is an interrupt pending flag.

1	=	End of conversion has occurred
0	=	End of conversion has not occurred

To clear this bit you must cause a new A/D conversion, perform a backplane or software reset, read the converted input data from the low order data byte, or select autoscanning mode.

Bits 1, 0 (LSB) — Reserved

End of Conversion Vector Register (base + 183h)

This register stores the vector used for end of A/D conversion interrupts.

A/D Gain/Channel Register (base + 184h)

This 16-bit register initiates A/D conversions when you write the desired channel to the lower byte while in random channel mode.

This register is also used to program a gain factor for input channels by writing to the higher byte while in programming gain mode. Use bits 8 and 9 to first select the gain, as shown in the table below.

Gain/Channel Register		Jumper-Selected Gain		
Bit 9	**Bit 8**	**Range 1**	**Range 2**	**Range 3**
0	0	1	4	10
0	1	2	8	20
1	0	5	20	50
1	1	10	50	100

Once the gain has been selected, write to the lower byte with the desired channel to program. Writing to the lower byte programs the gain for that channel. You may also write a word at a time to simultaneously select the gain and the desired channel to program.

A/D Scan Registers (base + 200h - 3FEh)

While in autoscanning mode, these registers are used to store A/D readings. Each register keeps an updated reading of the specified channel.

A/D Conversions

Following are some general steps for configuring the XVME-542 to convert analog inputs to digital data:

1. Configure jumpers and switches (refer to Chapter 2) for the desired interrupt level, input type (differential, single-ended, or pseudo-differential and bipolar or unipolar), input voltage range, input gain range, and input binary data format.
2. Program the gain RAM by setting programming gain mode, then writing to the gain/channel register (base + 184h).
3. Perform calibration (see Chapter 4).
4. Select one of the five A/D conversion modes by writing to the A/D mode register (base + 180h).
5. Initiate the A/D conversion process.

Chapter 4 – Calibration

Calibration facilities have been provided on the AIO module for both analog input and analog output circuits. The module is calibrated in the ±10 V A/D input voltage range and the 0-10 V D/A output voltage range before it leaves the factory. However, if the module is configured to operate in ranges other than these, it is recommended that the calibration be checked and adjusted. As a general rule, the input/output circuitry should be recalibrated whenever voltage range jumpers and voltage/current select jumpers are changed.

Resistor Number	**Type of Adjustment**
R69	Offset for A/D convertor
R70	Gain for input circuit
R76	Programmable gain amp offset

A/D Calibration Potentiometers

The calibration procedure is divided into two parts: input circuit calibration and output circuit calibration. Input circuit calibration entails offset nulling the instrumentation amplifier, and offset adjusting and gain adjusting the A/D converter. Output calibration entails offset and gain adjustment for each output channel in either unipolar or bipolar modes.

The table below defines the potentiometers for both A/D and D/A calibrations.

Resistor Number	Type of Adjustment
R19	Channel 7 gain
R26	Channel 6 gain
R33	Channel 5 gain
R40	Channel 4 gain
R45	Channel 3 gain
R52	Channel 2 gain
R57	Channel 1 gain
R64	Channel 0 gain
R20	channel 7 bipolar offset
R27	Channel 6 bipolar offset
R34	Channel 5 bipolar offset
R41	Channel 4 bipolar offset
R46	Channel 3 bipolar offset
R53	Channel 2 bipolar offset
R58	Channel 1 bipolar offset
R65	Channel 0 bipolar offset
R21	Channel 7 unipolar offset
R28	Channel 6 unipolar offset
R35	Channel 5 unipolar offset
R42	Channel 4 unipolar offset
R47	Channel 3 unipolar offset
R54	Channel 2 unipolar offset
R59	Channel 1 unipolar offset
R66	Channel 0 unipolar offset

Calibration Potentiometers

Input Calibration

You will need the following equipment to perform an input calibration:

- Five-digit volt meter capable of reading ±30 µV
- Small flat-bladed screw driver
- Precision voltage source capable of supplying 1.22 mV ±30 µV

Inputs can be calibrated in either single-ended or differential configuration. Calibration begins by offset nulling the instrumentation amplifier with channel 0 selected and its inputs grounded.

Programmable Gain Offset Adjustment

Perform the following steps to adjust the programmable gain offset for single-ended, unipolar operation:

1. Remove any connectors at JK1.
2. Ground input channel 0 by setting jumper J66 to B.
3. Measure and record the output voltage of gain amp U39, pin 6 using the Fluke 8860 DMM.
4. Next, measure the voltage of gain amp U37, pin 6.
5. Adjust R76 so the output voltage of U37, pin 6 matches the output voltage of U39, pin 6.
6. Reset jumper J66 to A for the rest of the calibration.

A/D Offset and Gain Adjustment

With the previous networks nulled, it is necessary to perform continuous conversion on channel 0. Channel 0 must be set for the lowest programmable gain (G=1; bits 6 and 7 of the gain/channel register must be set to 0).

There are two types of input calibration: zero (0 + .5 LSB) and full scale (+FS - 1.5 LSB). Conversion results should be display on a CRT in hex format for verification. Both must be performed on the XVME-542, as described below.

Zero Calibration

The table below provides information necessary to perform a zero calibration (+.5 LSB).

Binary Encoding Mode	Voltage Range	Analog Voltage In	Adjust POT	Transition Points
Unipolar (straight binary)	0-5 V	.04 mV	R69	0000h/0001h
	0-10 V	.08 mV	R69	0000h/0001h
Bipolar (offset binary)	±2.5 V	.04 mV	R69	8000h/8001h
	±5 V	.08 mV	R69	8000h/8001h
	±10 V	.15 mV`	R69	8000h/8001h
Bipolar	±2.5 V	.04 mV	R69	0000h/0001h
(two's	±5 V	.08 mV	R69	0000h/0001h
complement)	±10 V	.15 mV`	R69	0000h/0001h

A/D Zero Calibration Points

To perform a zero calibration,

1. Apply the .5 LSB analog voltage in (for binary encoding mode and the voltage range chosen) to channel 0.
2. Adjust the zero calibration and the POT until the display reading toggles between the zero calibration and transition point values.

For example, to perform a zero calibration on an XVME-542 configured for bipolar, offset binary, ±10 V range operation,

- Apply +.15 mV to channel 0
- Adjust R69 until the display reading toggles between 0000h and 0001h

Full Scale Calibration

The table below provides information necessary to perform a full scale calibration (+FS - 1.5 LSB).

Binary Encoding Mode	Voltage Range	Analog Voltage In	Adjust POT	Transition Points
Unipolar (straight binary)	0-5 V	4.99988 V	R70	FFFEh/FFFFh
	0-10 V	9.99977 V	R70	FFFEh/FFFFh
Bipolar (offset binary)	±2.5 V	2.49988 V	R70	FFFEh/FFFFh
	±5 V	4.99977 V	R70	FFFEh/FFFFh
	±10 V	9.99954 V	R70	FFFEh/FFFFh
Bipolar (two's complement)	±2.5 V	2.49988 V	R70	7FFEh/7FFFh
	±5 V	4.99977 V	R70	7FFEh/7FFFh
	±10 V	9.99954 V	R70	7FFEh/7FFFh

A/D Full Scale Calibration Points

To perform a full scale calibration,

1. Apply the analog voltage in (for binary encoding mode and the voltage range chosen) to channel 0.
2. Adjust the full scale calibration and the POT until the display reading toggles between the full scale calibration and transition point values.

For example, to perform a full scale calibration on an XVME-542 configured for bipolar, offset binary, ±10 V range operation,

- Apply +9.99954 V to channel 0
- Adjust R70 until the display reading toggles between FFFEh and FFFFh

Output Calibration

You need the following equipment to perform an output calibration:

- Five-digit volt meter capable of reading ±30 µV
- Small flat-bladed screw driver

Output calibration entails voltage offset and gain adjustments for each channel in both unipolar and bipolar configurations. The following table shows which potentiometers relate to which output channels.

Unipolar	Bipolar	Gain	Corresponding Channel
R66	R65	R64	Channel 0
R59	R58	R57	Channel 1
R54	R53	R52	Channel 2
R47	R46	R45	Channel 3
R42	R41	R40	Channel 4
R35	R34	R33	Channel 5
R28	R27	R26	Channel 6
R21	R20	R19	Channel 7

Output Offset Adjustment Potentiometers

Unipolar Offset Adjustment

Perform the following steps to adjust the unipolar offset:

1. Set jumpers to the desired unipolar range.
2. Turn all bits off (load binary zeros) to the channel being calibrated.
3. Make sure the channel is jumpered for voltage output (J39-J42).
4. Adjust the unipolar potentiometer that corresponds to the channel being calibrated until the output reads 0.0000 volts ±30 µV.
5. Turn all bits on (FFFh) to the channels being calibrated.
6. Adjust the corresponding gain potentiometer until the output is 1 LSB less than the nominal full scale.

Range	Output
0-5 V	4.9987 V
0-10 V	9.9976 V

Steps 2, 3, and 5 may also be executed with the channels configured for current output. In this case, the channel offset potentiometer is adjusted for an output of 4 mA (or 1.000 V ±30 µV across a 250 Ohm, 0.1% resistor returned to ground on connector JK2), and the gain potentiometer should be adjusted for an output of 20 mA (or 5.000 V).

Note

Make certain that the resistor used does not change value due to self-heating.

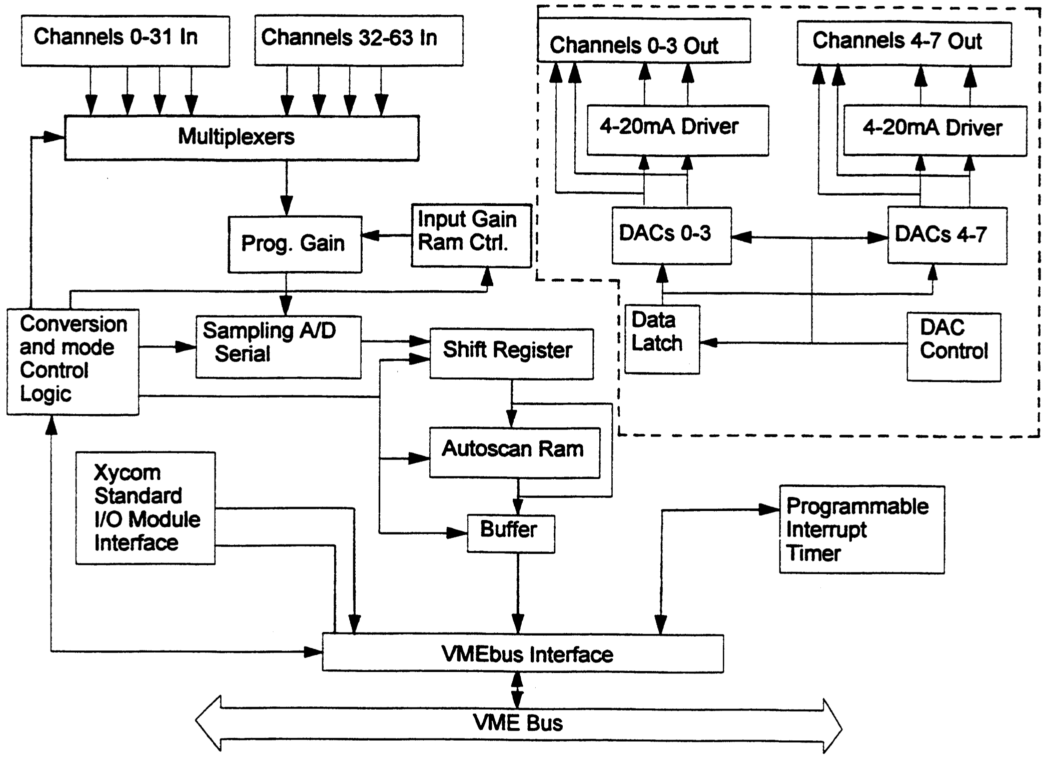
Bipolar Offset Adjustment

Perform the following steps for bipolar offset adjustment:

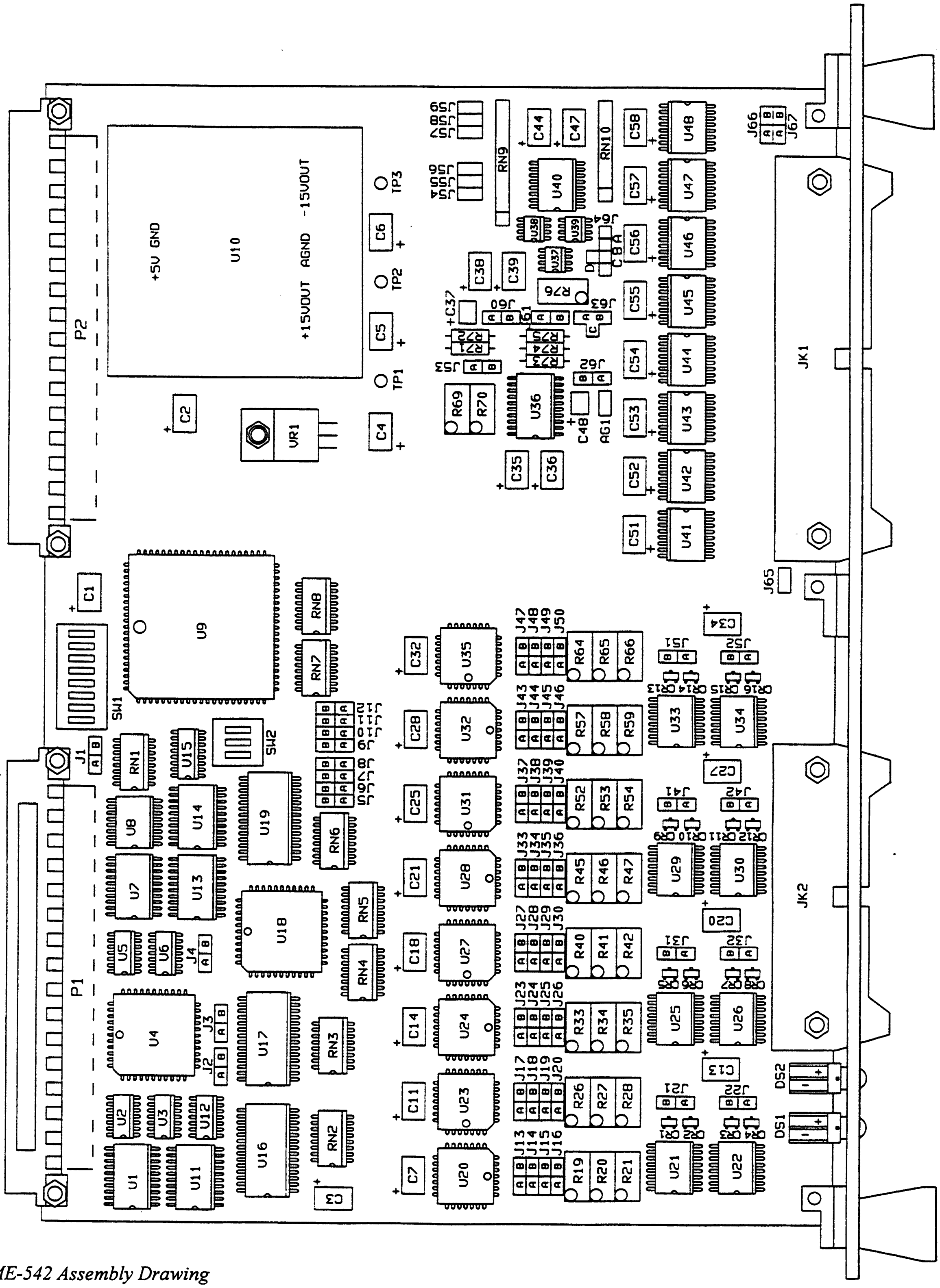
1. Set jumpers to the desired bipolar range.
2. Turn all bits off (load binary zeros) to the output channel being calibrated.
3. Adjust the bipolar potentiometer that corresponds to the channel being calibrated until the output reads -FS (-2.5, -5.0, -10.0)
4. Turn all bits on (load FFFh) to the output channel being calibrated.
5. Adjust the gain potentiometer until the output reads 1 LSB less than +FS.

Range	Output
±2.5 V	2.4988 V
±5.0 V	4.9976 V
±10.0 V	9.9951 V

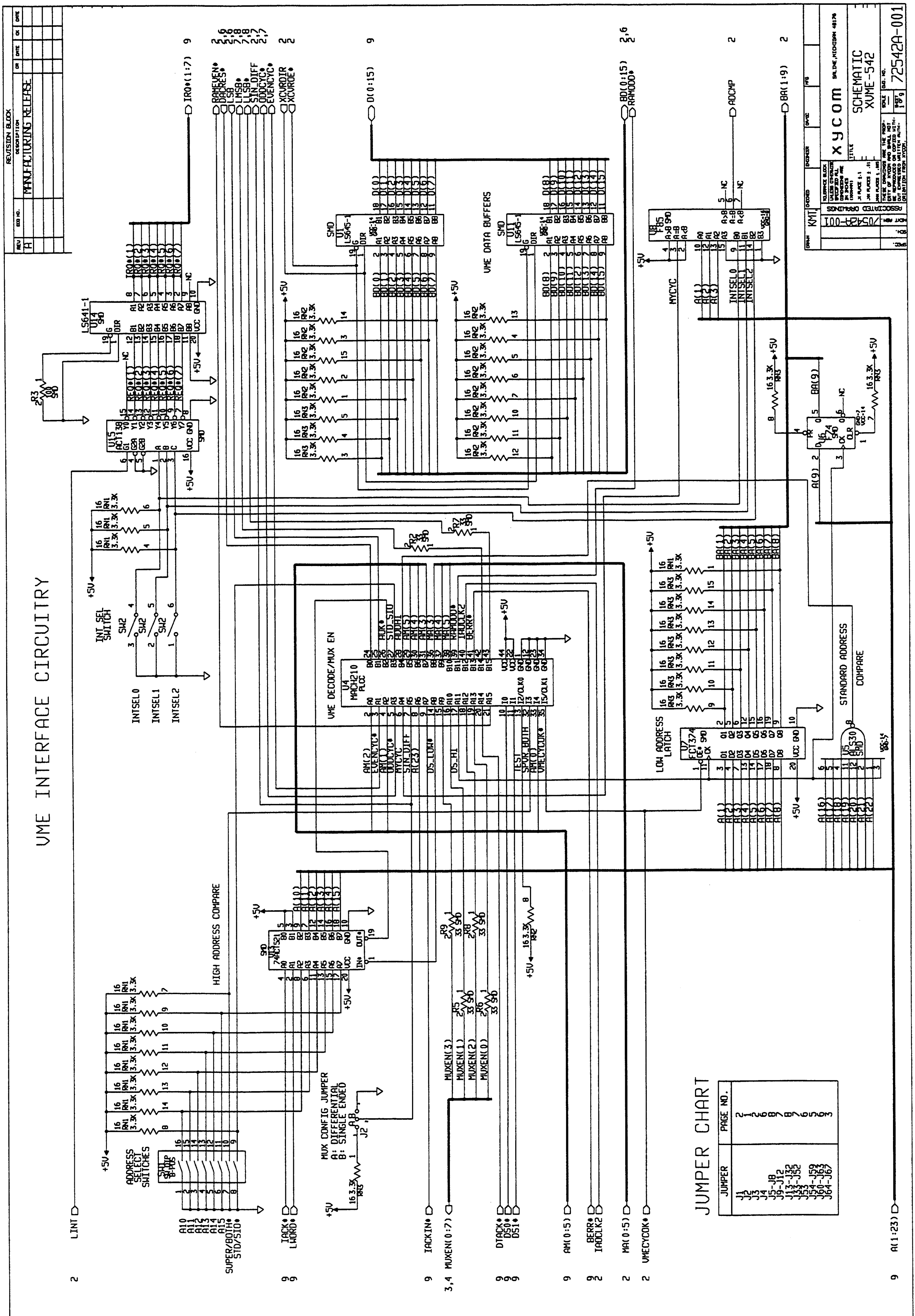
Appendix A – Schematics and Diagrams

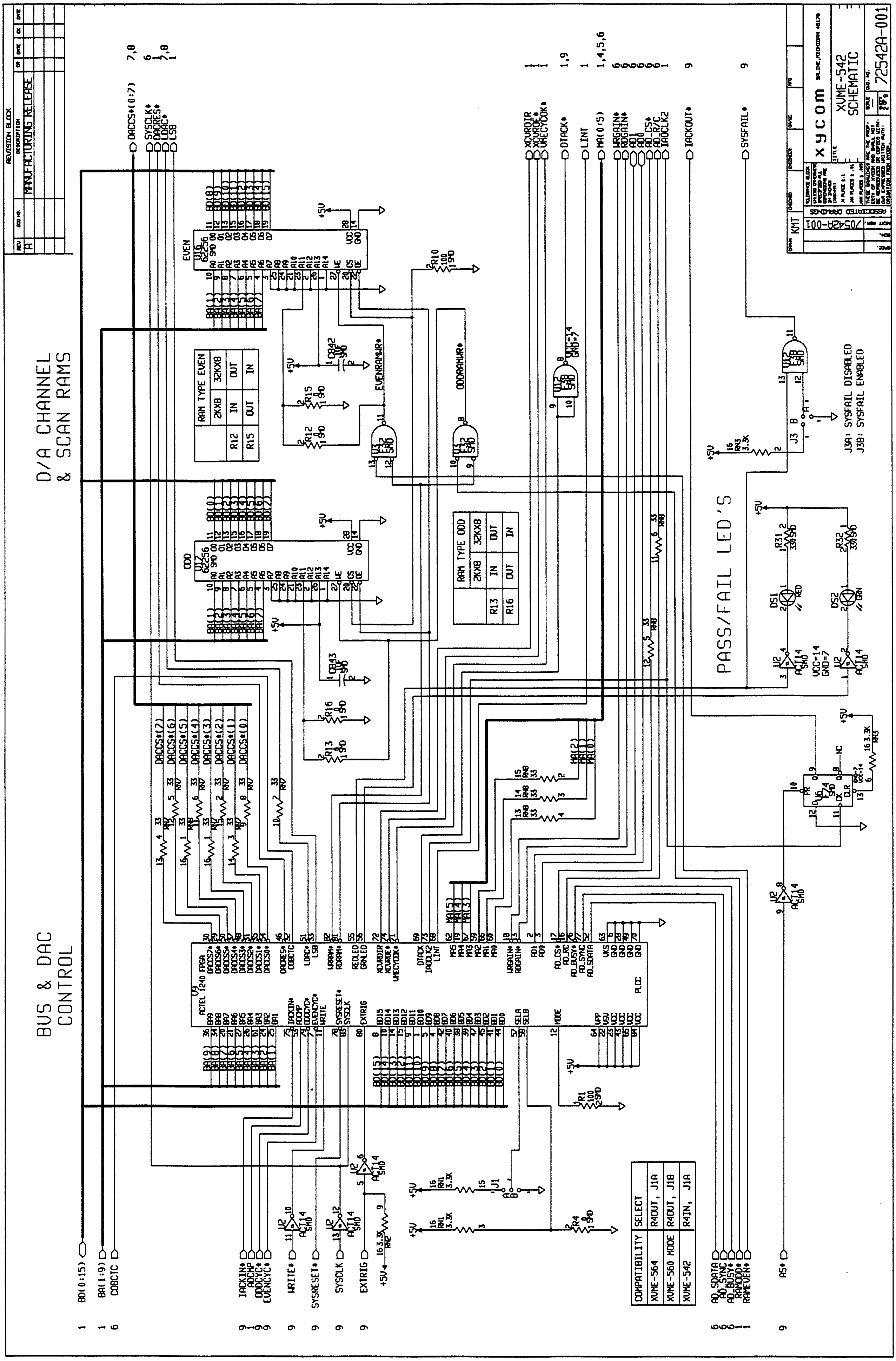


XVME-542 Block Diagram



XVME-542 Assembly Drawing


VME INTERFACE CIRCUITRY
VME DATA BUFFERS
VME DECODE/MUX EN
HIGH ADDRESS COMPARE
STANDARD ADDRESS COMPARE
LOW ADDRESS LATCH
ADDRESS SELECT SWITCHES
INT SEL SWITCH
MUX CONFIG JUMPER
A: DIFFERENTIAL
B: SINGLE ENDED
JUMPER CHART
MANUFACTURING RELEASE
xycom
SCHEMATIC
XVME-542
72542A-001



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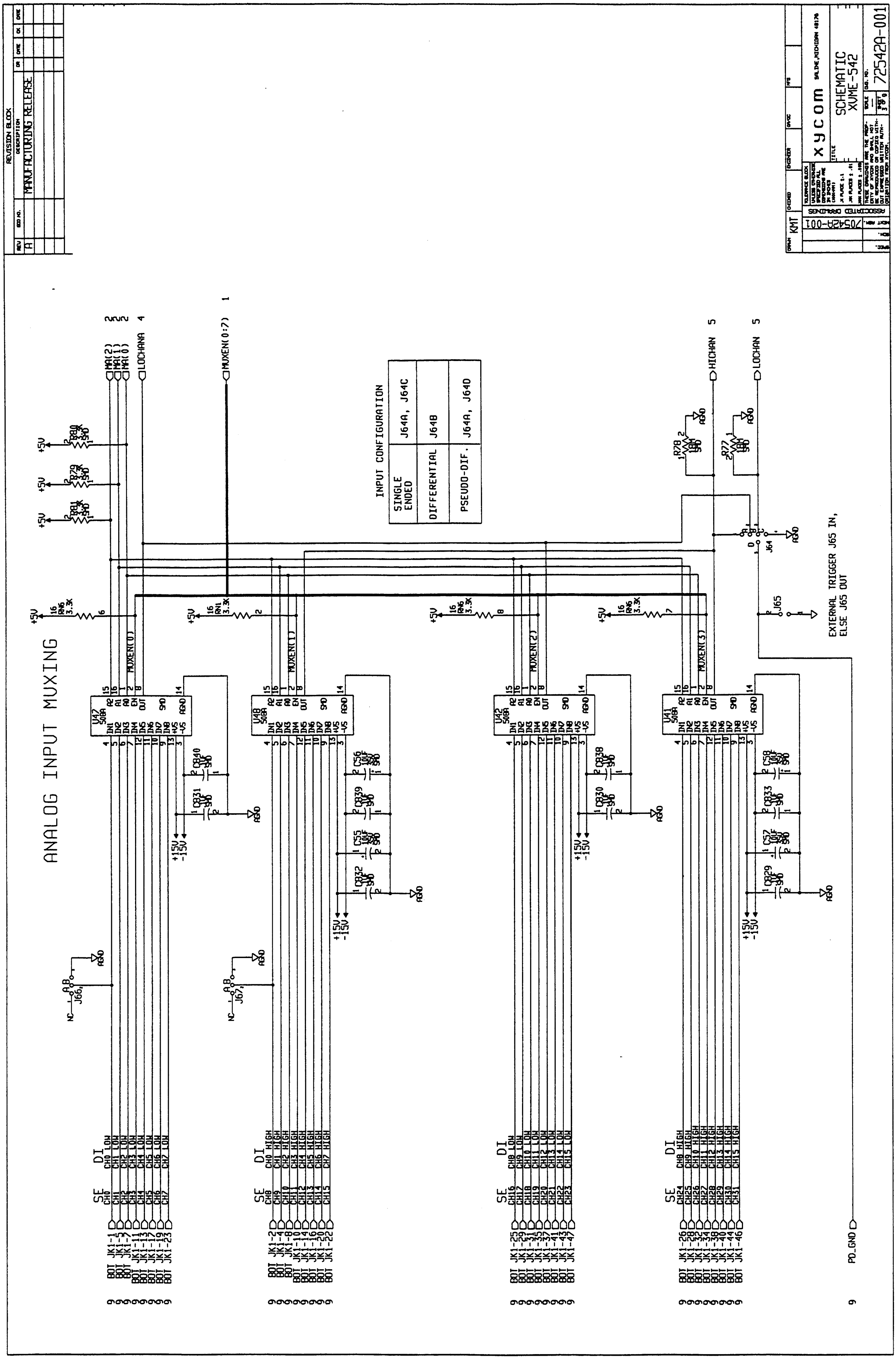
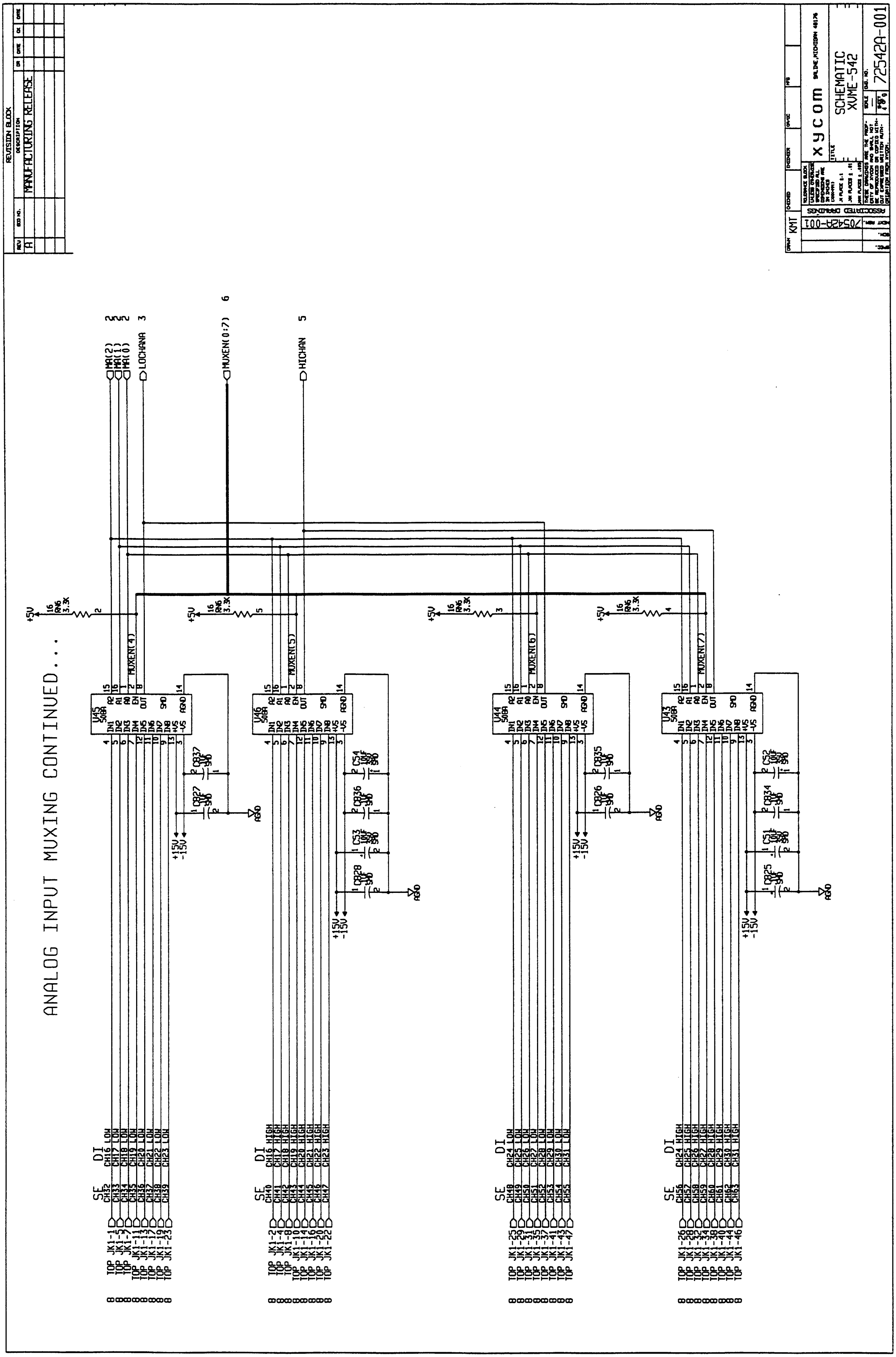
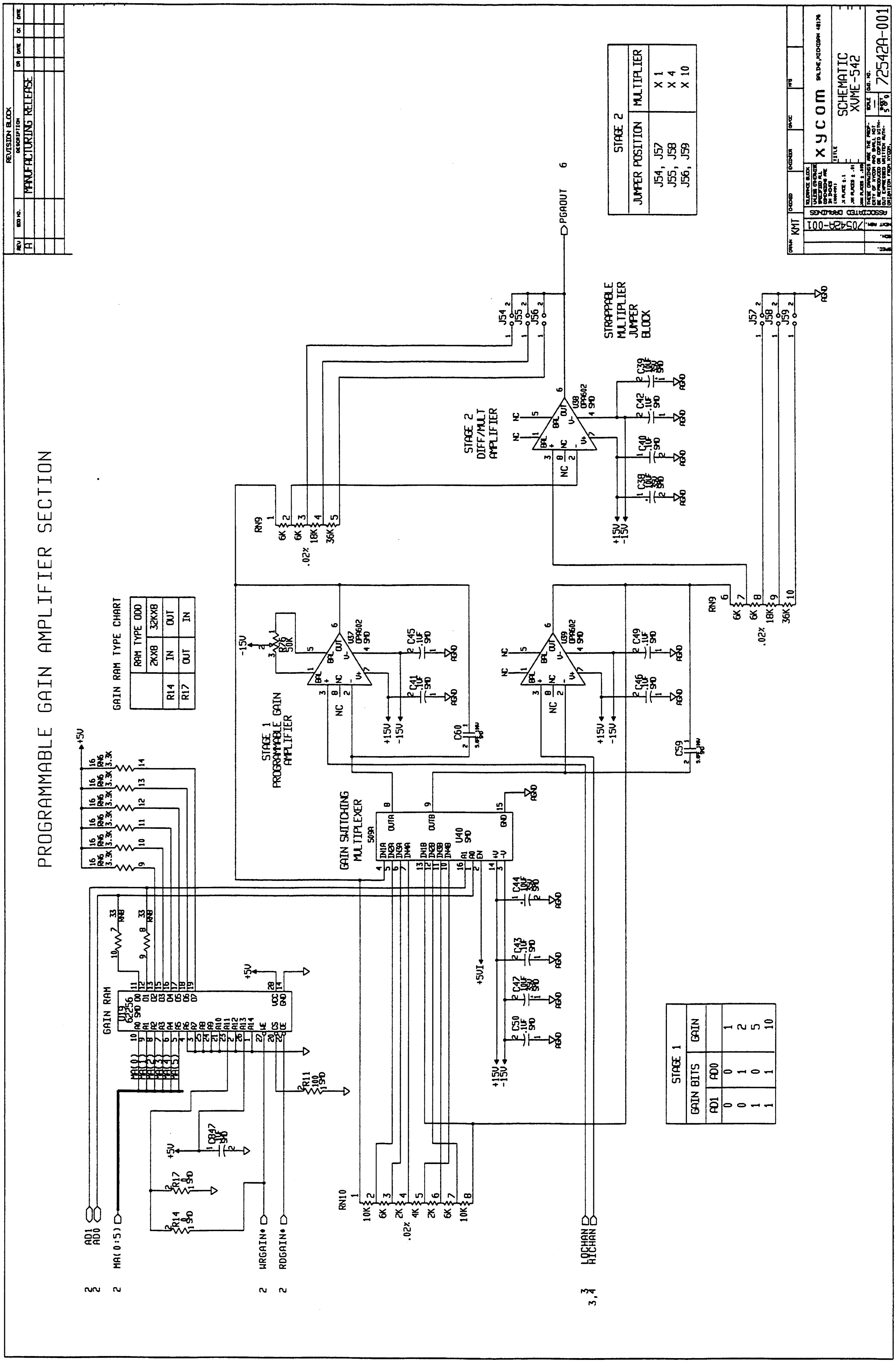
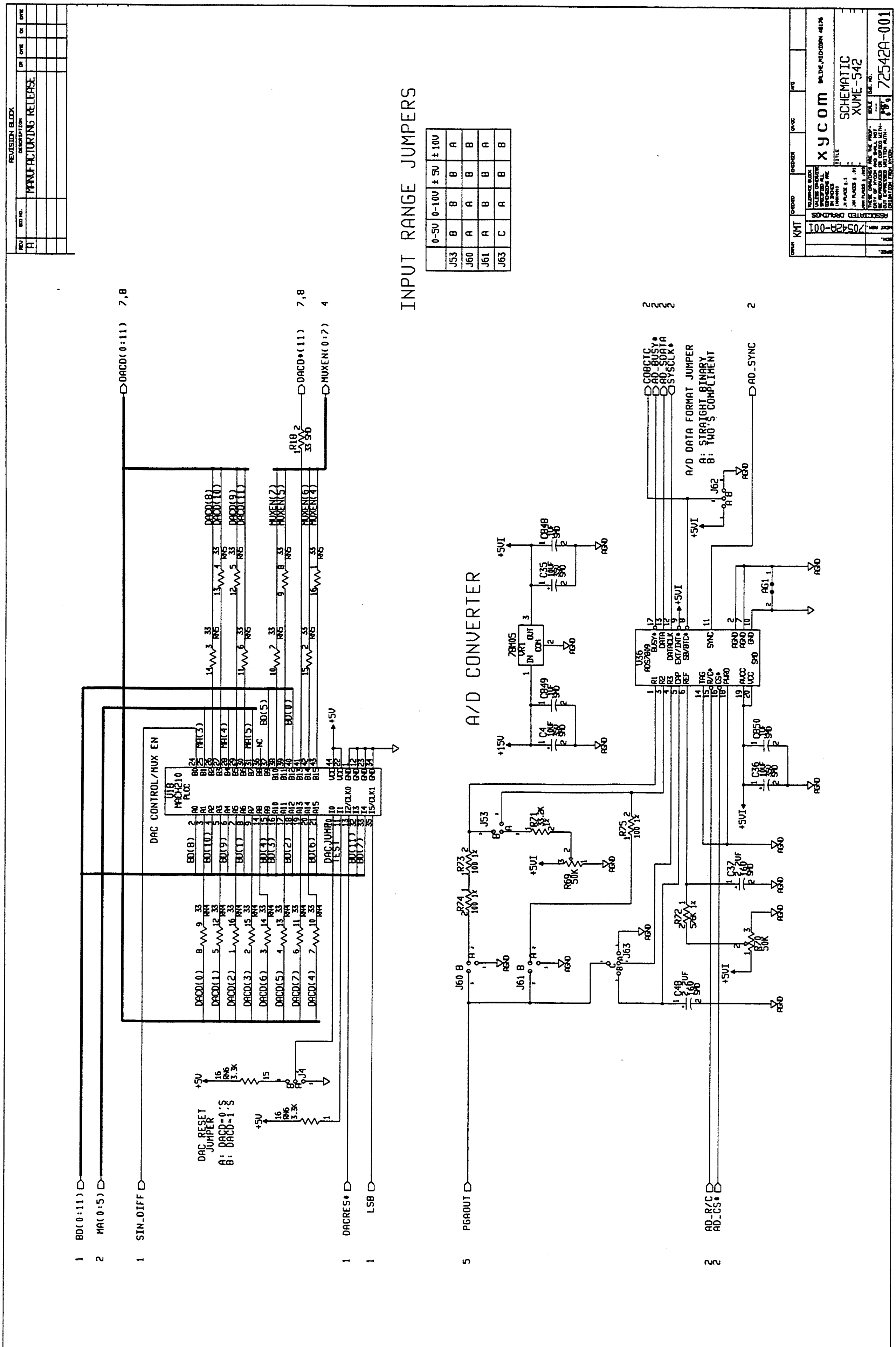

ANALOG INPUT MUXING
INPUT CONFIGURATION
SINGLE ENDED
J64A, J64C
DIFFERENTIAL
J64B
PSEUDO-DIF.
J64A, J64D
EXTERNAL TRIGGER J65 IN, ELSE J65 OUT
REVISION BLOCK
MANUFACTURING RELEASE
xycom
SCHEMATIC XVME-542
72542A-001


ANALOG INPUT MUXING CONTINUED...
xycom
SCHEMATIC
XVME-542
72542A-001
MANUFACTURING RELEASE


PROGRAMMABLE GAIN AMPLIFIER SECTION
STAGE 1 PROGRAMMABLE GAIN AMPLIFIER
STAGE 2 DIFF/MULT AMPLIFIER
GAIN SWITCHING MULTIPLEXER
STRAPPABLE MULTIPLIER JUMPER BLOCK
GAIN RAM
GAIN RAM TYPE CHART
RAM TYPE ODD
2KX8
32KX8
R14 IN OUT
R17 OUT IN
STAGE 1
GAIN BITS
AD1 AD0 GAIN
0 0 1
0 1 2
1 0 5
1 1 10
STAGE 2
JUMPER POSITION MULTIPLIER
J54, J57 X 1
J55, J58 X 4
J56, J59 X 10
PGAOUT
AD1
AD0
MA(0:5)
WRGAIN*
RDGAIN*
LOCHAN
HICHAN
REVISION BLOCK
MANUFACTURING RELEASE
xycom
SCHEMATIC XVME-542
72542A-001


INPUT RANGE JUMPERS
0-5V 0-10V ±5V ±10V
J53 B B B A
J60 A A B B
J61 A B B A
J63 C A B B
A/D CONVERTER
DAC CONTROL/MUX EN
A/D DATA FORMAT JUMPER
A: STRAIGHT BINARY
B: TWO'S COMPLIMENT
DAC RESET JUMPER
A: DACD=0'S
B: DACD=1'S
REVISION BLOCK
MANUFACTURING RELEASE
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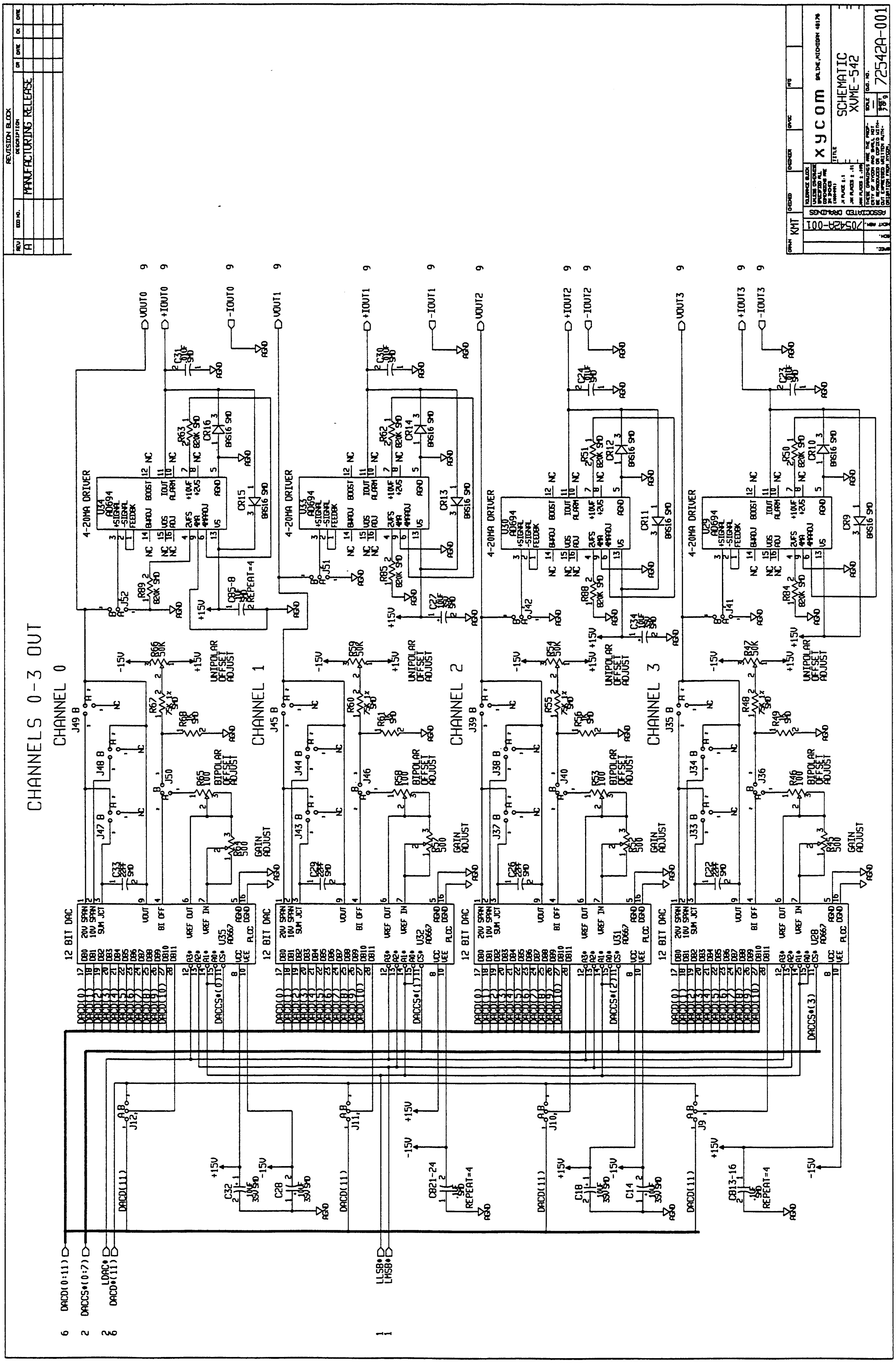
SCHEMATIC
XVME-542
72542A-001



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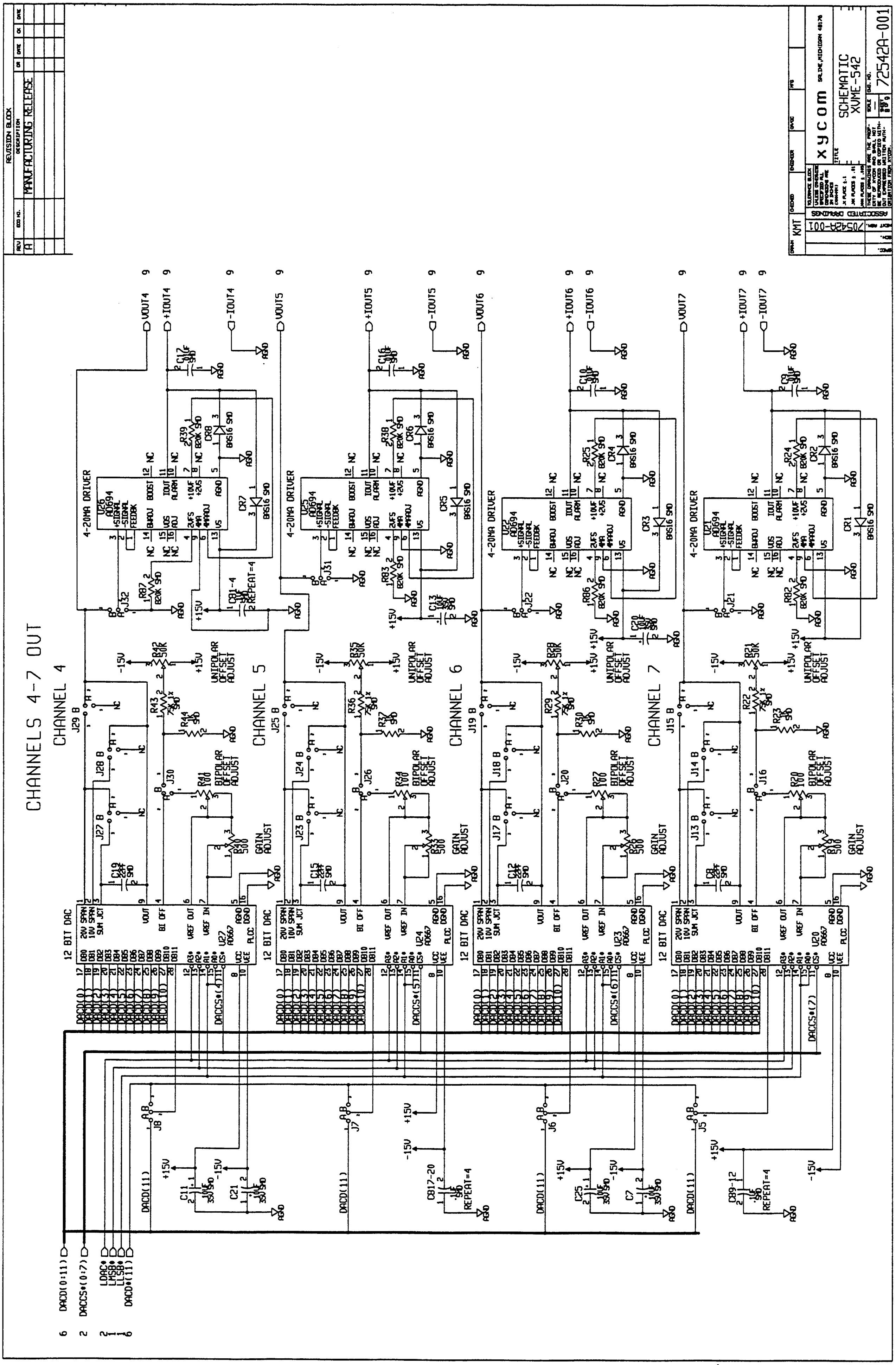
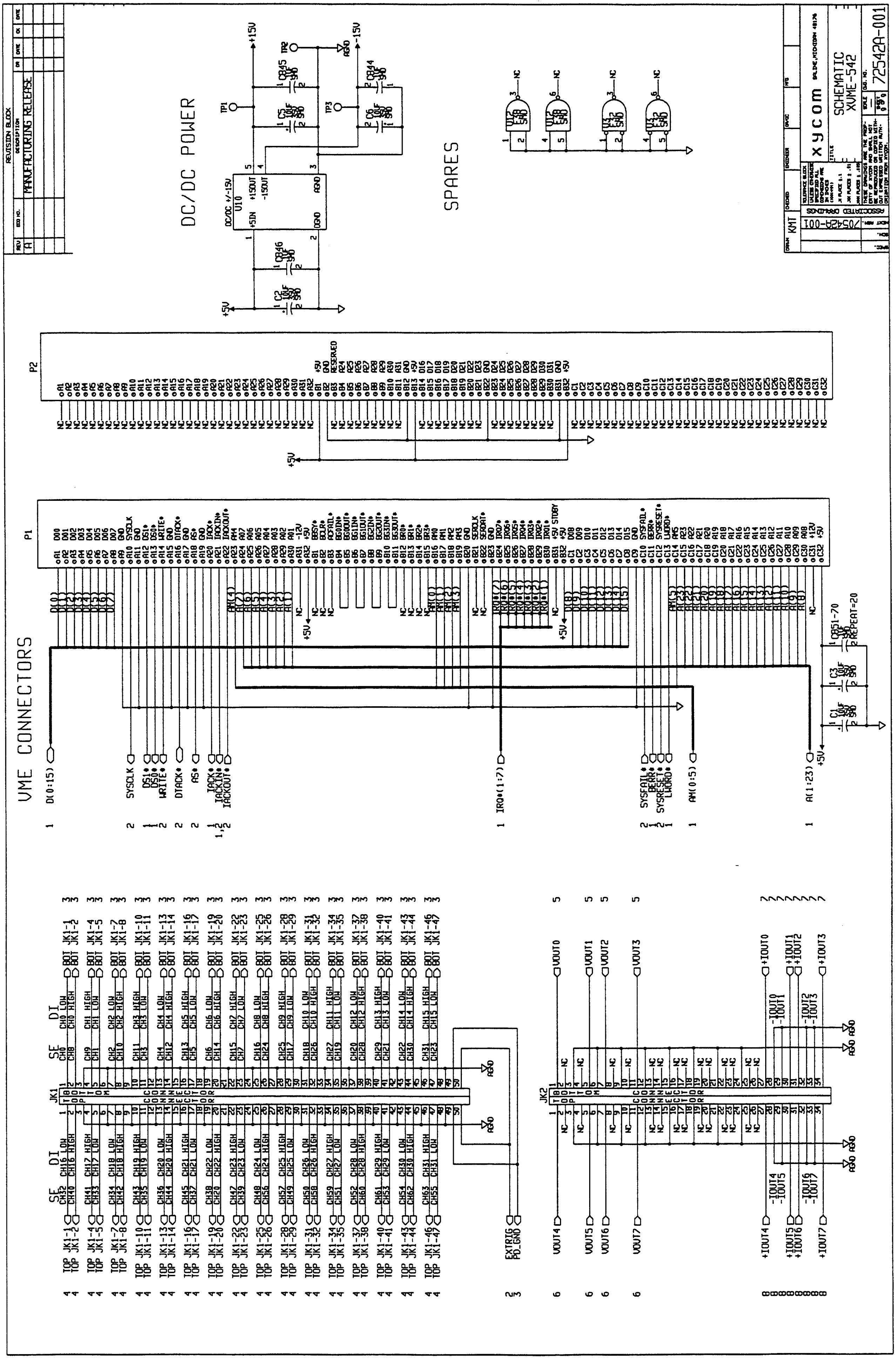

CHANNELS 4-7 OUT
CHANNEL 4
CHANNEL 5
CHANNEL 6
CHANNEL 7
4-20MA DRIVER
12 BIT DAC
UNIPOLAR OFFSET ADJUST
BIPOLAR OFFSET ADJUST
GAIN ADJUST
REVISION BLOCK
MANUFACTURING RELEASE
xycom
SCHEMATIC XVME-542
72542A-001



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