SIS3350
500 MHz 12-bit
VME Digitizer

User Manual

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Revision Table:

Revision	Date	Modification
0.00TH	27.04.07	Generation
0.01	24.09.07	Power Consumption
0.02	26.10.07	Front panel, silk, DAC registers
0.03	28.10.07	VGA Gain registers, update frequency synthesizer register
0.04	29.10.07	On Board
0.05	30.10.07	JP80 Vision drawing
0.06	26.11.07	Temporary release
1.00	04.09.08	Initial release for 0x0101 firmware
1.01	29.09.08	Bug fix in ring/DDR memory diagram, gate chaining diagram
1.02	28.01.09	N Divider frequency range setting table ADC DAC Data register explanation

- Table of contents

1 Introduction

The SIS3350 is the extension of our 12-bit digitizer family (so far consisting of the 100 MHz SIS3300 and the 250 MHz SIS3320-250) towards higher sampling speed and deeper memory. The unit has 4 digitizer channels sampling at up to 500 MSamples/s each, and a default memory depth of 128 MSamples per channel (i.e. acquisition of ¼ s at full sampling rate). The use of 512 MSamples per channel (allowing for 1s acquisition at full sampling speed) is prepared also.
An offset DAC per channel in combination with a variable gain amplifier (VGA) gives you oscilloscope like input stage behaviour in combination with superior resolution.
The module was designed in a fashion, that it can be operated in any 6U standard VME enclosure/crate, i.e. no non standard voltages going beyond +5, -12V and +12 V are required. The card is a single slot (4TE) design which is available with standard and VME64x lever handles.
Besides VME bus readout functionality a 4 GBit optical link and a 10/100/1000 raw Ethernet are available as data transfer options with given interest in the corresponding firmware implementation. The 4 GBit LC-LC SFF (small form factor) link medium connection is foreseen to be used in combination with the SIS1100-eCMC PCI Express card.

Applications comprise but are not limited to:

- digitization of fast detector signals
- accelerator/machine controls

As we are aware, that no manual is perfect, we appreciate your feedback and will try to incorporate proposed changes and corrections as quickly as possible. The most recent version of this manual can be obtained by email from info@struck.de, the revision dates are online under http://www.struck.de/manuals.htm.

1.1 Related documents

A list of available firmware designs can be retrieved from http://www.struck.de/sis3350firm.htm

2 Technical Properties/Features

2.1 Key functionality

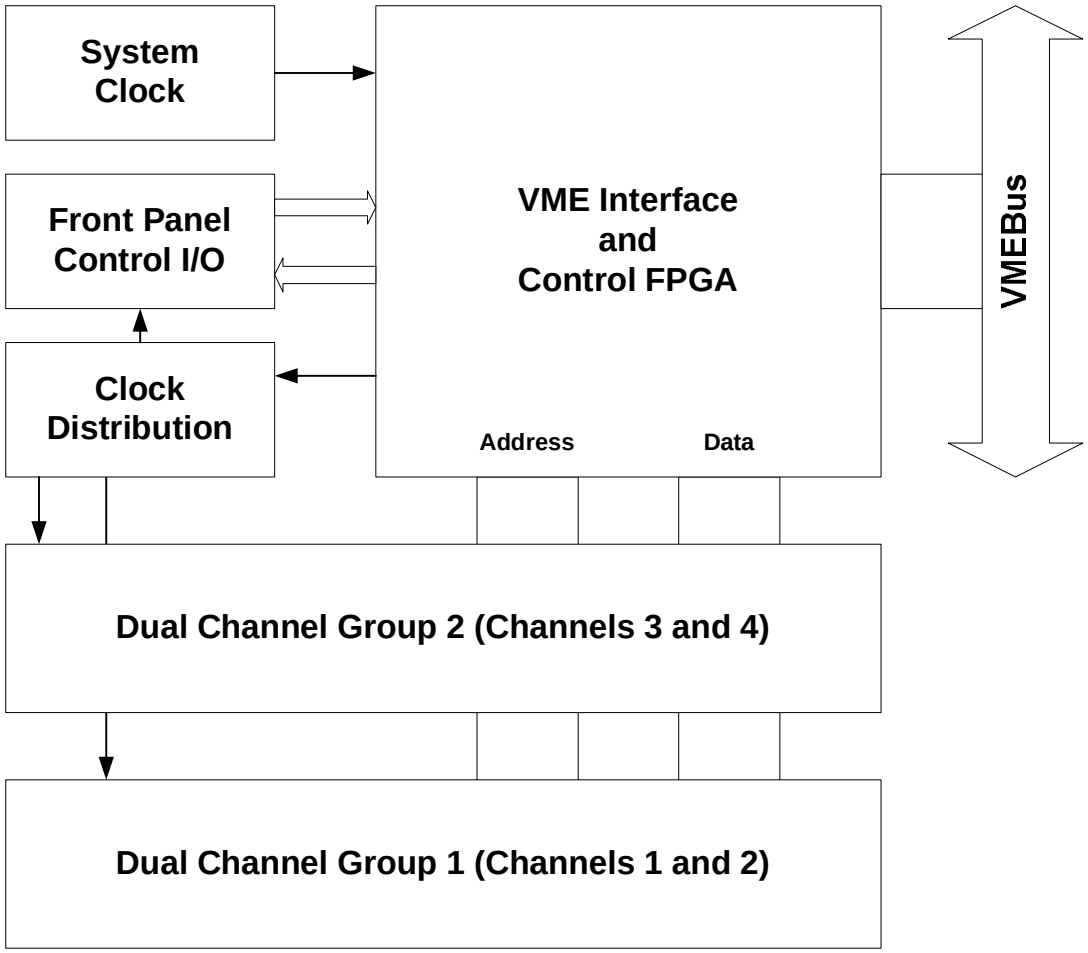
Find below a list of key features of the SIS3350 digitizer.

- 4 channels
- 12-bit resolution
- 128 MSamples/channel memory
- special clock modes (clock prescaling, external “arbitrary” clock)
- Variable gain amplifiers (VGA)
- offset DACs
- external/internal clock
- external random clock
- multi event mode
- read on the fly (actual sample value)
- pre/post trigger option
- readout in parallel to acquisition
- trigger generation (FIR trigger)
- 4 NIM control inputs/4 NIM control outputs
- A32 D32/BLT32/MBLT64/2eVME
- Hot swap (in conjunction with VME64x backplane)
- VME64x Connectors
- VME64x Front panel
- VME64x extractor handles (on request)
- F1002 compatible P2 row A/C assignment
- +5 V, +12V and –12 V VME standard voltages
- Optical 4-Gigabit link connection
- Ethernet connection

Note: The SIS3350 shall not be operated on P2 row A/C extensions, like VSB e.g. due to the compatibility to the F1001 FADC modules clock and start/stop distribution scheme. The P2 row A/C connections can be removed on request.

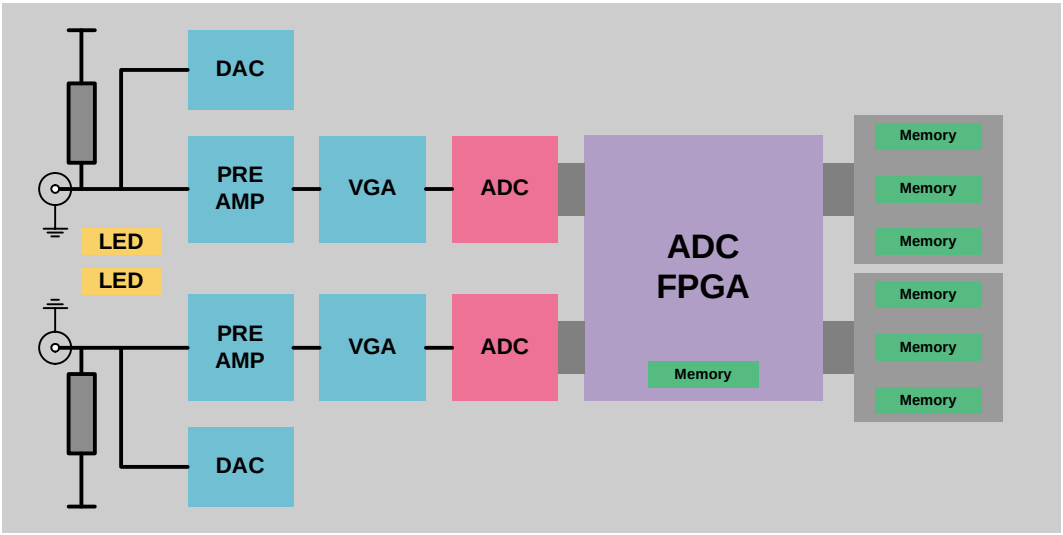
2.2 Module design

The SIS3350 consists of two identical groups of 2 ADC channels each and a control section as shown in the simplified block diagram below.



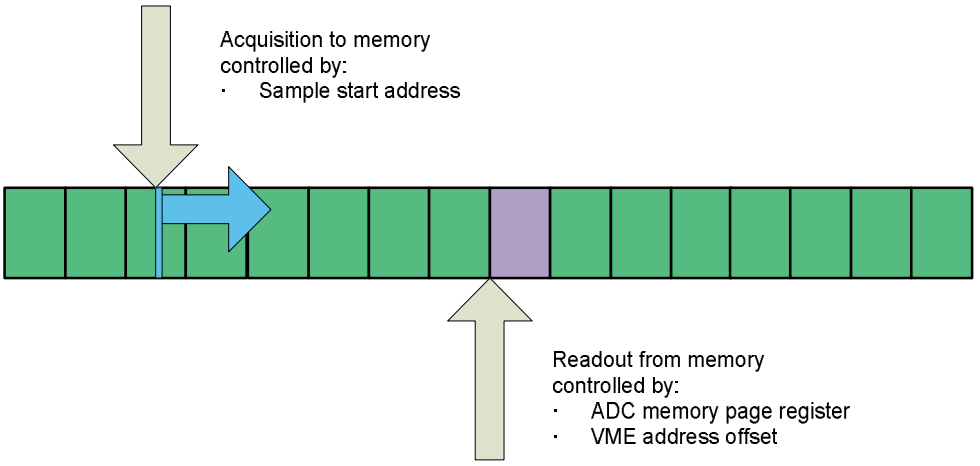
2.2.1 Dual channel group

Two ADC channels form a group, which memory is handled by one Field Programmable Gate Array (FPGA). A dual channel group has block memory, which resides in the FPGA, and external DDR2 memory (128 MSamples/channel default). The block memory holds a ring buffer with a “length” of 16 K samples per channel.



2.2.2 Memory philosophy

The DDR2 memory of the SIS3350 is controlled by the sample start address during acquisition. The default memory of 128 MSamples/channel is divided into 16 pages of 16 MByte each. The memory page register defines which page can be accessed over the VME bus. Full memory is accessible during acquisition however with the option to restrict the use to part of the memory, or to divide the memory into smaller events.

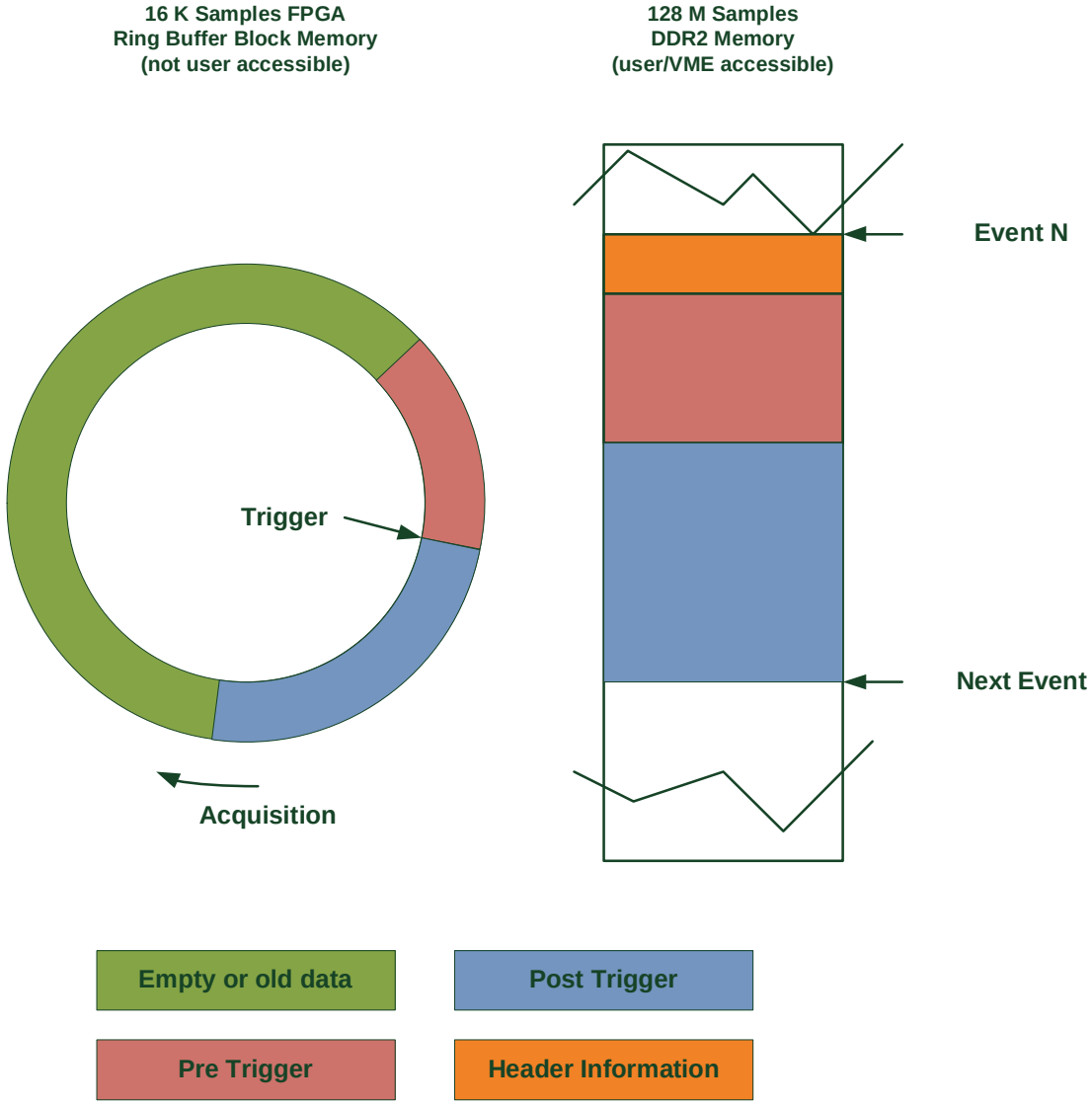


2.2.3 Internal memory handling

The stream of digitized data from the ADC chips is always recorded to the block memory of the FPGA chips. This mechanism facilitates DDR2 memory refresh handling and the implementation of parallel acquisition and readout.
We distinguish two basic memory modes

- Ring buffer acquisition
- Direct memory acquisition

Ring buffer acquisition is limited to events that fit completely into the 16K block memory and the complete event is transferred to DDR2 memory upon completion. In direct memory acquisition blocks of data are streamed to DDR2 memory during acquisition.
This internal memory handling implementation enables on board data rearrangement prior to readout in all modes of operation except for “Direct Memory Trigger Stop”.



Note: please refer to the PDF in case of black print

2.3 Modes of Operation

The implemented modes of operation of this generic SIS3350 firmware implementation are listed in this section.. The FPGA based design of the card allows to meet the requirements of many readout applications with dedicated firmware designs in the future.

6 modes of operation are implemented

- Ring buffer asynchronous
- Ring buffer synchronous
- Direct memory gate asynchronous
- Direct memory gate synchronous
- Direct memory stop
- Direct memory start

Note: the individual channels acquire data asynchronously in the two asynchronous modes of operation. This implies, that the user will want to use the address counter and/or the address threshold to decide on which channel(s) has/have to be read out.

2.3.1 Ring buffer asynchronous Mode

Trigger sources:
- internal Threshold Trigger (each channel individual)
- internal FIR Trigger Trigger (each channel individual)
- no external Trigger !
- no Trigger delay !

Used Parameters:
- programmable Ringbuffer PRE length (up to 16380 in steps of 2 samples)
- programmable Ringbuffer Sample length (up to 16384 in steps of 8 samples)

End of acquisition condition:
- Address Threshold

No explicit Multievent

2.3.2 Ring buffer synchronous Mode

Trigger source:
- internal Threshold Trigger (or of all channels)
- internal FIR Trigger (or of all channels)
- internal VME Key
- external Trigger (LEMO, LVDS)
- no Trigger delay !

End of acquisition condition:
- Single Event
- Multi Event (programmable nof_events)
- (Address Threshold !)
- Address Counter

Used Parameters:
- programmable Ringbuffer PRE length (up to 16380 in steps of 2 samples)
- programmable Ringbuffer Sample length (up to 16384 in steps of 8 samples)

2.3.3 Direct Memory Gate asynchronous Mode

Gate source:
- internal Threshold Gate (On,Off) (each channel individual)
- no Gate (Trigger) delay !

Used Parameters:
- programmable Ringbuffer PRE length (up to 16380 in steps of 2 samples)
- programmable Max Length
- programmable Gate Extend Length

End of acquisition condition:
- Address Threshold !
- Address Counter

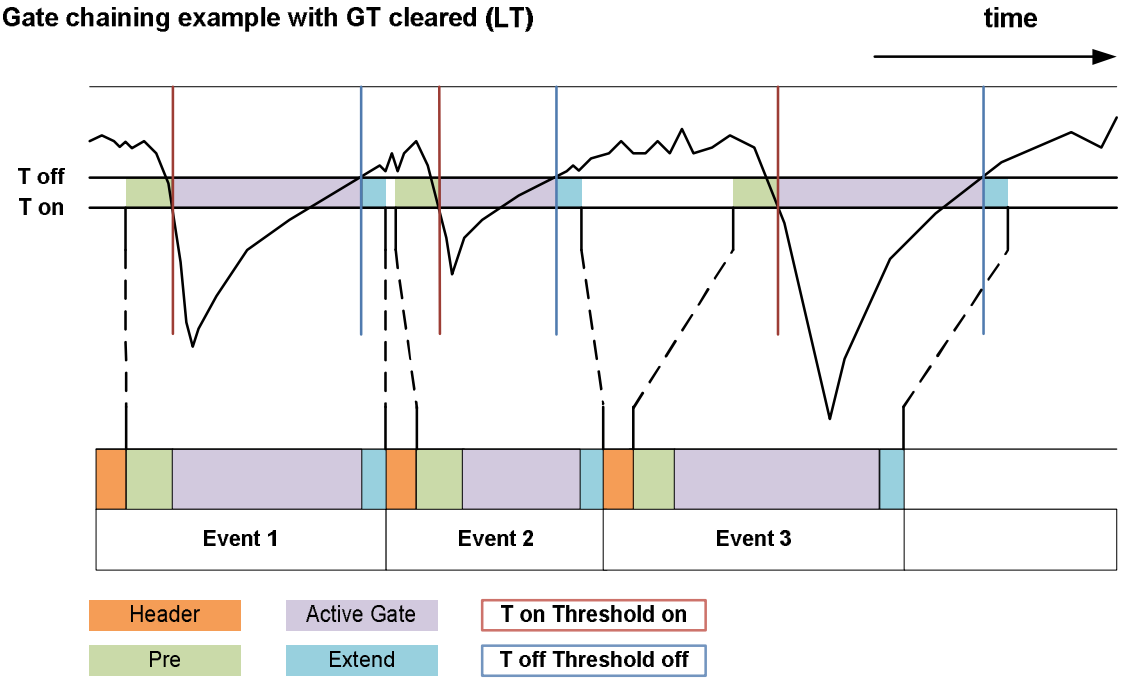
2.3.4 Direct Memory Gate synchronous Mode

Gate source:
- internal Threshold Gate (On,Off) (or of all channels)
- external Gate (Trigger) (LEMO, LVDS)
- no Gate (Trigger) delay !

Used Parameters:
- programmable Ringbuffer PRE length (up to 16380 in steps of 2 samples)
- programmable Max Length
- programmable Gate Extend Length

End of acquisition condition:
- Single Event
- Multi Event (programmable nof_events)
- Address Threshold

Find below a illustration for gate mode. Besides gate chaining you can see the effect of the pre length (pre) and gate extend length (extend) parameters. This mode of operation can be used for sparsified data acquisition also.



2.3.5 Direct Memory Stop Mode

Trigger source:
- internal Threshold Trigger (or of all channels)
- internal FIR Trigger (or of all channels)
- internal VME Key
- external Trigger (LEMO, LVDS)
- Trigger delay

End of acquisition condition:
- Single Event
- Multi Event (programmable nof_events)
- Address Threshold

Used Parameters:
- programmable Ringbuffer PRE length (up to 16380 in steps of 2 samples)

2.3.6 Direct Memory Start Mode

Trigger source:
- internal Threshold Trigger (or of all channels)
- internal FIR Trigger (or of all channels)
- internal VME Key
- external Trigger (LEMO, LVDS)
- Trigger delay

End of acquisition condition:
- Single Event
- Multi Event (programmable nof_events)
- Address Threshold

Used Parameters:
- Tbd.

2.4 Clock sources

The SIS3350 features following clock modes

- Internal fixed clock
- Internal frequency synthesizer
- External analog
- External LVDS

2.4.1 Internal clock

The internal clock is generated from an on board 100 MHz quartz or a frequency synthesizer.

Internal clock speeds
100 MHz fixed
Synthesizer 31.25 – 500 MHz

2.4.2 External clock (BNC analog or LVDS)

A analog (symmetric) external clock (ratio between 45:55 and 55:45) can be fed to the module through the BNC connector. The clock that is distributed to the digitizer chips is derived with the clock DAC and a comparator. The BNC clock output can be used to verify that the resulting meets symmetry requirements.
Alternatively a LVDS clock can be fed to the module over the HDMI connector (Pins 1-3).

Min. sym. clock	Max sym. clock
1 MHz	500 MHz

2.5 Trigger control (pre/post, start/stop and gate mode)

The SIS3350 features pre/post trigger capability as well as start/stop mode acquisition and a gate mode (in which start and stop are derived from the leading and trailing edge of a single control input signal).

2.6 Internal Trigger generation

The trigger output of the SIS3350 can be either used to interact with external trigger logic or to base start/stop on a threshold (i.e. one individual threshold per ADC channel) of the digitized data.
The user can select between triggering on the conditions above and below threshold
A FIR trigger mode is implemented as second trigger alternative..

2.7 VME Interrupts

Two registers, the Interrupt configuration and the Interrupt control register, are implemented for interrupt setup and control.
Four interrupt sources are implemented:

- Reached End Address Threshold (level sensitive)
- Reached End Address Threshold (edge sensitive)
- End of event
- End of last event in multi event mode

3 VME Addressing

As the SIS3350 VME FADC features memory options with up to 4 times 512 MSamples, A32 addressing was implemented as the only option for the time being. The module occupies an address space of 0x7FFFFFF Bytes, i.e. 128 MBytes are used by the module.
The base address is defined by the selected addressing mode, which is selected by jumper array JP80 and SW1 and SW2 (in non geographical mode).

The table below summarises the possible base address settings.

JP80 Setting			Bits					
A32	A16	GEO	31	30	29	28	27	
x			SW1				SW2=0...7 Bit 27=0	
x			SW1				SW2=8...F Bit 27=1	
	x		Not implemented in this design					
		x	Not implemented in this design					

Shorthand	Explanation
SW1/SW2	Setting of rotary switch SW1 or SW2 respective

Notes:

- This concept allows the use of the SIS3350 in standard VME as well as in VME64x environments, i.e. the user does not need to use a VME64x backplane.
- The factory default setting is EN_A32 closed, SW1=3, SW2=0 (i.e. the module will react to A32 addressing under address 0x30000000). With more than one unit shipped in one batch a set of addresses (like 0x10000000, 0x20000000, 0x30000000,...) may be used also.
- The A16 jumper allows for a future changed addressing scheme with different resource allocation

3.1 Address Map

The SIS3350 resources and their locations are listed in the table below.
Note: Write access to a key address (KA)with arbitrary data invokes the respective action

Offset	Size in Bytes	BLT	Access	Function
0x00000000	4	-	W/R	Control/Status Register (J-K register)
0x00000004	4	-	R only	Module Id. and Firmware Revision register
0x00000008	4	-	R/W	Interrupt configuration register
0x0000000C	4	-	R/W	Interrupt control register
0x00000010	4	-	R/W	Acquisition control/status register (J-K register)
0x00000014	4	-	R/W	Direct Memory Trigger Delay register
0x00000018	4	-	R/W	Direct Memory Start Mode Sample Length register
0x0000001C	4	-	R/W	Frequency Synthesizer register
0x00000020			R/W	MultiEvent Max Nof Events register
0x00000024			R only	MultiEvent Event Counter
0x00000028			R/W	Gate Synch Mode Event Length Limit register
0x0000002C			R/W	Gate Synch Mode Event Length Extend register
0x00000030	4	-	R/W	CBLT/Broadcast Setup register
0x00000034	4	-	R/W	ADC Memory Page register
0x00000038	4	-	R/W	Trigger Output Select register
0x00000050	4	-	R/W	Clock and Trigger Input DAC Control Status register (input threshold)
0x00000054	4	-	R/W	Clock and Trigger Input DAC Data register (input threshold)
0x00000060			R/W	XILINX JTAG_TEST/JTAG_DATA_IN
0x00000064			W only	XILINX JTAG_CONTROL
0x00000070			R only	Temperature Register
0x00000074			W only	ADC Serial Interface (SPI) register
0x00000400	4	-	KA	General Reset
0x00000410	4	-	KA	Arm Sampling Logic
0x00000414	4	-	KA	Disarm Sampling Logic
0x00000418	4	-	KA	Trigger
0x0000041C	4	-	KA	Timestamp Clear

Event information all ADC groups				
0x01000000	4	-	W	Event configuration register (all ADCs)
0x01000004	4		W	Direct Memory Stop Mode Sample Wrap Length register (all ADCs)
0x01000008	4	-	W	Sample Start address register (all ADCs)
0x01000020	4	-	W	Ringbuffer Sample Length (all ADCs)
0x01000024	4	-	W	Ringbuffer PRE Delay (all ADCs)
0x01000028	4	-	W	End Address Threshold (all ADCs)

Event information ADC group 1				
0x02000000	4	-	R/W	Event configuration register (ADC1, ADC2)
0x02000004	4		R/W	Direct Memory Stop Mode Sample Wrap Length register (ADC1, ADC2)
0x02000008	4	-	R/W	Sample Start address register (ADC1, ADC2)
0x02000010	4	-	R	Next Sample address register ADC1
0x02000014	4	-	R	Next Sample address register ADC2
0x02000020	4	-	R/W	Ringbuffer Sample Length (ADC1, ADC2)
0x02000024	4	-	R/W	Ringbuffer PRE Delay (ADC1, ADC2)
0x02000028	4	-	R/W	End Address Threshold (ADC1, ADC2)
0x02000030	4		R/W	ADC1 Trigger setup register
0x02000034	4		R/W	ADC1 Trigger Threshold register
0x02000038	4		R/W	ADC2 Trigger setup register
0x0200003C	4		R/W	ADC2 Trigger Threshold register
0x02000040	4		R/W	ADC1 Input Tap Delay register
0x02000044	4		R/W	ADC2 Input Tap Delay register
0x02000048	4		R/W	ADC1 VGA register
0x0200004C	4		R/W	ADC2 VGA register
0x02000050	4	-	R/W	ADC1/ADC2 DAC Control Status register
0x02000054	4	-	R/W	ADC1/ADC2 DAC Data register
0x02000070	4		R/W	ADC1 Sample Counter T1/T2 setup register
0x02000074	4		R/W	ADC1 Sample Counter T3/T4 setup register
0x02000078	4		R/W	ADC2 Sample Counter T1/T2 setup register
0x0200007C	4		R/W	ADC2 Sample Counter T3/T4 setup register

Event information ADC group 2				
0x03000000	4	-	R/W	Event configuration register (ADC3, ADC4)
0x03000004	4		R/W	Direct Memory Stop Mode Sample Wrap Length register (ADC3, ADC4)
0x03000008	4	-	R/W	Sample Start address register (ADC3, ADC4)
0x03000010	4	-	R	Next Sample address register ADC3
0x03000014	4	-	R	Next Sample address register ADC4
0x03000020	4	-	R/W	Ringbuffer Sample Length (ADC3, ADC4)
0x03000024	4	-	R/W	Ringbuffer PRE Delay (ADC3, ADC4)
0x03000028	4	-	R/W	End Address Threshold (ADC3, ADC4)
0x03000030	4		R/W	ADC3 Trigger setup register
0x03000034	4		R/W	ADC3 Trigger Threshold register
0x03000038	4		R/W	ADC4 Trigger setup register
0x0300003C	4		R/W	ADC4 Trigger Threshold register
0x03000040	4		R/W	ADC3 Input Tap Delay register
0x03000044	4		R/W	ADC4 Input Tap Delay register
0x03000048	4		R/W	ADC3 VGA register
0x0300004C	4		R/W	ADC4 VGA register
0x03000050	4	-	R/W	ADC3/ADC4 DAC Control Status register
0x03000054	4	-	R/W	ADC3/ADC4 DAC Data register
0x03000070	4		R/W	ADC3 Sample Counter T1/T2 setup register
0x03000074	4		R/W	ADC3 Sample Counter T3/T4 setup register
0x03000078	4		R/W	ADC4 Sample Counter T1/T2 setup register
0x0300007C	4		R/W	ADC4 Sample Counter T3/T4 setup register

ADC memory pages				
0x04000000	16 MByte	X	R	ADC 1 memory page
0x05000000	16 MByte	X	R	ADC 2 memory page
0x06000000	16 MByte	X	R	ADC 3 memory page
0x07000000	16 MByte	X	R	ADC 4 memory page

Note 2: MBLT64 read access is supported from memory (i.e. not from register space) only.

4 Register Description

The function of the individual registers is described in detail in this section.
The first line after the subsection header (in Courier font) like:

```
#define SIS3350_CONTROL_STATUS      0x0     /* read/write; D32 */
```

refers to the SIS3350.h header file.

4.1 Control/Status Register(0x0, write/read)

```
#define SIS3350_CONTROL_STATUS      0x0     /* read/write; D32 */
```

The control register is implemented as a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time. The only function at this point in time is user LED on/off.
On read access the same register represents the status register.

Bit	write Function	read Function
31	Clear reserved 15 (*)	0
30	Clear reserved 14 (*)	0
29	Clear reserved 13 (*)	0
28	Clear reserved 12 (*)	0
27	Clear reserved 11 (*)	0
26	Clear reserved 10 (*)	0
25	Clear reserved 9 (*)	0
24	Clear reserved 8 (*)	0
23	Clear reserved 7 (*)	0
22	Clear reserved 6 (*)	0
21	Clear reserved 5 (*)	0
20	Clear Invert Bit for external Lemo TRG IN (*)	0
19	Clear reserved 3 (*)	0
18	Clear reserved 2 (*)	0
17	Clear reserved 1 (*)	0
16	Switch off user LED (*)	0
15	Set reserved 15	Status reserved 15
14	Set reserved 14	Status reserved 14
13	Set reserved 13	Status reserved 13
12	Set reserved 12	Status reserved 12
11	Set reserved 11	Status reserved 11
10	Set reserved 10	Status reserved 10
9	Set reserved 9	Status reserved 9
8	Set reserved 8	Status reserved 8
7	Set reserved 7	Status reserved 7
6	Set reserved 6	Status reserved 6
5	Set reserved 5	Status reserved 4
4	Set Invert Bit for external Lemo TRG IN	Status Set Invert bit for external Lemo TRG IN
3	Set reserved 3	Status reserved 3
2	Set reserved 2	Status reserved 2
1	Set reserved 1	Status reserved 1
0	Switch on user LED	Status User LED (1=LED on, 0=LED off)

(*) denotes power up default setting

Invert bit for external Lemo TRG IN	function
0	Don't invert: Use for high active TTL signal (rising edge)
1	Invert: Use for low active TTL signals (falling edge) Use for NIM signals (leading edge)

4.2 Module Id. and Firmware Revision Register (0x4, read)

```
#define SIS3350_MODID              0x4      /* read only; D32 */
```

This register reflects the module identification of the SIS3350 and its minor and major firmware revision levels. The major revision level will be used to distinguish between substantial design differences and experiment specific designs, while the minor revision level will be used to mark user specific adaptations.

Bit	Function	Reading
31	Module Id. Bit 15	3
30	Module Id. Bit 14	
29	Module Id. Bit 13	
28	Module Id. Bit 12	
27	Module Id. Bit 11	3
26	Module Id. Bit 10	
25	Module Id. Bit 9	
24	Module Id. Bit 8	
23	Module Id. Bit 7	5
22	Module Id. Bit 6	
21	Module Id. Bit 5	
20	Module Id. Bit 4	
19	Module Id. Bit 3	0
18	Module Id. Bit 2	
17	Module Id. Bit 1	
16	Module Id. Bit 0	
15	Major Revision Bit 7	
14	Major Revision Bit 6	
13	Major Revision Bit 5	
12	Major Revision Bit 4	
11	Major Revision Bit 3	
10	Major Revision Bit 2	
9	Major Revision Bit 1	
8	Major Revision Bit 0	
7	Minor Revision Bit 7	
6	Minor Revision Bit 6	
5	Minor Revision Bit 5	
4	Minor Revision Bit 4	
3	Minor Revision Bit 3	
2	Minor Revision Bit 2	
1	Minor Revision Bit 1	
0	Minor Revision Bit 0	

4.2.1 Major revision numbers

Find below a table with major revision numbers used to date

Major revision number	Application/user
0x01	Generic designs

4.3 Interrupt configuration register (0x8)

```
#define SIS3350_IRQ_CONFIG      0x8      /* read/write; D32 */
```

This read/write register controls the VME interrupt behaviour of the SIS3350 ADC. Four interrupt sources are foreseen, for the time being three of them are associated with an interrupt condition, the fourth condition is reserved for future use.
The interrupter type is DO8 .

4.3.1 IRQ mode

In RORA (release on register access) mode the interrupt will be pending until the IRQ source is cleared by specific access to the corresponding disable VME IRQ source bit. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again.
In ROAK (release on acknowledge) mode , the interrupt condition will be cleared (and the IRQ source disabled) as soon as the interrupt is acknowledged by the CPU. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again.

Bit	Function	Default
31		0
...		0
16		0
15		0
14		0
13		0
12	RORA/ROAK Mode (0: RORA; 1: ROAK)	0
11	VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled)	0
10	VME IRQ Level Bit 2	0
9	VME IRQ Level Bit 1	0
8	VME IRQ Level Bit 0 (0 always)	0
7	IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle	0
6	IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle	0
5	IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle	0
4	IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle	0
3	IRQ Vector Bit 3; placed on D3 during VME IRQ ACK cycle	0
2	IRQ Vector Bit 2; placed on D2 during VME IRQ ACK cycle	0
1	IRQ Vector Bit 1; placed on D1 during VME IRQ ACK cycle	0
0	IRQ Vector Bit 0; placed on D0 during VME IRQ ACK cycle	0

The power up default value reads 0x 00000000

4.4 Interrupt control register (0xC)

```
#define SIS3350_IRQ_CONTROL          0xC      /* read/write; D32 */
```

This register controls the VME interrupt behaviour of the SIS3350 ADC. Eight interrupt sources are foreseen, for the time being two of them are associated with an interrupt condition, the others are reserved for future use.

Bit	Function (w)	(r)	Default
31	Update IRQ Pulse	Status IRQ source 7 (reserved)	0
30	unused	Status IRQ source 6 (reserved)	0
29	unused	Status IRQ source 5 (reserved)	0
28	unused	Status IRQ source 4 (reserved)	0
27	unused	Status IRQ source 3 (End Address Threshold Flag; level sensitive)	0
26	unused	Status IRQ source 2 (End Address Threshold Flag; edge sensitive)	0
25	unused	Status IRQ source 1 (End of last Event; edge sensitive)	0
24	unused	Status IRQ source 0 (End of Event; edge sensitive)	0
23	Disable/Clear IRQ source 7	Status flag source 7	0
22	Disable/Clear IRQ source 6	Status flag source 6	0
21	Disable/Clear IRQ source 5	Status flag source 5	0
20	Disable/Clear IRQ source 4	Status flag source 4	0
19	Disable/Clear IRQ source 3	Status flag source 3	0
18	Disable/Clear IRQ source 2	Status flag source 2	0
17	Disable/Clear IRQ source 1	Status flag source 1	0
16	Disable/Clear IRQ source 0	Status flag source 0	0
15	unused	Status VME IRQ	0
14	unused	Status internal IRQ	0
13	unused	0	0
12	unused	0	0
11	unused	0	0
10	unused	0	0
9	unused	0	0
8	unused	0	0
7	Enable IRQ source 7	Status enable source 7 (read as 1 if enabled, 0 if disabled)	0
6	Enable IRQ source 6	Status enable source 6 (read as 1 if enabled, 0 if disabled)	0
5	Enable IRQ source 5	Status enable source 5 (read as 1 if enabled, 0 if disabled)	0
4	Enable IRQ source 4	Status enable source 4 (read as 1 if enabled, 0 if disabled)	0
3	Enable IRQ source 3	Status enable source 3 (read as 1 if enabled, 0 if disabled)	0
2	Enable IRQ source 2	Status enable source 2 (read as 1 if enabled, 0 if disabled)	0
1	Enable IRQ source 1	Status enable source 1 (read as 1 if enabled, 0 if disabled)	0
0	Enable IRQ source 0	Status enable source 0 (read as 1 if enabled, 0 if disabled)	0

The power up default value reads 0x 00000000

IRQ source 3: reached Address Threshold (level sensitive)
IRQ source 2: reached Address Threshold (edge sensitive)
IRQ source 1: end of last event (disarm)
IRQ source 0: end of event

4.5 *Acquisition control register (0x10, read/write)*

```
#define SIS3350_ACQUISTION_CONTROL    0x10      /* read/write; D32 */
```

The acquisition control register is in charge of most of the settings related to the actual configuration of the digitization process.
Like the control register it is implemented in a J/K fashion.

Bit	Write Function	Read
31	Clear reserved 15 (*)	0
30	Clear reserved 14 (*)	0
29	Clear Clock Source Bit1	0
28	Clear Clock Source Bit0	0
27	Clear reserved 11 (*)	0
26	Clear reserved 10 (*)	0
25	Clear external LVDS TRG IN as Gate/Trigger (*)	0
24	Disable external Lemo TRG IN as Gate/Trigger (*)	0
23	Clear reserved 7 (*)	0
22	Disable internal trigger as Gate/Trigger (*)	0
21	Disable Multi Event mode (*)	0
20	Clear reserved 4 (*)	0
19	Clear reserved 3 (*)	Status of End Address Threshold Flag
18	Clear Operation Mode Bit 2 (*)	0
17	Clear Operation Mode Bit 1 (*)	ADC Sampling Busy
16	Clear Operation Mode Bit 0 (*)	ADC Sampling Logic Armed
15	Set reserved 15	Status reserved 15
14	Set reserved 14	Status reserved 14
13	Set clock source Bit 1	Status clock source Bit 1
12	Set clock source Bit 0	Status clock source Bit 0
11	Set reserved 11	Status reserved 11
10	Set reserved 10	Status reserved 10
9	Enable external LVDS TRG IN as Gate/Trigger	Status reserved 9
8	Enable external Lemo TRG IN as Gate/Trigger	Status reserved 8
7	Set reserved 7	Status reserved 7
6	Enable internal channel triggers as Gate/Trigger	Status enable internal channel triggers as Gate/Trigger
5	Enable Multi Event mode	Status Multi Event mode
4	Set reserved 4	
3	Set reserved 3	Status reserved 3
2	Set Mode of Operation Bit 2	Status Mode of Operation Bit 2
1	Set Mode of Operation Bit 1	Status Mode of Operation Bit 1
0	Set Mode of Operation Bit 0	Status Mode of Operation Bit 0

The power up default value reads 0x0

Operation Mode bit setting table:

Mode of Operation Bit 2	Mode of Operation Bit 1	Mode of Operation Bit 0	Mode of Operation
0	0	0	Ringbuffer Asynchronous Mode
0	0	1	Ringbuffer Synchronous Mode
0	1	0	Direct Memory Gate Asynchronous Mode
0	1	1	Direct Memory Gate Synchronous Mode
1	0	0	Direct Memory Trigger Stop Mode
1	0	1	Direct Memory Trigger Start Mode
1	1	0	reserved
1	1	1	reserved

Multi Event mode bit:

0 : Sampling Logic Armed state will be cleared at end of event

1 : Sampling Logic Armed state will be cleared at end of last event (defined with MultiEvent Max Nof Events register)

Clock source bit setting table:

Clock Source Bit1	Clock Source Bit0	Clock Source
0	0	Frequency Synthesizer (up to 500 MHz)
0	1	internal 100 MHz
1	0	external LVDS
1	1	external BNC

4.6 Direct Memory Trigger Delay register (0x14, read/write)

```
#define SIS3350_TRIGGER_DELAY     0x14      /* read/write; D32 */
```

The external trigger signals (LVDS, LEMO) and the internal trigger signal will be delayed by the value of the trigger delay register (in samples) in conjunction with the modes of operation "Direct Memory Trigger Stop Mode" and "Direct Memory Trigger Start Mode".
The maximum programmable delay is 64M samples (i.e. half memory depth).
(Pretrigger function!)

Bit	
31	unused, read as 0
...	
26	unused, read as 0
25	TRIGGER_DELAY_BIT25
..	
..	
1	TRIGGER_DELAY_BIT1
0	"0"

The power up default value is 0

4.7 Direct Memory Start Mode Sample Length register (0x18, read/write)

```
#define SIS3350_DIRECT_MEMORY_SAMPLE_LENGTH     0x18  /* read/write; D32 */
```

This register defines the number of samples in conjunction with the mode of operation "Direct Memory Trigger Start Mode".
The maximum programmable sample length is 128M - 8 .

Bit	
31	unused, read as 0
...	
27	unused, read as 0
26	SAMPLE_LENGTH_BIT26
..	
..	
3	SAMPLE_LENGTH_BIT3
2	"0"
1	"0"
0	"0"

The power up default value is 0

4.8 Frequency Synthesizer register (0x1C, read/write)

```
#define SIS3350_FREQUENCE_SYNTHESIZER      0x1C      /* read/write; D32 */
```

This register defines the sampling frequency of the SIS3350 in frequency synthesizer clock mode

The frequency is defined by the expression: Frequency = 25 MHz * M / 2^N

Bit	Function
31	unused, read as 0
...	
11	unused, read as 0
10	N1 (bit 1 of N Divider)
9	N0 (bit 0 of N Divider)
8	M8 (bit 8 of M)
..	
0	M0 (bit 0 of M)

The power up default value is 0x14 (20 -> 20 x 25MHz = 500MHz)

Note: The N Divider setting has to be chosen in accordance with the frequency limits specified in the table below

Valid N Divider frequency range setting table

Inputs		N Divider Value	Output Frequency (MHz)	
N1	N0		Minimum	Maximum
0	0	1	250	500
0	1	2	125	350
1	0	4	62.5	175
1	1		31.25	87.5

4.9 MultiEvent Max Nof Events register (0x20, read/write)

```
#define SIS3350_MULTIEVENT_MAX_NOF_EVENTS     0x20       /* read/write; D32
*/
```

The Sampling Logic will be disarmed in Multi Event mode as soon as the Event counter reaches the value of the MultiEvent_Max_Nof_Events register.

Bit	
31	unused, read as 0
...	
20	unused, read as 0
19	MAX NOF Events Bit19
..	
..	
0	MAX NOF Events Bit 0

The power up default value is 0

4.10 MultiEvent Event_Counter (0x24, read)

```
#define SIS3350_MULTIEVENT_EVENT_COUNTER        0x24      /* read; D32 */
```

This register holds the actual number of events in multi event mode.
The Event Counter is cleared when the Sampling Logic is armed and it is incremented with every start sampling.

Bit	
31	unused, read as 0
...	
20	unused, read as 0
19	Actual Event counter Bit 19
..	
..	
0	Actual Event counter Bit 0

The power up default value is 0

4.11 Gate Synch Mode Event Length Limit register (0x28, read/write)

```
#define SIS3350_GATE_SYNCH_LIMIT_LENGTH     0x28  /* read/write; D32 */
```

This register defines the maximum number of samples in conjunction with the mode of operation “Direct Memory Gate Synchronous Mode”.

The maximum programmable limit length is 64M - 8 .
The limit logic is disabled if the value is 0.

Bit	
31	unused, read as 0
...	
26	unused, read as 0
25	GATE_LIMIT_LENGTH_BIT25
..	
3	GATE_LIMIT_LENGTH _BIT3
2	“0”
1	“0”
0	“0”

The power up default value is 0

4.12 Gate Synch Mode Event Length Extend register (0x2C, read/write)

```
#define SIS3350_GATE_SYNCH_EXTEND_LENGTH     0x2C  /* read/write; D32 */
```

This register defines the additional sample length to the the gate length in conjunction with the mode of operation “Direct Memory Gate Synchronous Mode”.
In combination with the ringbuffer Delay register it is possible program the PreGate and PostGate length.

The maximum programmable extend length is 248 .

Bit	
31	unused, read as 0
...	
26	unused, read as 0
7	GATE_EXTEND_LENGTH_BIT7
..	
3	GATE_ EXTEND _LENGTH _BIT3
2	“0”
1	“0”
0	“0”

The power up default value is 0

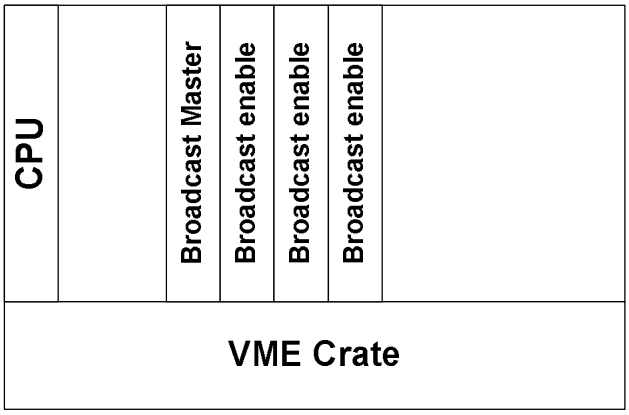
4.13 CBLT/Broadcast setup register

```
#define SIS3350_CBLT_BROADCAST_SETUP      0x30      /* read/write; D32 */
```

This read/write register defines, whether the SIS3350 will participate in a Broadcast. The configuration of this register and the registers of other participating modules is essential for proper Broadcast behaviour.

Bit	Function
31	CBLT/Broadcast address bit 31
30	CBLT/Broadcast address bit 30
29	CBLT/Broadcast address bit 29
28	CBLT/Broadcast address bit 28
27	CBLT/Broadcast address bit 27
26	CBLT/Broadcast address bit 26
25	CBLT/Broadcast address bit 25
24	CBLT/Broadcast address bit 24
23	reserved
22	reserved
21	reserved
20	reserved
19	reserved
18	reserved
17	reserved
16	reserved
15	reserved
14	reserved
13	reserved
12	reserved
11	reserved
10	0
9	0
8	0
7	0
6	0
5	Enable Broadcast Master
4	Enable Broadcast
3	0
2	reserved
1	reserved
0	reserved

Broadcast functionality is implemented for all Key address cycles.
Modules which are supposed to participate in a broadcast have to get the same broadcast address. The broadcast address is defined by the upper 8 bits of the broadcast setup register. One module has to be configured as broadcast master, the enable broadcast bit has to be set for the others as illustrated below.



Broadcast setup example (broadcast address 0x34000000):

Module	Broadcast Setup Register	Comment
1	0x34000020	Broadcast Master
2	0x34000010	Broadcast enable
3	0x34000010	Broadcast enable
4	0x34000010	Broadcast enable

All 4 modules will participate in a key reset (A32/D32 write) to address 0x34000400.

Note: Do not use a broadcast address that is an existing VME address of a VME card in the crate.

4.14 ADC Memory Page register

```
#define SIS3350_ADC_MEMORY_PAGE_REGISTER       0x34   /* read/write; D32 */
```

The SIS3350 default memory size per channel is 256 MByte (i.e. 128 MSample).

The VME address space window per ADC is limited to 16 MByte (8 MSample) however. The read/write ADC memory page register is used to select one of the 16 memory subdivisions (pages).

Bit	Function
31	Reserved
..	
..	
4	reserved
3	Page register bit 3
2	Page register bit 2
1	Page register bit 1
0	Page register bit 0

Example: readout routine for 128MSample readout
(see CVI/…./sis3350_configuration_readout_lib.c)

```
int sis3350_DMA_Read_MBLT64_ADC_DataBuffer(
        unsigned int module_address,               /* VME Base address */
        unsigned int adc_channel,                  /* 0 to 3 */
        unsigned int adc_buffer_sample_start_addr, /* 16-bit word start address */
        unsigned int adc_buffer_sample_length,     /* 16-bit word sample length */
        unsigned int*  dma_got_no_of_words,        /* read length of 32-bit words */
        unsigned int* uint_adc_buffer)             /* read buffer pointer*/
```

ADC Memory Sample Address table:

Samples / Bytes	Sample Address	Page register / VME Offset Address
0 / 0	0	0
1 / 2	1	0 / 0x2
..	..	..
8 MSample - 1 / 16 MByte -2	0x007F FFFF	0 / 0x00FF FFFE
8 MSample / 16 MByte	0x0080 0000	1 / 0x0
8 MSample + 8 / 16 MByte + 0x10	0x0080 0008	1 / 0x10
...		...
		1 / 0x00FF FFFE
16 MSample / 32 MByte	0x0100 0000	2 / 0x0
24 MSample / 48 MByte	0x0180 0000	3 / 0x0
32 MSample / 64 MByte	0x0200 0000	4 / 0x0
40 MSample / 80 MByte	0x0280 0000	5 / 0x0
48 MSample / 96 MByte	0x0300 0000	6 / 0x0
56 MSample / 112MByte	0x0380 0000	7 / 0x0
64 MSample / 128 MByte	0x0400 0000	8 / 0x0
72 MSample / 144 MByte	0x0480 0000	9 / 0x0
80 MSample / 160 MByte	0x0500 0000	10 / 0x0
88 MSample / 176 MByte	0x0580 0000	11 / 0x0
96 MSample / 192 MByte	0x0600 0000	12 / 0x0
104 MSample / 208 MByte	0x0680 0000	13 / 0x0
112 MSample / 224 MByte	0x0700 0000	14 / 0x0
120 MSample / 240 MByte	0x0780 0000	15 / 0x0
	..	..
128 MSample - 1 / 256 MByte - 2	0x07FF FFFF	15 / 0x00FF FFFE

4.15 Trigger Output Select register 0x38

```
#define SIS3350_LEMO_OUTPUT_SELECT_REGISTER     0x38  /* read/write; D32 */
```

This register is used to program on board trigger routing.

Bit	meaning	Function
31	reserved	
..	..	no
16	reserved	
15	ADC4 _Trigger	1: ADC4 _Trigger is ored to LVDS Trigger OUT (EXTERNAL_CONTROL2_LVDS_OUT)
14	ADC3 _Trigger	1: ADC3 _Trigger is ored to LVDS Trigger OUT
13	ADC2 _Trigger	1: ADC2 _Trigger is ored to LVDS Trigger OUT
12	ADC1 _Trigger	1: ADC1 _Trigger is ored to LVDS Trigger OUT
11	reserved	
10	reserved	
9	LVDS _Trigger_IN	1: LVDS_Trigger_IN is ored to LVDS Trigger OUT
8	LEMO_Trigger_IN	1: LEMO_Trigger_IN is ored to LVDS Trigger OUT
7	ADC4 _Trigger	1: ADC4 _Trigger is ored to LEMO OUT
6	ADC3 _Trigger	1: ADC3 _Trigger is ored to LEMO OUT
5	ADC2 _Trigger	1: ADC2 _Trigger is ored to LEMO OUT
4	ADC1 _Trigger	1: ADC1 _Trigger is ored to LEMO OUT
3	reserved	
2	reserved	
1	LVDS _Trigger_IN	1: LVDS_Trigger_IN is ored to LEMO OUT
0	LEMO_Trigger_IN	1: LEMO_Trigger_IN is ored to LEMO OUT

4.16 External Clock/Trigger Input DAC Control Registers

The external clock and trigger inputs of the SIS3350 accept analog input signals for maximum flexibility. The internal logic signals are generated on the card by comparing the input signal to a digital to analog converter (DAC) output value.

Example routine:
(see CVI/…./sis3350_configuration_readout_lib.c)

```
int sis3350_write_dac_offset(unsigned int module_dac_control_status_addr,
                             unsigned int dac_select_no,
                             unsigned int dac_value )       ;
```

4.16.1 Clock/Trigger DAC Control/Status register (0x50 read/write)

```
#define SIS3350_EXT_CLOCK_TRIGGER_DAC_CONTROL_STATUS 0x50      /* read/write; D32 */
```

Bit	Write Function	Read Function
31	None	0
..	..	..
..	..	..
16	None	0
15	None	DAC Read/Write/Clear Cycle BUSY
14	None	0
...		...
8	None	0
7	None	0
6	None	0
5	None	0
4	DAC Selection Bit	status of DAC selection Bit
3	..	..
2	none	0
1	DAC Command Bit 1	DAC Command Bit 1 Status
0	DAC Command Bit 0	DAC Command Bit 0 Status

DAC Selection Bit

Bit	Function
0	Clock Input DAC
1	Trigger Input DAC

DAC Command Bit

Bit 1	Bit 0	Function
0	0	No function
0	1	Load shift register of selected DAC
1	0	Load selected DAC
1	1	Clear all DACs

A “Clear DAC” command sets the value of all DACs to analog ground

4.16.2 Clock/Trigger DAC Data register (0x 54 read/write)

```
#define SIS3350_EXT_CLOCK_TRIGGER_DAC_DATA          0x54      /* read/write; D32 */
```

Bit	Write Function	Read Function
31	none	DAC Input Register Bit 15 (from DAC)
..	..	..
..	..	..
16	none	DAC Input Register Bit 0
15	DAC Output Register Bit 15	DAC Output Register Bit 15
..	..	0
..	..	0
0	DAC Output Register Bit 0	DAC Output Register Bit 0

The table below lists a set of DAC values and their corresponding threshold voltage.

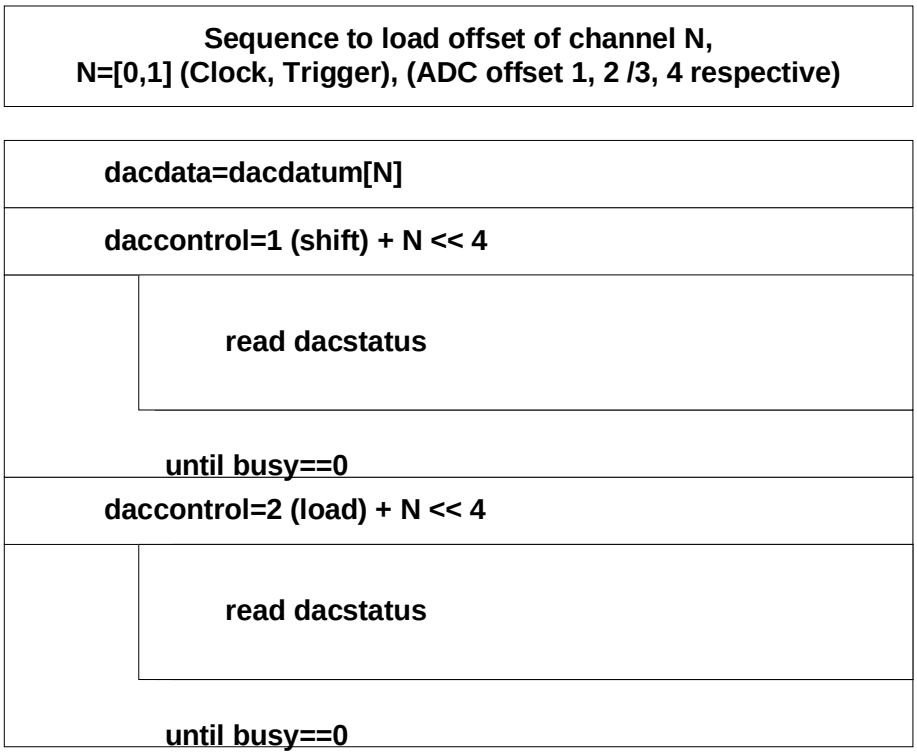
The table below lists a set of DAC values and their corresponding threshold voltage.
The maximum positive threshold value is +4,00V and the maximum negative threshold value is -2,75 V.

Clock and Trigger Input threshold setting table.

Value	Threshold Voltage
23700	- 2,75 V
30000	- 836 mV
31500	- 370 mV (NIM)
37500	+ 1,45 V (TTL)
40000	+ 2,2 V
46500	+ 4,00 V

4.16.3 DAC load sequence

The load sequence for the Analog Devices AD5570 DAC chip (please refer to the documentation of the chip for more details) is illustrated below. The sequence is identical for trigger/clock and ADC offset DACs (i.e. the same component is used in all places).



4.16.4 XILINX JTAG_TEST register

#define SIS3350_XILINX_JTAG_TEST 0x60 /* write only; D32 */

This register is used in the firmware upgrade process over VME only. A TCK is generated upon a write cycle to the register.

Bit	write Function
31	none
...	...
4	none
3	none
2	none
1	TMS
0	TDI

4.16.5 XILINX JTAG_DATA_IN register

#define SIS3350_XILINX_JTAG_DATA_IN 0x60 /* read only; D32 */

This register is used in the firmware upgrade process over VME only. It is at the same address as the JTAG_TEST register and is used in read access. It operates as a shift register for TDO. The contents of the register is shifted to the right by one bit with every positive edge of TCK and the status of TDO is transferred to Bit 30. Bit 31 reflects the current value of TDO during a read access.

4.16.6 XILINX JTAG_CONTROL register

#define SIS3350_XILINX_JTAG_CONTROL 0x64 /* write only; D32 */

This register is used in the firmware upgrade process over VME only.

Bit	Function	write
31	31	none
...	...	...
4	4	none
3	3	none
2	2	none
1	MUX_CMC_JTAG	0: tbd for VME/JTAG over CON100 1: tbd for VME/JTAG over CON100
0	JTAG_OUT_EN	0: Disable JTAG output 1: Enable JTAG output

4.17 Temperature register (0x70, read/only)

The SIS3350 is equipped with a serial 10-bit Analog Devices AD7314 temperature sensor. The temperature reading is stored in twos complement format.

Refer to the AD7314 data sheet for more detailed information.

```
#define SIS3350_INTERNAL_TEMPERATURE_REG          0x70      /* read; D32 */
```

Bit	
31	unused, read as 0
...	
...	
10	unused, read as 0
9	Data Bit 9 (MSB)
..	
1	Data Bit 1
0	Data Bit 0 (LSB)

The operating temperature ranges from -35 ^{O}C to +85 ^{O}C and is covered by the table below

Temperature	Data Bit 9 . . . Bit 0
–50 ^{O}C	11 0011 1000
–25 ^{O}C	11 1001 1100
–0.25 ^{O}C	11 1111 1111
0 ^{O}C	00 0000 0000
+0.25 ^{O}C	00 0000 0001
+10 ^{O}C	00 0010 1000
+25 ^{O}C	00 0110 0100
+50 ^{O}C	00 1100 1000
+75 ^{O}C	01 0010 1100
+100 ^{O}C	01 1001 0000

Note: The Celsius temperature reading is obtained by casting the read data to signed short and dividing the obtained value by 4.0 after float conversion.

4.18 ADC Serial Interface (SPI) register (0x74, read/write)

```
#define SIS3350_ADC_SERIAL_INTERFACE_REG      0x74   /* write; D32 */
```

Several parameters of the 12-bit 500 MS/s ADC AT85AS001 chip (like duty cycle stabilization e.g.) can be configured with the SPI (serial Peripheral Interface). The SPI register is the interface between the SIS3350 front end FPGAs and the ADC SPIs.
Please refer to the documentation of the AT85AS001 ADC chip for details.

Bit	
31	unused, read as 0
...	
...	
24	unused, read as 0
23	reserved
22	reserved
21	ADC Select Bit 1
20	ADC Select Bit 0
19	reserved
18	Address Bit 2
17	Address Bit 1
16	Address Bit 0
15	Data Bit 15 (MSB)
14	Data Bit 14
..	
1	Data Bit 1
0	Data Bit 0 (LSB)

The power up default value is 0x0

4.19 Key address general reset (0x400 write only)

```
#define SIS3350_KEY_RESET                0x400   /* write only; D32 */
```

A write with arbitrary data to this register (key address) resets the SIS3350 to it's power up state.

4.20 Key address VME arm sampling logic (0x410 write only)

```
#define SIS3350_KEY_ARM                  0x410   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will arm the sampling logic.

4.21 Key address VME disarm sampling logic (0x414 write only)

```
#define SIS3350_KEY_DISARM               0x414   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will disarm the sampling logic.

4.22 Key address VME Trigger

```
#define SIS3350_KEY_TRIGGER              0x418   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will generate an trigger.

4.23 Key address VME Timestamp Clear

```
#define SIS3350_KEY_TIMESTAMP_CLEAR      0x41C   /* write only; D32 */
```

A write with arbitrary data to this register (key address) will clear the 48-bit timestamp counter.

4.24 Event configuration registers(0x01000000, 0x02000000, 0x03000000 read/write)

```
#define SIS3350_EVENT_CONFIG_ALL_ADC     0x01000000  /* write only;D32 */

#define SIS3350_EVENT_CONFIG_ADC12       0x02000000  /* read/write;D32 */
#define SIS3350_EVENT_CONFIG_ADC34       0x03000000  /* read/write;D32 */
```

This register is implemented for each channel group and it has to be written with the same value, the best way is to make use of the address `SIS3350_EVENT_CONFIG_ALL_ADC` to write to the registers of all channel groups simultaneously.

Bit	Function
31	unused; read 0
…	…
25	unused; read 0
24	ADC group (0=group 0 [ADC 1 and 2], 1=group 1 [ADC 3 and 4])
23	unused; read 0
...	...
16	unused; read 0
15	ADC Memory Write via VME Test Enable
14	unused; read 0
13	unused; read 0
12	unused; read 0
11	unused; read 0
10	unused; read 0
9	unused; read 0
8	unused; read 0
7	unused; read 0
6	unused; read 0
5	unused; read 0
4	unused; read 0
3	unused; read 0
2	unused; read 0
1	unused; read 0
0	Extra Header Enable bit

4.25 Direct Memory Stop Mode Sample Wrap Length register

```
#define SIS3350_DIRECT_MEMORY_SAMPLE_WRAP_LENGTH_ALL_ADC   0x01000004
#define SIS3350_DIRECT_MEMORY_SAMPLE_WRAP_LENGTH_ADC12     0x02000004
#define SIS3350_DIRECT_MEMORY_SAMPLE_WRAP_LENGTH_ADC34     0x03000004
```

This register defines the number of samples of each event in conjunction with the mode of operation “Direct Memory Trigger Stop Mode”.
The maximum programmable sample wrap length is 128M - 8 .

Bit	
31	unused, read as 0
...	
25	unused, read as 0
26	Sample Wrap Length Register BIT26
..	
3	Sample Wrap Length Register BIT3
2	Unused
1	Unused
0	Unused

The power up default value is 0

4.26 Sample Start address register

```
#define SIS3350_SAMPLE_START_ADDRESS_ALL_ADC          0x01000008

#define SIS3350_SAMPLE_START_ADDRESS_ADC12            0x02000008
#define SIS3350_SAMPLE_START_ADDRESS_ADC34            0x03000008
```

These registers define the memory start address.
The value is given in samples (i.e. number of 16-bit words)

Only Sample Start addresses on a 8 16-bit (sample) boundary (i.e. 16 bytes) are valid.

Bit	
31	unused, read as 0
...	
25	unused, read as 0
26	Sample Start Address Register Bit 26
..	
3	Sample Start Address Register Bit 3
2	unused
1	unused
0	unused

The power up default value is 0

Explanation (sample start address)
The contents of the start sample register is assigned as memory data storage address with the arm command (key address arm sampling).

4.27 ADC Next Sample address register

```
#define SIS3350_ACTUAL_SAMPLE_ADDRESS_ADC1          0x02000010
#define SIS3350_ACTUAL_SAMPLE_ADDRESS_ADC2          0x02000014
#define SIS3350_ACTUAL_SAMPLE_ADDRESS_ADC3          0x03000010
#define SIS3350_ACTUAL_SAMPLE_ADDRESS_ADC4          0x03000014
```

These 4 read only registers hold the next sampling address for the given channel.

Bit	Function
31	unused, read as 0
...	
25	unused, read as 0
26	Sample Address Bit 26
..	
3	Sample Address Bit 3
2	0
1	0
0	0

The power up default value is 0

4.28 Ringbuffer Sample Length register

```
#define SIS3350_RINGBUFFER_SAMPLE_LENGTH_ALL_ADC     0x01000020
#define SIS3350_RINGBUFFER_SAMPLE_LENGTH_ADC12       0x02000020
#define SIS3350_RINGBUFFER_SAMPLE_LENGTH_ADC34       0x03000020
```

This register defines the number of samples in conjunction with the modes of operation "Ringbuffer Asynchronous Mode" and "Ringbuffer Synchronous Mode".
The maximum programmable sample length is 16376 (16K – 8) .

It defines also the additional sample length to the the gate length in conjunction with the mode of operation "Direct Memory Gate Asynchronous Mode".
In combination with the Ringbuffer Delay register it is possible program the PreGate and PostGate length.
The maximum programmable sample length is 65328 (64K – 8) .

Bit	
31	unused, read as 0
...	
16	unused, read as 0
15	RINGBUFFER_SAMPLE_LENGTH_BIT15*
14	RINGBUFFER_SAMPLE_LENGTH_BIT14*
13	RINGBUFFER_SAMPLE_LENGTH_BIT13
..	
3	RINGBUFFER_SAMPLE_LENGTH_BIT3
2	"0"
1	"0"
0	"0"

The power up default value is 0
* only in conjunction with the mode of operation "Direct Memory Gate Asynchronous Mode"

4.29 Ringbuffer Pre Delay register

```
#define SIS3350_RINGBUFFER_PRE_DELAY_ALL_ADC   0x01000024
#define SIS3350_RINGBUFFER_PRE_DELAY_ADC12     0x02000024
#define SIS3350_RINGBUFFER_PRE_DELAY_ADC34     0x03000024
```

This register defines the number of pre trigger delay samples in conjunction with all modes !
The maximum pretrigger delay is 16376 (16K – 8) .

Bit	
31	unused, read as 0
...	
14	unused, read as 0
13	RINGBUFFER_PRETRIGGER_DELAY_BIT13
..	
1	RINGBUFFER_PRETRIGGER_DELAY_BIT1
0	"0"

The power up default value is 0

4.30 End Address Threshold registers

```
#define SIS3350_END_ADDRESS_THRESHOLD_ALL_ADC        0x01000004

#define SIS3350_END_ADDRESS_THRESHOLD_ADC12          0x02000004
#define SIS3350_END_ADDRESS_THRESHOLD_ADC34          0x03000004
```

These registers define the "End Address Threshold" values for the ADC channel groups.

The value of the Actual Next Sample address counter will be compared with value of the End Address Threshold register.
The value is given in samples (i.e. number of 16-bit words)

Bit	
31	unused, read as 0
...	
24	unused, read as 0
23	Sample Start Address Register Bit 23
..	
2	Sample Start Address Register Bit 2
1	unused, read as 0
0	unused, read as 0

The power up default value is 0

4.31 Trigger setup register registers (0x02000030, 0x02000038, 0x03000030, 0x03000038)

```
#define SIS3350_TRIGGER_SETUP_ADC1          0x02000030
#define SIS3350_TRIGGER_SETUP_ADC2          0x02000038
#define SIS3350_TRIGGER_SETUP_ADC3          0x03000030
#define SIS3350_TRIGGER_SETUP_ADC4          0x03000038
```

These read/write registers hold the 8-bit wide trigger pulse length (in samples).
These read/write registers hold the Peaking and Gap Time of the trapezoidal FIR filter.
(Gap Time = SumG Time – Peaking Time)

Bit	Function	
31	Reserved	
..	..	
26	Enable Trigger	
25	GT trigger condition	
24	FIR Trigger Mode	
23	Puls Length bit 7	Trigger Pulse Length
22	Puls Length bit 6	
21	Puls Length bit 5	
20	Puls Length bit 4	
19	Puls Length bit 3	
18	Puls Length bit 2	
17	Puls Length bit 1	
16	Puls Length bit 0	
15	reserved	SumG time (only FIR trigger) (time between both sums)
14	reserved	
13	reserved	
12	SumG bit 4	
11	SumG bit 3	
10	SumG bit 2	
9	SumG bit 1	
8	SumG bit 0	
7	reserved	Peaking time P (only FIR trigger) $\sum_{i=x}^{x+P} Si$
6	reserved	
5	reserved	
4	P bit 4	
3	P bit 3	
2	P bit 2	
1	P bit 1	
0	P bit 0	

The power up default value reads 0x 00000000

Si: Sum of ADC input sample stream from x to x+P
P: Peaking time (number of values to sum)
SumG: SumGap time (distance in clock ticks of the two running sums)

The maximum SumG time: 16 (clocks)
The minimun SumG time: 1 (clocks)
Values > 16 will be set to 16
Value = 0 will be set to 1

The maximum Peaking time: 16 (clocks)
The minimun Peaking time: 1 (clocks)
Values > 16 will be set to 16
Value = 0 will be set to 1

4.32 Threshold registers (0x02000034, 0x0200003C, 0x03000034, 0x0300003C)

```
#define SIS3350_TRIGGER_THRESHOLD_ADC1              0x02000034
#define SIS3350_TRIGGER_THRESHOLD_ADC2              0x0200003C
#define SIS3350_TRIGGER_THRESHOLD_ADC3              0x03000034
#define SIS3350_TRIGGER_THRESHOLD_ADC4              0x0300003C
```

These read/write registers hold the threshold values for the 4 ADC channels.

4.32.1 Threshold Trigger

Bit	31-28	27-16	15-12	11-0
Function	None	none	None	Threshold value

default after Reset: 0x0

A Trigger Output pulse is generated on two conditions:

- GT is set (GT) in trigger setup register:
  the Trigger Out Pulse will be issued if the actual sampled ADC value **goes** above the threshold value

- GT is cleared (LT) in trigger setup register:
  the Trigger Out Pulse will be issued if the actual sampled ADC value **goes** below the threshold value.

GT: greater than
LT: lower than

4.32.2 Threshold FIR Trigger

Bit	31-28	27-16	15-0
Function	None	none	**Trapezoidal t**hreshold value

default after Reset: 0x0

The value of the Sum (trapezoidal value) depends on the peaking time P. Therefore the selection of the value of the Trapezoidal threshold depends on P also.

Trapezoidal value calculation:
Trapezoidal value = (SUM2 – SUM1)

Where

$$SUM1 = \sum_{i=x}^{x+P} Si$$

$$SUM2 = \sum_{j=x+sumG}^{x+P+sumG} Sj$$

The FIR Filter logic generates the Trapezoidal by subtraction of the two running sums. This implies, that the internal value of the trapezoid is on average 0.

A Trigger Output pulse is generated:
1GT is set (GT=1):

- GT is set (GT):
  the Trigger Out Pulse will be issued if the actual trapezoidal value **goes** above the programmable trapezoidal threshold value

- GT is cleared (LT):
  the Trigger Out Pulse will be issued if the actual trapezoidal value **goes** below the **negative** programmable trapezoidal threshold value

4.32.3 Threshold Gate

Bit	31-28	27-16	15-12	11-0
Function	None	Threshold value OFF	None	Threshold value ON

default after Reset: 0x0

A valid Gate Output is generated on two conditions:

- GT is set (GT) in trigger setup register:
  the Gate output signal will be set if the actual ADC value **goes** above the programmable threshold value ON **and** OFF and it is valid until the actual ADC value goes below the threshold value OFF .

- GT is cleared (LT) in trigger setup register:
  the Gate output signal will be set if the actual ADC value **goes** below the programmable threshold value ON **and** OFF and it is valid until the actual ADC value goes above the threshold value OFF .

4.33 ADC Input tap delay registers (0x2000030, 0x2000034, 0x3000030 0x3000034)

Internal use only.

```
#define SIS3350_ADC_INPUT_TAP_DELAY_ADC1     0x02000040
#define SIS3350_ADC_INPUT_TAP_DELAY_ADC2     0x02000044
#define SIS3350_ADC_INPUT_TAP_DELAY_ADC3     0x03000040
#define SIS3350_ADC_INPUT_TAP_DELAY_ADC4     0x03000044
```

4.34 VGA/gain registers (0x2000048, 0x200004C, 0x3000048 0x300004C)

These 4 read/write registers are used to set the gain of the four variable gain amplifiers (VGA).
The VGA setting is 7-bit wide.

```
#define SIS3350_ADC_VGA_ADC1                0x02000048
#define SIS3350_ADC_VGA_ADC2                0x0200004C
#define SIS3350_ADC_VGA_ADC3                0x03000048
#define SIS3350_ADC_VGA_ADC4                0x0300004C
```

Bit	Write Function	Read Function
31	None	0
..	..	..
..	..	..
7	None	0
6	VGA setting Bit 6	VGA setting Bit 6
…	…	…
1	VGA setting Bit 1	VGA setting Bit 1
0	VGA setting Bit 0	VGA setting Bit 0

Note: The resulting ADC input range depends on stuffing options and the offset DAC setting.

Find below a coarse range table with default stuffing .

VGA setting	Input range in V
10	7,992
11	7,414
12	6,884
13	6,554
14	6,113
15	6,068
22	4,000
31	2,960
47	1,940
63	1,430
79	1,160
95	0,950
111	0,816
127	0,720
162	0,376
178	0,260
194	0,200
210	0,160
226	0,130
242	0,110

Note: The maximum input voltage is 8V

4.35 ADC DAC Control Registers

This set of 4 registers is used to shift the input of the 4 ADC channels.

Example routine:
int sis3350_write_dac_offset(unsigned int module_dac_control_status_addr, unsigned int dac_select_no, unsigned int dac_value) ;

The sequence to load the DACs can be found in section 4.16.3

Note: The actual sample registers provide a good way to monitor offset shift during a DAC ramp

4.35.1 ADC DAC Control/Status registers (0x0x2000050, 0x0x3000050 read/write)

```
#define SIS3350_ADC12_DAC_CONTROL_STATUS  0x02000050  /* read/write; D32 */
#define SIS3350_ADC34_DAC_CONTROL_STATUS  0x03000050  /* read/write; D32 */
```

Bit	Write Function	Read Function
31	None	0
..	..	..
..	..	..
16	None	0
15	None	DAC Read/Write/Clear Cycle BUSY
14	None	0
...		...
8	None	0
7	None	0
6	None	0
5	None	0
4	DAC Selection Bit	status of DAC selection Bit
3	..	..
2	none	0
1	DAC Command Bit 1	DAC Command Bit 1 Status
0	DAC Command Bit 0	DAC Command Bit 0 Status

DAC Selection Bit

Bit	Function
0	ADC 1/3 respective
1	ADC 2/4 respective

4.35.2 ADC DAC Data registers (0x0x2000054, 0x0x3000054 read/write)

```
#define SIS3350_ADC12_DAC_DATA      0x02000054      /* read/write; D32 */
#define SIS3350_ADC34_DAC_DATA      0x03000054      /* read/write; D32 */
```

These registers are used to hold the data send the offset DACs of the 4 ADC channels. The DAC is selected via the DAC Selection Bit in the ADC DAC Control registers.

Bit	Write Function	Read Function
31	none	DAC Input Register Bit 15 (from DAC)
..	..	..
..	..	..
16	none	DAC Input Register Bit 0
15	DAC Output Register Bit 15	DAC Output Register Bit 15
..	..	0
..	..	0
0	DAC Output Register Bit 0	DAC Output Register Bit 0

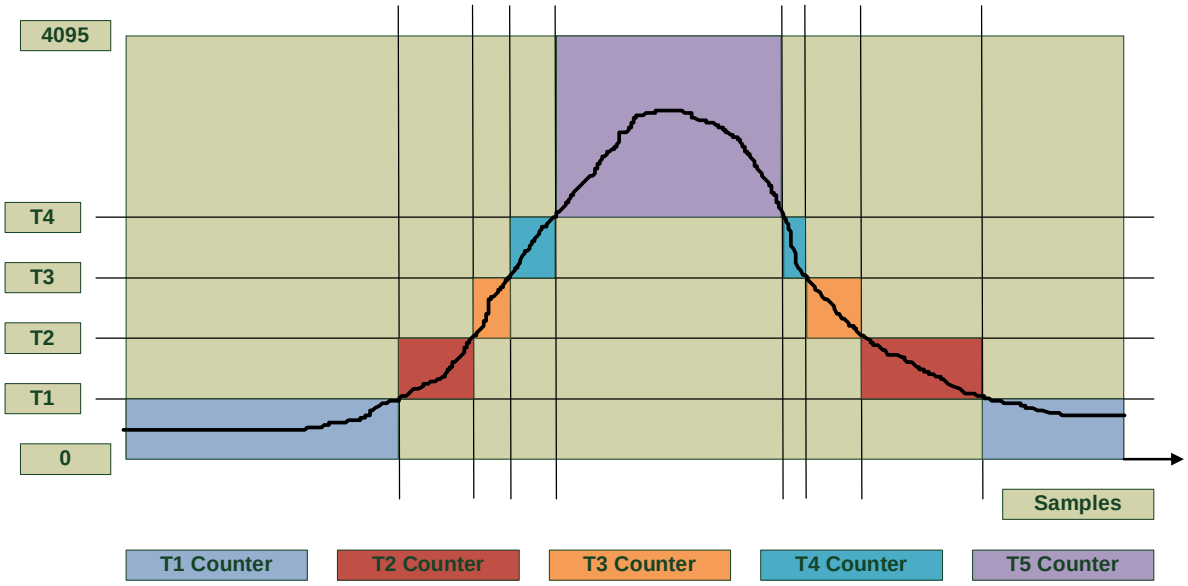
4.35.3 ADC Sample Counter TN setup register (0x2000070, 0x2000074, 0x20000078, 0x200007C, 0x3000070, 0x3000074, 0x30000078, 0x300007C read/write)

#define SIS3350_SAMPLE_COUNTER_THRESHOLD_T2T1_ADC1	0x02000070
#define SIS3350_SAMPLE_COUNTER_THRESHOLD_T4T3_ADC1	0x02000074
#define SIS3350_SAMPLE_COUNTER_THRESHOLD_T2T1_ADC2	0x02000078
#define SIS3350_SAMPLE_COUNTER_THRESHOLD_T4T3_ADC2	0x0200007C
#define SIS3350_SAMPLE_COUNTER_THRESHOLD_T2T1_ADC3	0x03000070
#define SIS3350_SAMPLE_COUNTER_THRESHOLD_T4T3_ADC3	0x03000074
#define SIS3350_SAMPLE_COUNTER_THRESHOLD_T2T1_ADC4	0x03000078
#define SIS3350_SAMPLE_COUNTER_THRESHOLD_T4T3_ADC4	0x0300007C

Five 12-bit counters named T1 to T5 counter are implemented for the individual ADC channel. The table below illustrates under which condition the 5 counters are incrementing their content with every sampling clock tick. The output of the counter values to the event data stream is activated by setting bit 0 (extra header enable bit) of the event configuration register.
The thresholds T1 through T4 are defined in the ADC sample counter Tn/Tm registers as shown in the table below..

Register	Bit [31:16]	Bit [15:0]
THRESHOLD_T2T1_ADCN	Threshold T2	Threshold T1
THRESHOLD_T4T3_ADCN	Threshold T4	Threshold T3

Counter	Count Condition
1	ADC value less than or equal T1
2	T1 < ADC value ≤ T2
3	T2 < ADC value ≤ T3
4	T3 < ADC value ≤ T4
5	T4 < ADC value ≤ 4095



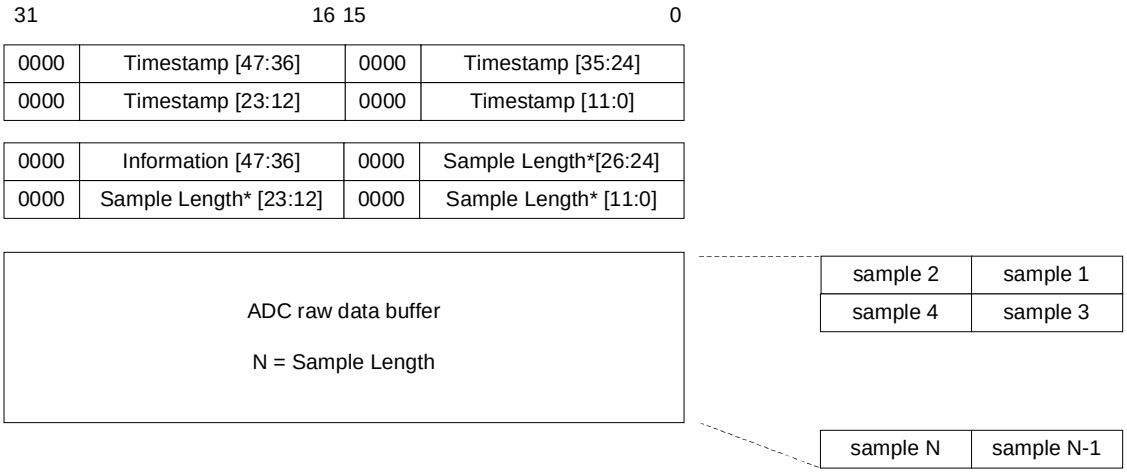
4.36 ADC memory

```
#define SIS3350_ADC1_OFFSET                    0x04000000
#define SIS3350_ADC2_OFFSET                    0x05000000
#define SIS3350_ADC3_OFFSET                    0x06000000
#define SIS3350_ADC4_OFFSET                    0x07000000
```

The 256 MByte ADC memory per channel can be address in pages of 16 MByte. The page is selected with the ADC Memory page register. One 32-bit word holds 2 ADC samples as shown in the table below.

4.36.1 Event Data format 1:

(used for all modes except “Direct Memory Trigger Stop Mode”)

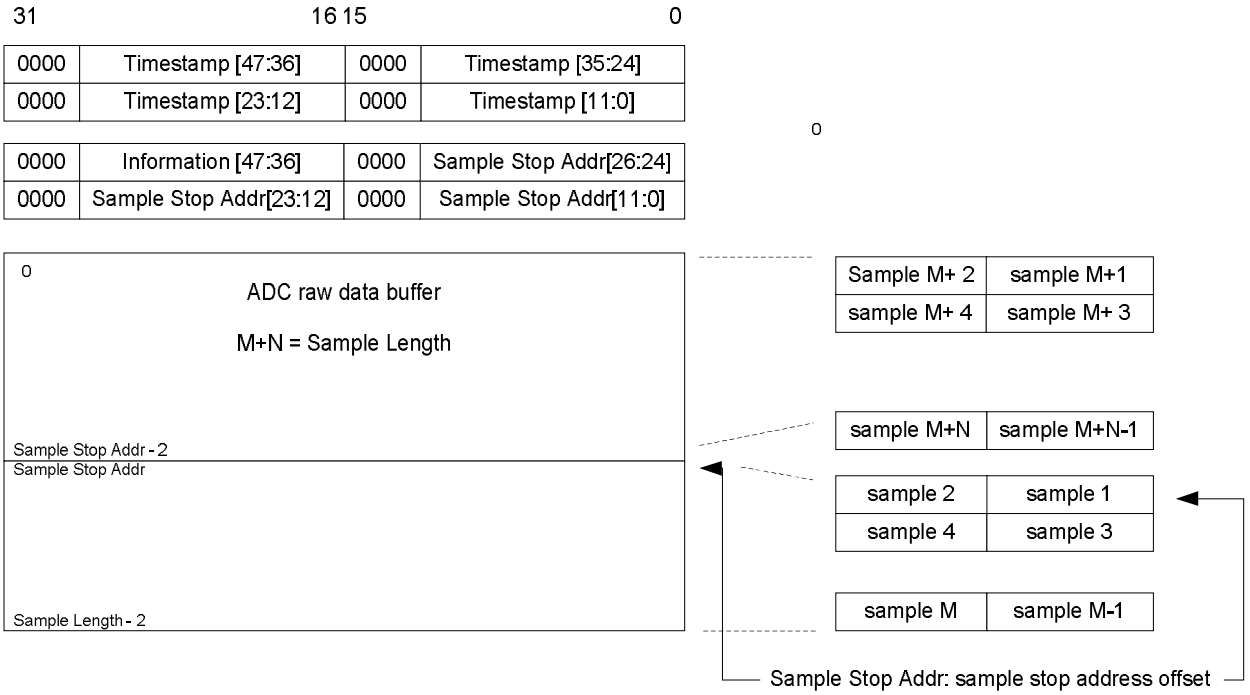


Note: The data representation of the ADC is shown below

Digitized Value	Analog input voltage
0xFFF	Highest input voltage (+2.5 V e.g.)
…	
0x000	Lowest input voltage (-2.5 V e.g.)

4.36.2 Event Data format 2:

(used in "Direct Memory Trigger Stop Mode" only)



Information bit table_

Bit	47	46	45-44	43-40	39-36
Function	Wrap	reserved	Stop delay counter	Trigger counter	Extra Header words

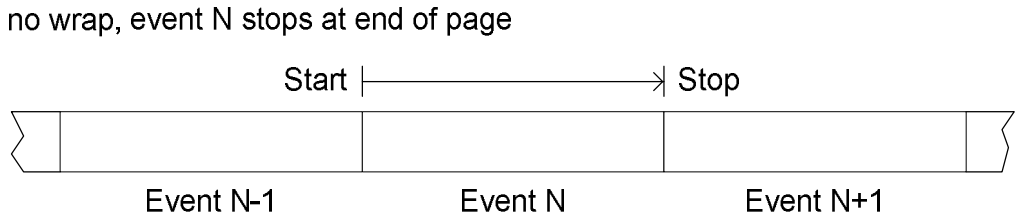
Trigger counter:
Counts the internal triggers.

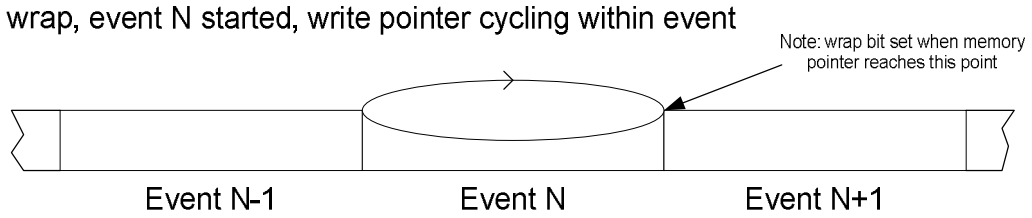
Stop delay counter:
The Sample Stop Address stops on an 8 sample boundary.
With the help of the Stop delay counter (multipy by 2) it is possible to rearange the trigger point.

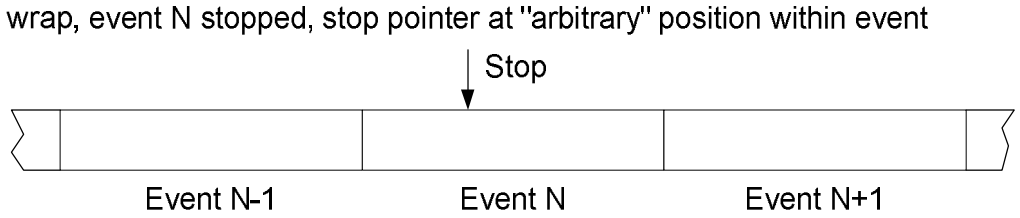
see CVI/…./sis3350_configuration_readout_lib.c:

```
int rearange_WrapRawDataOneChannelAllEvents(….)
```

Wrap (around) bit:
This bit is cleared at start of sampling and it is set when the number of samples reached the value of the Sample Wrap Length register.
See also “Direct Memory Stop Mode Sample Wrap Length register”.
Wrap = 0: data are only valid from offset 0 to (Sample_Stop_Addr – 2).







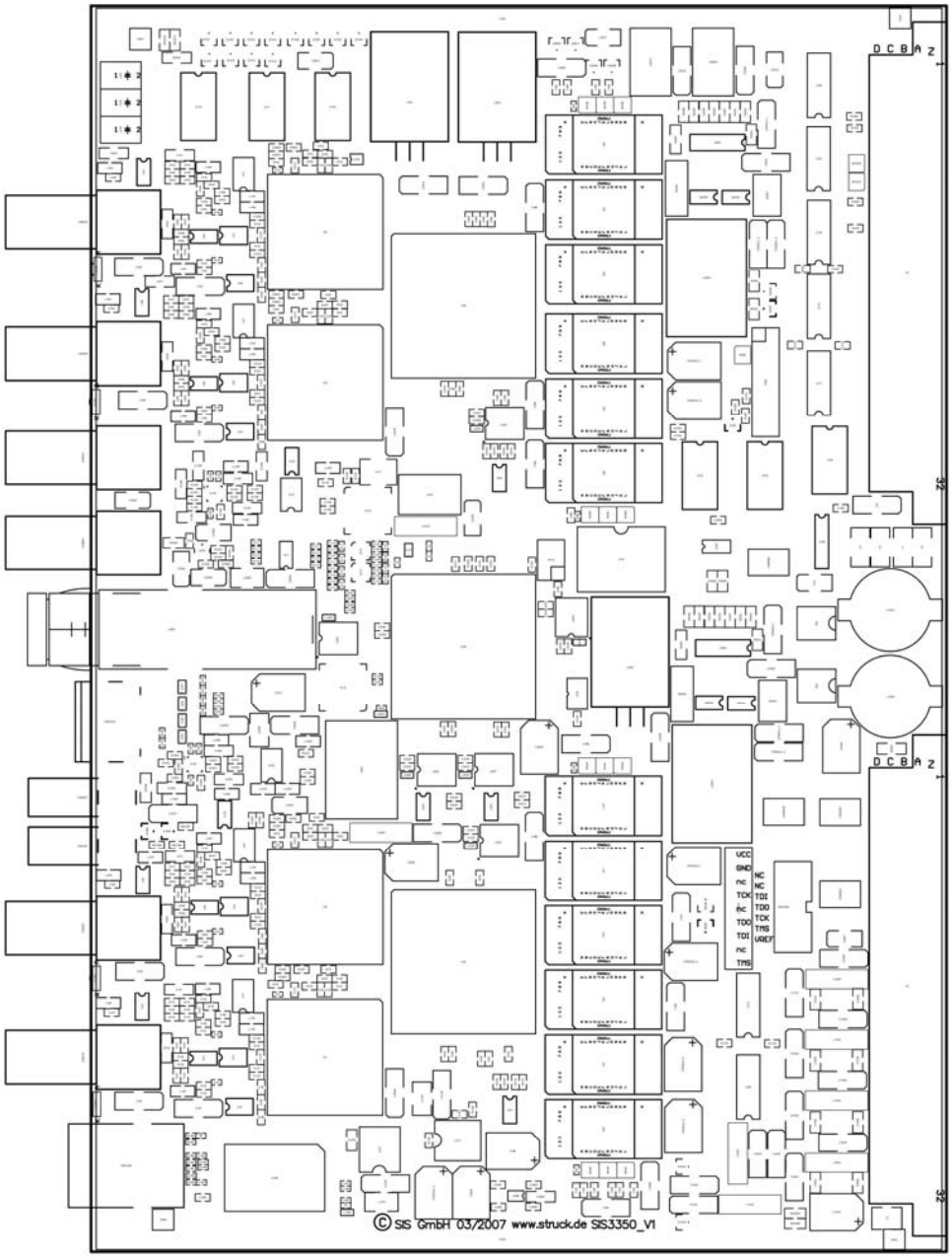
4.36.3 Extra Header

An extra header consisting of four 32-bit words is generated with bit 0 of the event configuration register set to 1. The extra header holds the 12-bit wide T1-T5 counter information as illustrated below.

31	16	15	0
0000	T1 counter [11:0]	0000	T2 Counter [11:0]
0000	T3 counter [11:0]	0000	T4 Counter [11:0]
0000	T5 counter [11:0]	0000	reserved
0000	reserved	0000	reserved

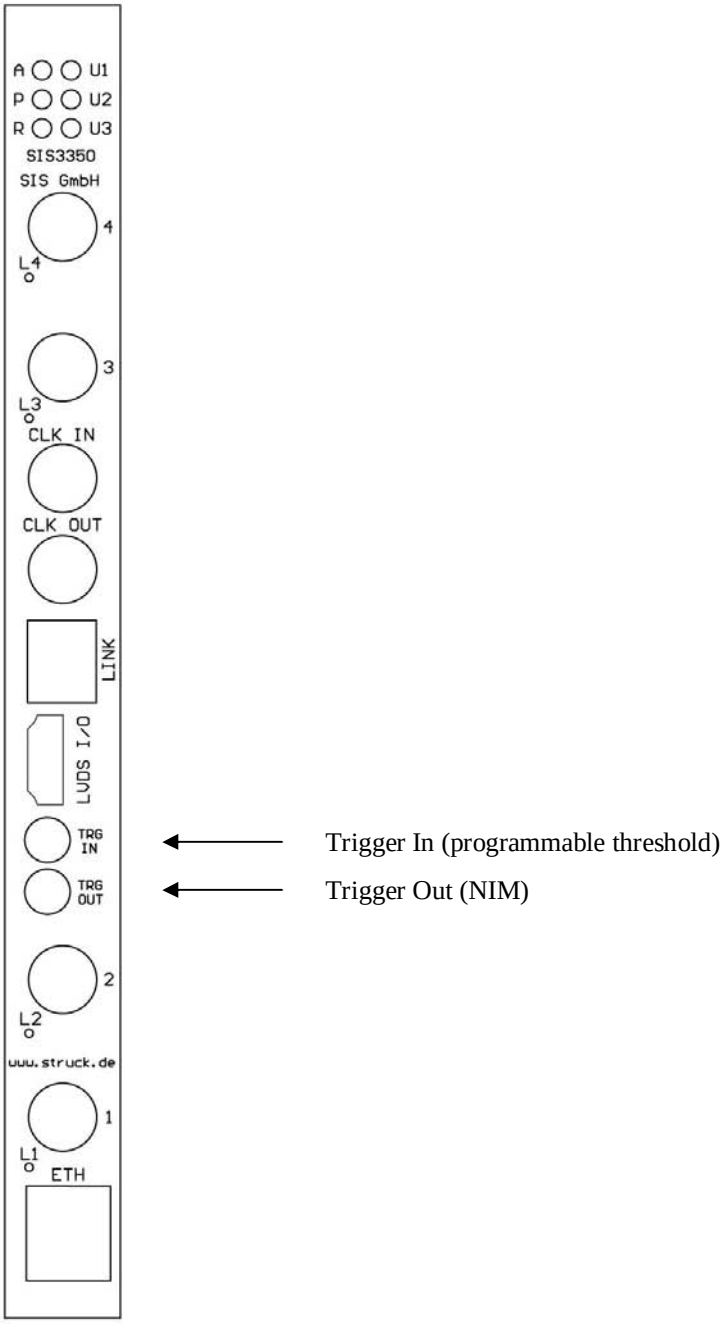
5 Board layout

A printout of the silk screen of the component side of the PCB is shown below.



6 Front panel

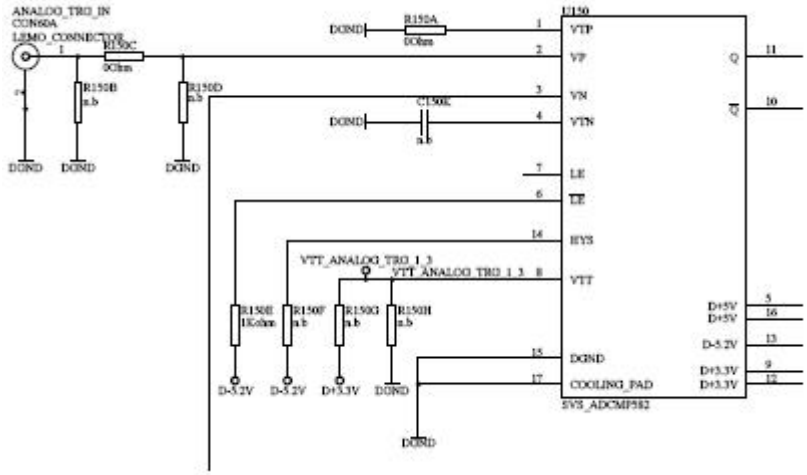
The SIS3350 is a single width (4TE) 6U VME module. A sketch of the SIS3350 front panel (without handles) is shown below.



6.1 Control In/Outputs

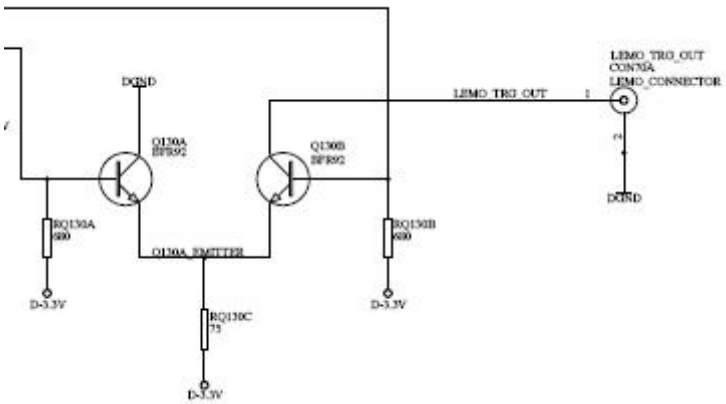
6.1.1 Trigger (Gate) Lemo input

The trigger (gate) input is a LEMO00 connector (CON60A) with programmable threshold level. The programmable threshold level range is from -2.75V to +4.0V and an input impedance of 50 Ohm.



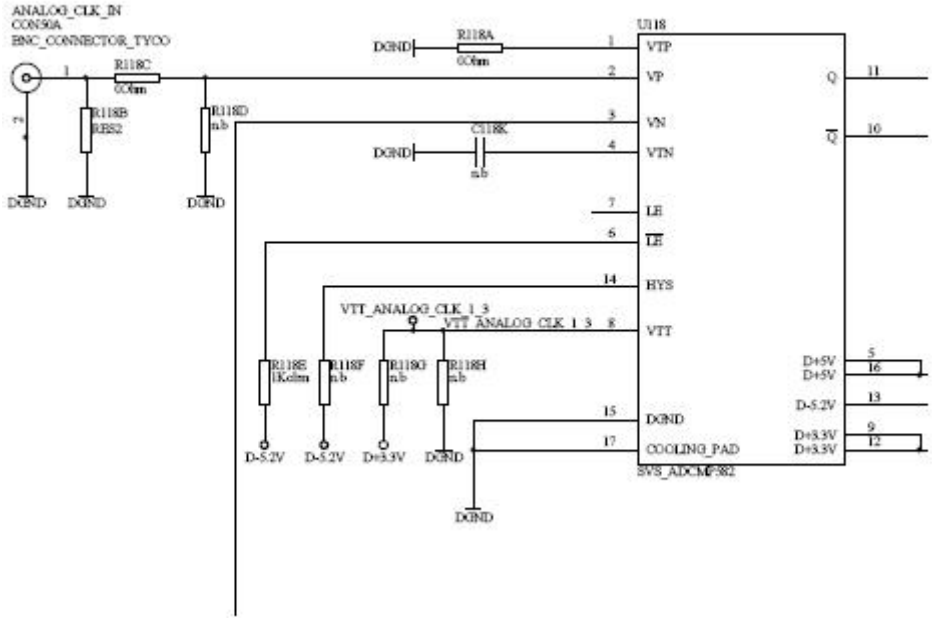
6.1.2 Trigger (Gate) Lemo output

The trigger (gate) output is a LEMO00 connector (CON70A) with NIM logic level.



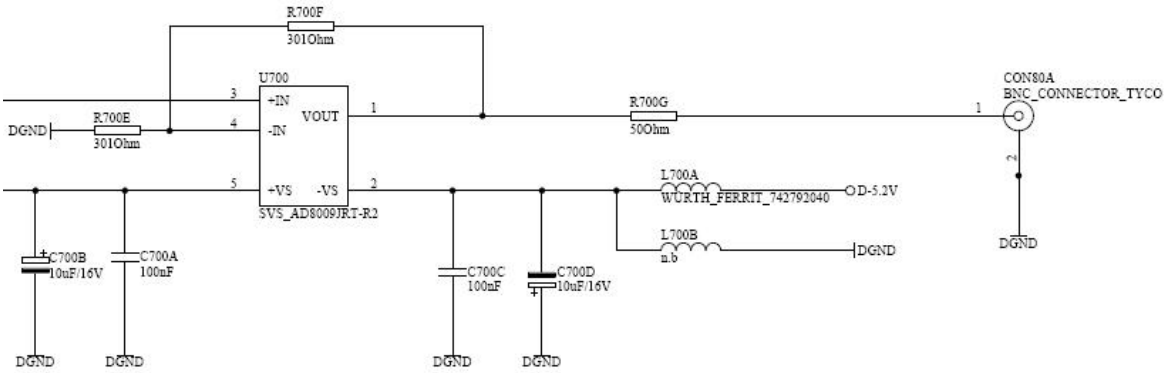
6.1.3 Clock BNC input

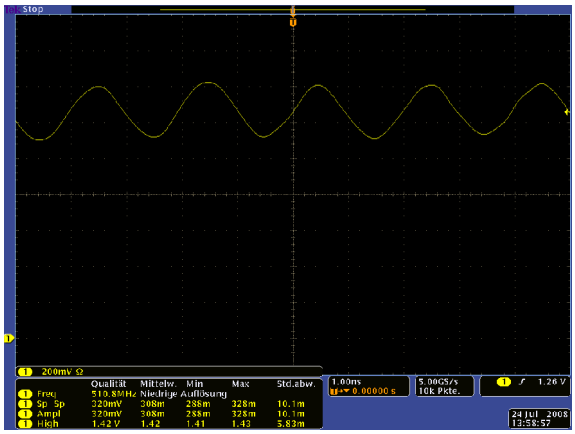
The clock input is a BNC connector (CON50A) with programmable threshold level.
The programmable threshold level range is from -2.75V to +4.0V and the input impedance is 50 Ohm.



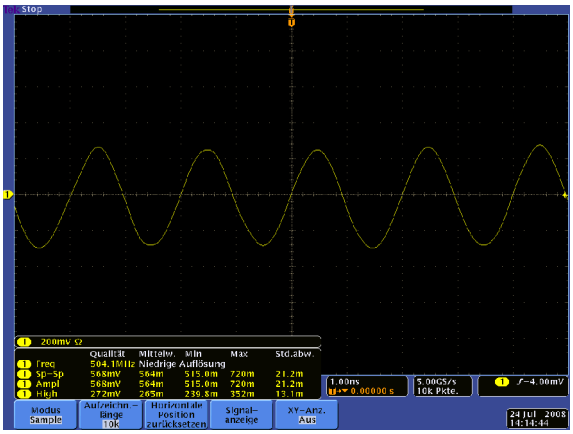
6.1.4 Clock BNC output

The clock output signal is available on a BNC connector for diagnosis purposes.
The output level in DC-coupling mode is 300mVpp and the offset is DC 1.1V into 50 Ohm termination.
The output level in AC-coupling mode is 560mVpp without an offset into 50 Ohm termination.





DC coupling mode
(R700G stuffed with 50 Ohm resistor)
DC coupling is factory default



AC coupling mode
(R700G stuffed with 100 nF capacitor)

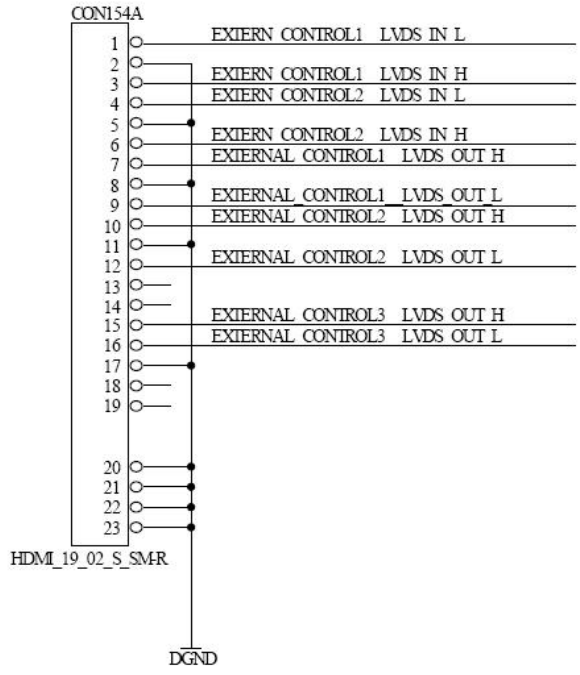
Note: the footprint of R700G is 0603

6.1.5 LVDS in/output

The control I/O section features one HDMI connector with LVDS levels.

PIN	Input Signal	Function
1	EXTERN_CONTROL1_LVDS_IN_L	Clock Input
2	DGND	
3	EXTERN_CONTROL1_LVDS_IN_H	
4	EXTERN_CONTROL2_LVDS_IN_L	Trigger (Gate) Input
5	DGND	
6	EXTERN_CONTROL2_LVDS_IN_H	

PIN	Output Signal	Function
7	EXTERNAL_CONTROL1_LVDS_OUT_H	Clock Output
8	DGND	
9	EXTERNAL_CONTROL1_LVDS_OUT_L	
10	EXTERNAL_CONTROL2_LVDS_OUT_H	Trigger (Gate) Output
11	DGND	
12	EXTERNAL_CONTROL2_LVDS_OUT_L	
13		
14		
15	EXTERNAL_CONTROL3_LVDS_OUT_H	BUSY Output
16	EXTERNAL_CONTROL3_LVDS_OUT_L	
17	DGND	
18	N/C	
..	..	
23	N/C	



6.2 LED's

The SIS3350 has 6 front panel LEDs to visualise part of the modules status. The access LED is a good way to check first time communication/addressing with the module.

Color	Designator	Function
Yellow	A	Access to SIS3350 VME slave port
Red	P	Power
Green	R	Ready, on board logic configured
Yellow	U1	Sample Logic armed
Red	U2	Sample Logic Busy
Green	U3	User, to be set/cleared under program control

The on duration of the access, sample logic armed and sample logic busy LEDs is stretched to guarantee visibility even under low rate conditions.

6.3 Channel LED's L1-L4

The 4 card edge surface mounted LEDs L1, ..., L4 can be seen through the corresponding holes in the front panel. They visualize the trigger status of the corresponding channel. The on duration is stretched for better visibility of short pulses.

6.4 PCB LEDs

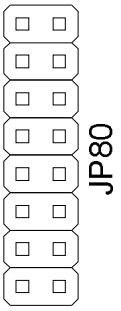
Surface mounted red LEDs are used to signal power status, trigger status and FPGA debug information (the use of the debug LEDs is firmware design dependent).
A table with the SMD LEDs is given below.

Designator	Function
D140A	Front panel trigger LED L1
D140B	Front panel trigger LED L2
D140C	Front panel trigger LED L3
D140D	Front panel trigger LED L4
D140E	VME_FPGA_DEBUG_INTERN_LED1
D140F	VME_FPGA_DEBUG_INTERN_LED2
D140G	VME_FPGA_DEBUG_INTERN_LED3
D140H	VME_FPGA_DEBUG_INTERN_LED4
D141A	FPGA1_DEBUG_INTERN_LED1
D141B	FPGA1_DEBUG_INTERN_LED2
D141C	FPGA1_DEBUG_INTERN_LED3
D141D	FPGA1_DEBUG_INTERN_LED4
D141E	FPGA2_DEBUG_INTERN_LED1
D141F	FPGA2_DEBUG_INTERN_LED2
D141G	FPGA2_DEBUG_INTERN_LED3
D141H	FPGA2_DEBUG_INTERN_LED4
D300A	Power D+2.5V
D301A	Power D+3.3V
D309A	Power_Fault_Sequencer
D309B	Power_Sequence_OK
D400A	Power A+12V
D410A	Power A-12V
D500B	Power D+1,8V
D600B	Power D+1,2V

7 Jumpers/Configuration

7.1 JP80 VME addressing mode/reset behaviour

This 8 position jumper array is used to select the addressing mode and the reset behaviour of the SIS3350.



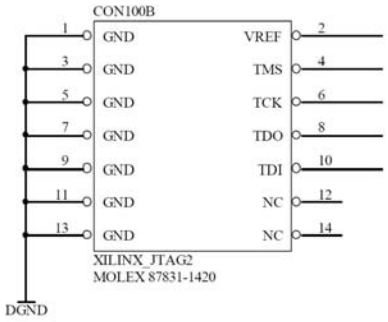
Pos	Function	Factory default
1	A32	closed
2	A16 (not supported)	open
3	GEO (not supported)	open
4	VIPA (not supported)	open
5	connect VME SYSRESET IN to FPGA reset	closed
6	unused	open
7	unused	open
8	connect VME SYSRESET to board reset	closed

The enable watchdog jumper has to be removed during (initial) JTAG firmware load.

NOTE: avoid a power up deadlock situation by not setting Pos. 5 and 8 at the same time

7.2 CON100B JTAG

The SIS3350 on board logic can load its firmware from a serial PROMs , via the JTAG port on connector CON100B or over VME. A list of firmware designs can be found under http://www.struck.de/sis3350firm.htm.
Hardware like the HW-USB-II-G-JTAG in connection with the appropriate software will be required for in field JTAG firmware upgrades. The JTAG chain configuration is selected with jumper JP101, Xilinx JTAG control register is used to select VME or CON100B as JTAG source.
CON100B is a 2mm (i.e. metric) 14 pin header that allows you to reprogram the firmware of the SIS3350 with a JTAG programmer. The pinout is shown in the schematic below. It is compatible with the cable that comes with the XILINX HW-USB platform cable.



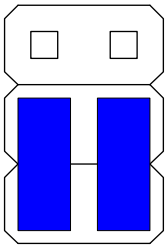
Note: The SIS3350 has to be powered for reprogramming over JTAG.

7.3 JP101 JTAG chain

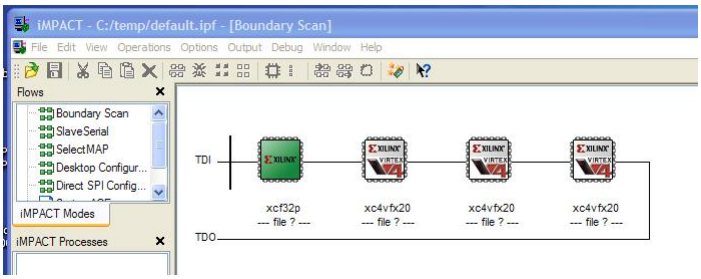
The JTAG chain on the SIS3350 can be configured to comprise the serial PROM only (short JTAG chain) or to comprise the serial PROM and the 3 Virtex FPGAs (long chain). The configuration is selected with the 6-pin array JP101 as sketched below:

Long Chain (1-3 and 2-4 closed):

JP101

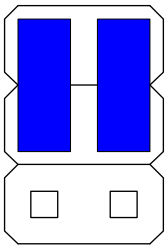


In the Impact software you will see:

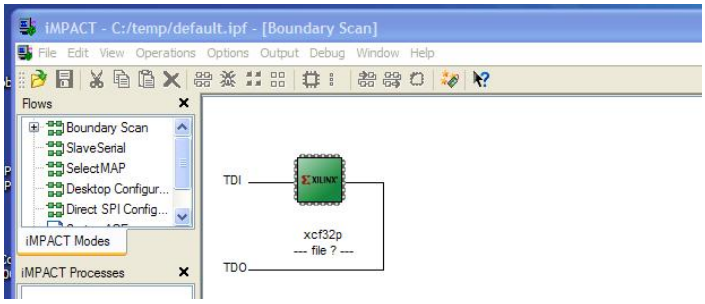


Short Chain (3-5 and 4-6 closed, factory default):

JP101



In the Impact software you will see:



7.4 SW1 and SW2, VME base address

These 2 rotary switches are used to define 2 nibbles of the VME base address in non geographical addressing (refer to section base address also).

Switch	Function
SW1	ADR_LO
SW2	ADR_UP

7.5 JTAG source

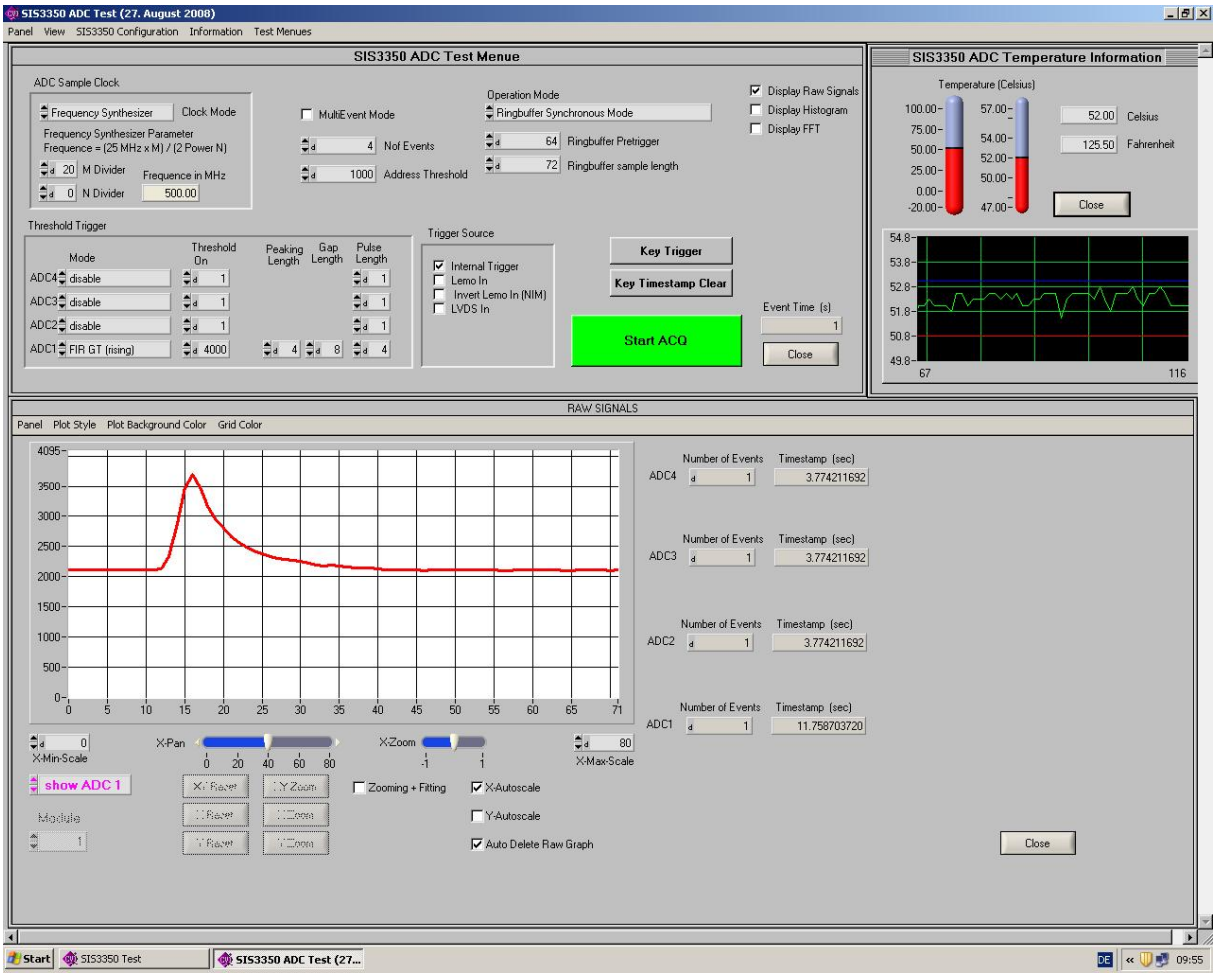
The JTAG chain can be connected to VME or to the JTAG connector CON100B
The source is programmable via the XILINX JTAG Control register

8 Getting started

The directory SIS3350\software of the Struck Innovative Systeme DVD holds example code for VisualC++ and National Instruments Labwindows CVI. The source code can be used as a base for ports to other environments.
The SIS3350.h header file can be found in the directory SIS3350\software.
The routine `ConfigurationSetup_SIS3350_Adc(void)` in the file `SIS3350_adc_test1.c` (CVI directory) can be used as starting point for a setup routine for the SIS3350.

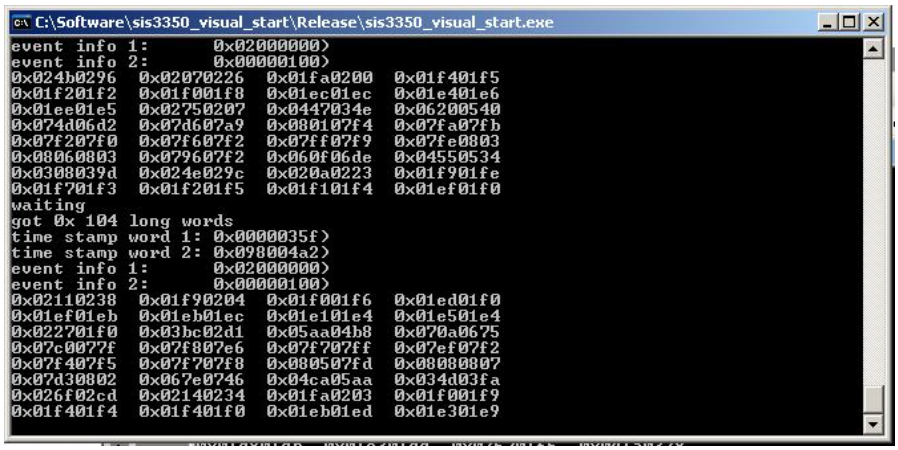
8.1 SIS3350 base program

The runtime version of the SIS3350 base program in combination with a SIS3150 USB to VME interface provides access to all implemented SIS3350 features without the need for coding in the first step under Windows. Feel free to inquire about the possibility for a loaner in case you are working with another VME master.
An example screen shot of the SIS3350 base program (a signal acquired in ring buffer synchronous mode of operation).



8.2 SIS3350 visual start

A minimum VisualC++ program to see first data can be found in the directory software\visual\application
The board is set up without VGA and DAC setting, what results in an input range of about -2.5, …,+2.5 V and operated in VME triggered mode in the example. Typical screen output is shown below.



9 Appendix

9.1 Power consumption

The SIS3350 uses standard VME voltages only.

Voltage	Current
+ 5V	9A
+12 V	100 mA
- 12 V	400 mA

9.2 Operating conditions

9.2.1 Cooling

Although the SIS3350 is mainly a 2.5 and 3.3 V low power design, substantial power is consumed by the Analog to Digital converter chips and linear regulators however. Hence forced air flow is required for the operation of the board. The board may be operated in a non condensing environment at an ambient temperature between 10 and 25 Celsius. A power up warm up time of some 10 minutes is recommended to ensure equilibrium on board temperature conditions.

9.2.2 Hot swap/live insertion

Please note, that the VME standard does not support hot swap by default. The SIS3350 is configured for hot swap in conjunction with a VME64x backplane. In non VME64x backplane environments the crate has to be powered down for module insertion and removal.

9.3 Connector types

The table below lists the connectors used on the SIS3350.

Connector/Purpose	Part number	Manufacturer
Analog in 1-4	Tyco 5413631-1	TYCO
Ethernet	HFJ11-1G01E-L12RL	HALO
External Clock	Tyco 5413631-1	TYCO
JTAG	87831-1420	Molex
LVDS bus	HDMI-19-02-S-SM-R	SAMTEC
Optical Link	FTLF8524E2KNL	FINISAR
Trigger input	EPL.00.250.NTN	LEMO
Trigger output	EPL.00.250.NTN	LEMO
VME (P1/P2) 160 pin zabcd	02 01 160 2101	HARTING

9.4 P2 row A/C pin assignments

The P2 connector of the SIS3350 has several connections on rows A and C for the F1002 compatible use at the DESY H1 FNC subdetector. This implies, that the module can not be operated in a VME slot with a special A/C backplane, like VSB e.g.. The pin assignments of P2 rows A/C of the SIS3350 is shown below:

P2A	Function	P2C	Function
1	not connected	1	not connected
2	not connected	2	not connected
3	not connected	3	not connected
4	not connected	4	not connected
5	not connected	5	not connected
6	DGND	6	DGND
7	P2_CLOCK_H	7	P2_CLOCK_L
8	DGND	8	DGND
9	P2_START_H	9	P2_START_L
10	P2_STOP_H	10	P2_STOP_L
11	P2_TEST_H	11	P2_TEST_L
12	DGND	12	DGND
13	DGND	13	DGND
14	not connected	14	not connected
15	not connected	15	not connected
16	not connected	16	not connected
...	...	17	...
31	not connected	18	not connected

Note: The P2 ECL signals are bussed and terminated on the backplane of F1002 crates. The user has to insure proper termination if a cable backplane or add on backplane is used.

9.5 Row d and z Pin Assignments

The SIS3350 is prepared for the use with VME64x and VME64xP backplanes. Foreseen features include geographical addressing and live insertion (hot swap). The prepared pins on the d and z rows of the P1 and P2 connectors are listed below.

Position	P1/J1		P2/J2	
	Row z	Row d	Row z	Row d
1		VPC (1)		
2	GND	GND (1)	GND	
3				
4	GND		GND	
5				
6	GND		GND	
7				
8	GND		GND	
9		GAP*		
10	GND	GA0*	GND	
11	RESP*	GA1*		
12	GND		GND	
13		GA2*		
14	GND		GND	
15		GA3*		
16	GND		GND	
17		GA4*		
18	GND		GND	
19				
20	GND		GND	
21				
22	GND		GND	
23				
24	GND		GND	
25				
26	GND		GND	
27				
28	GND		GND	
29				
30	GND		GND	
31		GND (1)		GND (1)
32	GND	VPC (1)	GND	VPC (1)

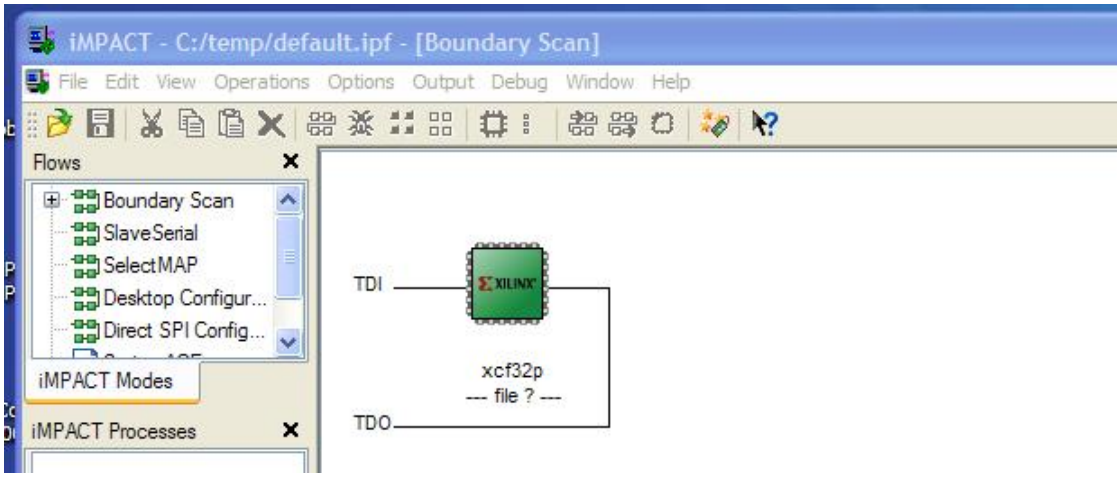
Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

9.6 Firmware upgrade

The firmware of the SIS3350 can be upgraded over JTAG. The upgrade options are VME (on units that have intact firmware) and the JTAG connector CON100. The VME upgrade option is not tested for the current firmware release yet.

9.6.1 Upgrade over CON100

The firmware can be upgraded with the Xilinx Impact software, which is part of the Webpack that can be downloaded from the Xilinx web page for free.
A Xilinx JTAG parallel cable or USB (Xilinx part number HW-USB) cable can be used to roll in the firmware.
Configure the SIS3350 for short JTAG chain (refer to section 7.3 JP101). CON 100 is JTAG source by default (unless programmed for VME with the Xilinx JTAG control register.
With your hard- and software properly set up you should see a screen as illustrated below after executing the initialize chain command.



Load the mcs file to the serial PROM (shown as xcf32p).

9.6.2 Upgrade over VME

Not supported with current SIS3350 firmware yet (i.e. JTAG source hard coded to CON100)

10 Index