TE2440-II Users Manual

Part 1 - Introduction

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TE2440-II is an updated version of TE2440, a Witech ARM9 embedded SBC (Single Board Computer) based on the Samsung S3C2440A with full featured MMU (Memory Management Unit). TE2440-II SBC consists of a 6-layer core board and a 4-layer base board, such structure not only makes the TE2440-II more flexible but also brings the SBC much more stable and reliable performance. Together with the TE2440-II we provide BSPs (Board Support Packages) for Embedded Linux and WindowsCE including basic drivers for all the components on the board and illustrating programs, which we believe can help the users in understanding the ARM architecture and shortening their development circle.

Here are some dos and don'ts for using the TE2440-II:

1. After opening the TE2440-II package, please check and make sure that the following components are all enclosed:
   - 1 × TE2440-II board
   - 1 × serial port cable
   - 1 × USB cable
   - 1 × Ethernet cable
   - 1 × JTAG wiggler with JTAG cable
   - 1 × 5V power supply
   - 1 × DVD
2. After purchasing the TE2440-II, please do inform us with your purchase information, including your name, registered email address, purchase date, invoice number and board ID to validate your membership for downloading the latest data from our website.
3. When using the SBC for the first time, please do read and follow the user manual to prevent unnecessary troubles and damages.
4. Every time before powering on the SBC, please touch anyone of the metallic interface with your fingers to unload the Electrostatic. Do not touch the chips with your fingers!
5. Before physically operating the SBC, please switch the power off. Hot plugging is **not** supported except on the USB and Ethernet interfaces.
6. We provide for the TE2440-II 12 weeks' guarantee (in the precondition of non-artificial damage) and 24 weeks technical support.

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Chapter One: Hardware Introduction

The TE2440-II Single Board Computer consists of a 6-layer core board and a 4-layer base board. Layout and wiring on the TE2440-II is meticulously designed by professionals to ensure stable performance, which, together with a variety of interfaces, connectors, and ports, makes the TE2440-II a reliable device for the development of hand-held device, consumer electronics and Industrial control equipment.

1.1 Components in the Package

Standard Components:

1. 1 × TE2440-II board
2. 1 × serial port cable
3. 1 × USB cable
4. 1 × Ethernet cable
5. 1 × JTAG wiggler with JTAG cable
6. 1 × 5V power supply
7. 1 × DVD

Optional Components:

1. 3.5" TFT LCD with touch panel and stylus.
2. 5.7" TFT LCD with touch panel and stylus.
3. 7" TFT LCD with touch panel and stylus.
4. OV9650 CMOS camera
5. USB camera
6. WIFI module

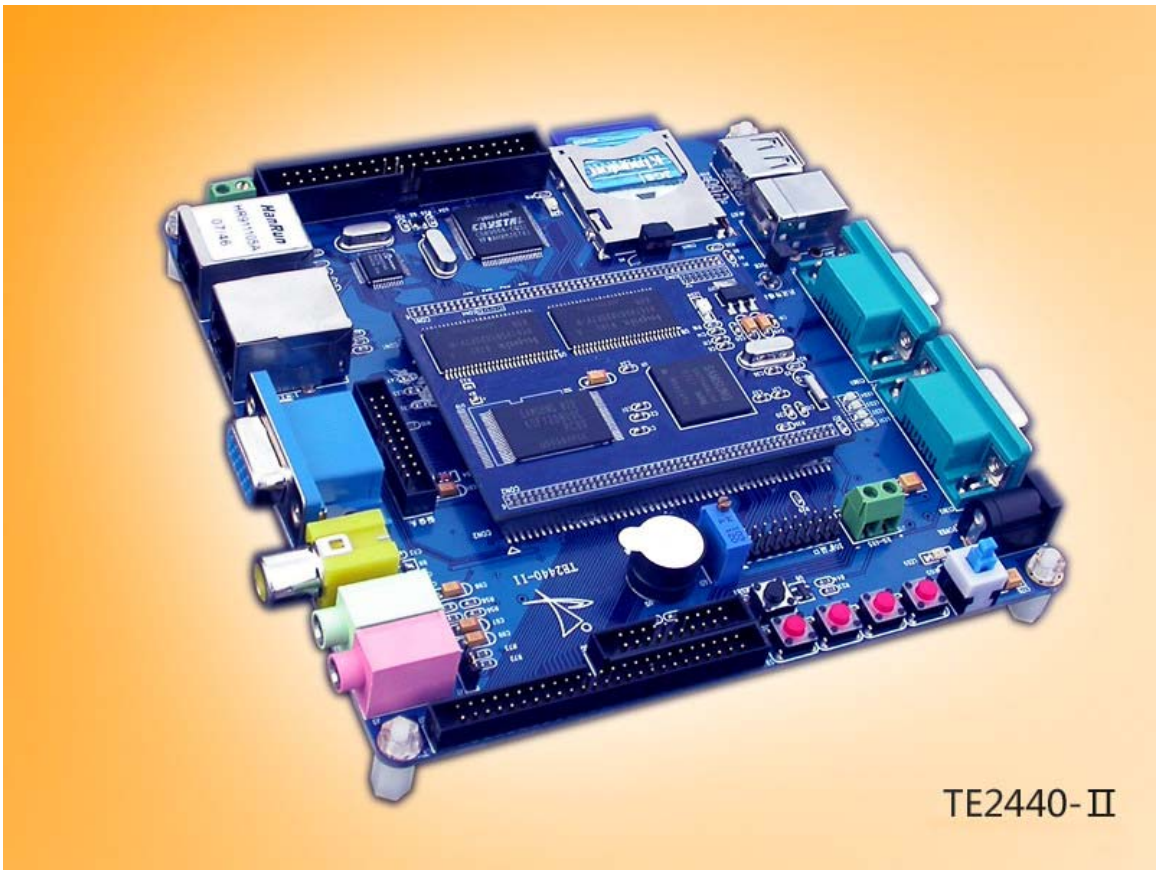
1.2 DVD contents

The DVD includes some documents and development resources for the TE2440-II SBC. In the DVD:

- The folder named as "bootloader" contains the source code and object files of the bootloader.
- Folder "Linux" contains kernel source code, filesystem and some related tools for Linux-2.6.12 and Linux-2.6.28.
- Folder "WinCE" contains the WindowsCE BSP source code, SDK, test program and binaries for both WinCE5.0 and WinCE6.0.
- Folder "ucos2" contains the source code and binaries of ucos2 operating system.
- "Drivers" contains USB driver, parallel port driver, JLINK driver, ActiveSync driver and USB-RS232 driver for the PC.

- "Schematics" contains the schematic of the TE2440-II base board and layout of the core board.
- "Demos" contains demonstration programs.
- "Tools" contains some utility programs such as DNW, H-JTAG, ActiveSync.
- "Datasheets" contains datasheets for the major on-board components and chips.
- "HardwareTest" contains the source code and binaries for the hardware test program.
- "Manuals" contains user manuals and operation instructions in PDF.

1.3 Appearance



1.4 Hardware Resources

CPU:

- Samsung S3C2440A microcontroller, running @400MHz

RAM:

- 64MB SDRAM

Flash:

- 4MB NOR Flash
- 128MB Nand Flash using K9F1208

Serial Ports:

- Two 5-wire RS232 ports, bard rate @ 115200bps
- One RS485 interface

Ethernet Ports:

- One 10M Ethernet with connection and transmission indicator, using CS8900Q3
- One 100M Ethernet with connection and transmission indicator, using DM9000

USB Interfaces

- One USB1.1 Host
- One USB1.1 Device

Audio:

- One stereo audio output socket for earphone or speaker, using IIS interface chip UDA1341

Storage Interfaces:

- One SD card slot
- One IDE connector, can be used for connecting hard disk or as Bus expansion interface.

LCD&Touch Interface:

- On-board 4-wire resistive touch screen interface
- One 50-pin LCD connector
- Support black and white, 4 level grayscale, 16 level grayscale, 256-color, 4096-color STN LCD
- 256K-color 320x240/3.5 inch TFT LCD with touch panel
- On-board 3.3V/5V power output interface for variety LCD models.

VGA/TV Interface:

- Supporting 800x600 VGA/TV output

Camera connector:

- One 20p 2.0mm pitch camera connector

Clock source:

- Internal real time clock

Reset Circuit:

- One reset button specific reset chip

JTAG Interface:

- One 20pin Multi-ICE JTAG interface, supporting SDT2.51, ADS1.2

Power Supply:

- 5V power supply with power switch and indicator

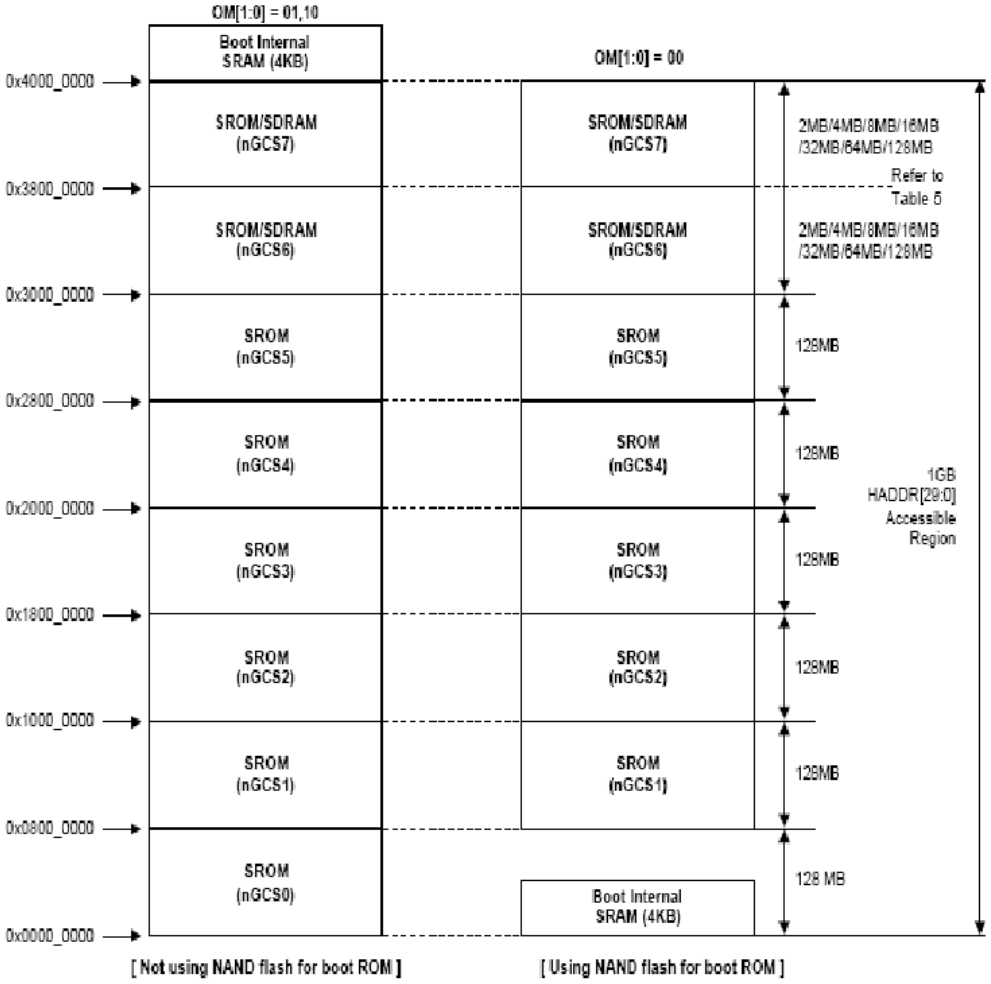
Others:

- Four user buttons
- Four user LEDs
- One PWM controlling buzzer
- One adjustable resistance connected to ADS pins for A/D conversion
- One infrared receiver
- One expansion interface, containing SPI/GPIO and I2C, etc.

1.5 Hardware Resource Distribution

1.5.1 Address Space and Chip Selection

The TE2440-II can be boot from either Nand Flash or NOR Flash. The distribution of storage space is different when booting from each Flash, as shown in the figure below:



The left drawing is the memory allocation diagram when the system is set to the Nor Flash boot mode with nGCS0 being set.

The right drawing is the memory allocation diagram when the system is set to the Nand Flash boot mode.

Note: SFR Area is reserved for special registers

nGCS0 will map its address space to different devices when the system boots in different modes

- When the system boots from the Nand Flash, its 4K Bytes BootSram will be mapped to nGCS0's address space;

- When the system boots from the Nor Flash (not the Nand Flash boot mode), the Nor Flash which is connected to nGCS0 will be mapped to nGCS0's address space.

SDRAM address space: 0x30000000 ~ 0x34000000

1.5.2 On-board Interfaces

Interface	Description
J1	Audio Output Interface (PHONE)
J3	Audio Input Interface (MIC)
U4	LCD/Touch Interface
Camera	Camera interface
CN2	Standard 20pin JTAG interface
J4	Power socket
CN3	GPIO interface
IDE	Hard disk connector

1.5.3 Buttons

Button	Description
S1(RESET)	Reset button (Black)
S6, S7, S8, S9	Four user buttons (Red)

1.5.4 LEDs

LED	Description
LED1, LED2, LED3, LED4	I/O indicator
LED5	5V power status indicator
LED6, LED7	Ethernet status indicators
LED8	Hard disk status indicator
LED9	Core board 3.3V power supply indicator

1.5.5 Jumpers

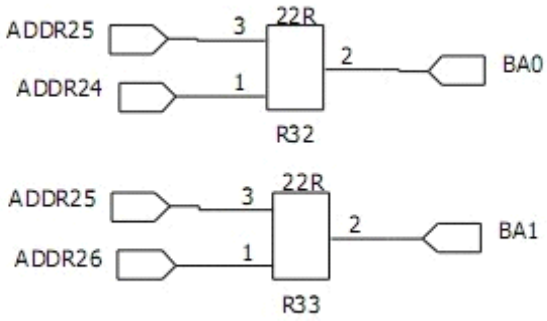
Jumper	Description
J2 on the base board	LCD power voltage selector. When pin1 and pin2 are connected, the LCD voltage is selected as 5V. When pin2 and pin3 are connected, the LCD voltage is selected as 3.3V
J2 on the core board	NOR Flash chip selection selector. When pin0 is connected, NGCS0 is selected as chip selection; When pin1 is connected, NGCS1 is selected as chip selection;
J5 on the core board	Boot mode selector. When J5 is connected, OM[1:0]=00, the system boots from Nand Flash; When J5 is disconnected, OM[1:0]=01, the system boots from NOR Flash;

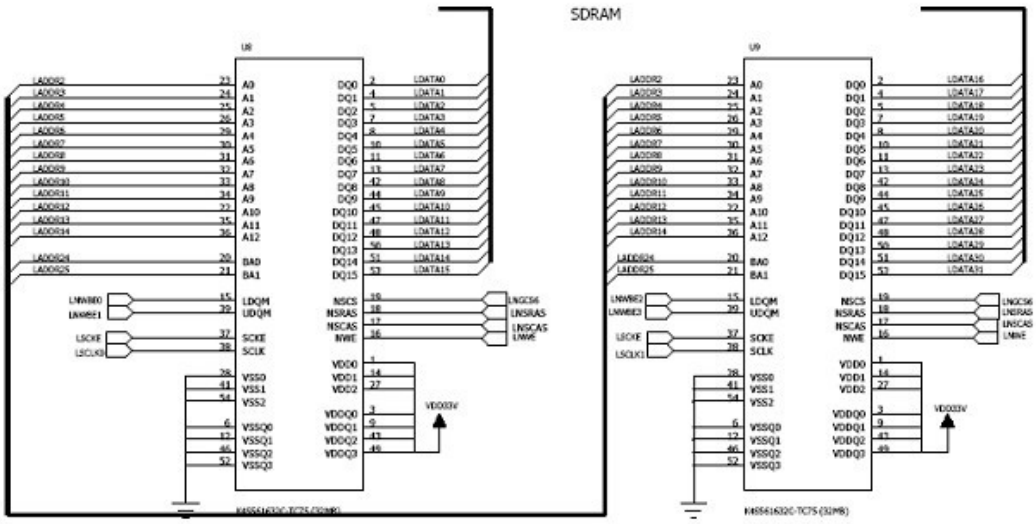
1.6 Major Hardwares

1.6.1 Storage Devices

Storage devices on the TE2440-II include SDRAM and Flashes, consists of two 32MB Samsung SDRAM chips, one 256MB Nand Flash chips. In order to improve the communication efficiency with the CPU, the 32bit SDRAM system consists of two half-word SDRAM chips.

Considering the actual needs of users', the SDRAM is designed as compatible, supporting 32MB or 64MB single chip SDRAM controlled by the two resistances shown in the figure below. As shown in the figure, for using 32MB SDRAM we should connect the pin2 and pin1 on the R32 with 22Ω resistance, and also connect the pin2 and pin3 on R33 with 22Ω resistance; for using 64MB SDRAM we should connect the pin3 and pin2 on the R32 with 22Ω resistance, and also connect the pin1 and pin2 on R33 with 22Ω resistance;





1.6.2 JTAG and Reset Logic

a) What is JTAG?

JTAG (Joint Text Action Group) was a standard for testing PCB and integrated circuit formed in 1985; in 1990 it became an IEEE standard as IEEE 1149.1-1990, it was used for

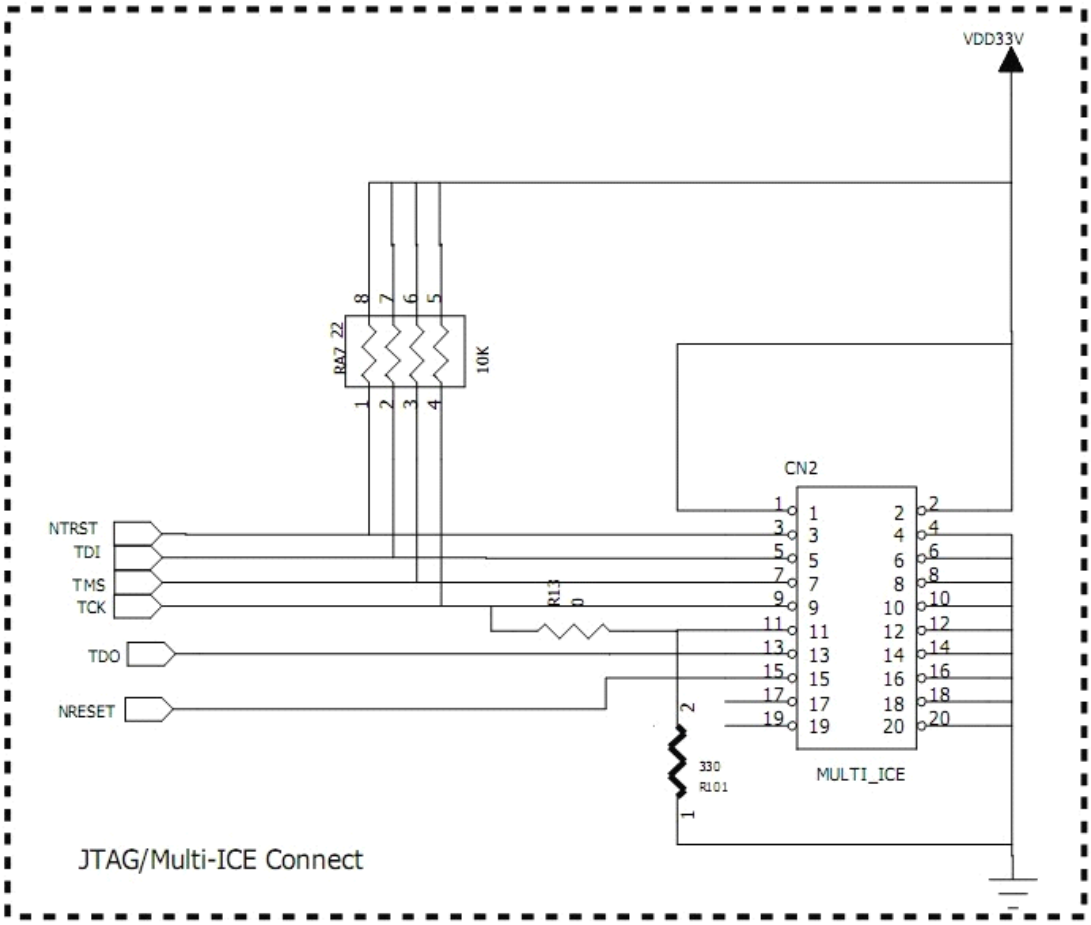
boundary scanning and fault detecting on hardware circuits with JTAG-interfaced ICs. Normally, a JTAG interface should include the following pins:

1. **TDI** (Test Data In)
2. **TDO** (Test Data Out)
3. **TCK** (Test Clock)
4. **TMS** (Test Mode Select)
5. **TRST** (Test Reset) optional.

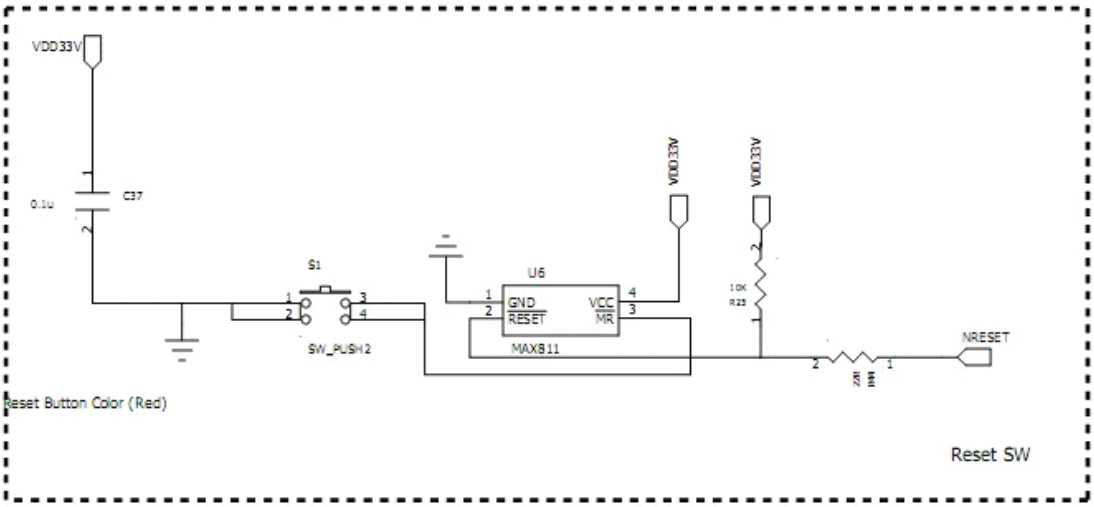
JTAG was initially formed to test ICs, in nowadays, JTAG interface is also used a lot for ISP (In System Programming) to program Flash and etc.

b) JTAG on the TE2440-II

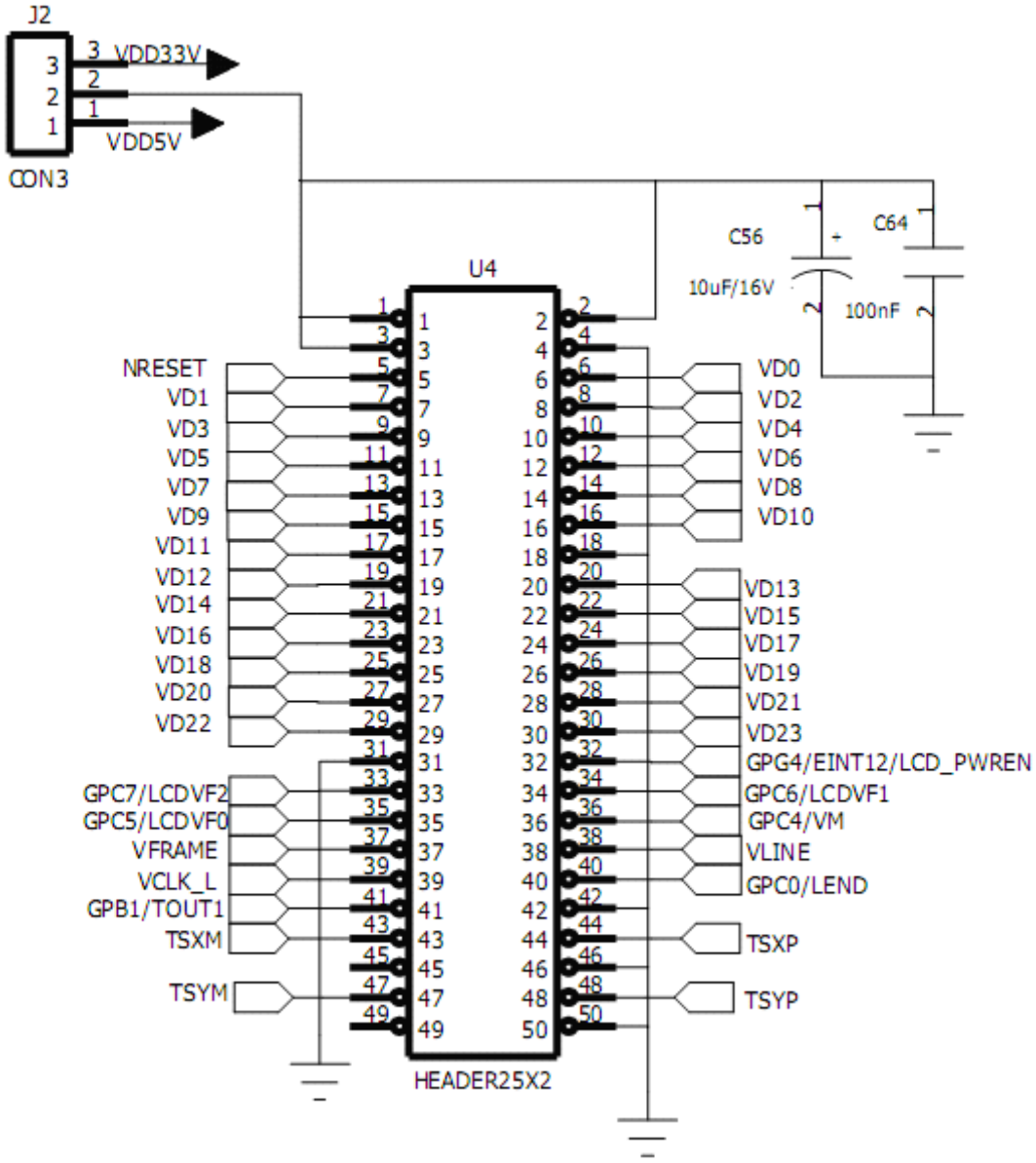
JTAG interface on the TE2440-II SBC is a standard 20-pin interface, supports Flash programming and debugging. Schematic of JTAG interface is shown in the figure below.



Reset circuit: Specialized reset chip is used on the TE2440-II to implement reset circuit. In order to ensure reliable reset operation, the system reset signal nREST keep low power level for 4 clock cycle. Once an external reset signal is received by the CPU, it will turn the CPU reset signal to low power level and keep for 128 clock cycle.



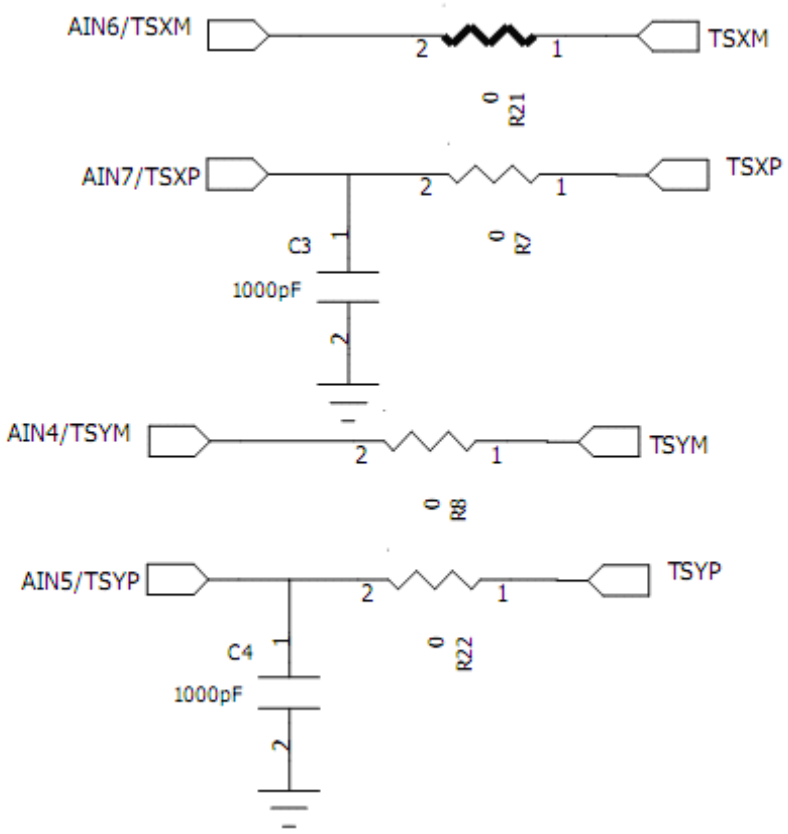
1.6.3 LCD/Touch Screen interface



Pin	Function	Pin	Function
1	VCC	2	VCC
3	VCC	4	GND
5	NRESET	6	VD0
7	VD1	8	VD2
9	VD3	10	VD4
11	VD5	12	VD6
13	VD7	14	VD8
15	VD9	16	VD10
17	VD11	18	GND
19	VD12	20	VD13
21	VD14	22	VD15
23	VD16	24	VD17
25	VD18	26	VD19
27	VD20	28	VD21
29	VD22	30	VD23
31	GND	32	LCD_P0
33	LCDVF	34	LCDVF1
35	LCDVF	36	VM
37	VFRAM	38	VLINE
39	VCLK	40	LEND
41	GPB1	42	GND
43	TSXM	44	TSXP
45	NC	46	GND
47	TSYM	48	TSYP
49	NC	50	GND

When LCD controlling signals are connected to matched resistance, we can transmit data to a greater distance. Among the LCD controlling signals, TSXP and TSXM are connected to pins in

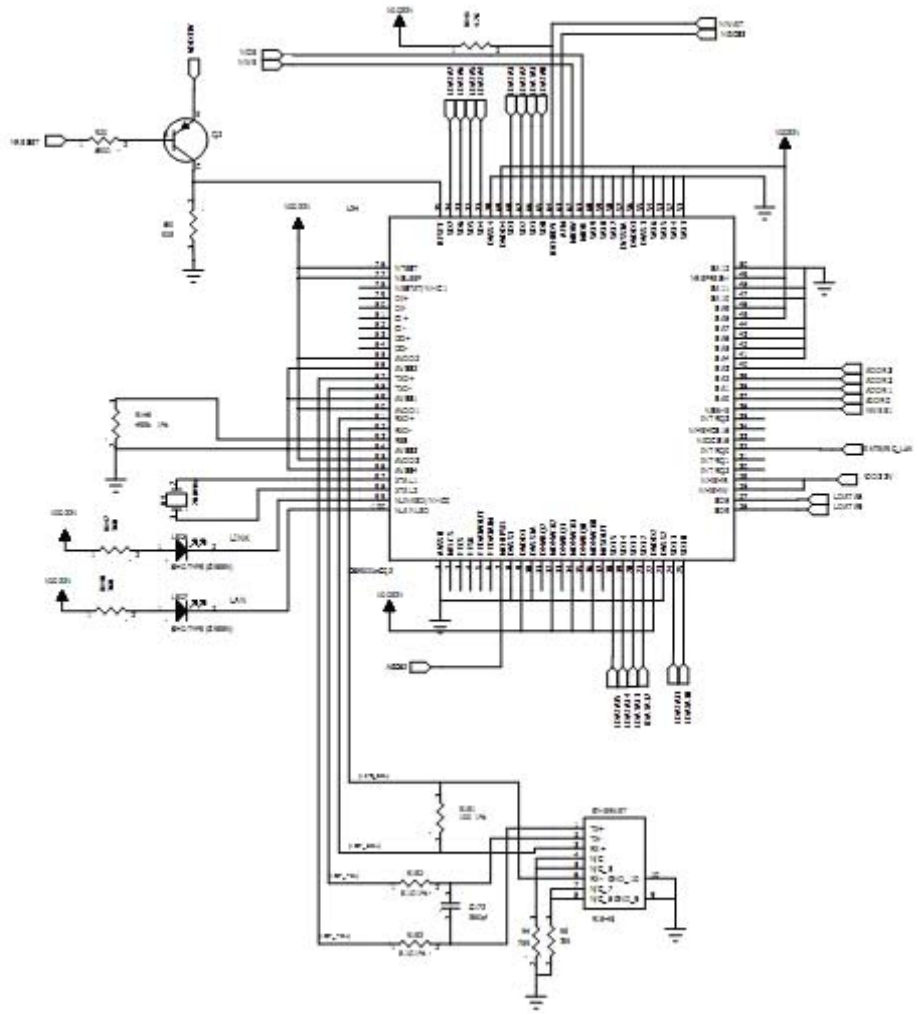
the X group on the 4-wire resistive touch screen, TSYP and TSYM are connected to the pins in the Y group. As shown in the figure below:



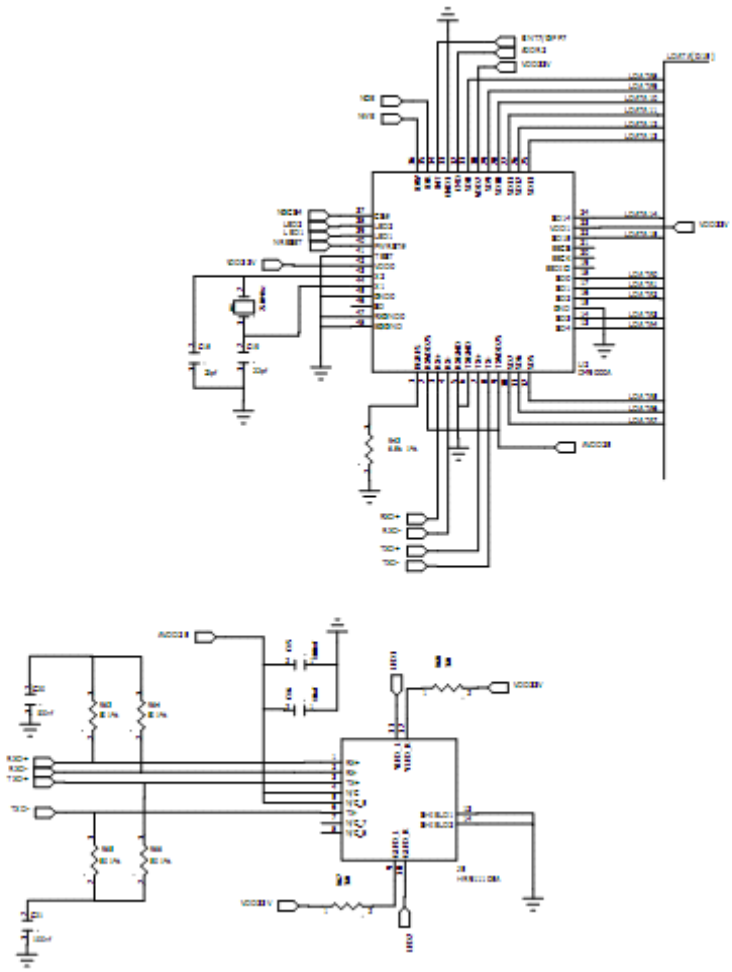
1.6.4 Ethernet Interfaces

a) 10M Ethernet circuit

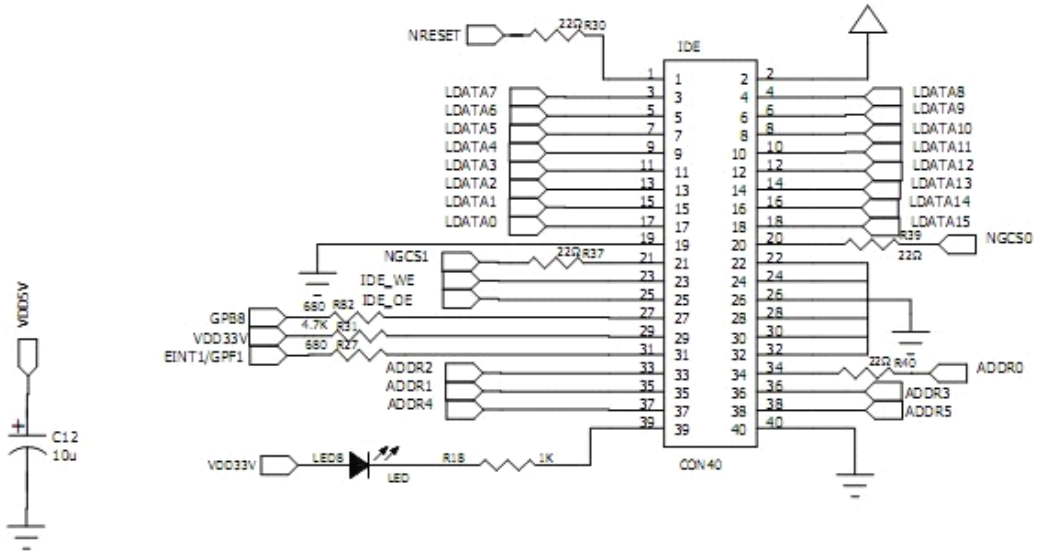
Schematic of the 10M Ethernet circuit is as shown in the figure below:

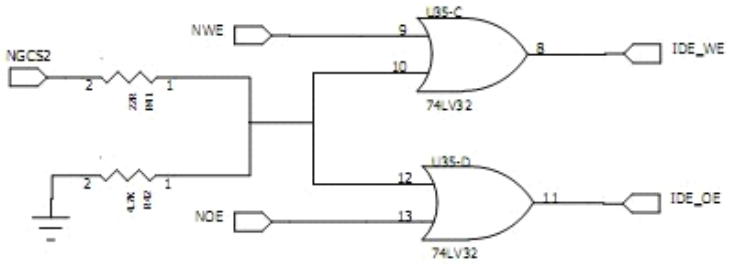


b) 100M Ethernet interface using DM9000



1.6.5 IDE (also Bus expansion) Interface

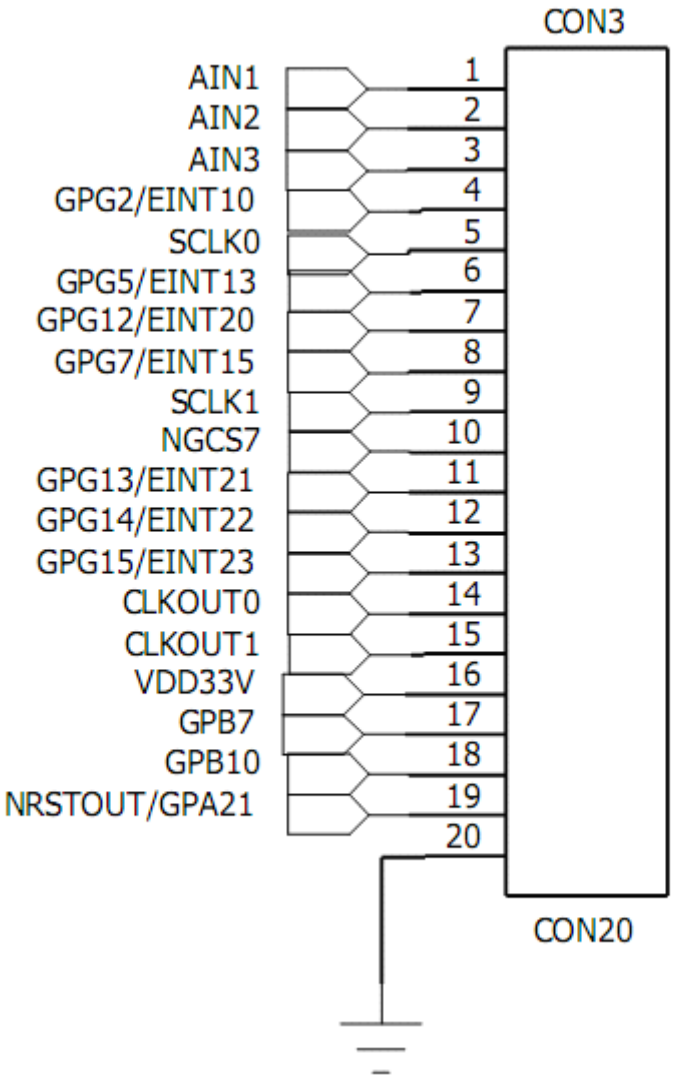




Pin	Function	Pin	Function
1	NRESET	2	GND
3	LDATA7	4	LDATA9
5	LDATA6	6	LDATA9
7	LDATA5	8	LDATA10
9	LDATA4	10	LDATA11
11	LDATA3	12	LDATA12
13	LDATA2	14	LDATA13
15	LDATA1	16	LDATA14

17	LDATA0	18	LDATA15
19	GND	20	NC as default, can be connected to NGS0
21	NC as default, can be connected to NGS0	22	GND
23	IDE_WE	24	GND
25	IDE_OE	26	GND
27	GPB8	28	GND
29	VDD5V	30	GND
31	EINT1	32	GND
33	ADDR2	34	NC as default, can be connected to ADD0
35	ADDR1	36	ADDR3
37	ADDR4	38	ADDR5
39	VDD	40	GND

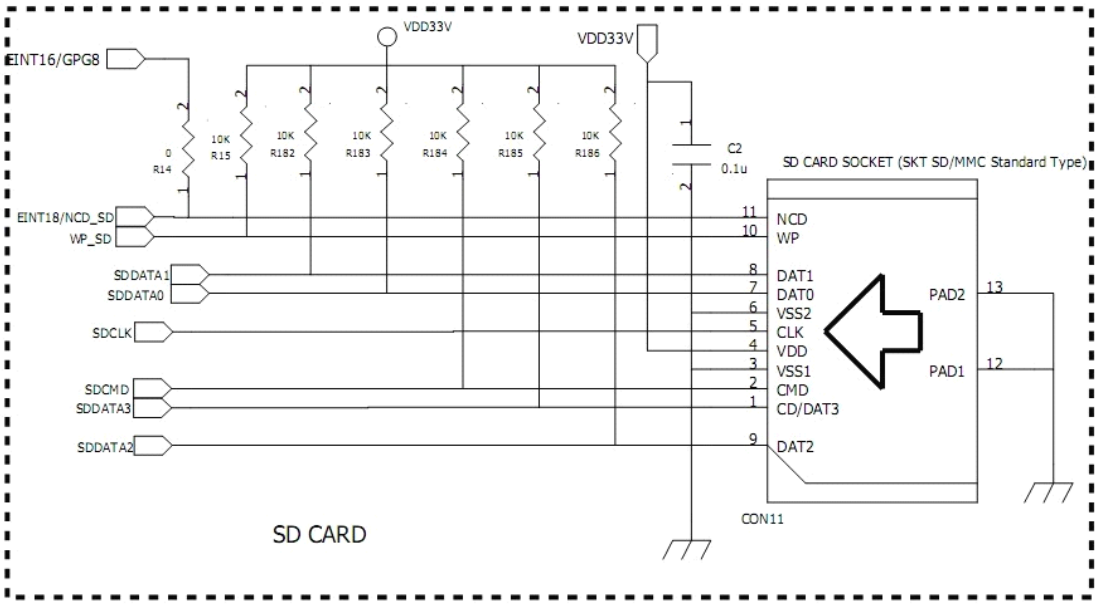
1.6.6 GPIO Interface



Pin	Function	Pin	Function
1	GPE11	2	GPE12
3	GPE13	4	GPG2/EINT10
5	GPG3/EINT11	6	GPG5/EINT13
7	GPG6/EINT14	8	GPG7/EINT15
9	GPG11/EINT19	10	GPG12/EINT20
11	GPG13/EINT21	12	GPG14/EINT22
13	GPG15/EINT23	14	CLKOUT0
15	CLKOUT1	16	GPB5
17	GPB9	18	GPB10
19	NRSTOUT/GPA21	20	GND

1.6.7 SD card slot

The SD card slot on the TE2440-II supports up to 2GB SD card. Schematic of the SD card slot is shown as below:

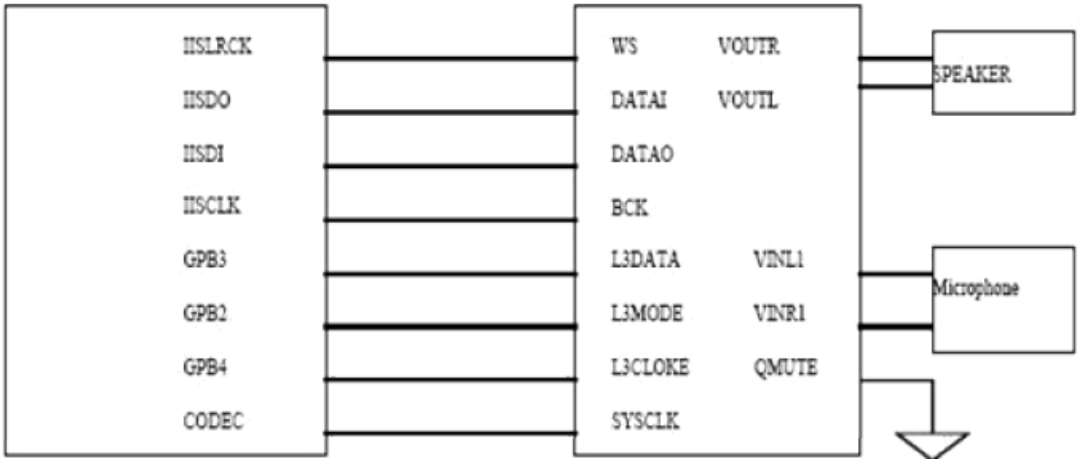


About SD card:

Secure Digital (**SD**) is a non-volatile memory card format developed by Panasonic, SanDisk, and Toshiba on the basis of MultiMedia Card (MMC) format for use in portable devices. Currently it is widely used in digital cameras, digital camcorders, handheld computers, netbook computers, PDAs, media players, mobile phones, GPS receivers, and video games. Standard SD card capacities have a maximum of 2 GB. With a physical profile of 24 mm × 32 mm × 2.1 mm, the new card provided both DRM up to the SDMI standard, and a high memory density for the time.

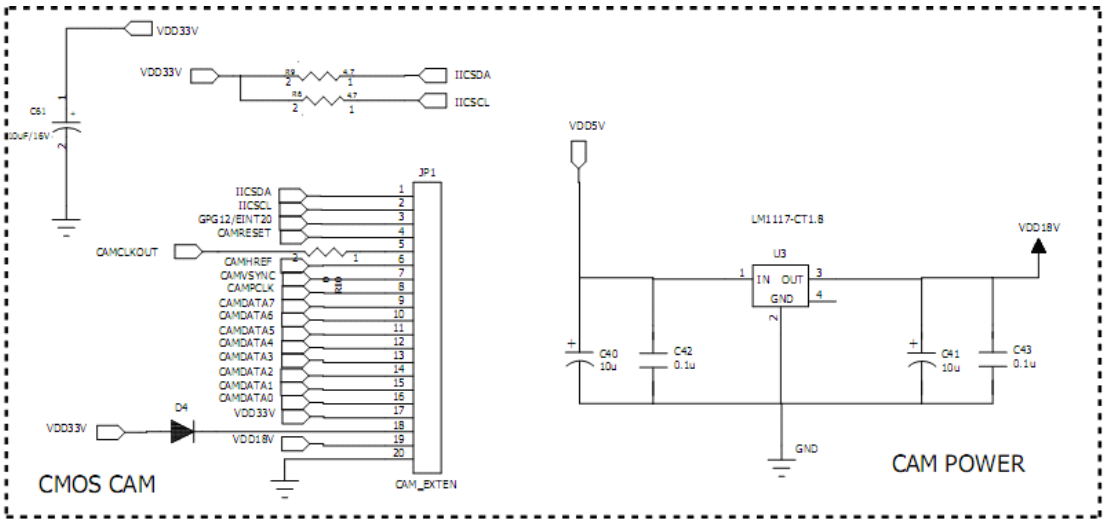
1.6.8 IIS Audio I/O Interface

IIS, also known as **Inter-IC Sound**, **Integrated Interchip Sound**, or **I^2S**, is an electrical serial bus interface standard used for connecting digital audio devices together. It is most commonly used to carry PCM information between the CD transport and the DAC in a CD player. As shown in the schematic below, on the TE2440-II the IIS Bus is connected to the PHILIPS audio digital signal decoder UDA1341TS and then lead out the MIC audio input channel and SPEAKER audio output channel. The IIS interface on the S3C2440X01 micro-controller is connected to the BCK, UWS, DATAI SYSCLK. L3 bus on the UDA1341TS works only when the microcontroller inputs, it includes L3DATA, L3MODE and L3CLOKE, respectively the microcontroller interface data, microcontroller interface mode, and microcontroller interface clock, via which the microcontroller is able to configure the DSP (Digital Signal Processing) parameters and system controlling parameters.



1.6.9 Camera Interface

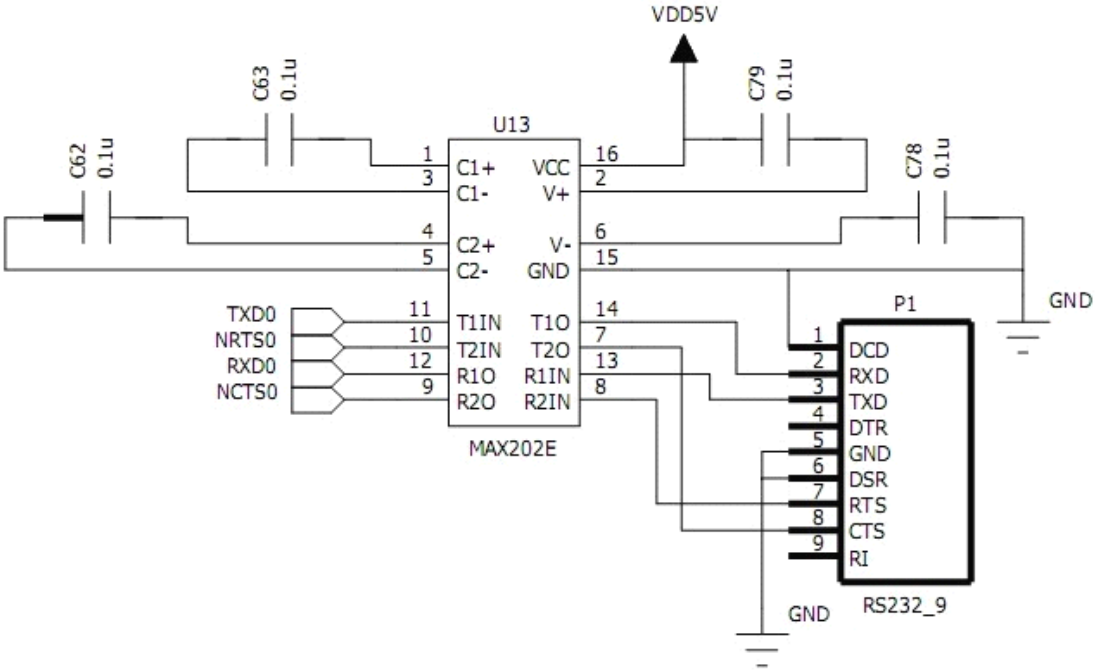
A 20-pin 2.0mm pitch connector is implemented on the TE2440-II as camera connector. Schematic of the camera interface is shown in the figure below:



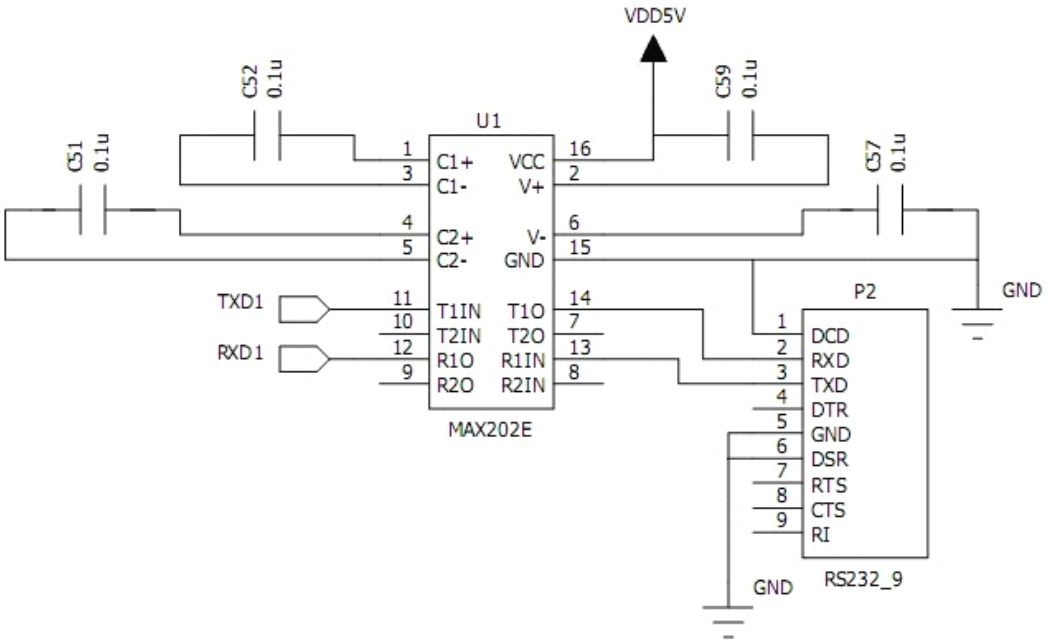
1.6.10 Serial Port Circuit

There are two RS232 (COM0 and COM1) and one RS485 (COM2) serial ports on the TE2440-II.

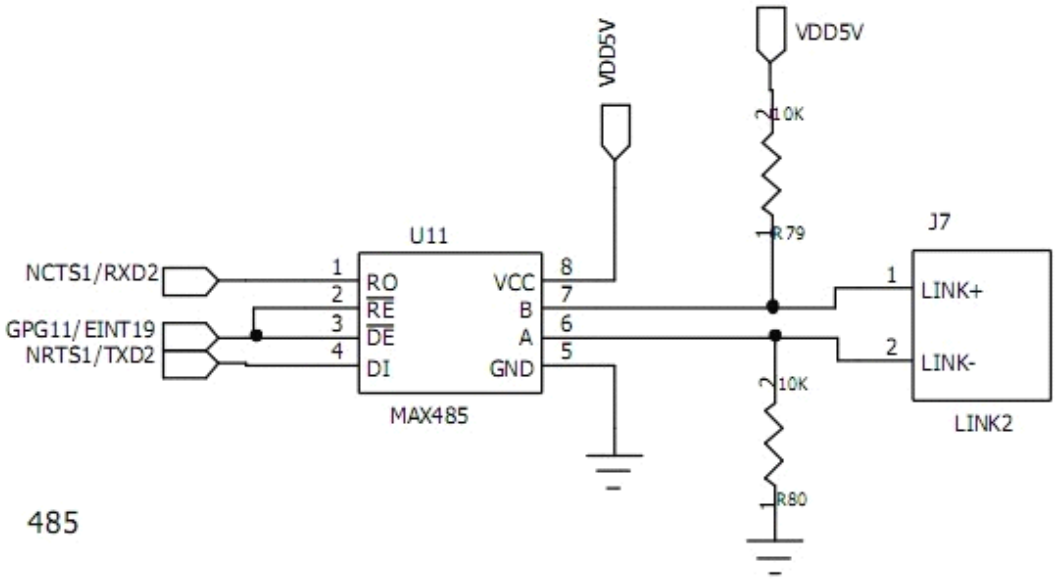
Schematic of COM0 is as shown below:



Schematic of COM1 is as below:



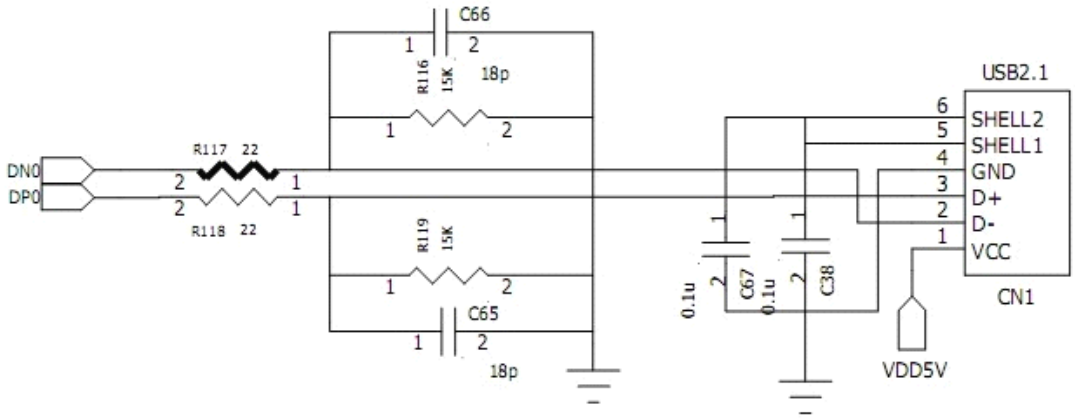
And the figure below shows the schematic of COM2 (RS485):



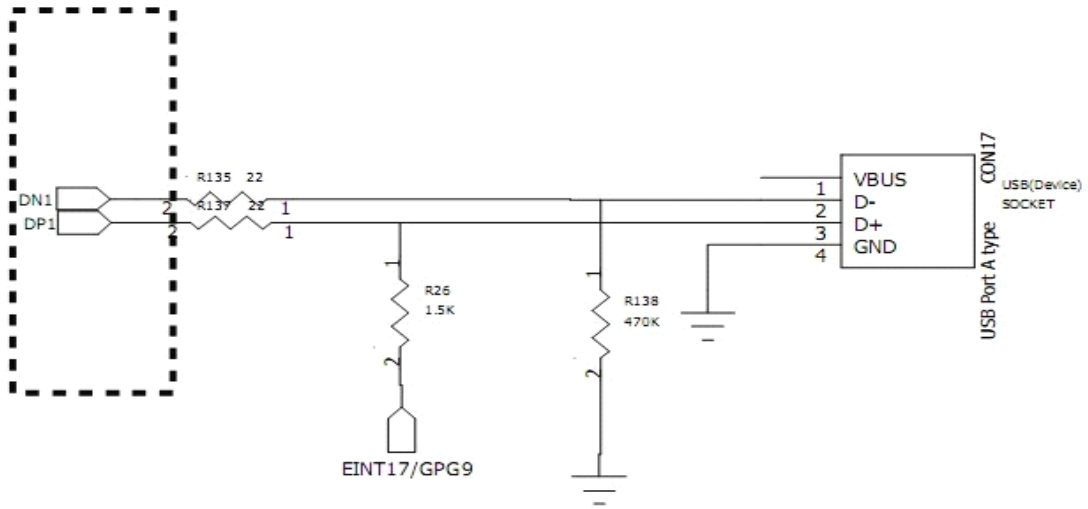
1.6.11 USB Interfaces

There are one USB Host interface and one USB Device interface on the TE2440-II:

Schematic of USB Host interface is shown in the figure:



And the figure below shows the circuits on the USB Device interface:

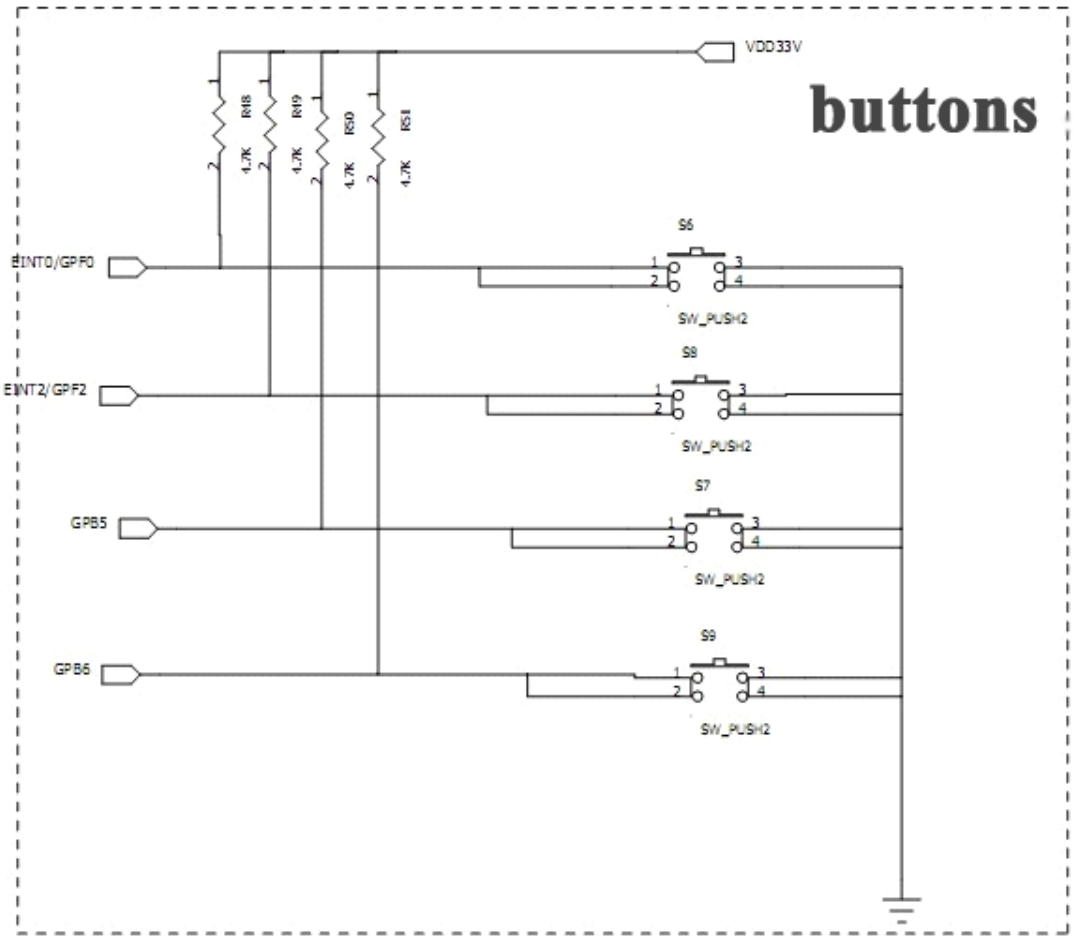


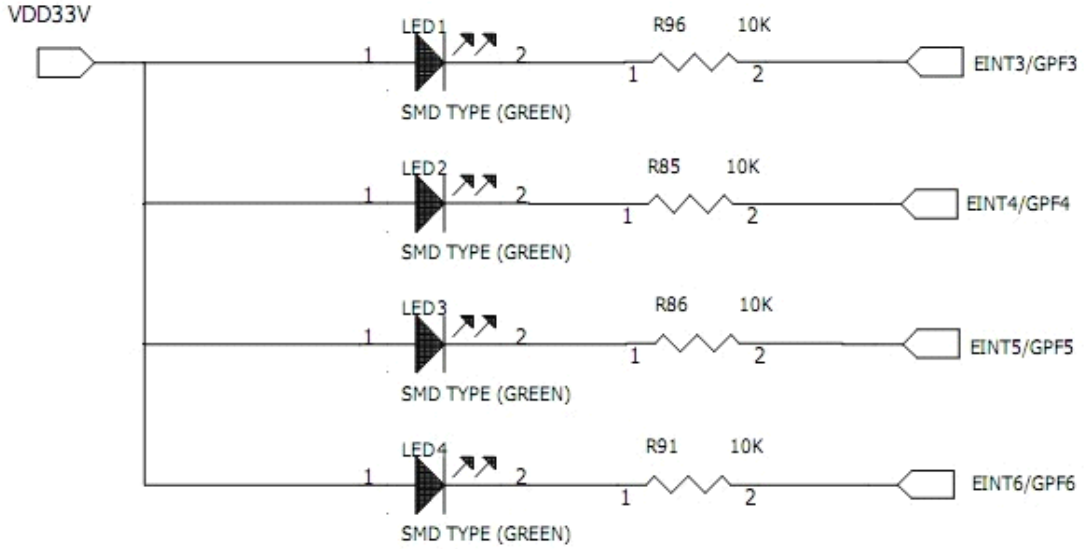
1.6.12 User buttons and User LEDs

Four buttons and four LEDs are reserved on the TE2440-II for the users. The following table shows the I/O ports that the buttons and LEDs are connected:

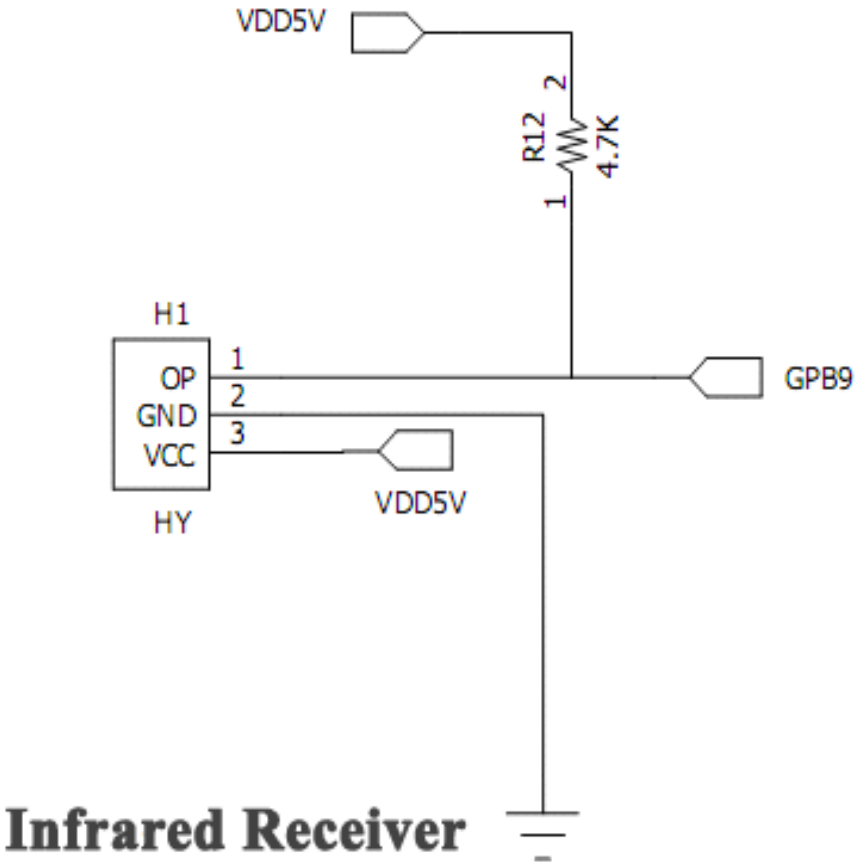
Button	I/O
S6	EINT0/GPF0
S7	EINT2/GPF2
S8	GPB5
S9	GPB6
LED	**I/O**
LED1	EINT3/GPF3
LED2	EINT4/GPF4
LED3	EINT5/GPF5
LED4	EINT6/GPF4

Schematics of the user buttons and LEDs are shown in the figures below:

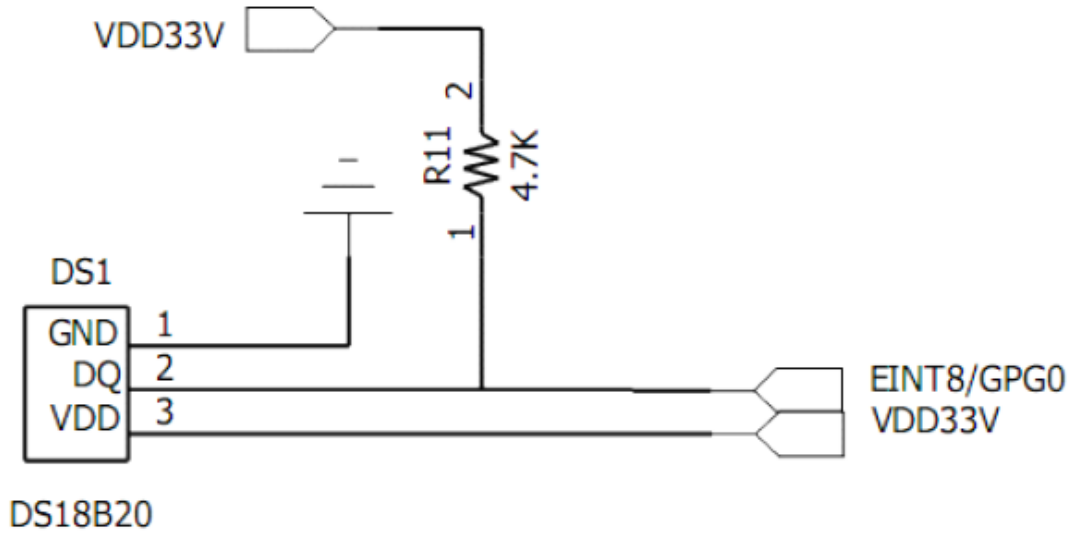




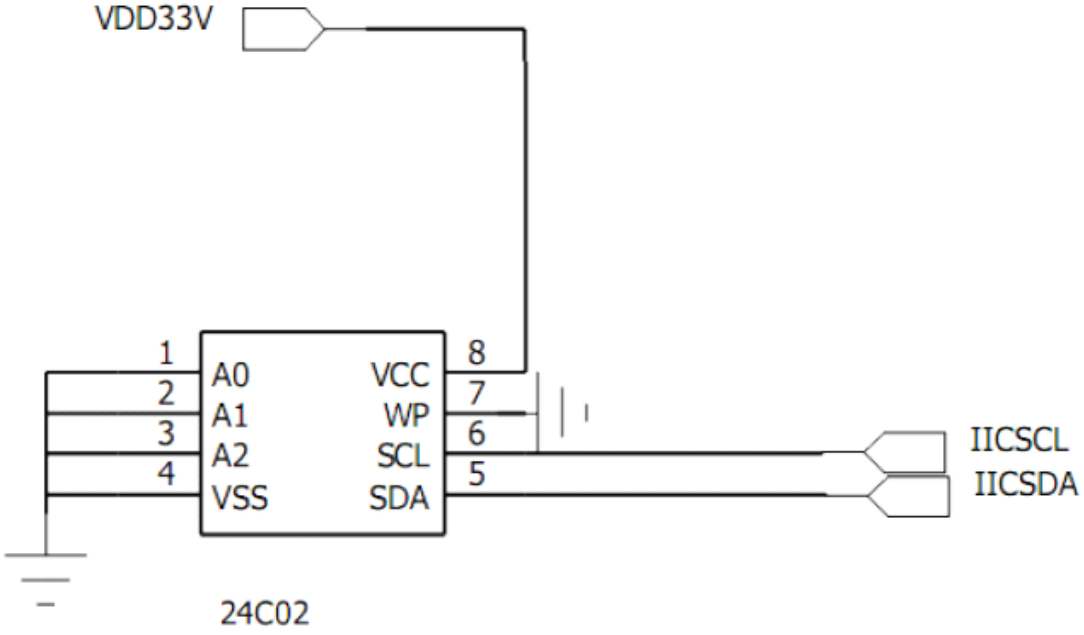
1.6.13 Infrared Receiver



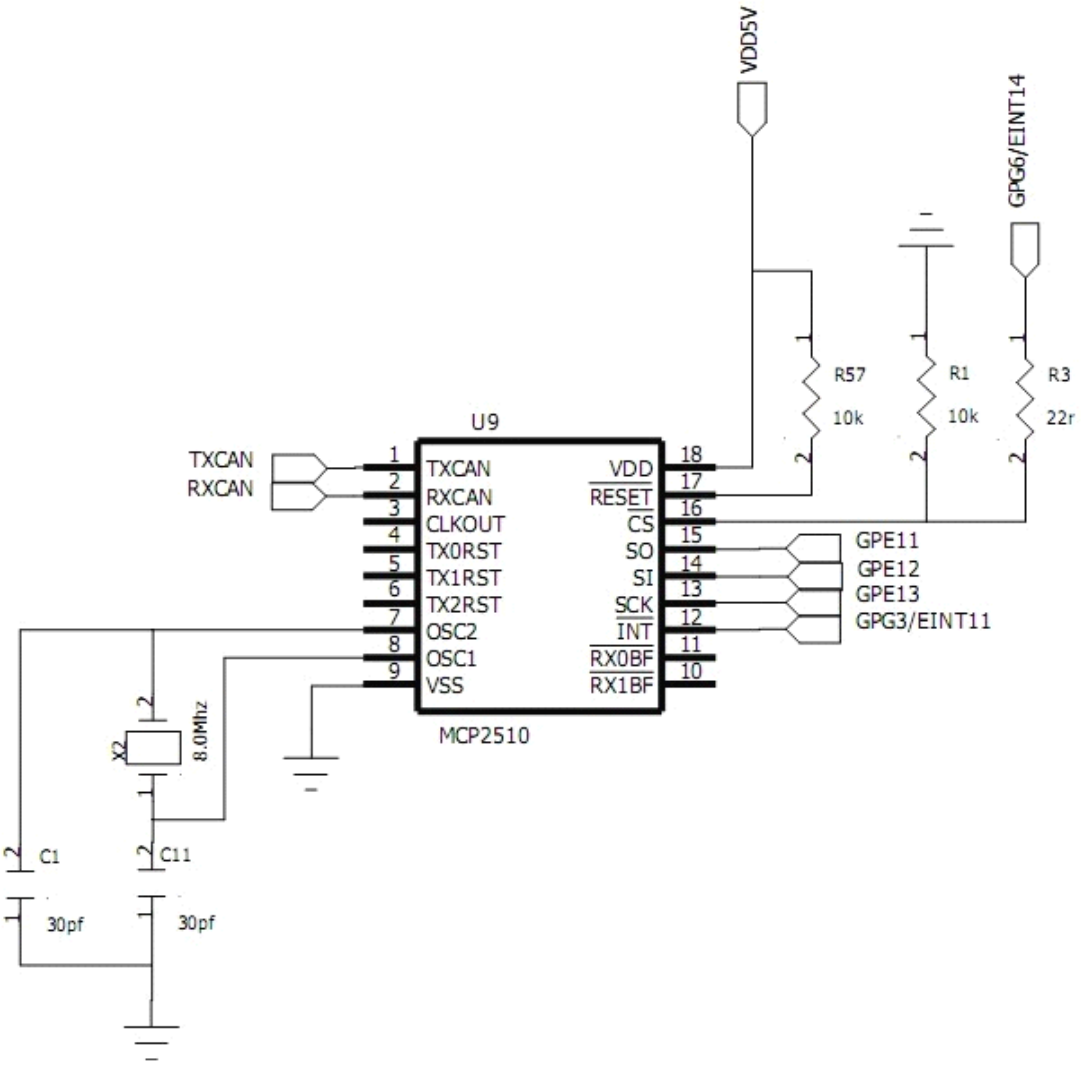
1.6.14 Temperature Sensor

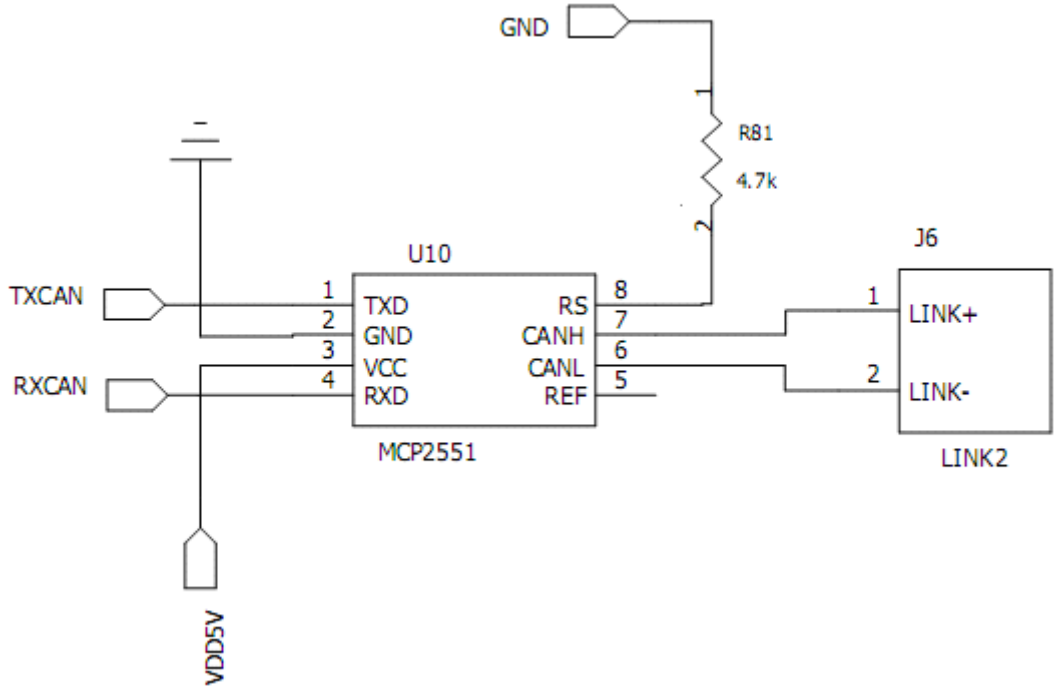


1.6.15 EEPROM (24C02)



1.6.16 CAN Bus Interface





About CAN Bus:

CAN-bus, short for Controller–area network, is a vehicle bus standard designed to allow microcontrollers and devices to communicate with each other within a vehicle without a host computer.

CAN is a message based protocol, designed specifically for automotive applications but now also used in other areas such as industrial automation and medical equipment.

CAN features an automatic 'arbitration free' transmission. A CAN message that is transmitted with highest priority will 'win' the arbitration, and the node transmitting the lower priority message will sense this and back off and wait.

This is achieved by CAN transmitting data through a binary model of "dominant" bits and "recessive" bits where dominant is a logical 0 and recessive is a logical 1. This means open collector, or 'wired or' physical implementation of the bus (but since dominant is 0 this is sometimes referred to as wired-AND). If one node transmits a dominant bit and another node transmits a recessive bit then the dominant bit "wins" (a logical AND between the two).

Truth tables for dominant/recessive and logical AND

Bus state with two nodes transmitting

	dominant	**recessive**
dominant	dominant	dominant
recessive	dominant	recessive

Logical AND

	0	**1**
0	0	0
1	0	1

So, if you are transmitting a recessive bit, and someone sends a dominant bit, you see a

dominant bit, and you know there was a collision. (All other collisions are invisible.) A dominant bit is asserted by creating a voltage across the wires while a recessive bit is simply not asserted on the bus. If any node sets a voltage difference, all nodes will see it. Thus there is no delay to the higher priority messages, and the node transmitting the lower priority message automatically attempts to re-transmit 6 bit clocks after the end of the dominant message.

When used with a differential bus, a Carrier Sense Multiple Access/Bitwise Arbitration (CSMA/BA) scheme is often implemented: if two or more devices start transmitting at the same time, there is a priority based arbitration scheme to decide which one will be granted permission to continue transmitting. The CAN solution to this is prioritised arbitration (and for the dominant message delay free), making CAN very suitable for real time prioritised communications systems.

During arbitration, each transmitting node monitors the bus state and compares the received bit with the transmitted bit. If a dominant bit is received when a recessive bit is transmitted then the node stops transmitting (i.e., it lost arbitration). Arbitration is performed during the transmission of the identifier field. Each node starting to transmit at the same time sends an ID with dominant as binary 0, starting from the high bit. As soon as their ID is a larger number (lower priority) they'll be sending 1 (recessive) and see 0 (dominant), so they back off. At the end of ID transmission, all nodes but one have backed off, and the highest priority message gets through unimpeded.

1.7 Board Support Packages

Together with the TE2440-II single board computer we provide Board Support Packages for WinCE and Embedded Linux.

1.7.1 Embedded Linux

- Kernel: Linux-2.6.12 and Linux-2.6.28
- Supported Filesystem: cramfs/ramfs/etx2/fat32/nfs/yaffs2/jffs2
- Drivers included:
  - ✓ System interrupt and system clock driver
  - ✓ Serial device driver
  - ✓ Block device (IDE hard disk, SD card) drivers
  - ✓ Nand Flash driver
  - ✓ Ethernet driver
  - ✓ RTC driver
  - ✓ USB Host driver
  - ✓ LCD driver
  - ✓ Touch screen driver
- Busybox commands:

  cat，chmod，discard，echo，flashfsd，flashwrite， free，genhtml，hostname，init，kill，loader，ls，mkdir，mount，ps，reboot，rm，smanaged，sysconf， yes，insmod，lsmod，rmmod
- Graphical Interface: Qtopia provided as source code. Other GUIs such as MIZI, microwindows, minigui and etc are also supported.
- Ethernet service: web server, ftp, telnet
- Applications: MP3 player and etc.
- Ethernet protocol: complete TCP/IP

1.7.2 WinCE

- Version: WindowsCE 5.0 and WinCE6.0 R3
- Drivers:
  - ✓ System interrupt and system clock driver
  - ✓ Serial device driver
  - ✓ Block device (SD card) drivers
  - ✓ Nand Flash driver
  - ✓ Ethernet driver
  - ✓ RTC driver
  - ✓ USB Host driver
  - ✓ USB Slave
  - ✓ LCD driver

- ✓ Touch screen driver
- ✓ VGA driver
- ✓ TV driver
- ✓ CAN BUS driver
- ✓ LED/BELL driver
- ✓ Temperature sensor driver
- ✓ ADC driver
- ✓ CMOS camera driver

- ♦ Ethernet protocols: standard IPV4 protocols including TCP/IP, UDP, SMTP, etc.
- ♦ Display: supporting LCD/VGA/TV displaying
- ♦ Applications: IE, MediaPlayer, ActiveSync,
- ♦ MFC and .NET2.0 supported
- ♦ Other WinCE standard functions