The Embedded I/O Company

TIP845

48 Channel 14 bit A/D Conversion

Version 1.0

User Manual

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TIP845-10

48 Channel 14 bit A/D Conversion

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	Initial Issue	November 2003
1.1	Changed ADC correction formula, corrected typos	April 2004
1.2	Added Programming Note and Installation Note	October 2004
1.3	Updated Technical Specification	June 2005
1.4	Summarization of Important Notes	October 2005

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1 Product Description

The TIP845 is an IndustryPack® compatible module providing 48 single-ended or 24 differential ADC input channels. The data acquisition and conversion time is up to 2.5µs without channel / gain change and up to 10.5µs with channel / gain change. The resolution is 14 bit.

The input multiplexer of the A/D circuit offers analog overvoltage protection of up to 70Vpp. A programmable gain amplifier allows gains of 1, 2, 4 or 8 resulting in input voltage ranges of +/-10V, +/-5V, +/-2.5V or +/-1.25V.

Additionally the TIP845 provides a sequencer to control the analog inputs without wasting CPU time. Each of the A/D channels can be independently enabled and configured by a sequencer instruction RAM. After the last instruction of a programmed sequence has completed, the ADC data of all enabled channels are stored in the data RAM. The repeat frequency of the sequencer can be programmed by using the sequence timer. The sequence timer is programmable from 100µs to 6.5535s in steps of 100µs. The sequencer starts a new sequence whenever the timer reaches the programmed value. A special function is the sequencer continuous mode. It is activated by setting the Sequence Timer Register to ‘0’. In this mode the sequencer will start again with the first instruction of the sequence as soon as the last instruction of the previous sequence has been completed.

An interrupt can be generated at end-of-settling, end-of-conversion or end-of-sequencer cycle supporting an 8 bit vector.

Each TIP845 is factory calibrated. The calibration information is stored in the Identification-PROM unique to each IP.

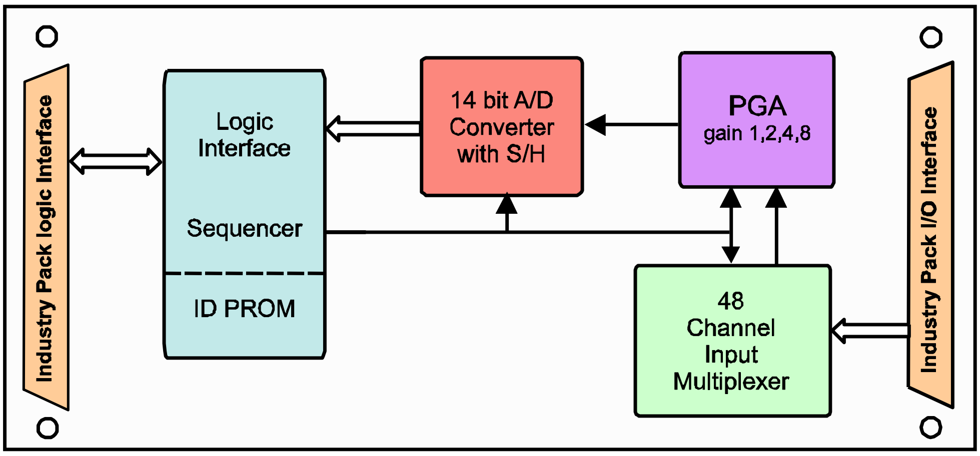

Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I 1 wait state	
I/O Space	Used with no wait states	
Memory Space	Used with 1 wait state	
Interrupts	Int0 used / Int1 not used	
DMA	Not supported	
Clock Rate	8 MHz	
Module Type	Type I	
I/O Interface		
Number of Analog Inputs	48 single-ended or 24 differential channels	
Input Gain Amplifier	Programmable for gain 1, 2, 4 and 8	
Input Voltage Range	±10V for gain = 1 ±5V for gain = 2 ±2.5V for gain = 4 ±1.25V for gain = 8	
Input Overvoltage Protection	70Vpp	
Calibration Data	Calibration data for gain and offset correction in ID PROM	
Conversion Time	2.5µs without channel/gain change 10.5µs with channel/gain change 8µs in sequencer mode	
ADC Resolution	14 bit with no missing codes	
ADC INL/DNL Error	±2/±1 LSB	
Interface Connector	50-conductor flat cable	
Power Requirements	140mA typical @ +5V DC	
Physical Data		
Temperature Range	Operating Storage	-40°C to +85 °C -40°C to +125°C
MTBF	738000 h	
Humidity	5 – 95 % non-condensing	
Weight	31 g	

Figure 2-1 : Technical Specification

3 Functional Description

The TIP845-10 provides 48 single-ended or 24 differential multiplexed analog inputs. The desired input channel and the mode (single-ended or differential) are selected by programming the input multiplexer.

A software programmable gain amplifier with gain settings of 1, 2, 4 and 8 allows a direct connection of a wide range of sensors and instrumentation. The maximum analog input voltage range is ±10V at a gain of 1.

Because the TIP845 is a multiplexed analog input system, a settling time is required to pass after changing the input channel and / or gain. The TIP845 provides a status bit for polling the settling time status. An *Automatic Settling Time Control Mode* is also provided. In this mode, data conversion is automatically started after the settling time has elapsed.

The absolute accuracy of the module can be increased by performing a data correction in software, using the factory calibration factors stored in the on board ID PROM.

3.1 Data Correction

There are two errors which affect the DC accuracy of the ADC.

- ADC Offset Error:

  The Offset Error is the data value if converting with the connected input to its own ground in single-ended mode, or with shorted inputs in differential mode. This error is corrected by subtracting the known error from the *Readings*.

- ADC Gain Error:

  The Gain Error is the difference between the ideal gain and the actual gain of the programmable gain amplifier and the ADC. It is corrected by multiplying the *Reading* with a correction factor.

The data correction values are obtained during factory calibration and are stored in the modules individual version of the ID PROM. The ADC has a pair of offset and gain correction values for each of the programmable gains. The offset and gain error values are the same for all channel 1-48.

3.1.1 ADC Correction Formula

Please use the total 16 bit data register value for the ADC correction formula.

The basic formula for correcting any ADC reading for the TIP845-10 (bipolar input voltage range) is:

$$Value = Reading \cdot \left(1 - \frac{Gain_{corr}}{32768}\right) - Offset_{corr}$$

Value is the corrected result.

Reading is the data read from the ADC Data Register.

$Gain_{corr}$ and $Offset_{corr}$ are the correction factors from the ID PROM stored for each gain factor.

The correction values are stored as two's complement 8 bit values in the range -128 to 127. For higher accuracy they are scaled to ¼ LSB.

Floating point arithmetic or scaled integer arithmetic is necessary to avoid rounding error while computing above formula.

4 ID PROM Contents

Address	Function	Contents
0x01	ASCII 'I'	**0x49**
0x03	ASCII 'P'	**0x50**
0x05	ASCII 'A'	**0x41**
0x07	ASCII 'C'	**0x43**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	**0x39**
0x0D	Revision	**0x10**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x14**
0x17	CRC	**variable**
0x19	Offset Error Gain 1	**Board dependent**
0x1B	Offset Error Gain 2	**Board dependent**
0x1D	Offset Error Gain 4	**Board dependent**
0x1F	Offset Error Gain 8	**Board dependent**
0x21	Gain Error Gain 1	**Board dependent**
0x23	Gain Error Gain 2	**Board dependent**
0x25	Gain Error Gain 4	**Board dependent**
0x27	Gain Error Gain 8	**Board dependent**
0x29…0x3F	Not used	

Figure 4-1 : ID PROM Contents

The ID PROM data is available 200 µs after reset.

5 IP Addressing

5.1 I/O Addressing

The TIP845 is controlled by a set of registers which are directly accessible in the I/O space of the IP module.

Address	Symbol	Description	Size (Bit)	Access
0x00	CONTREG	ADC Control Register	16	R/W
0x02	DATAREG	ADC Data Register	16	R
0x05	STATREG	ADC Status Register	8	R
0x07	CONVERT	ADC Conversion Start Register	8	W
0x09	INTSTAT	Input Interrupt Status Register	8	R/W
0x0B	SEQCONT	Sequencer Control Register	8	R/W
0x0D	SEQSTAT	Sequencer Status Register	8	R/W
0x0E	SEQTIMER	Sequencer Timer Register	16	R/W
0x11	IVEC	Interrupt Vector Register	8	R/W
0x12.. 0x20	-	Reserved, do not write	-	-
0x21.. 0x4F	SIRAM1-24	Sequencer Instruction RAM	24 x byte	R/W

Figure 5-1 : Register Set

ADC Register Set

5.1.1 ADC Control Register CONTREG (Address 0x00)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>15:12</td><td>-</td><td>Reserved
Write: don't care
Read: always reads as '0'</td><td>R</td><td>0</td></tr>
<tr><td>11</td><td>IRQC</td><td>IRQ after Conversion
0 = No interrupt generation after finished conversion
1 = Interrupt generation after finished conversion</td><td>R/W</td><td>0</td></tr>
<tr><td>10</td><td>IRQST</td><td>IRQ after Settling Time
0 = No interrupt generation after settling time has elapsed
1 = Interrupt generation after settling time has elapsed</td><td>R/W</td><td>0</td></tr>
<tr><td>9</td><td>ASTC</td><td>Automatic Settling Time Control
0 = OFF (Normal Mode)
A conversion must be initiated manually in the CONVERT register
1 = ON (Automatic Mode)
A conversion is automatically initiated after the settling time has elapsed.
The settling time for the TIP845 is appr. 8µs</td><td>R/W</td><td>0</td></tr>
<tr><td>8:7</td><td>GAIN[1:0]</td><td>Gain Selection (Analog Input Amplifier)
<table><tr><th>GAIN1</th><th>GAIN0</th><th>Gain Factor</th><th>Input Voltage Range</th></tr><tr><td>0</td><td>0</td><td>1</td><td>±10V</td></tr><tr><td>0</td><td>1</td><td>2</td><td>±5V</td></tr><tr><td>1</td><td>0</td><td>4</td><td>±2.5V</td></tr><tr><td>1</td><td>1</td><td>8</td><td>±1.25V</td></tr></table></td><td>R/W</td><td>00</td></tr>
<tr><td>6</td><td>SE/DIFF</td><td>Single/Differential Mode Control
0 = Single-ended mode
48 single-ended input channels available
1 = Differential mode
24 differential input channels available
Mixed modes are possible</td><td>R/W</td><td>0</td></tr>
</table>

Bit	Symbol	Description	Access	Reset Value
5:0	CS[5:0]	Channel Select (Analog Input Channel) CS[5:0] / Single-ended Channel SE/DIFF = 0 / Differential Channel SE/DIFF = 1: 000000: CH1, CH1 …: …, … 010111: CH24, CH24 011000: CH25, N/A …: …, … 101111: CH48, N/A 110000: N/A, N/A …: …, … 111111: N/A, N/A 'N/A' = ADC Input connected to GND	R/W	0x3F

CS[5:0]	Single-ended Channel SE/DIFF = 0	Differential Channel SE/DIFF = 1
000000	CH1	CH1
…	…	…
010111	CH24	CH24
011000	CH25	N/A
…	…	…
101111	CH48	N/A
110000	N/A	N/A
…	…	…
111111	N/A	N/A

Figure 5-2 : ADC Control Register

A write to this register sets the new channel and gain. Subsequent write accesses are ignored until the settling time has elapsed. To change both channel and gain, or to archive a full channel setup, a word access is recommended.

5.1.2 ADC Data Register DATAREG (Address 0x02)

The ADC Data Register contains the converted data value. Output coding is two's complement binary (1 LSB = FSR/16384 = 1.22 mV for the ±10 V range). This 14 bit ADC value is shifted to the higher bits of the register by hardware. This allows direct processing of the data as a 16 bit two's complement integer value.

Bit	Symbol	Description	Access	Reset Value
15:2		Stores the converted 14 bit data value, shifted by hardware to the higher bits	R	0
1:0		Always read as '0'	R	0

Figure 5-3 : ADC Data Register

Description	Shifted ADC Data Value
Full Scale (pos.)	0x7FFC
…	…
Midscale + 1 LSB	0x0004
Midscale	0x0000
Midscale – 1 LSB	0xFFFC
…	…
Full Scale (neg.)	0x8000

Figure 5-4 : ADC Data Coding

5.1.3 ADC Status Register STATREG (Address 0x05)

Bit	Symbol	Description	Access	Reset Value
7:2	-	Reserved Read: always read as '0'	R	000000
1	SETTL BUSY	SETTL_BUSY Indicates that the required settling time after a write to the CONTREG register is not yet done. If *Automatic Settling Time Mode* is OFF, this bit is set by writing to the CONTREG register. The bit is cleared if the required settling time has elapsed. This bit must be read as '0' before a conversion is started by a write to the CONVERT register. The settling time for the TIP845 is appr. 8µs	R	0
0	ADC BUSY	ADC_BUSY Indicates if an actual data conversion is in progress. If *Automatic Settling Time Mode* is OFF, this bit is set by writing to the CONVERT register. If *Automatic Settling Time Mode* is ON, this bit is set automatically after the settling time has elapsed. This bit must be read as '0' before the conversion data is read from the DATAREG register.	R	0

Figure 5-5 : ADC Status Register

5.1.4 ADC Conversion Start Register (Address 0x07)

The ADC Conversion Start Register CONVERT is an 8 bit wide write only register. The ADC Conversion Start Register is used to start an ADC conversion if *Automatic Settling Time Mode* is OFF. The user must read the SETTL_BUSY bit in the ADC Status Register as '0' before the conversion is started. The ADC_BUSY bit in the ADC Status Register indicates if the conversion data in the ADC Data Register is valid (ADC_BUSY bit = '0').

It is allowed to set up a new channel/gain by writing to the ADC Control Register CONTREG immediately after starting an ADC conversion.

If *Sequencer Mode* is selected (SEQCONT Register bit 0 is set to ‘1’) a write access to the ADC Conversion Start Register is ignored.

Please pay attention to the chapter “Important Notes”.

5.2 Sequencer Register Set

5.2.1 Sequencer Control Register SEQCONT (Address 0x0B)

Bit	Symbol	Description	Access	Reset Value
7:2	-	Reserved Write: don't care Read: always reads as '0'	R	0
1	SEQ INT ENA	Sequencer Interrupt Enable Control 0 = Sequencer interrupt disabled 1 = Sequencer interrupt enabled An interrupt request will be generated if any bit is set in the SEQSTAT register (sequencer data valid or sequencer error).	R/W	0
0	SEQ ON	Sequencer Start / Stop Control 0 = Stops the sequencer after the last instruction 1 = Starts the sequencer immediately	R/W	0

Figure 5-6 : Sequencer Control Register

If an error flag is set in the Sequencer Status Register SEQSTAT, the sequencer will be stopped after the last instruction (SEQ_ON will be set to '0'). The user must clear the status bits and start the sequencer again.

Please pay attention to the chapter "Important Notes" before using the sequencer.

5.2.2 Sequencer Status Register SEQSTAT (Address 0x0D)

Bit	Symbol	Description	Access	Reset Value
7:4	-	Reserved Write: don't care Read: always reads as '0'	R	0
3	I-RAM ERROR	Instruction RAM Error Flag Set by the sequencer if the sequencer has been started and there is no correct instruction in the Instruction RAM. To clear this flag the user must write ‘1’ to this bit.	R/W	0
2	TIMER ERROR	Time Error Flag Set by the sequencer if the sequencer timer has elapsed but the actual sequence is still in progress. To clear the Timer Error Flag the user must write ‘1’ to this bit. If the Sequencer Timer Register is 0 (Sequencer Continuous Mode) the Timer Error Flag always read as ‘0’.	R/W	0
1	DATA OF ERROR	Data Overflow Error Flag Set by the sequencer if the last sequencer instruction is done and the Data Available Flag of the previous sequence has not yet been cleared by the user. To clear the error flag the user must write ‘1’ to this bit. If the Sequencer Timer Register is 0 (Sequencer Continuous Mode) the Data Overflow Error Flag always read as ‘0’.	R/W	0
0	DATA AV	Data Available Flag Set if a sequence is done and new ADC Data is available in the ADC Data RAM. After reading the ADC Data RAM the user must clear the Data Available Flag by writing ‘1’ to this bit.	R/W	0

Figure 5-7 : Sequencer Status Register

As long as any of the bits [3:1] (error flags) of the Sequencer Status Register SEQSTAT is read as ‘1’, the sequencer will be stopped after the last instruction (SEQ_ON will be set to '0'). The user must clear the status bit and start the sequencer again.

5.2.3 Sequencer Timer Register SEQTIMER (Address 0x0E)

The Sequencer Timer Register SEQTIMER is a 16 bit wide read/write register.

The Sequence Timer is programmable from 100µs to 6.5535s in 100µs steps.

Whenever the timer reaches the programmed value the sequencer starts a new sequence with the first instruction found in the instruction RAM.

Assure that the needed time to complete a sequence is suitable to the chosen sequence timer value. If the sequence timer elapses while a sequence is still in progress, a timer error will be asserted.

If the Sequencer Timer Register is set to '0', the *Sequencer Continuous Mode* is selected. The sequencer will start again with the first instruction of the sequence immediately after the last instruction of the previous sequence has been completed.

5.2.4 Sequencer Instruction RAM (Address 0x21…0x4F)

The Sequencer Instruction RAM is a 24 x 8 bit wide RAM which is accessible in the I/O space.

In each sequencer instruction byte configures either one differential ADC channel or two single-ended ADC channels.

The following table shows which sequencer instruction byte is allocated to which channels:

SIRAM Address	Diff. Channel	SE Channels A	B	SIRAM Address	Diff. Channel	SE Channels A	B
0x21	1	1	2	0x39	13	25	26
0x23	2	3	4	0x3B	14	27	28
0x25	3	5	6	0x3D	15	29	30
0x27	4	7	8	0x3F	16	31	32
0x29	5	9	10	0x41	17	33	34
0x2B	6	11	12	0x43	18	35	36
0x2D	7	13	14	0x45	19	37	38
0x2F	8	15	16	0x47	20	39	40
0x31	9	17	18	0x49	21	41	42
0x33	10	19	20	0x4B	22	43	44
0x35	11	21	22	0x4D	23	45	46
0x37	12	23	24	0x4F	24	47	48

Figure 5-8 : Sequencer Instruction RAM addressing

Each sequencer instruction byte is subdivided into following parts:

Sequencer Instruction Byte	Bits [6:4]	Bits [3:0]
Differential configuration	Ignored	Differential Channel
Single-ended configuration	Single-Ended Channel B	Single-Ended Channel A

Figure 5-9 : Sequencer Instruction Byte breakdown

Examples:

To configure single-ended channel 3 to gain 2 and single-ended channel 4 to gain 1 write 0x16 to SIRAM address 0x23.

To configure channel 3 as differential channel with gain 4, write 0x0B to SIRAM address 0x23. By configuration Channel 4 is not available and any settings for channel 27 are ignored.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Power-up Value</th></tr>
<tr><td>7</td><td>-</td><td>Reserved
Write: don't care
Read: always reads as '0'</td><td>R</td><td>0</td></tr>
<tr><td>6:5</td><td>GAIN[1:0]</td><td>Single-Ended Channel B:
Gain Selection (Analog Input Amplifier)
<table>
<tr><th>GAIN1</th><th>GAIN0</th><th>Gain Factor</th><th>Input Voltage Range</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>±10V</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>±5V</td></tr>
<tr><td>1</td><td>0</td><td>4</td><td>±2.5V</td></tr>
<tr><td>1</td><td>1</td><td>8</td><td>±1.25V</td></tr>
</table>
If SE/DIFF = '1', this bits are ignored.</td><td>R/W</td><td>00</td></tr>
<tr><td>4</td><td>ENA</td><td>Single-Ended Channel B:
Enable the ADC Channel for the sequencer
0 = Sequencer will pass over the ADC Channel
1 = Sequencer converts the ADC Channel and updates the ADC Data in the Sequencer Data RAM at the end of the sequence.
If SE/DIFF = '1', this bit is ignored.</td><td>R/W</td><td>0</td></tr>
<tr><td>3:2</td><td>GAIN[1:0]</td><td>Single-Ended Channel A / Differential Channel:
Gain Selection (Analog Input Amplifier)
<table>
<tr><th>GAIN1</th><th>GAIN0</th><th>Gain Factor</th><th>Input Voltage Range</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>±10V</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>±5V</td></tr>
<tr><td>1</td><td>0</td><td>4</td><td>±2.5V</td></tr>
<tr><td>1</td><td>1</td><td>8</td><td>±1.25V</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
<tr><td>1</td><td>ENA</td><td>Single-Ended Channel A / Differential Channel:
Enable the ADC Channel for the sequencer
0 = Sequencer will pass over the ADC Channel
1 = Sequencer converts the ADC Channel and updates the ADC Data in the Sequencer Data RAM at the end of the sequence.
If SE/DIFF = '1', this bit enables the differential channel. Example: If only channel 1, channel 2 and channel 8 are enabled, only the three ADC RAM locations for channel 1, channel 2 and channel 8 are updated at the end of the sequence.
The user must only read these three ADC RAM locations then.</td><td>R/W</td><td>0</td></tr>
</table>

Bit	Symbol	Description	Access	Power-up Value
0	SE/DIFF	Single/Differential Mode Control 0 = Single-ended mode 48 single-ended channels available 1 = Differential mode 24 differential channels 1 to 24 available Mixed mode is possible. E.g. channel 1 to channel 8 selected as differential inputs (equivalent to single-ended inputs 1-16), and channel 17 to channel 48 as single-ended input channels.	R/W	0

Figure 5-10: Sequencer Instruction RAM

The Sequencer Instruction RAM is not cleared by a reset. Be sure to set up the entire Sequencer Instruction RAM if it is used after a reset.

5.3 Additional Registers

5.3.1 Interrupt Status Register INTSTAT (Address 0x09)

Bit	Symbol	Description	Access	Reset Value
7:3	-	Reserved Write: don't care Read: always reads as '0'	R	0
2	SEQ READY	Sequencer Interrupt Pending Flag (bit is controlled by the sequencer logic) If sequencer interrupts are enabled (SEQCONT register bit 1 set to '1') and a sequencer interrupt is pending (any of the SEQSTAT register bits [3:0] is '1') the sequencer interrupt pending flag is read as '1'. The interrupt is cleared by writing '1' to the corresponding status bits in the SEQSTAT register.	R/W	0
1	SETTL READY	SETTL_READY Interrupt Flag (bit is controlled by the settling time controller) If interrupts are enabled (CONTREG register bit 10 is set to '1') and *Automatic Settling Time Mode* is OFF (CONTREG register bit 8 is set to '0') this interrupt is generated, if the settling time is expired. The interrupt is cleared by writing '1' to this bit.	R/W	0
0	ADC READY	ADC_READY Interrupt Flag (bit is controlled by the ADC controller) If interrupts are enabled (CONTREG register bit 11 is set to '1') this interrupt is generated, if a data conversion is done. The interrupt is cleared by writing '1' to this bit.	R/W	0

Figure 5-11: Interrupt Status Register

5.3.2 Interrupt Vector Register IVEC (Address 0x11)

Bit	Symbol	Description	Access	Reset Value
7:0	IVEC	Interrupt Vector	R/W	0

Figure 5-12: Interrupt Vector Register

5.4 Memory Addressing

In *Sequencer Mode* the converted ADC data is accessible in the IP Memory Space.

5.4.1 Sequencer Data RAM SDRAM0-47 (Offset 0x00 to 0x5E)

The Sequencer Data RAM is a 48 x 16 bit wide RAM storing the converted data values.

Address	Symbol	Description	Size (Bit)	Access
0x00… 0x5E	SDRAM1- 48	Sequencer Data RAM	48 x 16	R

Figure 5-13: Sequencer Data RAM

Each channel has its own ADC Data location.

Address	Symbol	Description	Size (Bit)	Access
0x00	SDRAM1	Differential Channel 1 / Single-Ended Channel 1	16	R
0x02	SDRAM2	Single-Ended Channel 2	16	R
0x04	SDRAM3	Differential Channel 2 / Single-Ended Channel 3	16	R
0x06	SDRAM4	Single-Ended Channel 4	16	R
…	…	…	…	…
0x2C	SDRAM23	Differential Channel 12 / Single-Ended Channel 23	16	R
0x2E	SDRAM24	Single-Ended Channel 24	16	R
0x30	SDRAM25	Differential Channel 13 / Single-Ended Channel 25	16	R
0x32	SDRAM26	Single-Ended Channel 26	16	R
…	…	…	…	…
0x58	SDRAM45	Differential Channel 23 / Single-Ended Channel 45	16	R
0x5A	SDRAM46	Single-Ended Channel 46	16	R
0x5C	SDRAM47	Differential Channel 24 / Single-Ended Channel 47	16	R
0x5E	SDRAM48	Single-Ended Channel 48	16	R

Figure 5-14: Sequencer Data RAM locations

Note that only enabled channels in the Sequencer Instruction RAM are updated. Channels that are not enabled in the Sequencer Instruction RAM are not updated and may contain invalid data from former conversions.

The Sequencer Data RAM is not cleared by a reset and may contain invalid data from former conversions.

Word accesses are recommended to read this registers.

6 Operating Modes

There are two modes of operation: the *Manual Mode*, with little or none support through automation, and the *Sequencer Mode*, with large support through automation.

- Manual Mode

  In this mode, the converter operation relies on the user. The channel and gain are set by the user, and the user has large influence on the converter operation.

  Use this mode to convert specific channels and to control conversion timing or to read a channel repeatedly without the need to await the settling time.

- Sequencer Mode

  In this mode almost everything is automated and the converter operation is transparent to the user.

  Use this mode to convert all channels at specific time intervals, or to have always current data available.

6.1 Manual Mode

The *Manual Mode* is useful, if direct control of converter operation is needed. Setup the desired channel and gain by writing to the CONTREG register. If the *Automatic Settling Time Control* is deactivated, the user has to wait until the ADC_SETTL flag reads '0'. Then the conversion can be started by writing to the CONVERT register. If the *Automatic Settling Time Control* is activated, the conversion starts automatically after the settling time has elapsed.

It is possible to select the next channel and/or gain by writing to the CONTREG register immediately after the write to the CONVERT register. Then the conversion and the settling time will proceed simultaneously.

The conversion data is available in the DATAREG register if the ADC_BUSY flag in the STATREG register reads as '0'.

If interrupts are enabled, two interrupts will be generated: the first interrupt is generated if the settling time has elapsed (and the *Automatic Settling Time Control* is deactivated); the second interrupt is generated if the conversion has finished. Using the interrupts exempts from polling the ADC_SETTL and ADC_BUSY flags.

Without Automatic Settling Time Control:

→ Setup the conversion in the ADC Control Register

→ Poll for SETTL_BUSY flag

→ After settling time has elapsed, write to the CONVERT register to start conversion

→ Poll for ADC_BUSY flag

→ After conversion time has elapsed, read conversion data in the ADC Data Register

With Automatic Settling Time Control:

→ Setup the conversion in the ADC Control Register

→ Poll for SETTL_BUSY flag

→ Poll for ADC_BUSY flag

→ After conversion time has elapsed, read conversion data in the ADC Data Register

6.2 Sequencer Mode

The *Sequencer Mode* is very useful for periodic measurements or to always provide actual conversion data. The sequencer converts all enabled ADC channels and stores the results in the Sequencer Data RAM. After a programmable time the sequencer repeats the sequence.

To use the sequencer, all channels must be configured for the sequence in the Sequencer Instruction RAM. In the Sequencer Instruction RAM the channels are enabled for the sequence, and the gain and the mode (single-ended or differential) are selected.

Once the sequencer is started, all enabled channels are converted and the results are stored in the Sequencer Data RAM. If the last sequencer instruction has been completed, the Data Available Flag DATA_AV in the Sequencer Status Register (SEQSTAT) is set to '1' and, if enabled, an interrupt request will be asserted. The user can now read the ADC data from the Sequencer Data RAM. Afterwards the DATA_AV flag must be cleared by writing a '1' to the Sequencer Status Register SEQSTAT bit 0.

Only the enabled channels are updated; not enabled channels in the Sequencer Instruction RAM are not updated and may contain invalid data from former conversions.

The repeat frequency of the sequencer can be programmed in the Sequencer Timer Register. The Sequencer Timer is programmable from 100µs to 6.5535s in steps of 100µs. Whenever the timer reaches the programmed value the sequencer starts a new sequence.

A special function is the *Sequencer Continuous Mode*. It is activated if the Sequencer Timer Register is set to 0x0000. In this mode the sequencer immediately starts a new sequence if the actual sequence has been completed. If the sequencer is in *Sequencer Continuous Mode*, the user can read valid data from the Sequencer Data RAM at any time. The Sequencer Data RAM locations of the enabled ADC channels are updated with every sequence.

If the *Sequencer Continuous Mode* is active, the Data Overflow Error Flag DATA_OF_ERROR is deactivated and always reads as '0'. Clearing the Data Available Flag DATA_AV is not necessary in the *Sequencer Continuous Mode*, but it is recommended to monitor the completion of the sequences.

The update rate depends on the number of enabled channels:

Update Rate = 8µs · number of enabled channels

6.2.1 Sequencer Errors

If the sequencer detects an error, it will stop after the last instruction and sets the corresponding error flag in the Sequencer Status Register SEQSTAT.

Error	Description	Sequencer Action	User Action
Data Overflow Error	Error occurs if the sequencer has new data to store but the user has not yet acknowledged that the data from the previous sequence has been read out. (Sequencer Timer Mode only)	Sequencer stops after the last instruction is done. Data Overflow Error Flag is set. If it is enabled, an interrupt request will be asserted.	Write a '1' to the Sequencer Status Register bit 1. Make sure the Sequencer Data is read and acknowledged within the programmed sequence time. Start sequencer again.
Timer Error	Error occurs if the programmed sequencer time is shorter than the sequence itself. (Sequencer Timer Mode only)	Sequencer stops after the last instruction is done. Timer Error Flag is set. If it is enabled, an interrupt request will be asserted.	Write a '1' to the Sequencer Status Register bit 2. Program a longer sequence time. Start sequencer again.
Instruction RAM Error	Error occurs if no channel is enabled for the sequence (bit 1 or bit 4 of sequencer Instruction RAM word) and the sequencer is started.	Sequencer stops after the last instruction is done. Instruction RAM Error Flag is set. If it is enabled, an interrupt request will be asserted.	Write a '1' to the Sequencer Status Register bit 3. Correct the Sequencer Instruction RAM setting. Start sequencer again.

Figure 6-1 : Sequencer Errors

If the Sequence Timer Register is set to 0x0000 (Sequencer Continuous Mode) the sequencer ignores the data overflow. The Data Overflow Error Flag is always read as '0' in this mode.

6.3 Application Examples

All following examples use interrupts. The use of interrupts can be replaced by polling the according status flags in the ADC Status Register or the Sequencer Status Register.

6.3.1 Fastest Conversion of an Arbitrary Single Channel

→ Program the desired channel and gain in the ADC Control Register CONTREG. Activate the Automatic Settling Time Control (ASTC = '1') and the IRQ after conversion (IRQC = '1')

→ The channel is now converted without any further user action. After completion of the conversion an interrupt is issued which signals that the conversion data is available in the DATAREG Register

→ Acknowledge the interrupt in the Interrupt Status Register INTSTAT (ADC_READY = '1') and read DATAREG

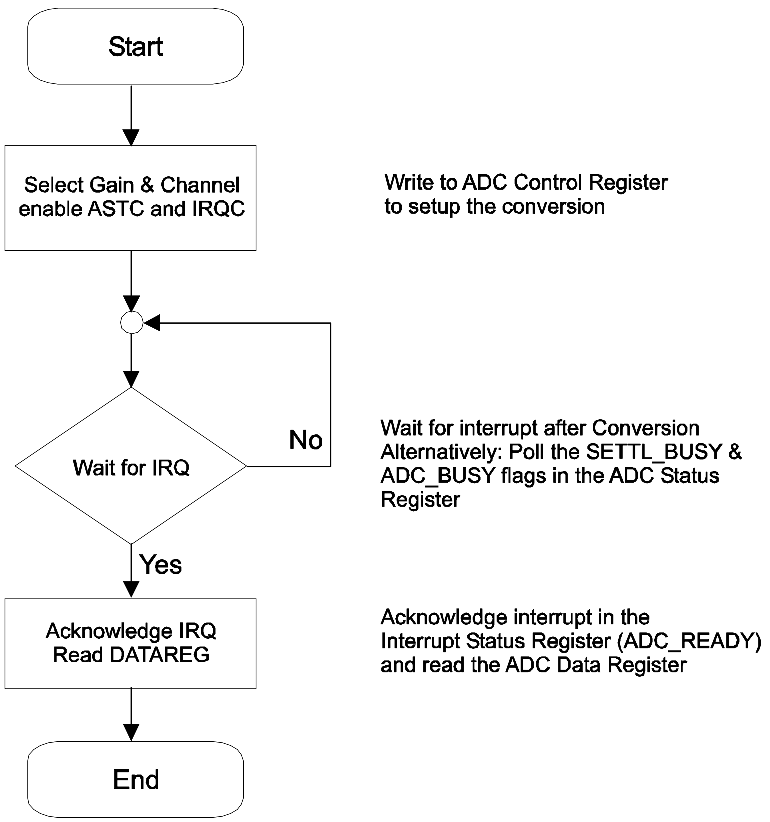

Figure 6-2 : Flow of fastest conversion of an arbitrary single channel

Conversion time is approx. 10.5µs.

6.3.2 Fastest Conversion of a Specific Single Channel

→ Program the ADC Control Register with desired channel and gain, and activate the IRQ after Settling Time (IRQS = '1'), and the IRQ after conversion (IRQC = '1').

- → If the IRQ after settling time is issued, the channel is ready for conversion. Write to the CONVERT register and acknowledge the interrupt in the Interrupt Status Register INTSTAT (SETTL_READY = '1').
- → After completion of the conversion an interrupt is issued which signals that the conversion data is available in the DATAREG register.
- → Write again to the CONVERT register to start the next conversion of this channel, acknowledge the interrupt in the Interrupt Status Register INTSTAT (ADC_READY = '1') and read DATAREG.

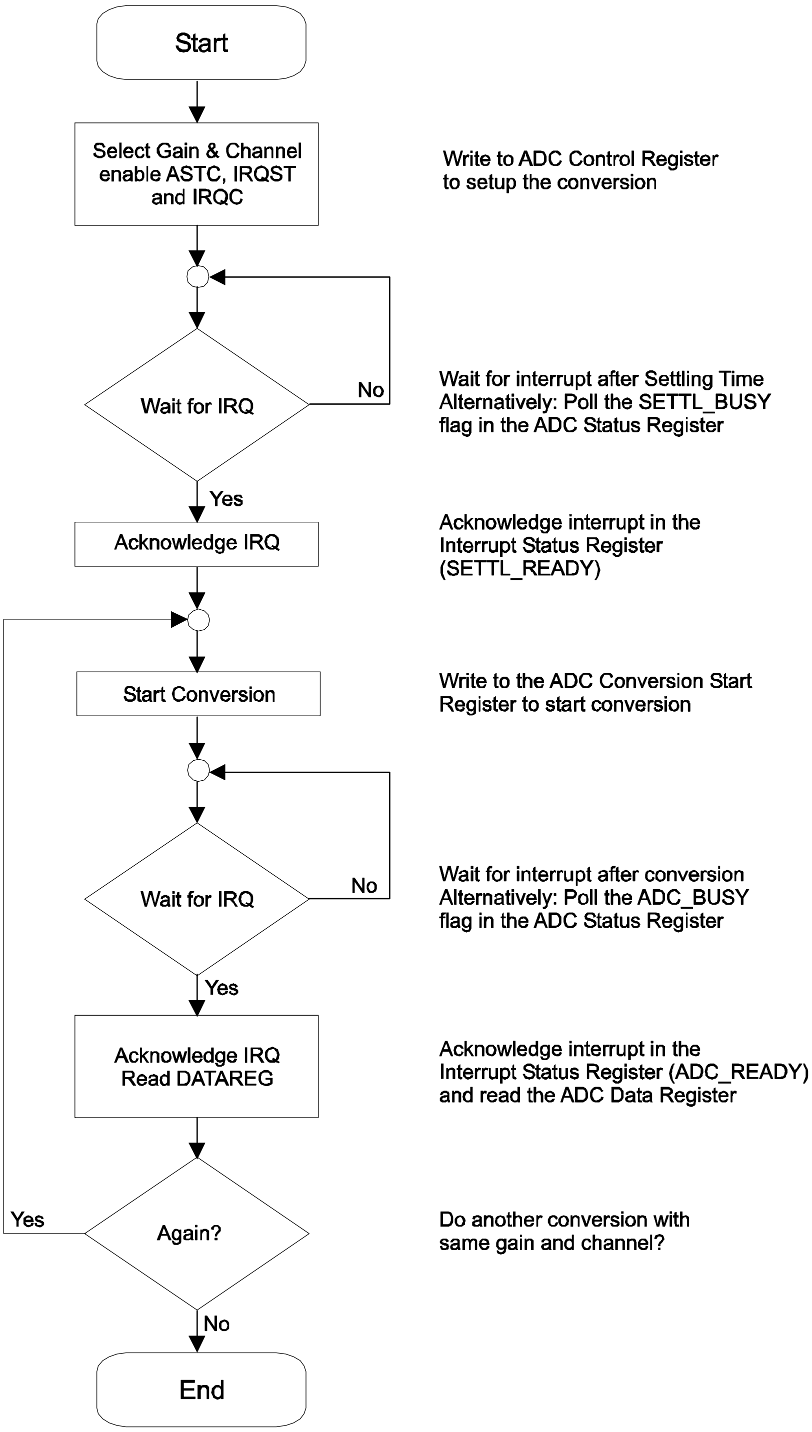

Figure 6-3 : Flow of fastest conversion of a specific single channel

Conversion time is approx 2.5µs, as long as neither the channel nor the gain is changed.

6.3.3 Periodic Conversion of Multiple Channels

→ Activate the channels to be converted and program the gain in the Sequencer Instruction RAM.

→ Set the sequencer period in the Sequencer Timer Register SEQTIMER.

→ Enable the Sequencer Interrupt SEQ_INT_ENA and start the sequencer in the Sequencer Control Register SEQCONT.

→ After completion of the sequence an interrupt is issued which signals that the conversion data is available in the Sequencer Data RAM.

→ Acknowledge the interrupt in the Interrupt Status Register INTSTAT (SEQ_READY = '1'), clear the DATA_AV flag in the Sequencer Status Register and read the Sequencer Data RAM.

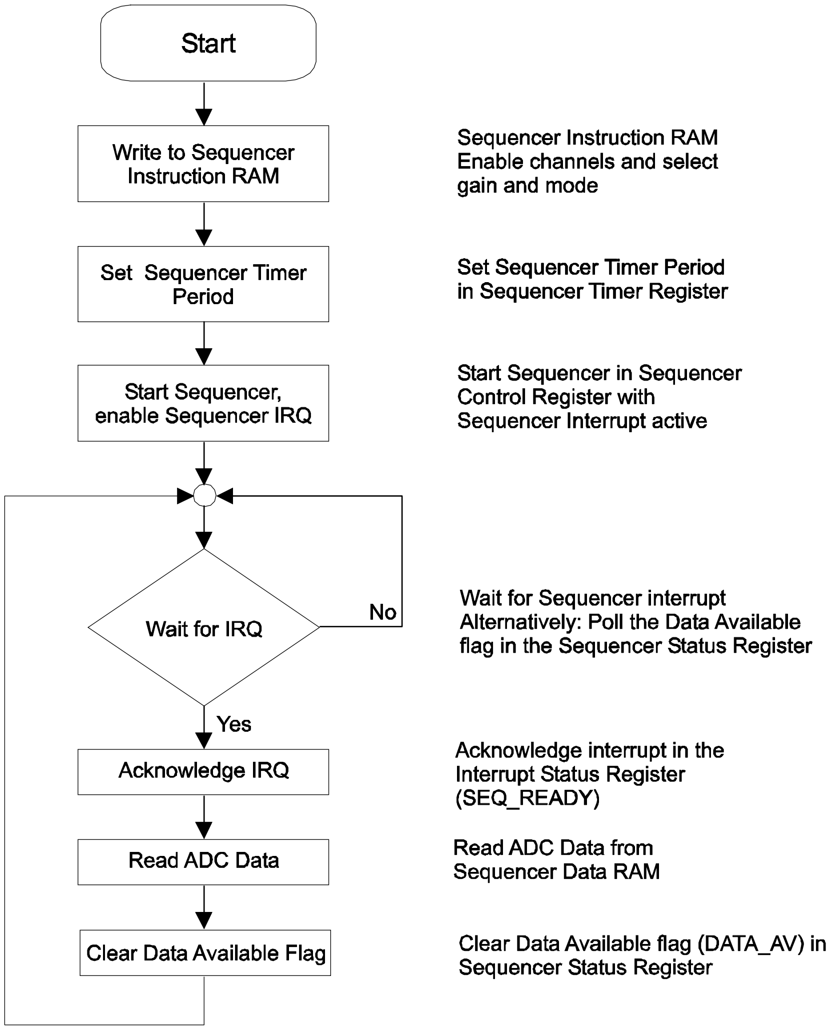

Figure 6-4 : Flow of periodic conversion of multiple channels

6.3.4 Continuous Conversion of Multiple Channels

→ Activate the channels to be converted and program the gain and mode of these channels in the Sequencer Instruction RAM.

→ Set the Sequencer Timer Register SEQTIMER to 0x0000.

→ Start the sequencer in the Sequencer Control Register SEQCONT.

→ Read the data from the Sequencer Data RAM as needed.

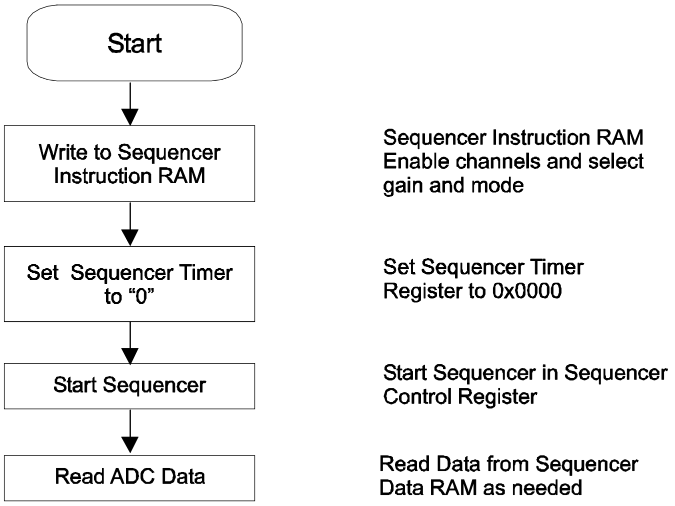

Figure 6-5 : Flow of continuous conversion of multiple channels

7 Pin Assignment – I/O Connector

Pin	Differential mode	Single-ended mode
1	ADC Input 1+	ADC Input 1
2	ADC Input 1-	ADC Input 2
3	ADC Input 2+	ADC Input 3
4	ADC Input 2-	ADC Input 4
5	ADC Input 3+	ADC Input 5
6	ADC Input 3-	ADC Input 6
7	ADC Input 4+	ADC Input 7
8	ADC Input 4-	ADC Input 8
9	ADC Input 5+	ADC Input 9
10	ADC Input 5-	ADC Input 10
11	ADC Input 6+	ADC Input 11
12	ADC Input 6-	ADC Input 12
13	ADC Input 7+	ADC Input 13
14	ADC Input 7-	ADC Input 14
15	ADC Input 8+	ADC Input 15
16	ADC Input 8-	ADC Input 16
17	ADC Input 9+	ADC Input 17
18	ADC Input 9-	ADC Input 18
19	ADC Input 10+	ADC Input 19
20	ADC Input 10-	ADC Input 20
21	ADC Input 11+	ADC Input 21
22	ADC Input 11-	ADC Input 22
23	ADC Input 12+	ADC Input 23
24	ADC Input 12-	ADC Input 24
25	GND	GND
26	GND	GND
27	ADC Input 13+	ADC Input 25
28	ADC Input 13-	ADC Input 26
29	ADC Input 14+	ADC Input 27
30	ADC Input 14-	ADC Input 28
31	ADC Input 15+	ADC Input 29
32	ADC Input 15-	ADC Input 30
33	ADC Input 16+	ADC Input 31
34	ADC Input 16-	ADC Input 32
35	ADC Input 17+	ADC Input 33
36	ADC Input 17-	ADC Input 34
37	ADC Input 18+	ADC Input 35
38	ADC Input 18-	ADC Input 36
39	ADC Input 19+	ADC Input 37

Pin	Differential mode	Single-ended mode
40	ADC Input 19-	ADC Input 38
41	ADC Input 20+	ADC Input 39
42	ADC Input 20-	ADC Input 40
43	ADC Input 21+	ADC Input 41
44	ADC Input 21-	ADC Input 42
45	ADC Input 22+	ADC Input 43
46	ADC Input 22-	ADC Input 44
47	ADC Input 23+	ADC Input 45
48	ADC Input 23-	ADC Input 46
49	ADC Input 24+	ADC Input 47
50	ADC Input 24-	ADC Input 48

Figure 7-1 : Pin Assignment I/O Connector

8 Important Notes

8.1 Dummy Conversions after Power-up

After power-up the ADC's logic will be in a random state and may not perform correctly. This has two consequences:

1. The first conversion results are not valid and should be ignored.
2. The ADC starts in a mode that prevents a correct start of the sequencer.

Therefore, two dummy conversions are required after each power-up, whose results should be ignored.

Use the ADC Conversion Start Register (CONVERT) Register to perform the dummy conversions.

If the sequencer is to be used, these two dummy conversions are absolutely necessary.

If one of our software drivers is used, these two dummy conversions are already included.

8.2 Open Multiplexer Inputs

Unused Multiplexer inputs can pick up stray signals which are injected into the device's substrate. This turns on spurious substrate devices which badly degrade the performance of the whole multiplexer device.

Make sure that all unused analog input pins are tied to the analog ground signal level (or any other valid signal level within the analog input voltage range). This is required even if the unused channels are turned off by software.