

Application Note



Single-phase Energy Meter Application

Watt-hour meter is the measurement of electric energy measurement tool, the relationship between the measurement of fair use of electricity, with the development of science and technology as well as the microprocessor in the power meter in the application of high precision power meter is moving, multi-functional, low-cost, long-range wireless intelligent meter reading, such as direction.

This article describes the use of NEC ALL FLASH Products developed Energy Meter uPD78F9224 control application example.

Document No. NECEC-OS-SA-AN-0006-01
Date Published December 2008

© NEC Electronics Corporation 2008

Content

CHAPTER I SUMMARY	5
1.1 SINGLE-PHASE ENERGY METER WORKING PRINCIPLE	5
1.2 SYSTEM DESIGN	6
CHAPTER II MICROCONTROLLER	8
2.1 FUNCTIONAL OVERVIEW	9
2.2 STRUCTURE DIAGRAM	11
2.3 UPD78F9224 THE CPU STORAGE MAPPING TABLE	12
2.4 THE MAIN FUNCTIONS USED TO INTRODUCE	13
2.4.1 Watchdog timer.....	13
2.4.2 Power-Clear Circuit.....	26
2.4.3 8-bit timer 80 as the basic time interval timer.....	30
2.4.4 The Notes of 8-bit timer 80	34
2.4.5 8-bit timer H1 as a square-wave output	35
2.4.6 Optional Bytes	39
CHAPTER III HARDWARE DESIGN	44
3.1 SYSTEM BLOCK DIAGRAM	44
3.2 PIN MAPPING TABLE	45
3.3 CONTROL CIRCUIT POWER-METER	46
3.3.1 Power supply circuit.....	46

3.3.2 Display circuit.....	47
3.3.3 Measurement Acquisition Circuit	48
3.3.4 Infrared Communication Circuit	50
3.3.5 485 Communications Circuit	51
3.3.6 Port detection circuit	52
3.3.7 I ² C and EEPROM communications circuit	53
3.4 MACHINE SCHEMATIC	54
4.1 CONTROL OPERATION DISPLAY INTERFACE	55
4.1.1 LCD display interface reference chart is as follows :	55
4.1.2 Can be set up display	56
4.2 FUNCTIONAL REQUIREMENTS.....	57
4.2.1 Basic Functions	57
4.3 EXTENSIONS FUNCTION	57
4.3.1 Communication Functions	57
4.3.2 Security	58
4.3.3 Programming function	59
4.3.4 Meter Reading functions:	60
4.4.5 Automatic School Table Function	61
CHAPTER V THE SOFTWARE FLOW CHART	63
5.1 PROCEDURES FOR THE TOTAL PROCESS MODULE	63
5.2 CYCLE THE MAIN MODULE.....	64
5.3 POWER-PROCESSING MODULE.....	67

5.4 DISPLAY PROCESSING MODULE	70
5.5 I ² C MODULE DEAL	76
5.6 INFRARED COMMUNICATION MODULE	83
5.7 485 COMMUNICATION MODULE.....	88
5.8 FRAME COMMUNICATION MODULE	92
5.9 ORDER PROCESSING MODULE.....	95
5.10 4MS TIMER TM80 INTERRUPT REGULAR PROCESSING MODULE...	96
5.11 PORT DETECTION MODULE	99
5.12 SOFTWARE SCHOOL TABLE MODULE.....	100
5.13 CONSTANT POWER PORT DETECTION MODULE	104
5.14 HIGH-FREQUENCY PULSE PROCESSING MODULE.....	105
5.15 LOW-FREQUENCY PULSE PROCESSING MODULE.....	106
5.16 POWER + = 0.01 DEGREES OF THE PROCESSING MODULE	108
CHAPTER VI THE LIST OF PROGRAMS.....	110
6.1 VARIABLE NAMING RULES	110
6.2 VARIABLE LIST.....	111

Chapter I Summary

Watt-hour meter is the measurement of electric energy measurement tool, the relationship between the measurement of fair use of electricity, with the development of science and technology as well as the microprocessor in the power meter in the application of high precision power meter is moving, multi-functional, low-cost, long-range wireless intelligent meter reading, such as direction.

This article describes the use of NEC ALL FLASH Products developed Energy Meter uPD78F9224 control application example.

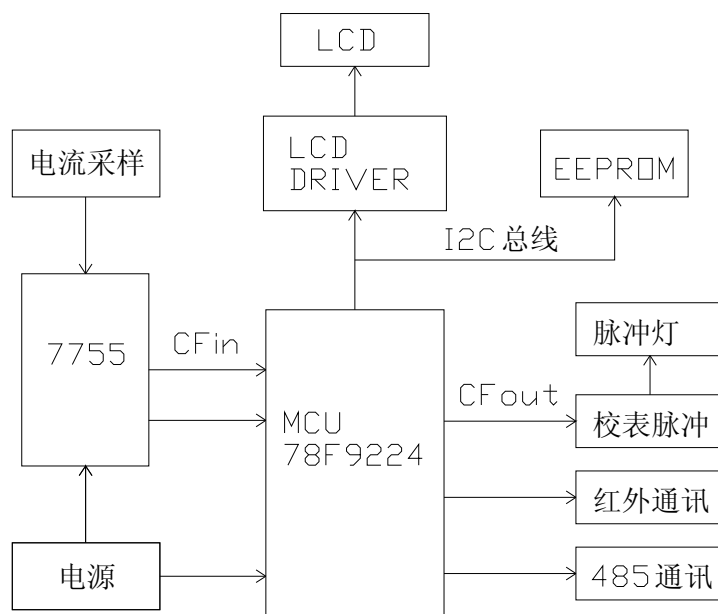
1.1 Single-phase energy meter working principle

Watt-hour meter working principle is: 7755 samples voltage and current signals, the output power line and load power pulse CF; single-chip high-frequency pulses of electrical energy of the CF treatment, the output pulse signal for the pulse table lamps and school use, Single-chip signal through the CF treatment, the calculated consumption of electricity, to the LCD driver, in the LCD display, at the same time, write EEPROM; EEPROM in addition to electricity consumption information to preserve, there are a table, such as information, which can be infrared and 485 Reading copied

and settings can also be displayed in the LCD.

Schematic diagram is shown below :

Figure 1-1 Schematic energy meter work



1.2 System Design

The Application Notes in the energy meter applications include the following major functional modules: the measurement module, I²C module, communication module, order processing module, LCD display module, and so on .

The energy meter application program control flow is: power system, the controller started to work, first of all, the first detection of power supply voltage is greater than 4.3V, if more than on the CPU is initialized from the EEPROM read data, read to the RAM variable area, and then entered the main circle, in the main loop, LCD in accordance with the procedures set by the state of display;

Singlechip once every 4ms inquiries P22, P23 I, for electric energy metering system to determine the corresponding energy constant; INTP0 interruption of the mouth Detection of rising edge of the energy pulse counting, in accordance with the system detects a constant power for electric energy metering; RXD moment to respond to external falling edge, the implementation of 485 communications; infrared INTP2 interrupted waiting for falling edge detection, at any time to respond to infrared communication; and INTP3 ordinary I/O port mode, each query detection 4ms time, if indeed there are external programming I shorted on the open-enabled programming, hardware programming events permit; P123 also query an external every 4ms formatting button, if press, will implement the format command EEPROM; pulsed light, communications, light, display symbols such as the corresponding state of the corresponding instructions in accordance with the procedure showed that pulsed light to eliminate Always 80ms recovery, communications, light and liquid crystal display on the Newsletter sign-liang 1s after the eradication, programming shorted until programming symbols disappear after I disconnect, the system in such a detection process cycle.

The chosen microcontroller is : NEC78F9224, the next chapter of its detail .

Chapter II microcontroller

The applications of microcontrollers from NEC ALL FLASH products 78K0S/KB1 + series uPD78F9224. NEC's products are ALL FLASH alternative MASK for NEC Products introduced a new 8bit general-purpose CPU products, is designed to overcome the MASK Product manufacturers can only be carried out by the curing process, and after the curing process should not carry out further revision of shortcomings.

NEC's Product ALL FLASH using the world's leading 0.15um SST Flash technology, performance is greatly improved, relative previous MASK products have a wider range of voltage range and speed, lower power consumption, higher reliability, more strong adaptability, low-end product coverage areas and high-end general-purpose CPU dedicated areas, such as automotive electronics fields, according to different users and different applications to provide different products ALL FLASH.

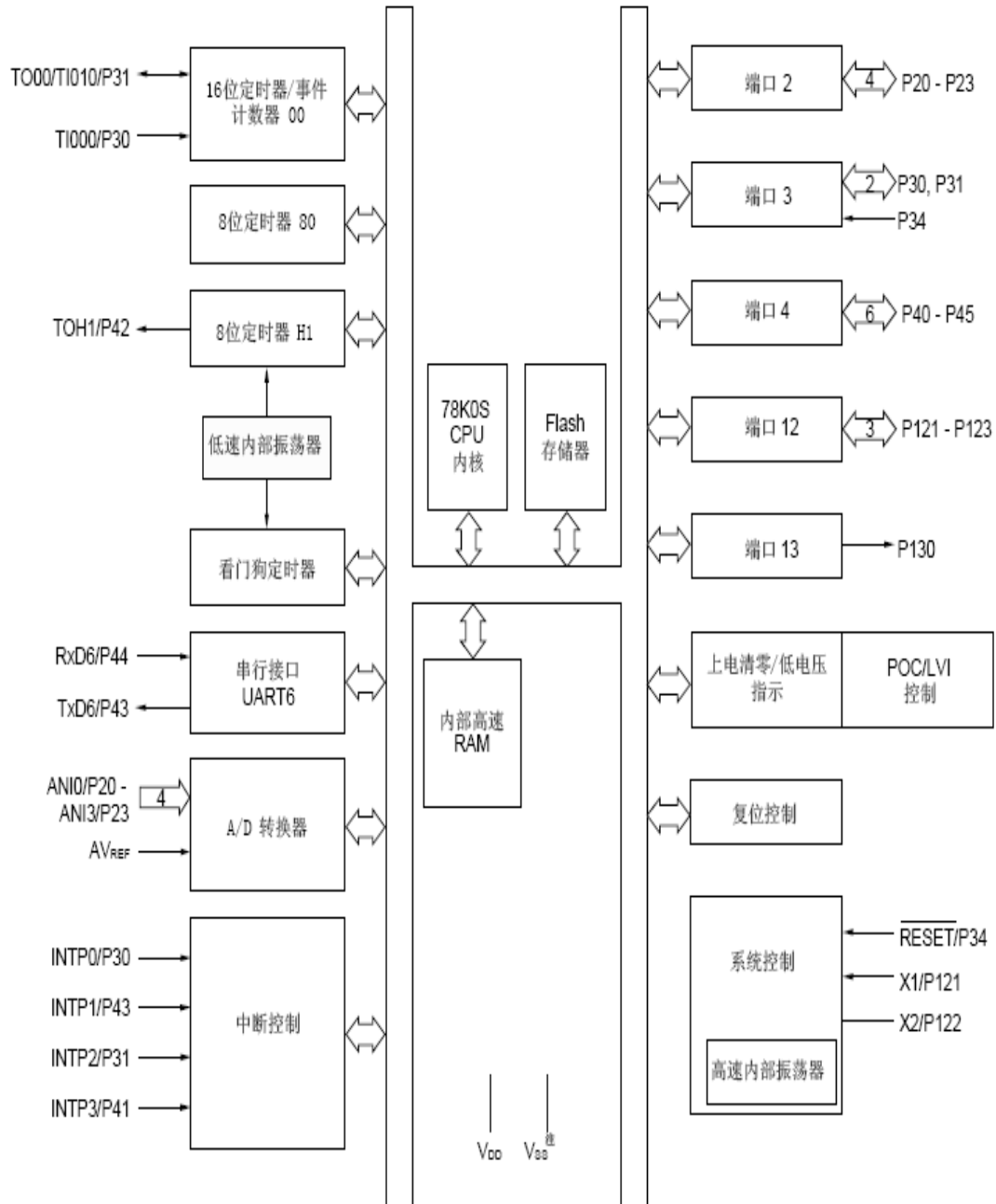
The following application-based program used by 78K0S/KA1 + Products of a brief introduction, the detailed features of the product please refer to the product user manual.

2.1 Functional overview

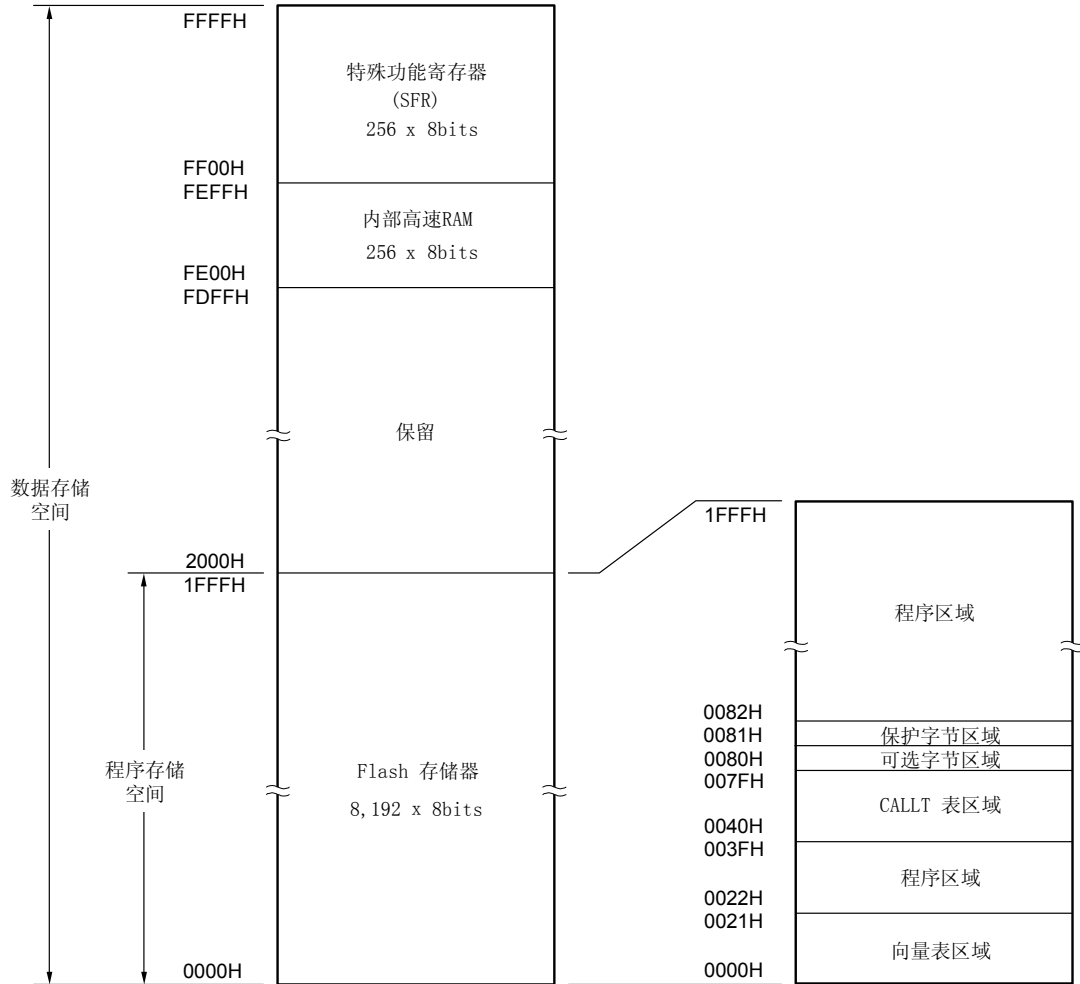
Item		μPD78F9222	μPD78F9224
Internal memory	Flash memory	4 KB	8 KB
	High-speed RAM	256 Bytes	
Memory space		64 KB	
X1 input clock (oscillator frequency)		Crystal / ceramic / external clock input: 10 MHz ($V_{DD} = 2.0 \sim 5.5$ V)	
Ring-OSC Clock	High-speed (oscillator frequency)	Internal Ring-OSC: 8 MHz (typical value)	
	Low-speed (TMH1 and WDT)	Internal Ring-OSC: 240 kHz (typical value)	
General Register		8 Bit × 8 Register	
Shortest instruction execution time		0.2 μs/0.4 μs/0.8 μs/1.6 μs/3.2 μs (X1 input clock: $f_X = 10$ MHz)	
I/O Port		Total : 17 Pin CMOS I/O : 15 Pin CMOS Input : 1 Pin CMOS Output : 1 Pin	
Timer		<ul style="list-style-type: none"> • 16-bit timer / event counter : 1 Ch • 8-bit timer (Timer H1) : 1 Ch • 8-bit timer (Timer 80) : 1 Ch • Watchdog Timer : 1 Ch 	
		Timer output 2-pin (PWM: 1 pin)	
A/D converter		10-bit resolution × 4 ch	
Serial interface		Support the LIN Bus UART mode : 1 ch	
Vector Interrupt Sources	External	4	
	internal	9	
Reset		<ul style="list-style-type: none"> • Reset using RESET pin • The use of an internal watchdog timer reset • The use of POC to conduct an internal reset • The use of low-voltage detector to conduct an internal reset 	
Supply voltage		$V_{DD} = 2.0 \sim 5.5$ V ^註	
Working ambient temperature		$T_A = -40 \sim +85^\circ\text{C}$	
Package		20-pin plastic SSOP	

Note Because the power-Clear (POC) test voltage (V_{POC}) at $2.1 \text{ V} \pm 0.1 \text{ V}$ between, so this product is the voltage range $2.2 \sim 5.5 \text{ V}$.

2.2 Structure diagram



2.3 uPD78F9224 The CPU Storage Mapping Table



2.4 The Main Functions Used To Introduce

2.4.1 Watchdog timer

2.4.1.1 Watchdog timer function

Watchdog timer for detecting non-expected program cycle. If detected in such a program cycle, will generate an internal reset signal. If you have a watchdog timer reset, then reset control register mark (RESF) section 4 (WDTRF) buy one.

The following table for the watchdog timer detection time of the cycle :

Cycle detection time	
Low-speed Ring-OSC clock operation	During system clock operation
$211/f_{RL}$ (4.27 ms)	$213/f_X$ (819.2 μ s)
$212/f_{RL}$ (8.53 ms)	$214/f_X$ (1.64 ms)
$213/f_{RL}$ (17.07 ms)	$215/f_X$ (3.28 ms)
$214/f_{RL}$ (34.13 ms)	$216/f_X$ (6.55 ms)
$215/f_{RL}$ (68.27 ms)	$217/f_X$ (13.11 ms)
$216/f_{RL}$ (136.53 ms)	$218/f_X$ (26.21 ms)
$217/f_{RL}$ (273.07 ms)	$219/f_X$ (52.43 ms)
$218/f_{RL}$ (546.13 ms)	$220/f_X$ (104.86 ms)

Note

1. f_{RL} : Low-speed Ring-OSC clock oscillation frequency .
2. f_X : System clock oscillation frequency.
3. Figure in brackets correspond to the value of $f_{RL} = 480$ kHz (MAX.), $f_X = 10$ MHz.

Watchdog timer mode of operation under low-speed-chip Ring-OSC clock switch option byte settings.

The following table is optional bytes of set-up and watchdog timer mode of operation :

	Optional byte setting	
	Low-speed Ring-OSC clock can not be stopped	Low-speed Ring-OSC clock can be stopped by software
Watchdog timer clock source	fixed at f_{RL} ^{Note1}	<ul style="list-style-type: none"> • Can be select by software (f_X, f_{RL} or stop) • reset: f_{RL}
After the reset operation	Maximum time interval to start the operation ($218/f_{RL}$)	Maximum time interval to start the operation ($218/f_{RL}$)
Operation mode selection	Time interval can only be changed one time	Clock selection / interval can only be changed one time
Features	Watchdog timer can not be stopped	Watchdog timer can be stopped ^{Note2}

Note

1. Can not stop when the power supply low-speed Ring-OSC oscillator (except during reset).

2. If the watchdog timer clock source is different, the watchdog timer to stop the clock supply of the necessary conditions are also different.

<1> If the clock source is f_X , then the following conditions are met when the watchdog timer to stop the supply of the clock.

- When f_X been stopped.
- In HALT/STOP mode.

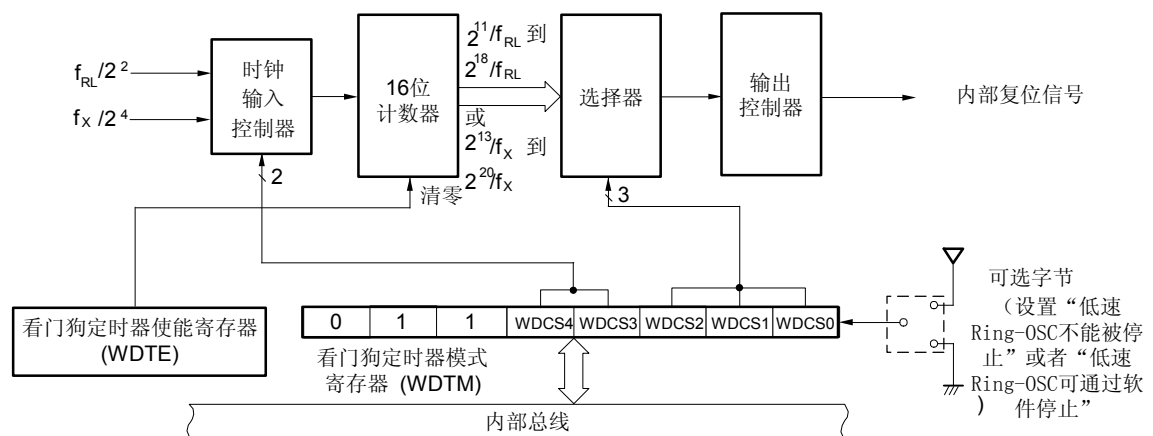
- In the oscillator stable time.
- <2> If the clock source is f_{RL} , then the following conditions are met when the watchdog timer to stop the supply of the clock.
- If the CPU clock is f_x and STOP in the implementation of instructions by the software to stop f_{RL} .
 - In HALT/STOP mode.

2.4.1.2 Watchdog timer configuration

Watchdog timer from the following hardware components.

Item	Configuration
Control register	Watchdog timer mode register (WDTM) Watchdog timer enable register (WDTE)

The next photo shows the block diagram of watchdog timer :



2.4.1.3 Watchdog Timer control register

Watchdog timer control register by the following two:

- Watchdog timer mode register (WDTM)
- Watchdog timer enable register (WDTE)

(1) Watchdog timer mode register (WDTM)

The register set watchdog timer overflow time and operation of the clock.

The register can be 8-bit memory operation instruction set, and can be read many times, but the reduction can only be written after the release of one meeting. Reset input of the register Purchase 67H.

The photo shows the next watchdog timer mode register (WDTM) format:

地址: FF48H 复位后: 67H 读/写
符号

	7	6	5	4	3	2	1	0
WDTM	0	1	1	WDCS4	WDCS3	WDCS2	WDCS1	WDCS0

WDCS4 Note1	WDCS3 Note1	Operation clock selection
0	0	Low-speed Ring-OSC clock (f_{RL})
0	1	System clock (f_X)
1	×	Stop watchdog timer

WDCS2 Note2	WDCS1 Note2	WDCS0 Note2	Overflow time setting	
			During low-speed Ring-OSC clock operation	During system clock operation
0	0	0	211/f _{RL} (4.27 ms)	213/f _X (819.2 μs)
0	0	1	212/f _{RL} (8.53 ms)	214/f _X (1.64 ms)
0	1	0	213/f _{RL} (17.07 ms)	215/f _X (3.28 ms)
0	1	1	214/f _{RL} (34.13 ms)	216/f _X (6.55 ms)
1	0	0	215/f _{RL} (68.27 ms)	217/f _X (13.11 ms)
1	0	1	216/f _{RL} (136.53 ms)	218/f _X (26.21 ms)
1	1	0	217/f _{RL} (273.07 ms)	219/f _X (52.43 ms)
1	1	1	218/f _{RL} (546.13 ms)	220/f _X (104.86 ms)

Note

1. If the optional byte designated as "low-speed Ring-OSC can not be stopped", then should not the setting up of such. Regardless of the value written into the DR, will choose low-speed Ring-OSC clock.
2. With the greatest reduction and the release cycle (WDCS2, 1,0 = 1,1,1).

Cautions

1. The first bit 7,6,5 and 0,1, respectively, set to 1 (when the adoption of an optional byte select "Can not stop the low-speed Ring-OSC clock oscillator," ignore the other values).
2. Reset, only by the eight memory operation instruction to write a WDTM. If you try to write the

second time, it will generate an internal reset signal.

3. Can not use a memory operation command to operate WDTM.

4. When using self-written on the flash memory operation, as the watchdog to provide sufficient time for the overflow (for example, one byte write: Minimum 200ms, delete a block: Minimum 10ms).

Remarks

1. f_{RL} : Low-speed Ring-OSC clock oscillation frequency
2. f_X : System clock oscillation frequency
3. \times : Do not consider
4. The figure in brackets corresponds to the value $f_{RL} = 480 \text{ kHz (max)}$, $f_X = 10 \text{ MHz}$.

(2) The watchdog timer enable register (WDTE)

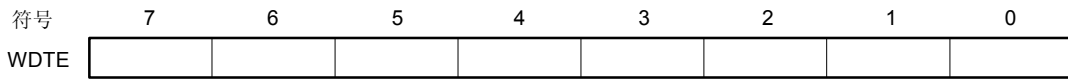
ACH will write WDTE watchdog timer counter can be cleared and re-start the counting operation.

8-bit memory operation by setting the command register.

Reset input of the register Purchase 9AH.

The showing is watchdog timer enable register (WDTE) format :

地址: FF49H 复位后: 9AH 读/写



Note

1. If one is not the value of ACH are written WDTE, will generate an internal reset signal.
2. If you use a memory operation command WDTE operate on, will produce an internal reset signal.
3. WDTE read from the value 9AH (with the written value (ACH) different).

2.4.1.4 Watchdog Timer operation

(A) When i choose from the optional byte as "low-speed Ring-OSC can not be stopped" when the watchdog timer operation

Watchdog timer operation clock is fixed at low-speed Ring-OSC clock.

Reset release, to the maximum cycle (watchdog timer mode register (WDTM) the first bit 2,1,0 for 1 (WDCS2, WDCS1, WDCS0) = 1,1,1) to start operation, the watchdog timer Operation should not be stopped.

Following is reset after the release of the watchdog timer operation.

1. The state after reset release is as follows.

- Clock operation: low-speed Ring-OSC clock
- Cycle: $218/f_{RL}$ (546.13 ms: operating frequency $f_{RL} = 480$

kHz (max))

- Start counting

2. By 8-bit memory operation mode command of the watchdog timer register (WDTM) in the following settings.

- Cycle: using the first 0 to 2 (WDCS2 to WDCS0) settings

3. In the implementation of the above process, will be ACH write WDTE, this counter has been cleared to allow the re-count.

In this mode, even if the implementation of STOP instruction, but also should not stop the watchdog timer operation. For 8-bit timer H1 (TMH1), optional low-speed internal clock frequency of a sub-source as a count, so STOP instruction execution, the watchdog timer overflow before TMH1 can be used for the watchdog timer interrupt request Clear. If there is no implementation of the process, then after STOP instruction execution when the watchdog timer overflow will generate an internal reset signal.

(B) When choosing from the optional byte as "low-speed Ring-OSC can be stopped by software" at the time of watchdog timer operation . Selectable watchdog timer operation clock for the low-speed Ring-OSC clock or system clock.

Reset release, to low-speed Ring-OSC clock cycle of the largest (watchdog timer mode register (WDTM) section 2, para 1 and 0 (WDCS2, WDCS1, WDCS0) = 1,1,1)) to start operation.

Following is reset after the release of the watchdog timer operation :

1. The state after reset release is as follows.
 - Clock operation: low-speed Ring-OSC clock

- Cycle: $218/f_{RL}$ (546.13 ms: operating frequency $f_{RL} = 480$ kHz (MAX.))

- Start counting

2. By 8-bit memory operation mode command of the watchdog timer register (WDTM) to carry out the following settings.

- Operation clock: from the first three and four (WDCS3 and WDCS4) select one of the following clock.

Low-speed Ring-OSC clock (f_{RL})

System clock (f_X)

Watchdog timer operation stopped

- Cycle: from 2 to 0 bit (WDCS2 to WDCS0) settings

3. The implementation of the process, will be ACH write WDTE, this counter has been cleared to allow the re-count.

This mode, the HALT/STOP instruction execution during the watchdog timer operation has been suspended. In the release of HALT/STOP mode, through the use of the HALT/STOP instruction execution WDTM set before the watchdog timer operation clock counter will start again. At this point, the counter has not been cleared, but keep original value.

(C) STOP mode, watchdog timer operation (when the optional

byte select for the "software to stop the clock speed Ring-OSC")

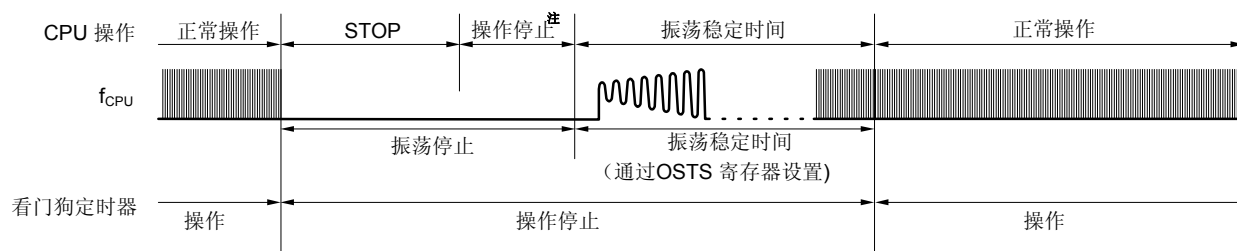
Regardless of the system clock or low-speed Ring-OSC clock, in the implementation of STOP instruction when the watchdog timer to stop counting.

(1) When the watchdog timer operation clock is the peripheral hardware clock (f_x), and the implementation of STOP instruction.

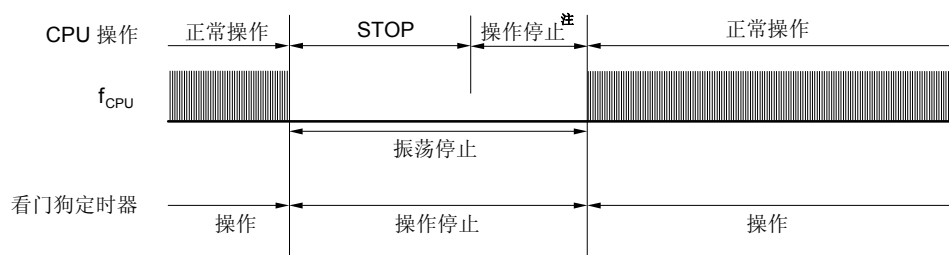
When the implementation of STOP instruction, the watchdog timer to stop the operation. In the release of STOP mode, the operation stopped 34 ms (typical values) (the value is in the use of crystal / ceramic oscillator when the oscillator stabilization time select register (OSTS) set oscillator oscillation stability waiting time), then operation to stop the clock before the operation began counting again. At this point, the counters have not been cleared, but keep original value.

The photo shows STOP mode under operation (WDT Operation Clock: Peripheral hardware clock)

<1> CPU clock: Crystal/ceramic oscillator clock



<2> CPU clock: High-speed Ring-OSC clock or external clock input



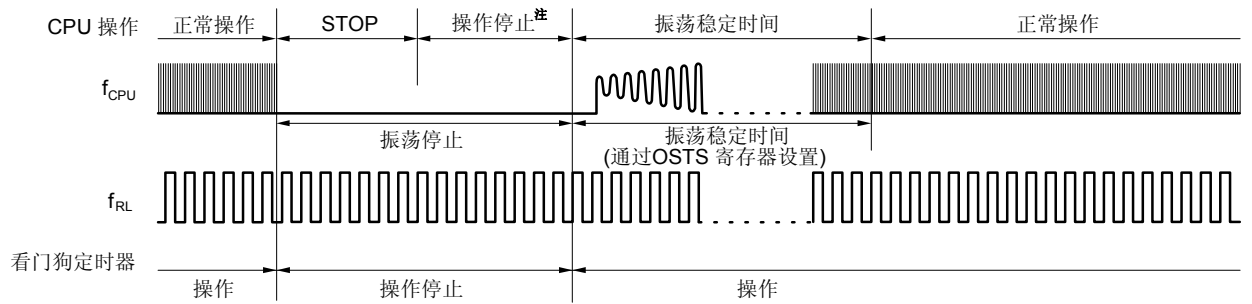
Note Operation stop time is 17 ms (minimum), 34 ms (typical value) and 67 ms (max).

(2) when the watchdog timer operation clock is a low-speed Ring-OSC clock (f_{RL}), and the implementation of STOP instruction.

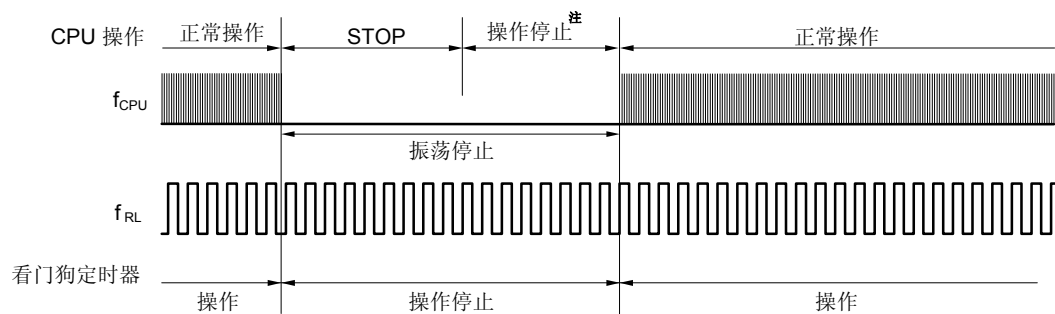
When the implementation of STOP instruction, the watchdog timer to stop the operation. In the release of STOP mode, the operation stopped 34 ms (typical value), then use the operation to stop the operation before the clock to start counting. At this point, the counters have not been cleared, but keep original value.

The photo shows STOP mode under operation (WDT Operation Clock: low-speed Ring-OSC clock)

<1> CPU clock: Crystal/ceramic oscillator clock



<2> CPU clock: High-speed Ring-OSC clock or external clock input

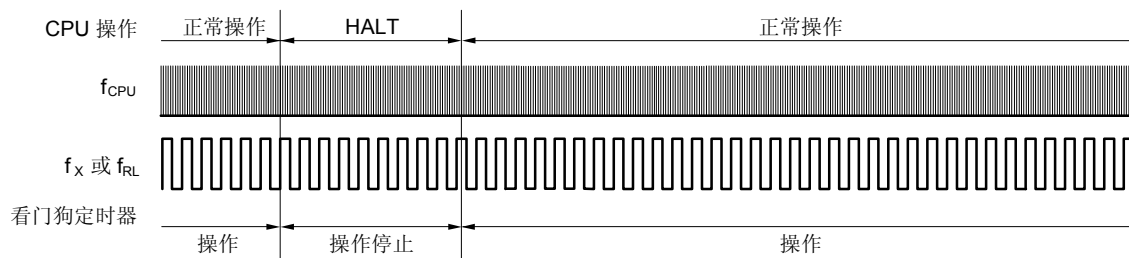


Note Operation stop time is 17 ms (minimum), 34 ms (typical value) and 67 ms (max) .

(D) HALT mode operation (when the optional byte select for the "software to stop the clock speed Ring-OSC")

Regardless of the system clock (f_X) or low-speed Ring-OSC clock (f_{RL}), in the implementation of HALT instruction when the watchdog timer to stop counting. HALT mode release, use the operation to stop the operation before the clock to start counting. At this point, the counters have not been cleared, but keep original value.

HALT mode under the map operation.



2.4.2 Power-Clear Circuit

2.4.2.1 Power-Clear function circuit (POC) has the following functions:

- Electricity generated in the internal reset signal
- Comparison of supply voltage (V_{DD}) and the detection voltage ($V_{POC} = 2.1\text{ V} \pm 0.1\text{ V}$), and $V_{DD} < V_{POC}$ generated when the internal reset signal.
- Comparison of supply voltage (V_{DD}) and the detection voltage ($V_{POC} = 2.1\text{ V} \pm 0.1\text{ V}$), and $V_{DD} \geq V_{POC}$ release the internal reset signal.

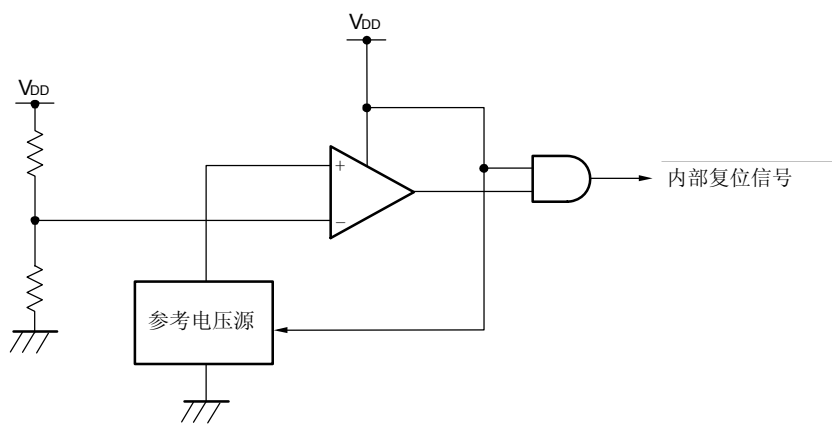
If the POC circuit internal reset signal will reset register mark (RESF) cleared.

POC circuit detection voltage (V_{POC}) value range of $2.1\text{V} \pm 0.1\text{V}$, it is the normal operating voltage range of $2.2 \sim 5.5\text{V}$.

This product integrates a wide range of signals used to generate internal hardware reset function. When the watchdog

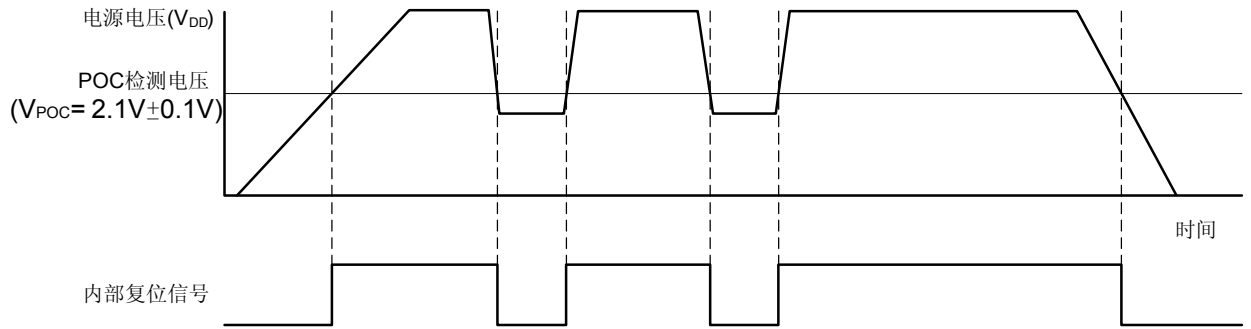
timer (WDT) and low-voltage detection circuit (LVI) reset when aroused, RESF in a sign of the reasons for the reset instructions. When the WDT and the LVI reset signal when the internal, RESF can not be cleared, and the flag was one home .

2.4.2.2 Power Reset circuit (POC) of the diagram shown below.



2.4.2.3 Clear power circuit operation

POC circuit in comparison supply voltage (V_{DD}) and the detection voltage ($V_{POC} = 2.1V \pm 0.1V$), when $V_{DD} < V_{POC}$ when an internal reset signal, when the $V_{DD} \geq V_{POC}$, the release of internal reset signal. POC under the photo shows an internal reset circuit timing signals.



Note the internal reset signal is active-low

2.4.2.4 Power-Clear Circuit Caution

For a supply voltage at a certain time POC detection voltage (V_{POC}) fluctuations in the vicinity of the system, may be repeatedly reset and release of reset. Under such circumstances, the following methods can be reset any settings from being released into the microcontroller experienced start-up time.

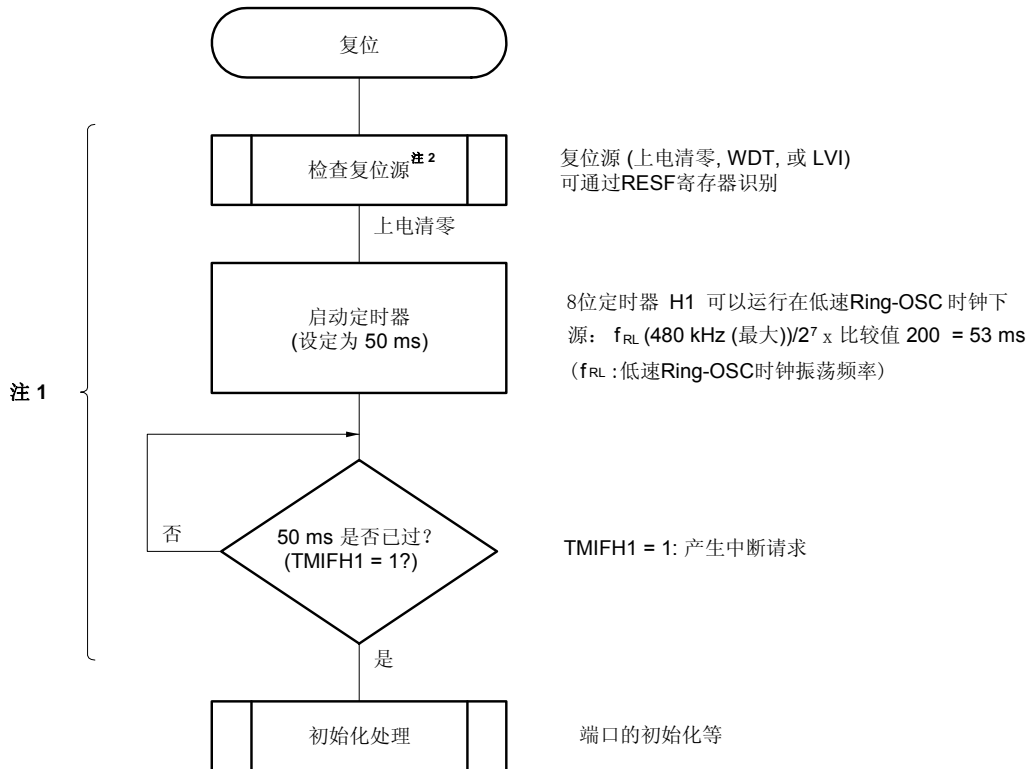
<Method>

In the release of reset signal through the software counter (use a timer) to wait for the system supply voltage fluctuation period, and then on the port initialization.

After the release of the next picture shows the reset software process example:

- If the supply voltage close to POC detection voltage, the fluctuations in time less than or equal to 50ms

图 (a)



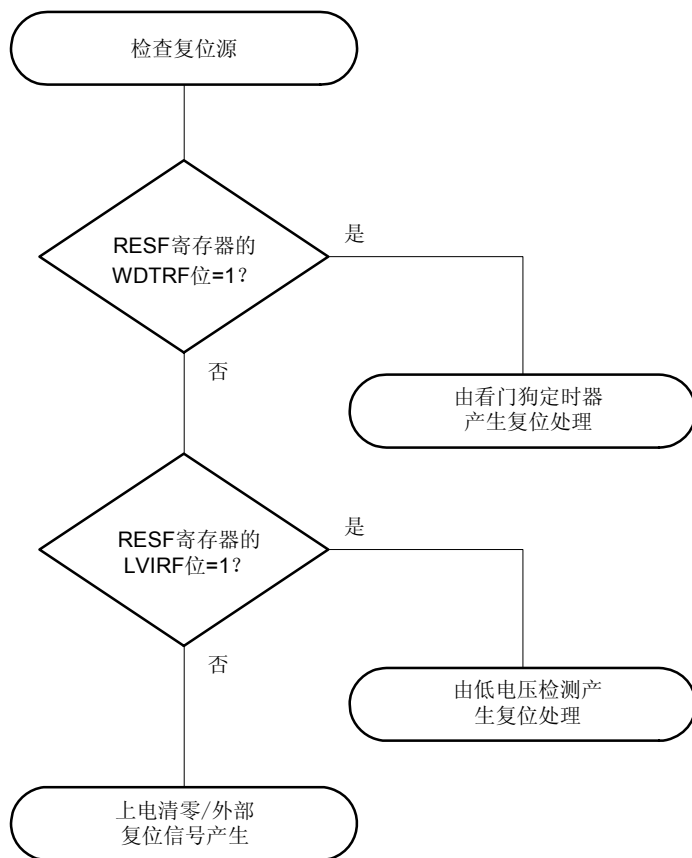
Note

1. If during this period once again have a reset, the initialization can not begin.

2. Flowchart shows the next page.

- Check the reset source

Figure (b)



2.4.3 8-bit timer 80 as the basic time interval timer

When 8-bit timer 80 as an interval timer, you can register in accordance with the 8-bit comparison (CR80) in the pre-set values for the interval of repeat interruption generated.

8-bit timer 80 will be used as a timer interval, follow these steps:

<1> Prohibit the operation of 8-bit timer counter 80 (the 8-bit timer mode control register 80 (TMC80) of section 7 (TCE80) is set to 0).

<2> Set the 8-bit timer 80 counts clock (see table 2-1 and

2-2).

- <3> Set the value of the CR80.
- <4> Permit the operation of TM80 (TCE80 settings for 1).

When 8-bit timer counter 80 equal to the total numerical value of CR80 settings, TM80 value was cleared and then continue to count, at the same time generate an interrupt request signal INTTM80.

Table 2-1 and Table 2-2 lists the time interval, Figure 2-1 express timing interval timer operation.

Cautions

- 1. Timers work, can not change the value of CR80. If the timer while working to change the value of CR80, then immediately have the same interrupt request signal.**

- 2. When using 8-bit memory operation instruction set TMC80 count TM80 clock and at the same time permit, then the timer starts a cycle of error may be one or more of the clock. Therefore, as interval timer TM80 to use, must be set according to the above sequence.**

Table 2-1. 8-bit timer 80 time interval ($f_{XP} = 8.0 \text{ MHz}$)

TCL801	TCL800	The smallest time interval	The largest time interval	Resolution
0	0	$26/f_{XP}$ (8 μs)	$214/f_{XP}$ (2.05 ms)	$26/f_{XP}$ (8 μs)
0	1	$28/f_{XP}$ (32 μs)	$216/f_{XP}$ (8.19 ms)	$28/f_{XP}$ (32 μs)
1	0	$210/f_{XP}$ (128 μs)	$218/f_{XP}$ (32.7 ms)	$210/f_{XP}$ (128 μs)
1	1	$216/f_{XP}$ (8.19 ms)	$224/f_{XP}$ (2.01 s)	$216/f_{XP}$ (8.19 ms)

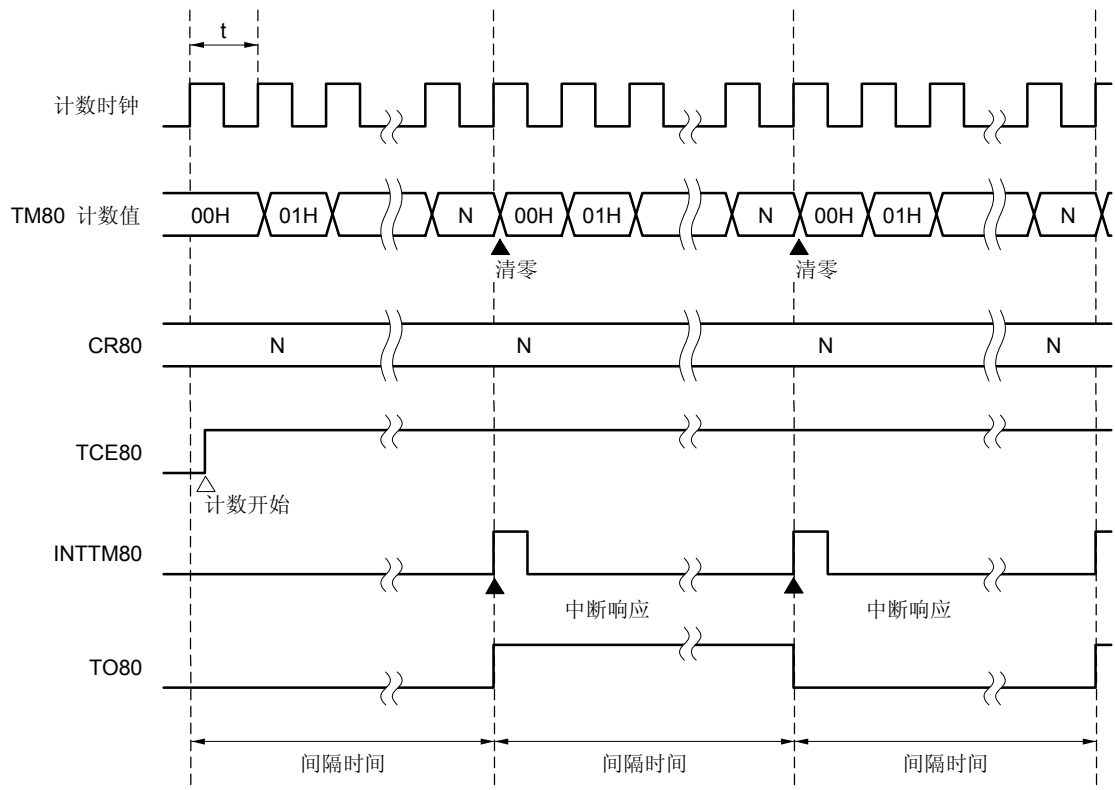
Remarks f_{XP} : Peripheral hardware clock oscillation frequency.

Table 2-2. 8-bit timer 80 time interval ($f_{XP} = 10.0 \text{ MHz}$)

TCL801	TCL800	The smallest time interval	The largest time interval	Resolution
0	0	$26/f_{XP}$ (6.4 μs)	$214/f_{XP}$ (1.64 ms)	$26/f_{XP}$ (6.4 μs)
0	1	$28/f_{XP}$ (25.6 μs)	$216/f_{XP}$ (6.55 ms)	$28/f_{XP}$ (25.6 μs)
1	0	$210/f_{XP}$ (102 μs)	$218/f_{XP}$ (26.2 ms)	$210/f_{XP}$ (102 μs)
1	1	$216/f_{XP}$ (6.55 ms)	$224/f_{XP}$ (1.68 s)	$216/f_{XP}$ (6.55 ms)

Remarks f_{XP} : Peripheral hardware clock oscillation frequency.

Figure 2-1. Interval timer operation timing diagram



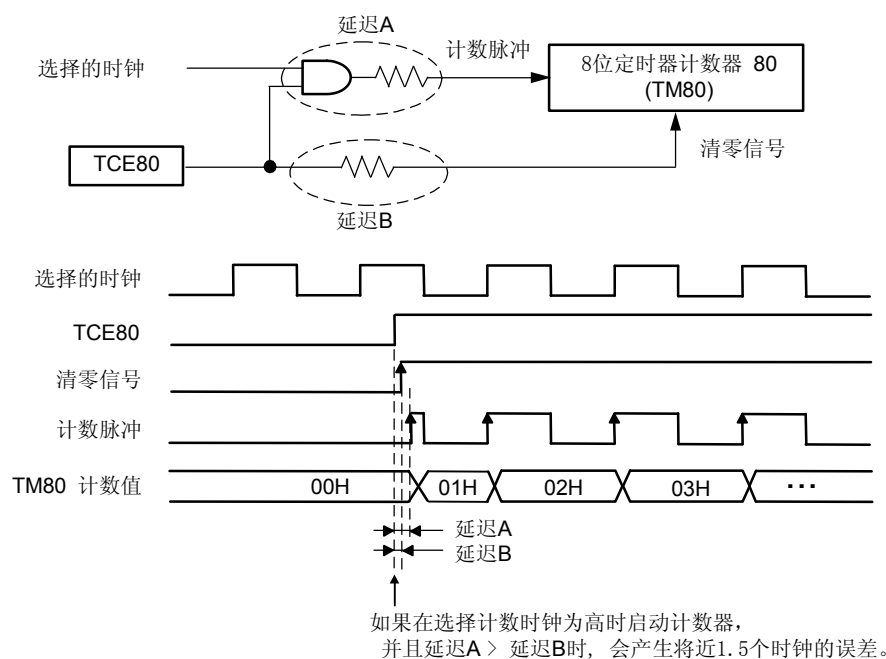
Remarks Time interval = $(N + 1) \times t$: $N = 00H \sim FFH$

2.4.4 The Notes of 8-bit timer 80

(1) Timer start error

From the start the timer to generate an interrupt signal includes a nearly 1.5 clock cycle error. This is because if the count when the clock is high to start the timer, then the rising edge may be detected immediately, and cumulative counters (see Figure 2-3).

Figure 2-3. 1.5 (maximum) clock cycle error situation



(2) 8-bit compare register 80 settings

8-bit compare register 80 (CR80) can be set to 00H.

(3) The Notes of setting to STOP mode

In the implementation of STOP command must first stop the timer before the operation (TCE80 = 0).

2.4.5 8-bit timer H1 as a square-wave output

When 8-bit timer counter H1 and compare register 01 (CMP01) are equal, generate an interrupt request signal INTTMH1, 8-bit timer counter H1 has been cleared.

In interval timer mode, do not use compare register 11 (CMP11). Because even if the CMP11 register setting, it will not 8-bit timer counter H1 and the CMP11 register the same test, therefore, does not affect the timer output.

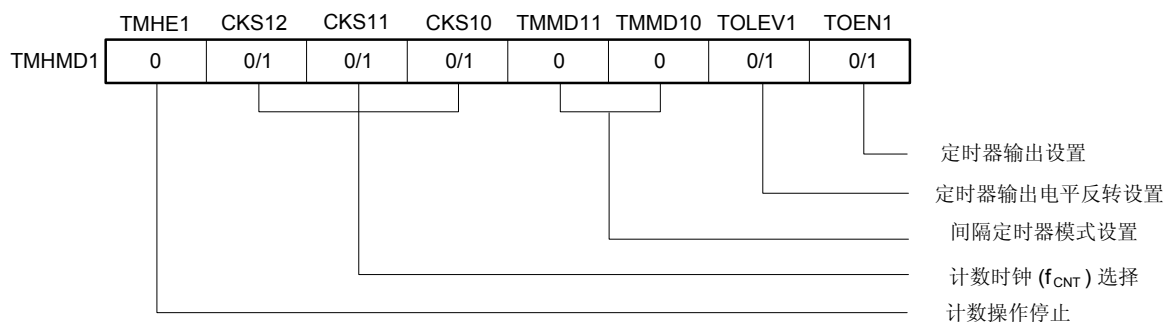
When the set timer H mode register 1 (TMHMD1) the first 0 (TOEN1) to 1:00, from TOH1 output square wave of any frequency (duty cycle 50%).

(1) Usage

Repeat the same time interval INTTMH1 generated signal.

<1> Various register settings

(i) Timer H mode register 1 (TMHMD1) settings



(ii) CMP01 register setting

- Comparison of values (N)

<2> When TMHE1 = 1 to start counting operation.

<3> When 8-bit timer counter H1 value of the CMP01 register value, the interrupt request signal generated INTTMH1, 8-bit timer counter H1 has been cleared.

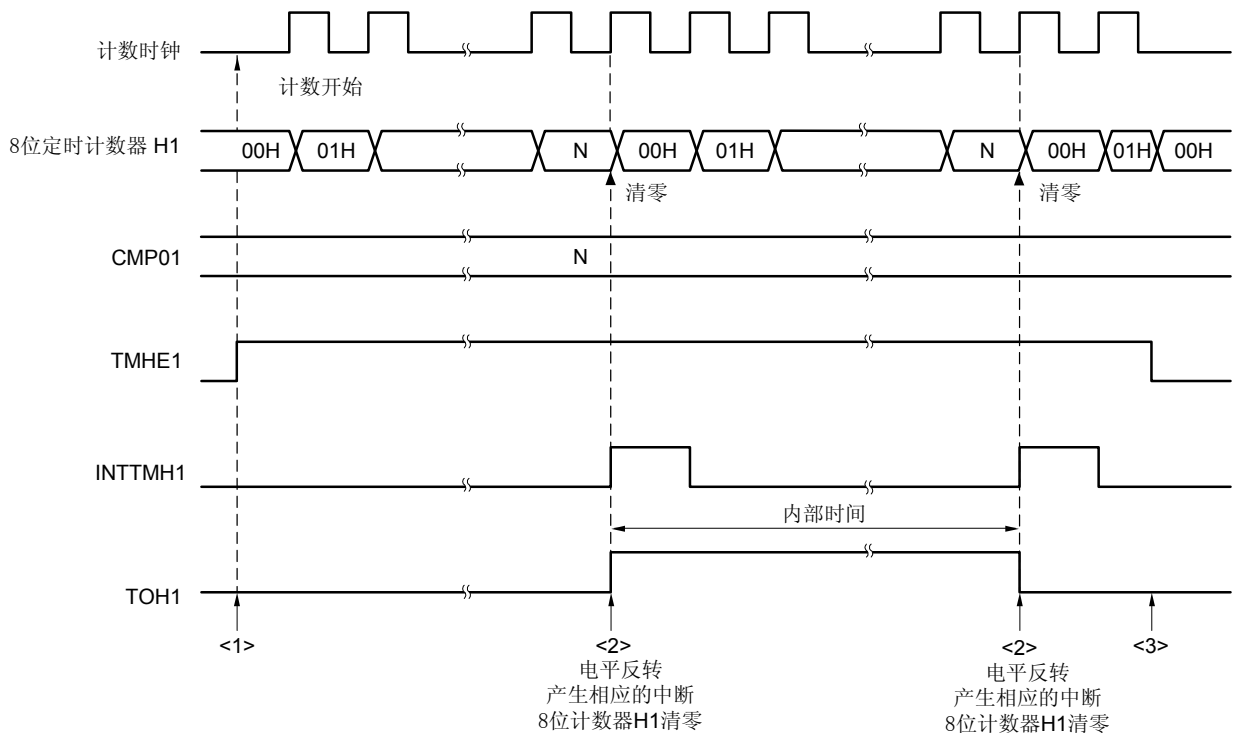
$$\text{Time interval} = (N + 1)/f_{\text{CNT}}$$

<4> Since then, the same time interval have INTTMH1 interruption. To stop the count operation, will be cleared to TMHE1.

(2) Timing diagram

Interval timer/square-wave output operation timing diagram is as follows:

(a) Basic Operation



<1> TMHE1 bit set to 1 to allow the counting operation. After the permit to operate in less than one clock cycle time to start counting the clock count.

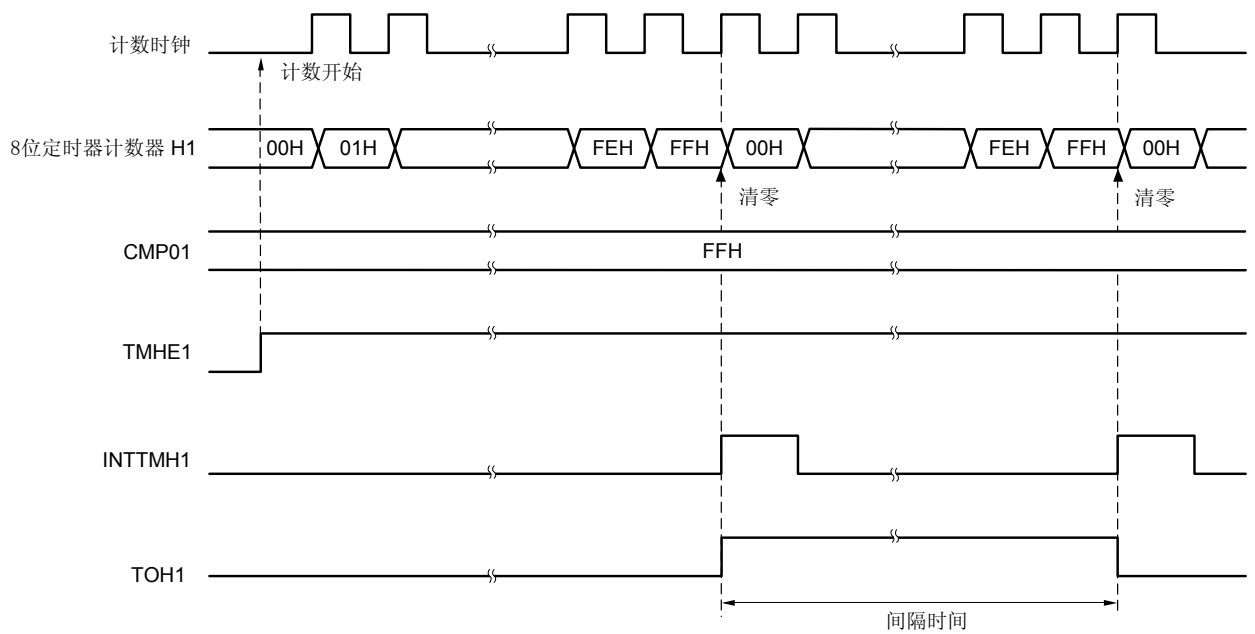
<2> When the 8-bit timer counter H1 and the CMP01 register value equal to, the 8-bit timer counter H1 value of zero, TOH1 output switch and output INTTMH1 vindication of the signal.

<3> In the timer to operate during H1-bit cleared TMHE1 allows

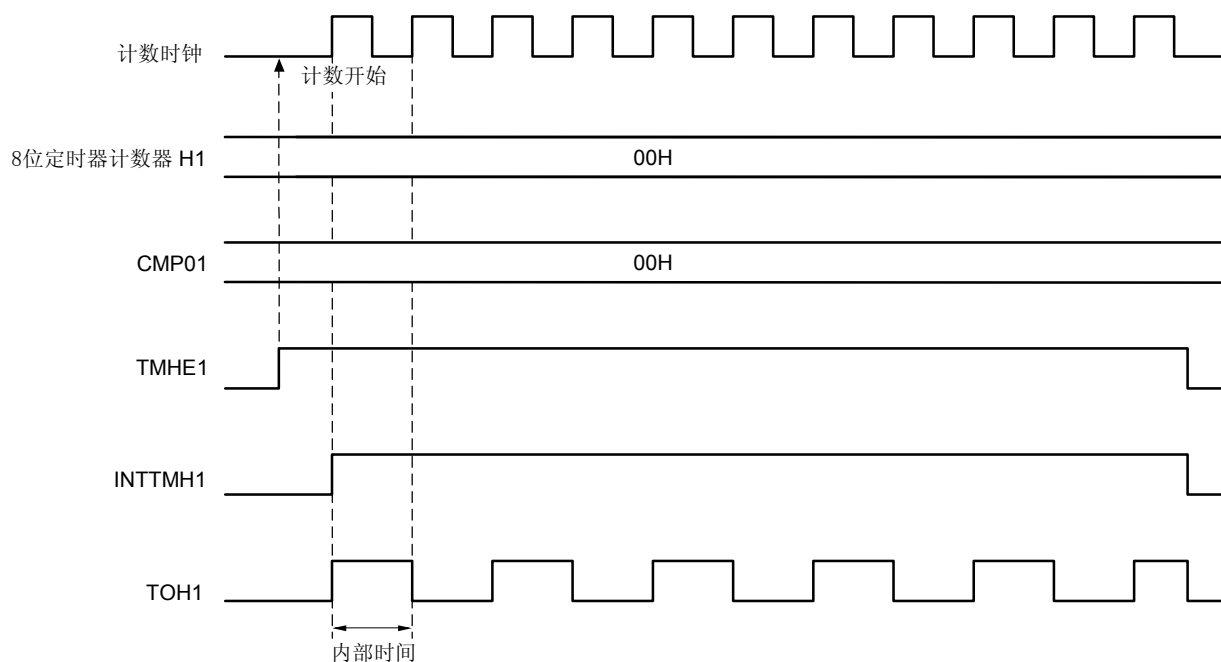
INTTMH1 output signal and TOH1 invalid. If there is no INTTMH1 signal and TOH1 output, the level remained unchanged.

Remarks N = 01H ~ FEH

(b) When CMP01 = FFH, when the operation



(c) When CMP01 = 00H when the operation



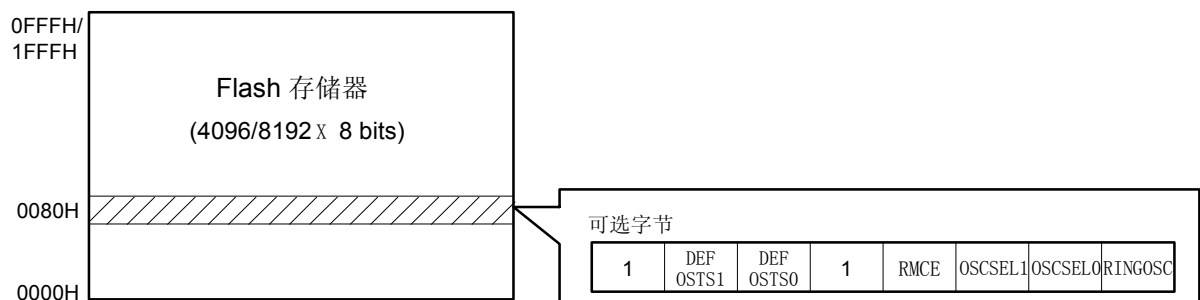
2.4.6 Optional Bytes

78K0S/KB1+ there is a region known as optional byte in the Flash memory address 0080H Department. When using the product, it is necessary to set the following optional features bytes .

1. The system clock source selection
 - High-speed Ring-OSC clock
 - Crystal/ceramic oscillation clock
 - External clock input
2. Low-speed Ring-OSC clock
 - Can not be stopped

- Can be stopped by software
3. RESET pin control
- Used as a RESET pin
 - RESET pin can be used as input port pin (P34)
4. Power or reset after the release of oscillation stabilization time
- $210/f_x$
 - $212/f_x$
 - $215/f_x$
 - $217/f_x$

The next photo shows optional configuration byte :



The next picture shows the optional byte format (1/2)

地址： 0080H

7	6	5	4	3	2	1	0
1	DEFOST S1	DEFOST S0	1	RMCE	OSCSEL 1	OSCSEL 0	RINGOSC C

RINGO SC	Low-speed Ring-OSC clock
1	Can not stop (even if LSRSTOP bit was written for one, will not stop oscillating)
0	Through software to stop (when LSRSTOP bit was written for one, the oscillation stopped)

Note

1. If you choose low-speed Ring-OSC clock oscillation can not be stopped, watchdog timer (WDT) clock counters will be fixed at low-speed Ring-OSC clock .
2. If you choose low-speed Ring-OSC clock can be stopped by software, regardless of low-speed Ring-OSC mode register (LSRCM) the first 0 (LSRSTOP) how to set up, WDT counter clock in the HALT / STOP mode has been suspended. Similarly, when you select in addition to low-speed Ring-OSC clock of any one clock as the WDT counter clock, the clock to provide also been stopped. However, if the choice of low-speed Ring-OSC clock as 8-bit timer H1 count clock, then in the low-speed Ring-OSC working hours (LSRSTOP = 0), in the STOP mode the clock counts are available to use 8-bit timer H1 .

OSCS EL1	OSCSE L0	System clock source selection
0	0	Crystal/ceramic oscillation clock
0	1	External clock input
1	×	High-speed Ring-OSC clock

Note Because the X1 and X2 pins as P121 and P122 pins to use, X1 and X2 pins used in different conditions, depending on the system clock source choices .

(1) Choose the crystal/ceramic oscillation clock

X1 and X2 pins can not be used as I/O port to use, because they are as a clock input port .

(2) Choose the external clock input

Because X1 pin as an external clock input, P121 I can not be used as I/O port to use .

(3) Choose high-speed internal oscillator clock

Ports P121 and P122 can be used as I/O port .

RMCE	RESET pin control
1	RESET pin for the reset input
0 ^注	RESET pin for input pins (P34)

Note When RMCE cleared, the pull-up resistor to be connected .

Cleared through the power-on reset state after the release function and again reference optional byte before a low-level input to the RESET pin, 78K0S/KB1 + reset, and the state of maintaining

a high level input to the RESET pin .

The next picture shows the optional byte format (2/2)

DEFO STS1	DEFO STS0	Power or reset after the release of oscillation stabilization time
0	0	$210/f_x$ (102.4 μ s)
0	1	$212/ f_x$ (409.6 μ s)
1	0	$215/ f_x$ (3.27 ms)
1	1	$217/ f_x$ (13.1 ms)

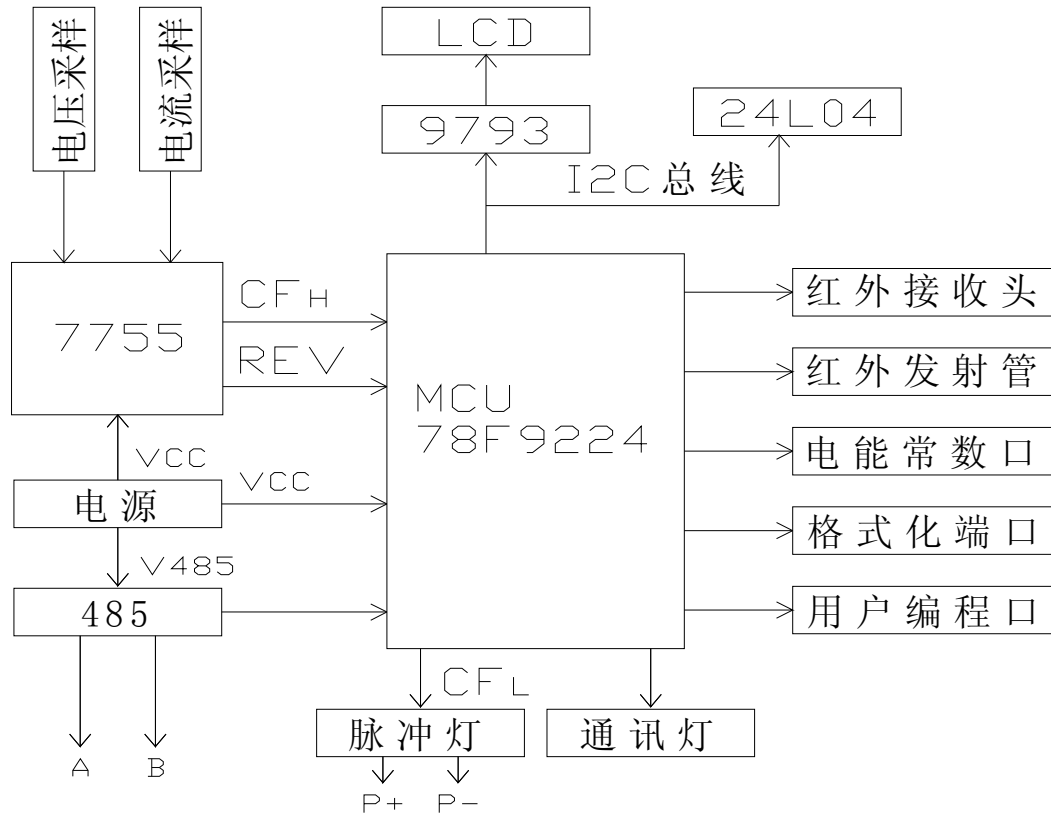
Only elected crystal/ceramic oscillation clock as system clock source, this setting is valid. If I choose to high-speed Ring-OSC clock or external clock input as the system clock source, without having to wait for time.

Note

1. (): $f_x = 10$ MHz
2. Need to be aware of the oscillator oscillation stabilization time can be used in reference to the characteristics of the oscillator.

Chapter III Hardware Design

3.1 System Block Diagram



As shown, the energy meter applications include the following functions of the main circuit: power supply circuit, display circuit, measurement acquisition circuit, infrared communications circuit, communication circuit 485, port detection circuit, I2C communications circuit .

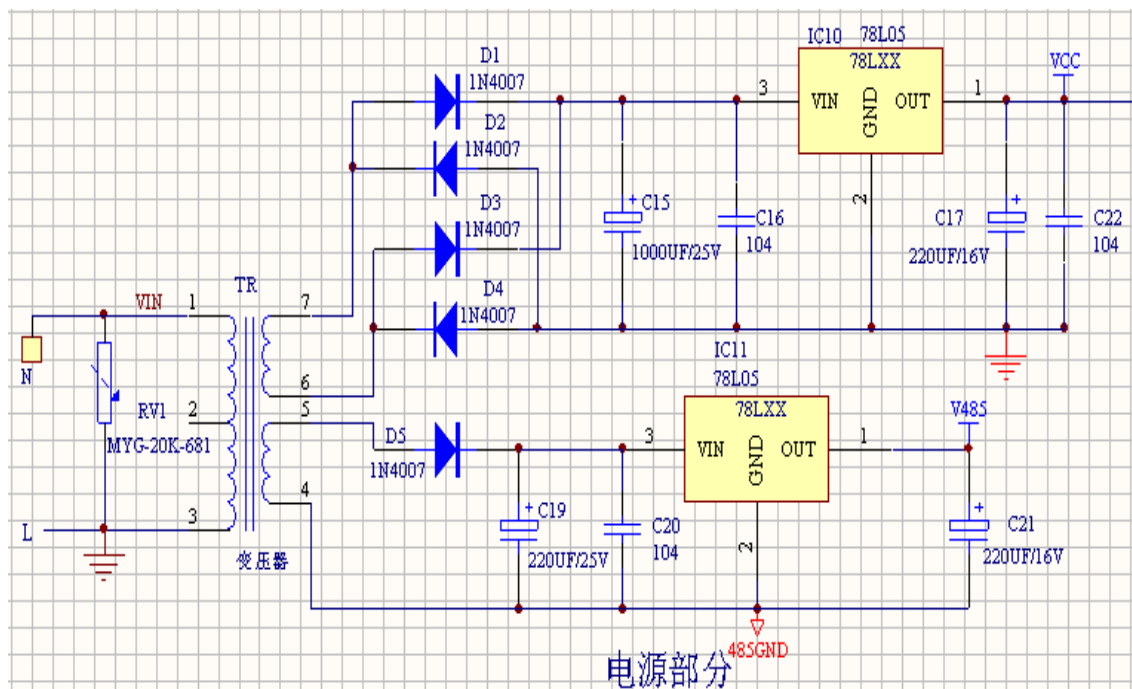
3.2 Pin mapping table

Pin number	Name	I/O	Signal Name
1	V _{SS}	-	GND
2	P121/X1	-	System clock
3	P122/X2	-	System clock
4	P123	I/O	Port input format EEPROM function
5	V _{DD}	-	Supply Voltage
6	P34/RES ET	-	Vacant
7	INTP2	-	Infrared receiver
8	INTP0	-	High-frequency pulse input
9	P40	I/O	Power directional detection input
10	P41	I/O	User programming input port detection
11	P42	I/O	INFRARED 38KHz output
12	TXD6	I/O	485 send
13	RXD6	I/O	485 receive
14	P45	I/O	Communication indicator
15	P130	I/O	Pulse output
16	P23	I/O	Pulse constant choice fractograph CON2
17	P22	I/O	Pulse constant choice fractograph CON1
18	P21	I/O	I ² C-bus data communication port
19	P20	I/O	I ² C -bus communication port clock
20	AVref	-	Connect with V _{CC}

3.3 Control Circuit Power-Meter

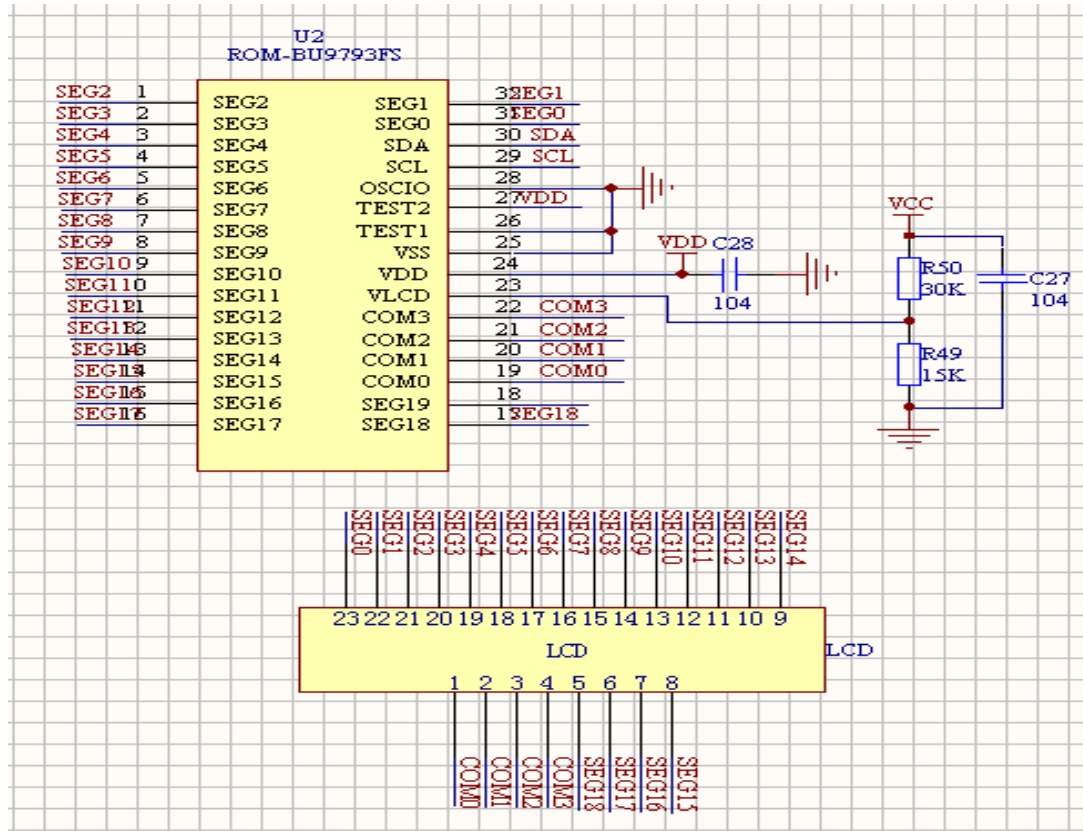
Following is the power-meter control circuit of the circuit examples .

3.3.1 Power supply circuit



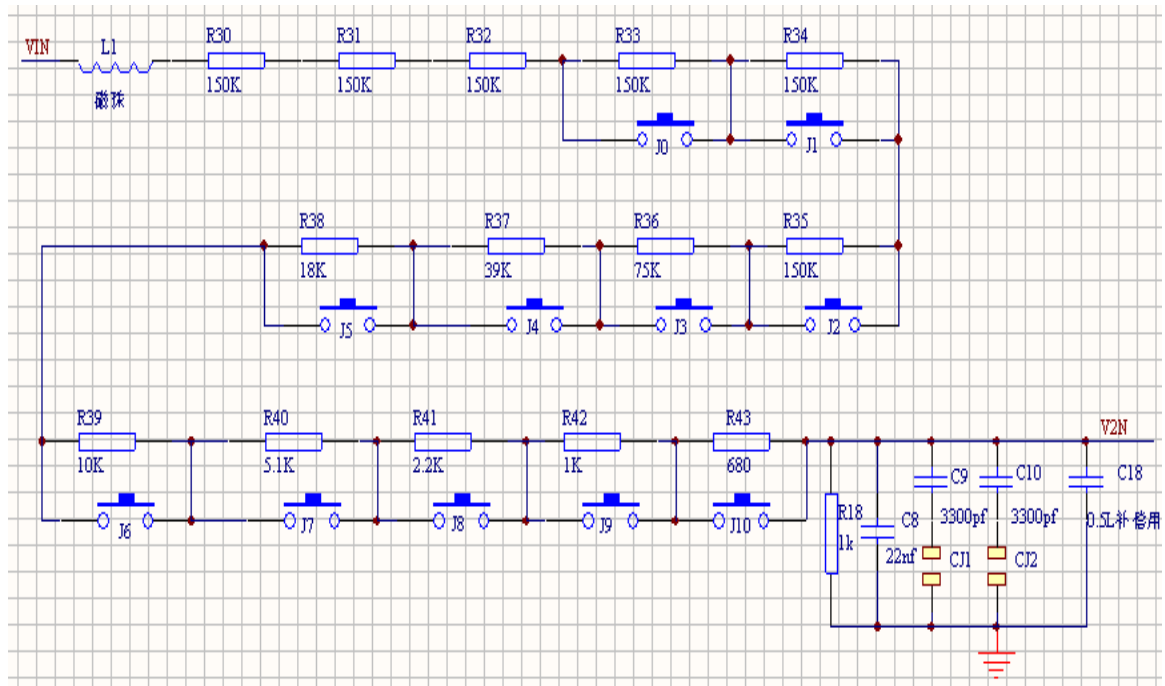
Power principle is very simple, not in detail .

3.3.2 Display circuit

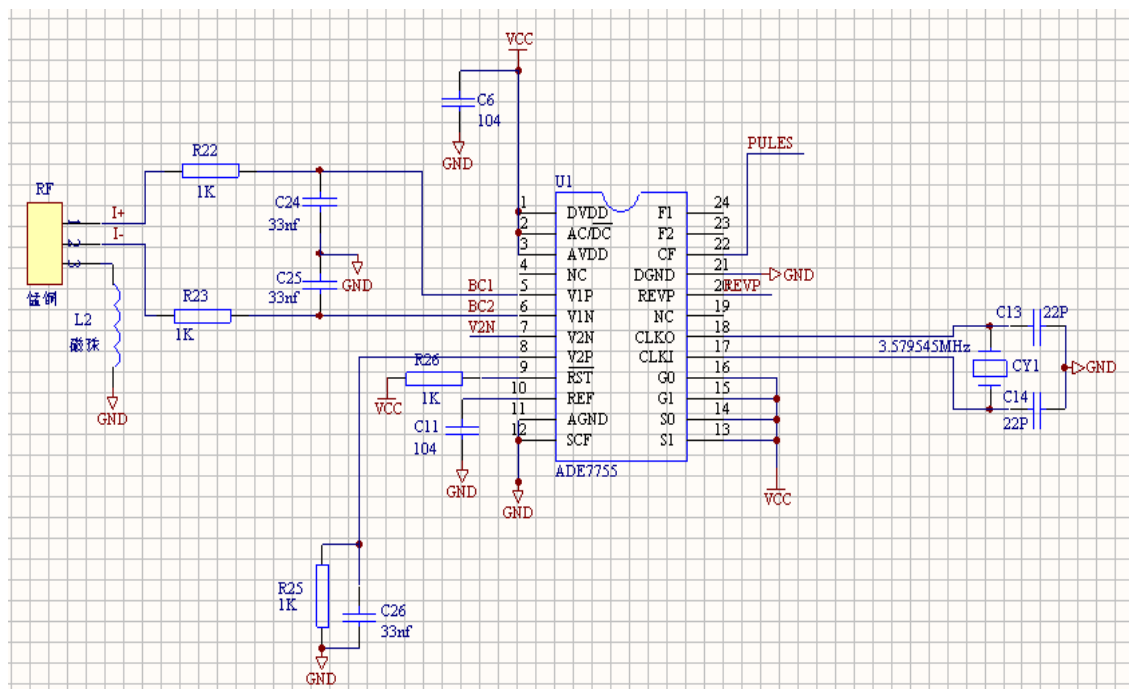


In the circuit, SDA and SCL is the I2C bus with the CPU communication, 9793 is a LCD driver chip, it sent the CPU data into a paragraph code and code to the LCD, the realization of show. In the circuit design, attention should be paid to the design of VLCD, see data sheet 9793.

3.3.3 Measurement Acquisition Circuit

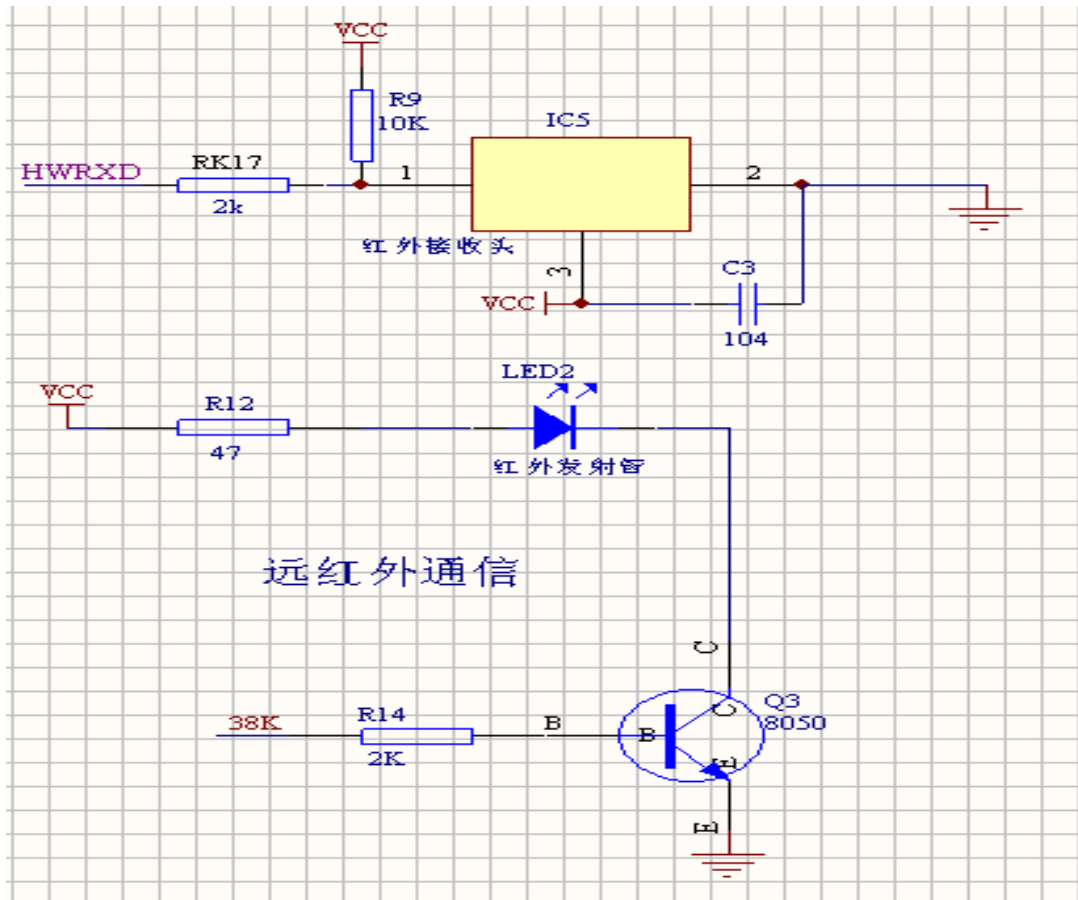


VIN graph is zero line N, V2N is sampling voltage signal into the voltage channel 7755.



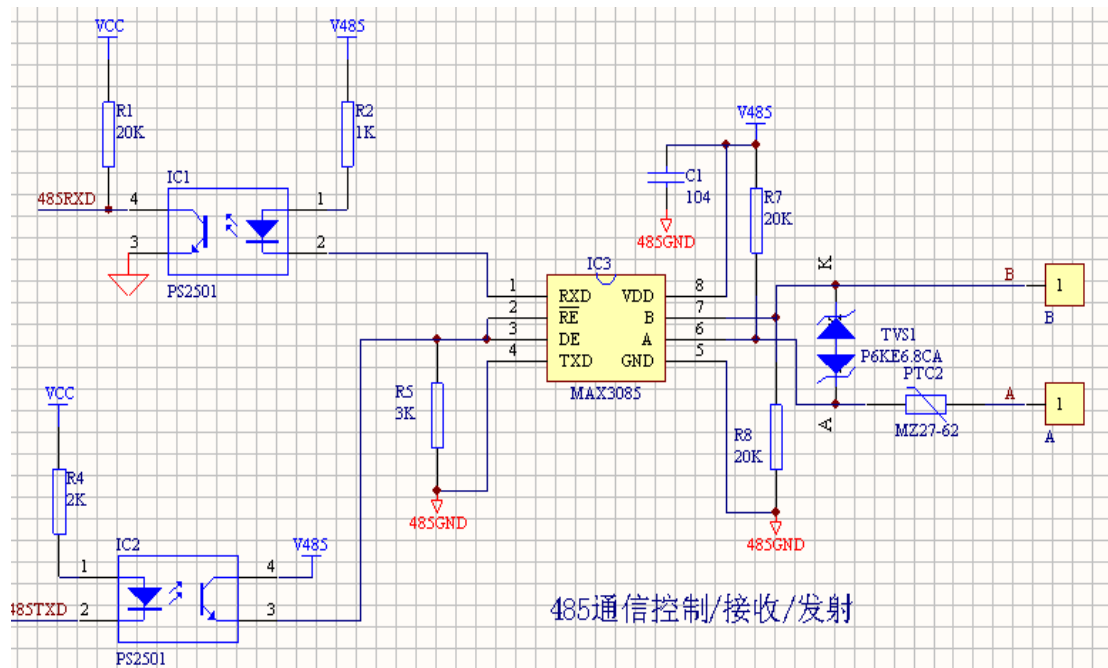
The 7755 sample is the schematic diagram, RF is manganese copper, for sampling current signal through the current sampling circuit into VIP, V1N current channel sampling. Pulses is the high frequency pulse signal for the CPU power sampling. REVP is the direction of electric power signal for the CPU deal with.

3.3.4 Infrared Communication Circuit



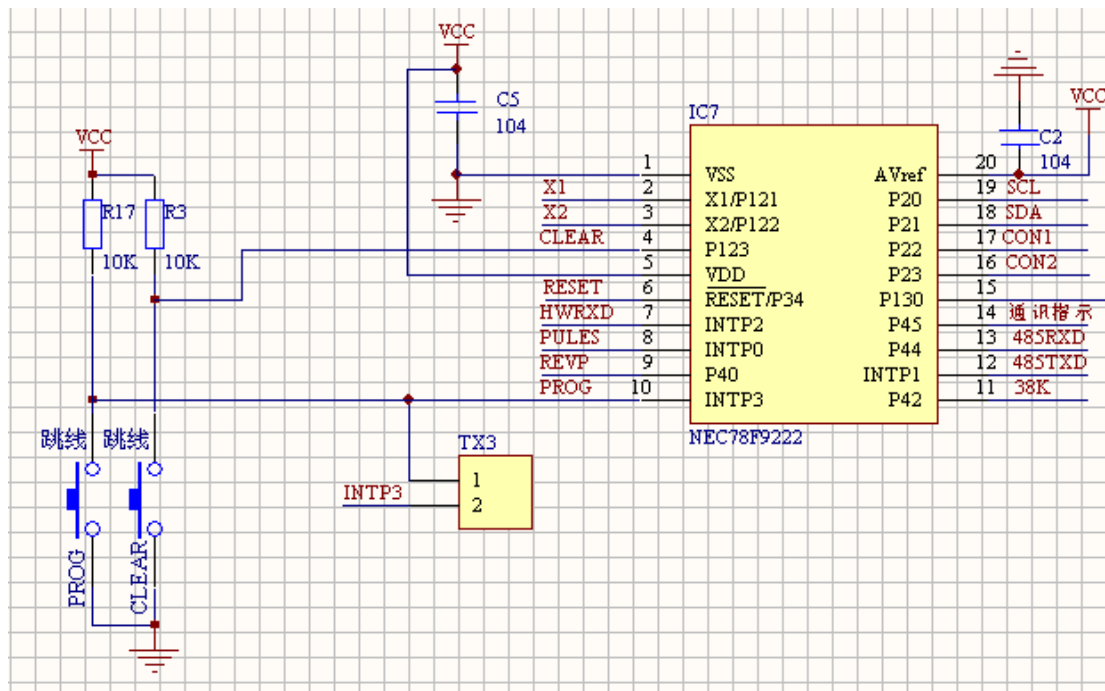
The communication circuit through the single-chip design process to achieve infrared communication functions. When the infrared emission tube to 38KHz frequency of firing, the infrared receiver to the first low-level output; when the infrared emission did not launch tube, the infrared receiver head high output.

3.3.5 485 Communications Circuit



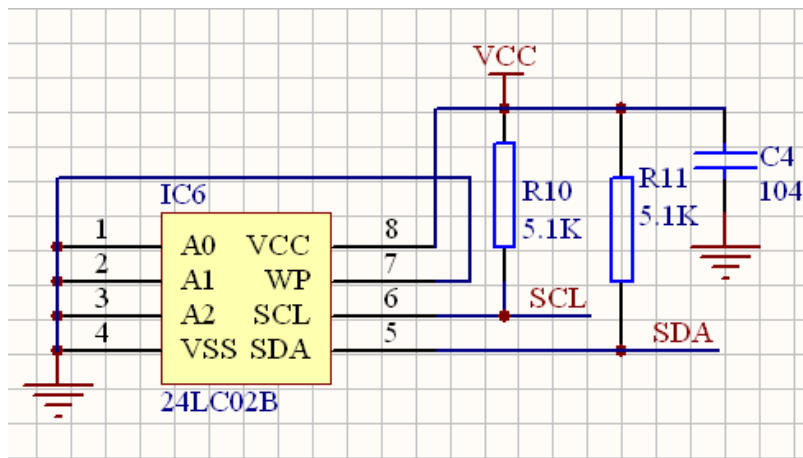
In 485 communication circuit , CPU and communications circuits to achieve electrical isolation by optocoupler circuit , prevent users from mistakenly 220V received A, B terminal, the damage to the hardware circuit.

3.3.6 Port detection circuit



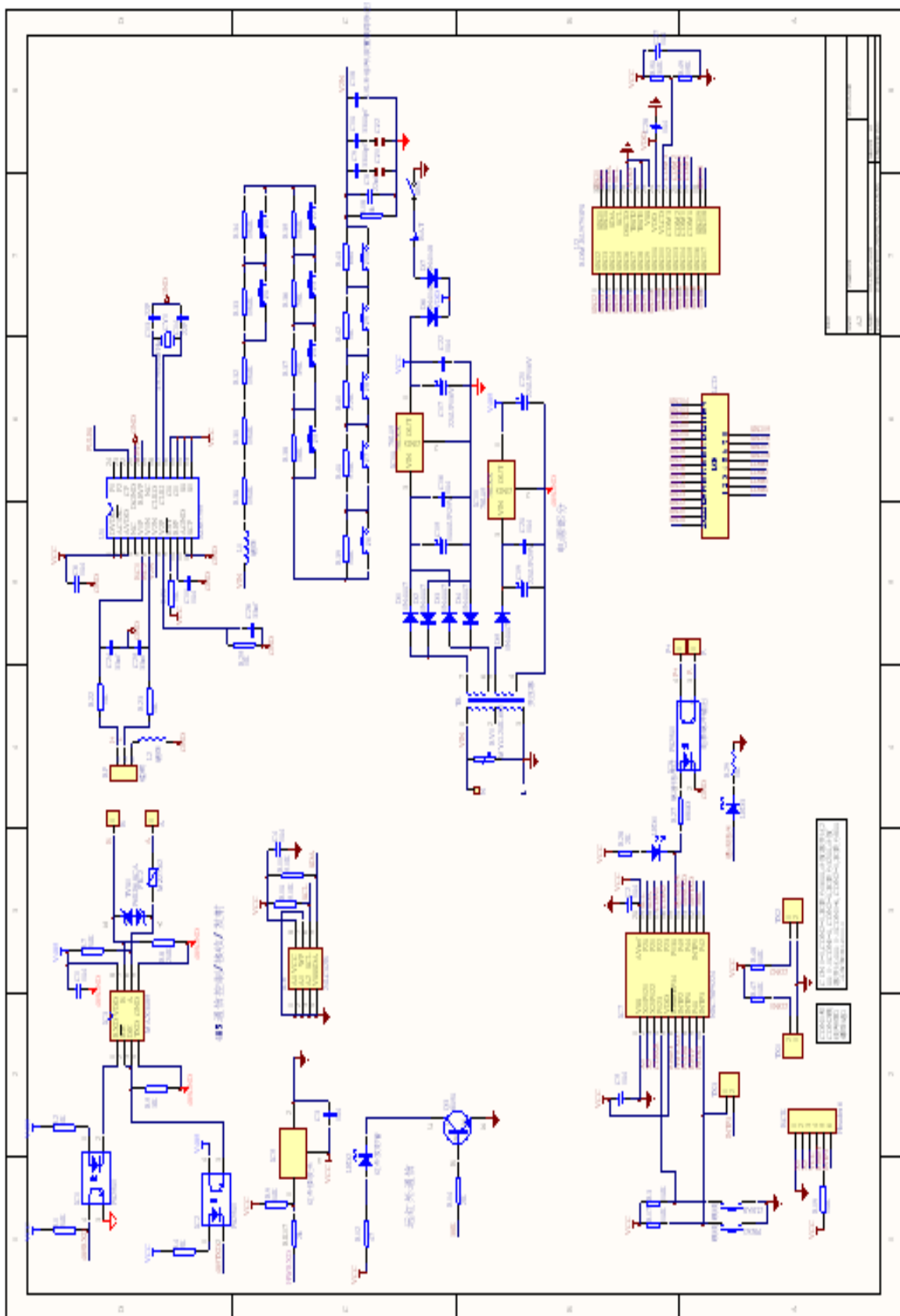
The figure above, PROG button and the CLEAR and CPU detection circuit composed of the port, did not press the button, the port is on the drawing for the high; when the button is pressed, the port and GND shorted, low.

3.3.7 I²C and EEPROM communications circuit



Under normal circumstances, SDA and SCL to be pull-high, CPU access, it will pull down SCL to arouse the attention of EEPROM, the establishment of communication.

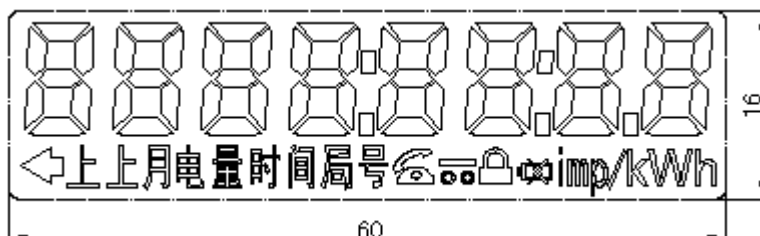
3.4 Machine Schematic



Chapter IV Functional Design

4.1 Control Operation Display Interface

4.1.1 LCD display interface reference chart is as follows :



Electricity above shows: 6 integers, 2 decimals. LCD display that there are many icons, the icon used for the following functions :

← The icon used to indicate the reverse power, when power for the reverse direction, the display; Otherwise, do not show .

电量 The icon is used to indicate the current display shows the contents of electricity .


局号 The icon is used to indicate the current display shows the contents of the correspondence address energy meter.


☎ The icon is used to indicate successful communication, when communication is successful, the icon shows that the continuing disappearance of one seconds later .

☎ The icon used to indicate the status of the mouth programming, programming port shorted, the icon shows, and continued until I disconnect disappear after programming .

🔒 The icon used to indicate the wrong password three times,

and if the wrong password more than 3 times, the icon, users will not be able to re-programming of the energy meter or cleared; to a power blackout, the icon disappears, you can normal programming or cleared .

 The icon used to indicate the current display shows the contents of the unit, which shows the constant power units .

 The icon used to indicate the current display shows the contents of the unit, which shows the power unit .

4.1.2 Can be set up display

Way 1 - shows the current power

Way 2 - Timing flip screen shows the following content (flip screen cycle 1 ~ 9 seconds) :

Display Interface:

First screen - Displays the current power


second screen - Display Energy Meter No. Bureau (low 8bit)

Third Screen - Display Energy Meter constant

4.2 Functional Requirements

4.2.1 Basic Functions

4.2.1.1 Meter using the internal power transformer.

4.2.1.2 Energy Measurement: positive, active energy metering function RP, reverse active electric power by being cumulative. When the power reverse, the screen icon  display .

4.2.1.3 Energy Meter constant power through the hardware settings, you can set a constant value of power there: 800,1600,3200 imp / KWh.

4.2.1.4 Have capability for school, collecting electric energy, active power pulse output for the Passive Optical Isolated OC output ports doors, waveform for the square wave, pulse width: 80ms \pm 20ms. Pulsed light in the power supply when there is no current, Always, used to indicate power status; in to pulse when the anti-Semitic 80ms \pm 20ms, and then lit.

4.3 Extensions Function

4.3.1 Communication Functions

4.3.1.1 Infrared communication and RS485 communication at the physical layer independence, a communications channel to another shall not affect the damaged channel. Communication baud rate:

2400bps, half duplex, in the light of DL/T645-2007 standards.

Command response time frames in the 20-500 ms.

4.3.1.2 Infrared communication interface: Communication distance:

$\geq 5\text{m}$, communications angle: $\geq \pm 15^\circ$.

4.3.1.3 RS485 communication interface: In order to protect the meter, RS485 communication interface and the internal meter circuit implementation of the Electrical isolation and failure protection circuit (to be capable of sustaining AC220V attacks, the duration of 2 minutes is not damaged).

4.3.1.4 After the success of communications, communications indicator lit, the screen icon indicates that one seconds after the indicator light is off, the icon disappears.

4.3.2 Security

4.3.2.1 Meter with a hardware switch programming, and can be sealed .

4.3.2.2 With the programming software password, the factory is 000000, table of the power enterprises, the re-replacement password .

4.3.2.3 Must be programmed in hardware switch closed and the correct password can be programmed .

4.3.2.4 Verify that the password wrong three times, the icon

🔒 ,users will not be able to re-programming of the energy meter or cleared; to a power blackout, the icon disappears, you can normal programming or cleared .

4.3.2.5 Zero-power complex: programming in hardware switch closure and password are correct, the permit for the restoration of electricity meter zero .

4.3.3 Programming function

4.3.3.1 Programming Control: must refer to program security requirements.

4.3.3.2 Programming Password: programming of the meter when the meter in order to protect the reliability of data for password-protected.

4.3.3.3 Programming Content: programming content including: meter Address (Board No.) settings, programming modifications, such as a password.

4.3.3.4 Programming inspection: the programming project can check the function of meter reading and meter management master station computers to achieve. Back copied all the settings and display data for staff than for inspection.

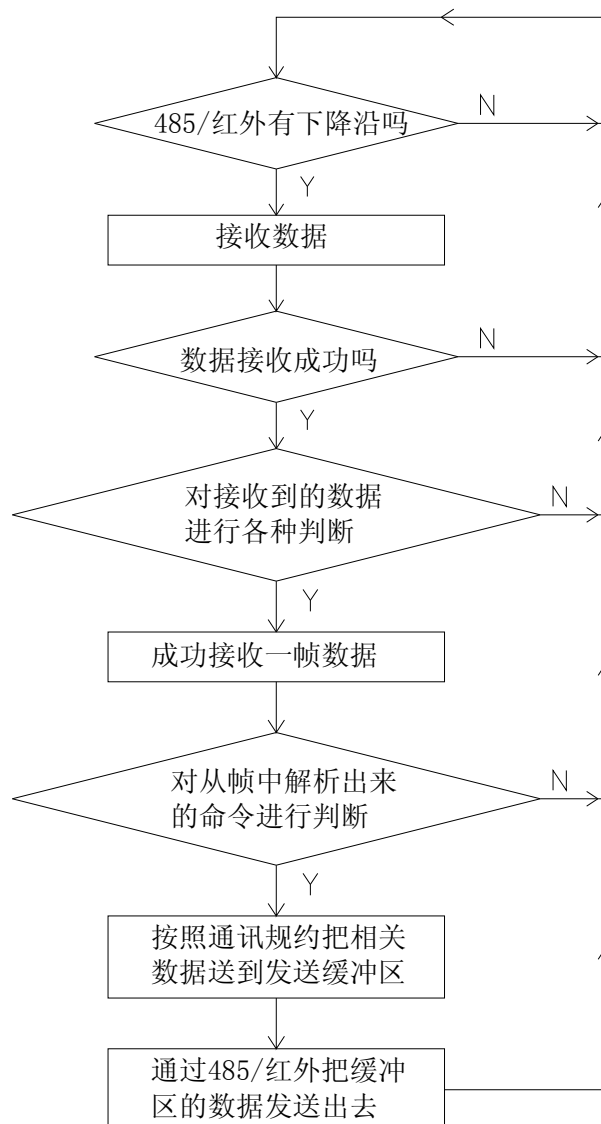
4.3.3.5 Formatted EEPROM: Energy Meter I have to format (or button), when I shorted when formatted, EEPROM data cleared,

that is, electricity, password, table address, through a significant number of screens, each screen display time, software, school tables, etc. into the correct value of zero.

4.3.4 Meter Reading functions:

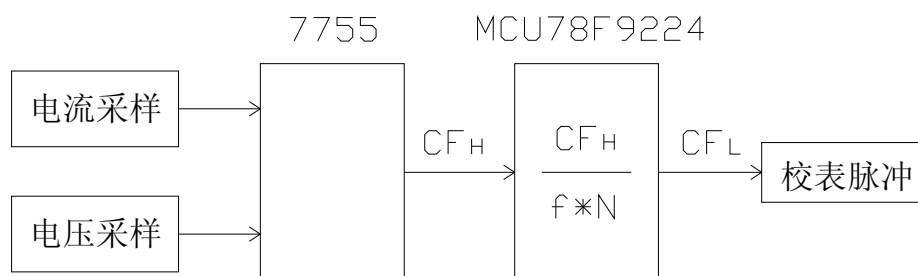
4.3.4.1 The Reading Machine can be copied code, the current consumption data.

4.3.4.2 Flow of meter reading as follows:



4.4.5 Automatic School Table Function

Through infrared, or 485 pairs of 7755 pulses of high frequency numerical adjustments, software school table.



Software on the school map is schematic form, the figure was 7755 of the CFH output high-frequency pulse, CFL is a single-chip microcomputer software school after the low-frequency pulses, namely, School Table pulse, **f** is the correction factor, **N** is equivalent to sub - frequency coefficient, the error in the test table for 0:00, the figure above correction factor $f = 1$, when the school for x when the error, $f = 1 + x$, x can be a positive number can also be negative. Software School table is calculated through the error correction coefficient, thereby changing the frequency coefficient, the realization of the frequency of CFL and standard tables are consistent.

School tables software error correction range: in the EEPROM format after less than $\pm 25.99\%$ in error, software, schools can form a good school; other cases, software can not guarantee the school

table.

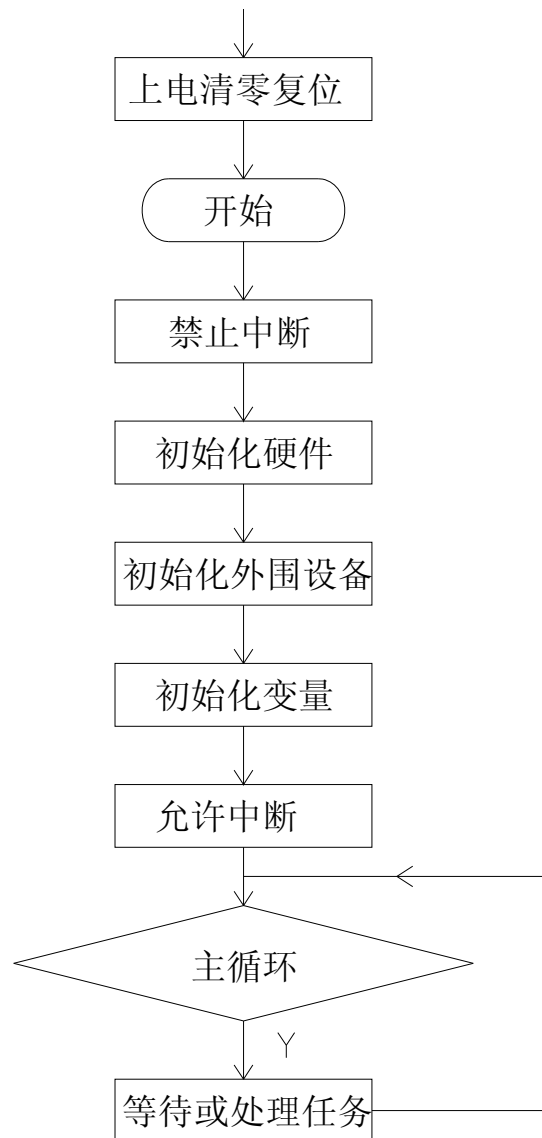
Software School Table error adjustment fineness: EEPROM in the format, the error of adjustment for fineness of 0.10%; other cases, regulation of uncertain size, but should be close to 0.10 percent.

Chapter V The Software Flow Chart

5.1 Procedures For The Total Process Module

Module Function Description: procedural power, the hardware implementation of Power-Clear function, when the voltage > 2.2V, the hardware reset signal release, procedures to enter the initialization, configuration procedures, in the configuration process to prohibit interruption, configuration is complete, permit interruption, into the main circle, on the procedures to respond to inquiries or interruption.

The total flow chart :

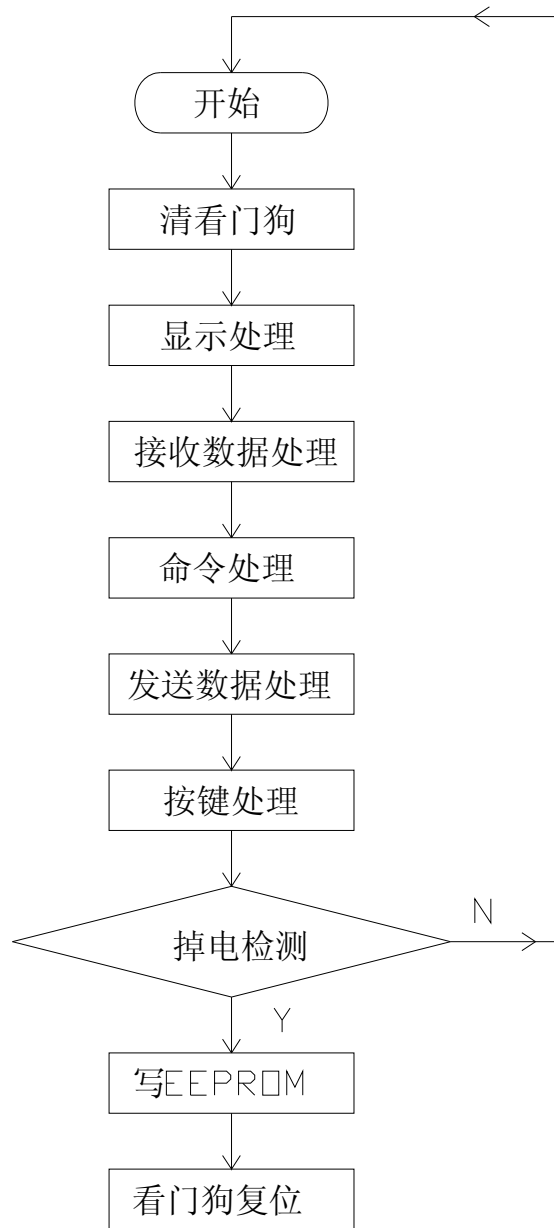


5.2 Cycle The Main Module

Module Function Description: power on initialization procedure done after the main cycle, in the main loop, the program first-money watchdog, followed by a second query, in accordance with each display time and display the contents of display counter to determine the content and the display content into the display

buffer is displayed; in the detected data symbol received after the data reception function call, receiving an order, according to the received identification data to determine the order of implementation of the corresponding treatment; when the command after treatment, Return prepare data and send into the buffer zone; when detected signs send data after the call Send function, each time I send a byte, until 16H send completed; when the program detects that EEPROM formatting marks, the Executive formatted EEPROM key treatment procedures; When detected after the power-down signs, procedures and so on need to preserve the power to write data EEPROM, and start the cycle of death, waiting for the hardware end of capacitor discharge; in the above-mentioned process, if there is interruption occurs, the program will be interrupted at any time embedded service procedures, response-related events, then return to the pre-interruption position to continue to implement; procedures in the entire process, constantly judge signs and the implementation of eligible events mark again and again.

The main cycle diagram :



5.3 Power-processing module

Module Function Description: In the deal with aspects of power, mainly through the use of low-voltage detector to achieve the function of LVI. Procedure after power-on detection of power supply voltage V_{DD} is greater than the detection voltage V_{LVI} , each detection time, delay of 50 milliseconds, if ten consecutive times detected power, let down treatment program, otherwise, the program reset, re-detection of the beginning of power.

Related register applications: low-voltage detector LVI here is so used :

Low-voltage detection register LVIM:

7	6	5	4	3	2	1	0
LVION	0	0	0	0	0	LVIMD	LVIF
1	0	0	0	0	0	1	0

LVION: = 0, the prohibition of operation;

= 1, permit to operate.

LVIMD: = 0, the supply voltage V_{DD} < detection voltage V_{LVI} ,
the resulting interruption;

= 1, power supply voltage V_{DD} < detection voltage
when V_{LVI} , resulting in reset;

LVIF: = 0, the supply voltage V_{DD} > = detection voltage V_{LVI} ,

or when the prohibition of operation;

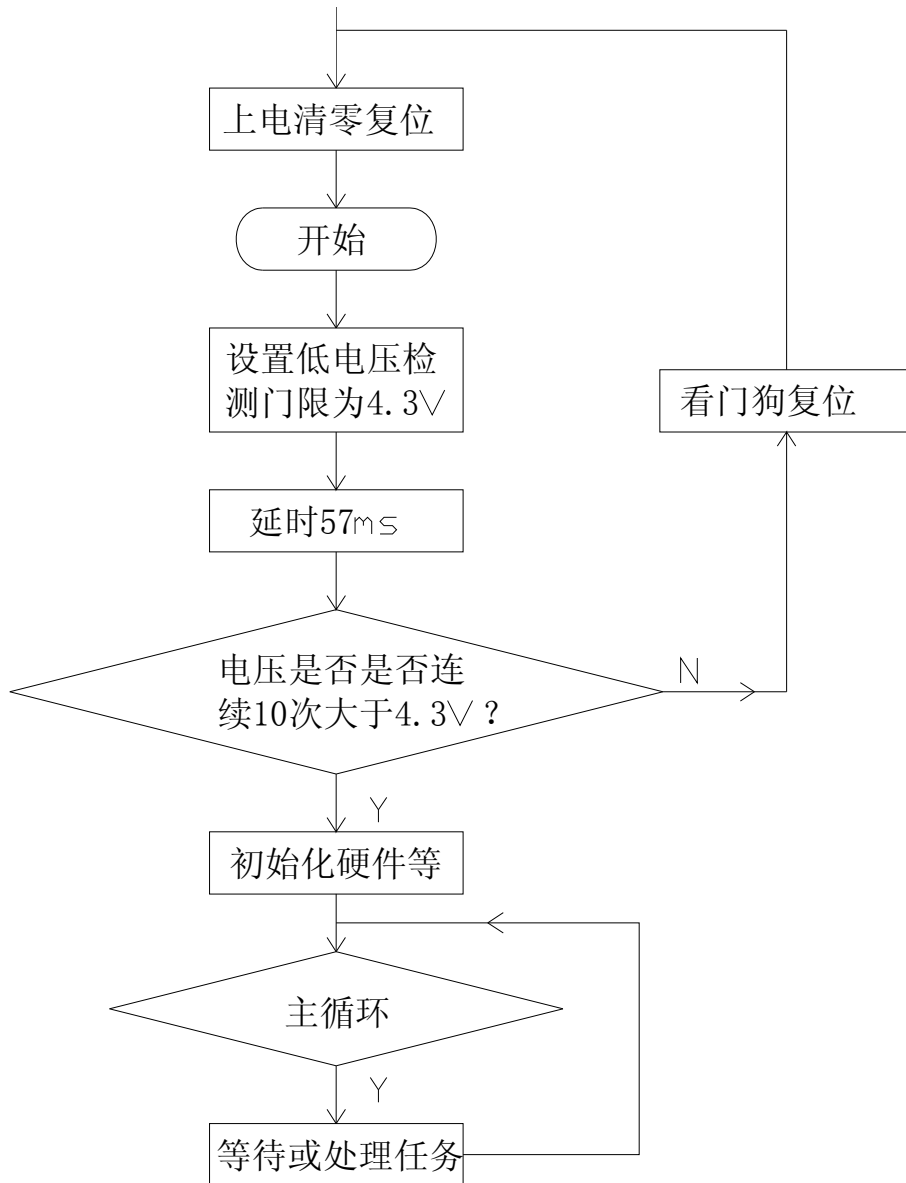
= 1, power supply voltage $V_{DD} < \text{detection voltage}$
when VLVI;

Low-voltage detection level select register LVIS:

7	6	5	4	3	2	1	0
0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0
0	0	0	0	0	0	0	0

LVIS0 ~ LVIS3: = 0, set the detection voltage of $4.3V \pm 0.2V$.

Deal with power-diagram:



5.4 Display processing module

Module Function Description: LCD in the handle area, mainly through the use of LCD Driver IC BU9793FS to achieve, the chip data sheet can be downloaded from http://www.gezhou.net/pro_more.asp?unid=866 . The main loop in procedure, procedures query once per second, to determine whether the implementation of display processing module, when the per-screen display continued after the end of time, the program shows the contents of the counter plus one, to determine the next screen shows the content and display content delivery into the display buffer, if this is the first time to the display buffer to send data, first configuration register 9793 to 9793 the data into the display buffer, and displayed; after the procedure to re-screen display time for each delay length of time, cycle the contents of the above, when the display shows the contents of counter is greater than a few hours to show the contents of counter cleared, a fresh start, to achieve round-screen display.

9793 related to register the application:

Chip set registers operate ICSET:

7	6	5	4	3	2	1	0
C	1	1	0	1	*	P1	P0

1	1	1	0	1	0	1	0
---	---	---	---	---	---	---	---

C: command or data to determine bit:

= 0, the next BYTE data is written into the RAM;

= 1, under the command of a BYTE.

P1:

= 0, not to implement the software reset;

= 1, the implementation of software reset;

P0: OSC mode:

= 0, the internal shock circuit;

= 1, external clock input;

Display Control Register DISCTL:

7	6	5	4	3	2	1	0
C	0	1	P4	P3	P2	P1	P0
1	0	1	1	1	1	1	1

C: command or data to determine bit:

= 0, the next BYTE data is written into the RAM;

= 1, under the command of a BYTE.

P3, P4: Power saving mode settings:

Power saving mode	P4	P3	RESET Initial status
Normal mode	0	0	○

Power-saving mode 1	0	1	
Power-saving mode 2	1	0	
Power-saving mode 3	1	1	

Current work is based on: normal mode> power-saving mode 1> power-saving mode 2> power-saving mode to reduce the order of 3 .

P2: Set LCD driver waveform:

Setting	P2	Initial value
LINE flip	0	○
FRAME flip	1	

Current work is LINE flip> FRAME's.

P1, P0: power-saving mode settings:

Power saving mode	P1	P0	Initial value
Power-saving mode 1	0	0	
Power-saving mode 2	0	1	
Normal mode	1	0	○
High-level consumption mode	1	1	

Current work is based on power-saving mode 1> power-saving mode 2> Normal mode>高耗电 model order increased.

All show the paragraph control register APCTL:

7	6	5	4	3	2	1	0
C	1	1	1	1	1	P1	P0
1	1	1	1	1	1	0	0

C: command or data to determine bit:

= 0, the next BYTE data is written into the RAM;

= 1, under the command of a BYTE.

P1: setting full-screen display lit:

APON	P1	Initial value
Normal Mode	0	○
Full Highlight	1	

P0: the abolition of full-screen display lit:

APON	P0	Initial value
Normal Mode	0	○
Full Highlight	1	

Model shows that register MODESET:

7	6	5	4	3	2	1	0
C	1	0	*	P3	P2	*	*
1	1	0	0	1	0	0	0

C: command or data to determine bit:

= 0, the next BYTE data is written into the RAM;

= 1, under the command of a BYTE.

P3: set display On, Off:

APON	P3	Initial value
Display On	0	○
Display Off	1	

P2: Setting Bias:

APON	P2	Initial value
1/3Bias	0	○
1/2Bias	1	

Address setting register ADSET:

7	6	5	4	3	2	1	0
C	0	0	P4	P3	P2	P1	P0
0	0	0	0	0	0	0	0

C: command or data to determine bit:

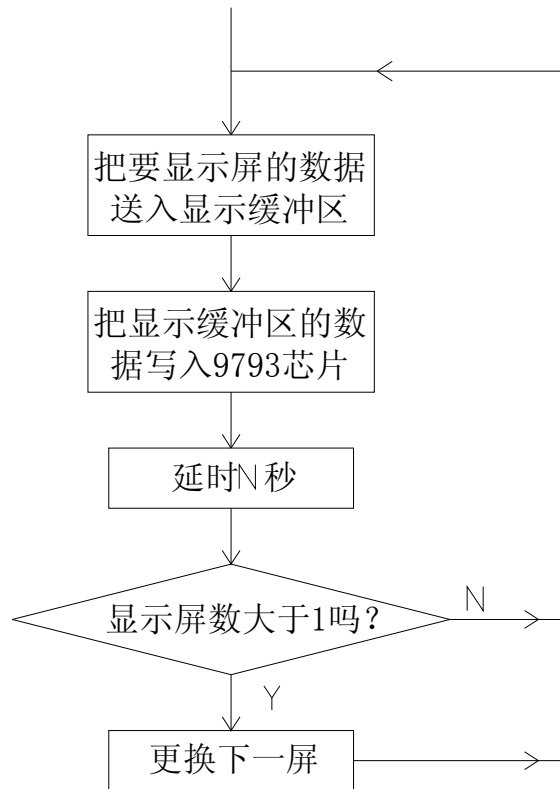
= 0, the next BYTE data is written into the RAM;

= 1, under the command of a BYTE.

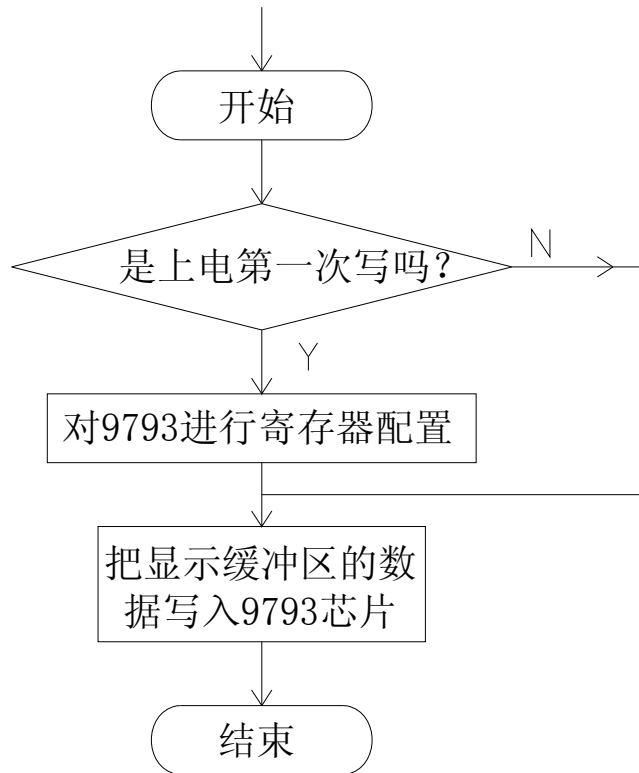
P4 ~ P0: According to P4 ~ P0 designated address data to set the

address counter.

Diagram shows the procedure:



给9793芯片写入数据:



5.5 I²C module deal

Module Function Description: I2C-bus using 2-wire bus interface circuit to achieve the exchange of information between devices, 2-wire serial interface circuit is the clock line SCL and the serial data line SDA composed. Each device has a unique address, and, in accordance with the details of function can be divided into transmitter and receiver, in accordance with the role of different sub-device-based devices and from devices, the main device is to initiate, control, the end of the exchange of information devices, from devices Addressing the main device to device; SDA and SCL

are bi-directional, and pull-through resistance was as high, which constitute the circuit is idle. Their communications rate of 100 ~ 400Kbps, in the SCL is high during the period, SDA line high to low-level changes in the formation of START timing, and the SDA line low to high changes in the formation of STOP timing.

See the figure below :

Figure 1: START and STOP circumstances

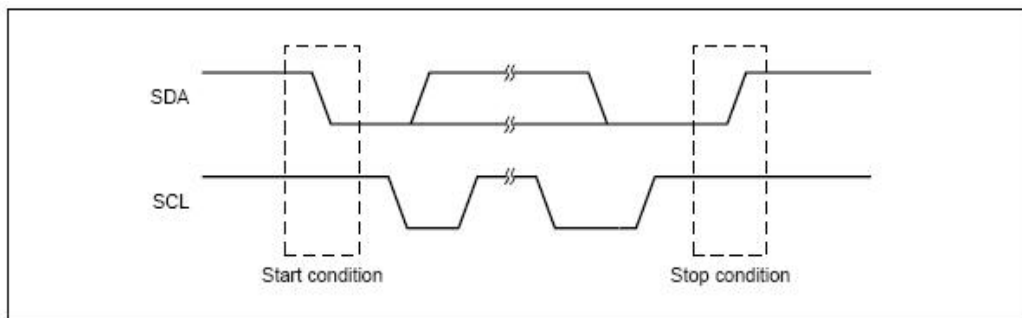
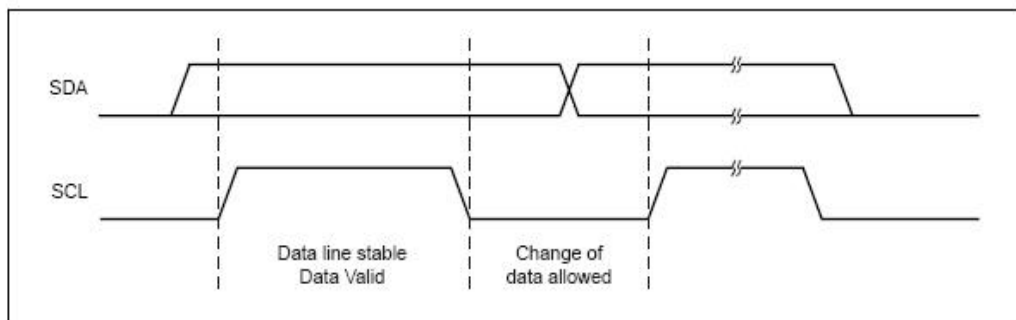


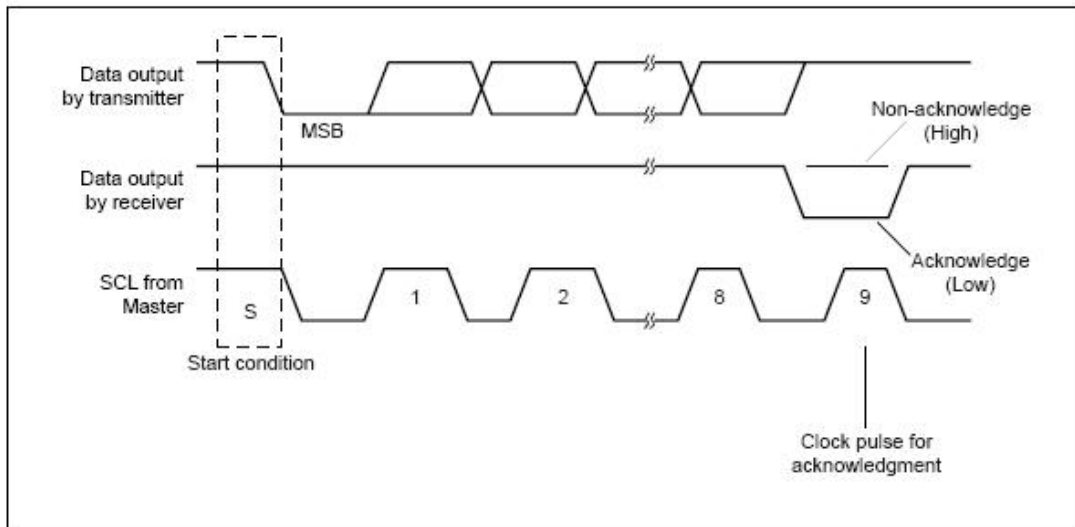
Figure 2: I²C bus valid data



Data on SDA in the SCL is high when effective, will be in the low-level change, every time data transmission are high in the former, low in the post, all the byte bus, there will be a response to

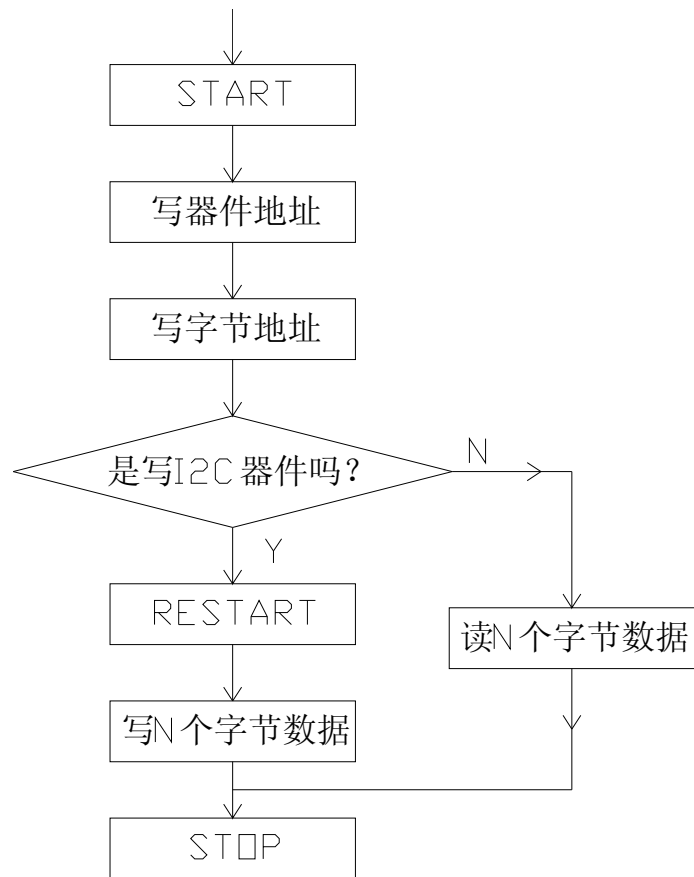
treatment, response is the in the SCL the first nine cycles appears low, it is generated by the receiver. Data transmission timing is as follows:

Figure 3: I²C bus video tapes, non-response



If the receiver can not receive data or in the beginning and after the transfer from the device, between master and slave devices in accordance with the requirements of data exchange, once the last byte and respond to the exchange after the end of the device issued by the end of the main signal, the release of I²C bus.

I²C program diagram



EEPROM Description :

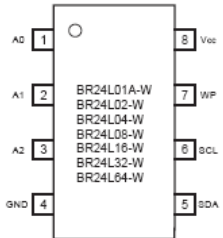
Here, we ROHM's EEPROM to tell, ROHM's EEPROM and other generic manufacturers, are in strict conformity with the I2C bus protocol, in single-phase watt-hour meter used on the capacity of EEPROM is generally less than 64Kbit, we here used is the capacity of 4Kbit the BR24L04-W, BR24L04-W data sheet <http://www.gezhou.net/down.asp?classid=172> can go to download; EEPROM using I2C interface circuit of the device, the device A2-A0 is the device hardware address, the adoption of the address, can be achieved in the I2C bus articulated on a number of EEPROM, articulated the following table is the quantity and the types of correspondence :

Setting R/\overline{W} to 0 --- write (setting 0 to word address setting of random read)
 Setting R/\overline{W} to 1 --- read

Type	Slave address							Maximum number of connected buses	
BR24L01A-W	1	0	1	0	A2	A1	A0	R/\overline{W}	8
BR24L02-W	1	0	1	0	A2	A1	A0	R/\overline{W}	8
BR24L04-W	1	0	1	0	A2	A1	PS	R/\overline{W}	4
BR24L08-W	1	0	1	0	A2	P1	P0	R/\overline{W}	2
BR24L16-W	1	0	1	0	P2	P1	P0	R/\overline{W}	1
BR24L32-W	1	0	1	0	A2	A1	A0	R/\overline{W}	8
BR24L64-W	1	0	1	0	A2	A1	A0	R/\overline{W}	8

PS, P0 ~ P2 are page select bits.

Note) Up to 4 units of BR24L04-W, up to 2 units of BR24L08-W, and one unit of BR24L16-W can be connected.
 Device address is set by "H" and "L" of each pin of A0, A1, and A2.



EEPROM in the main device to find the address, we will in accordance with the design requirements for data reading and writing, for continuous time, continuous time can be 256 bytes; for

consecutive write can only write one, if in excess of the page quantity, it will cause a somersault, and then from the page address of the location of the first began to write, each page number of bytes to write as follows :

List of numbers of page write

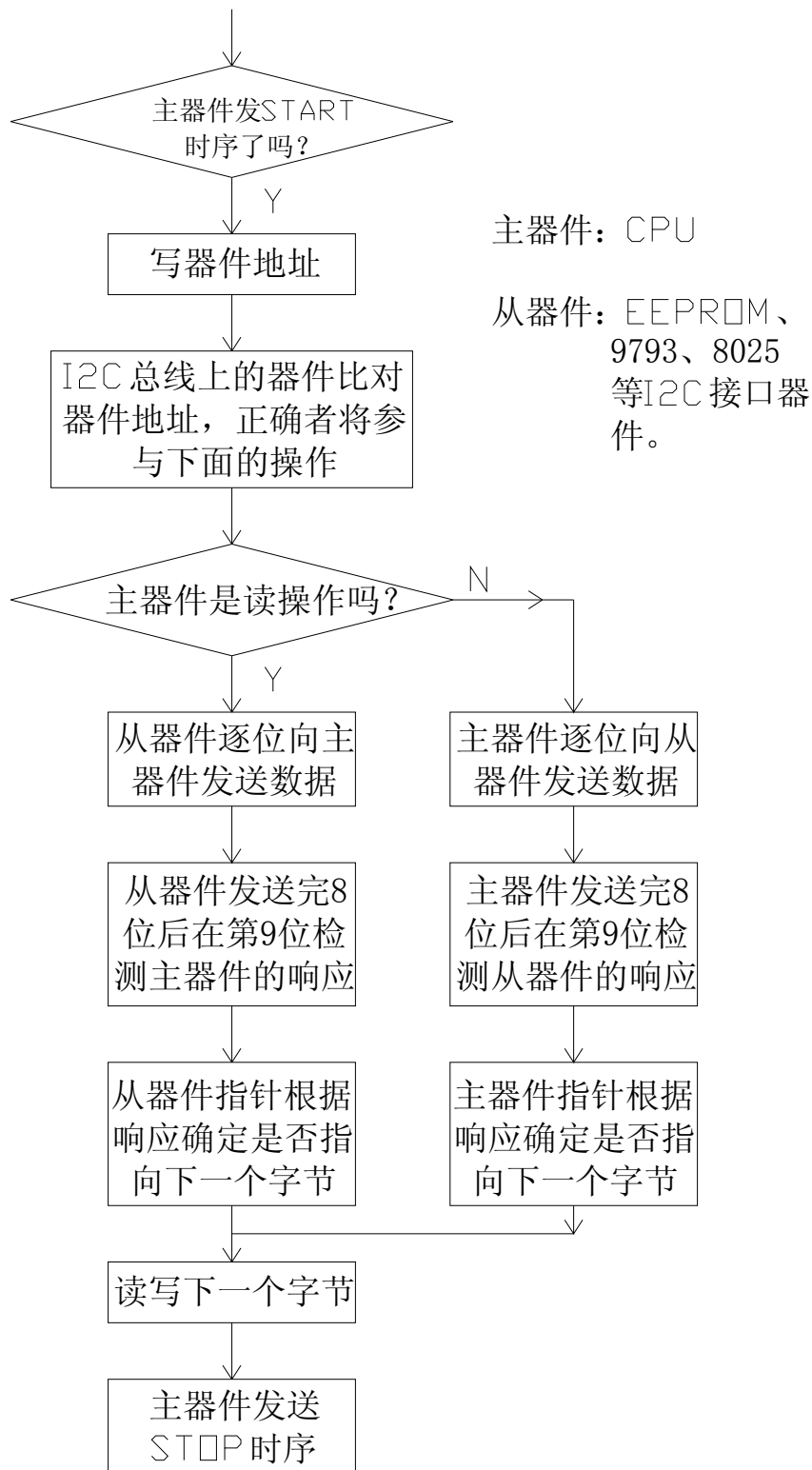
Number of pages	8 Byte	16 Byte	32 Byte
Product number	BR24L01A-W BR24L02-W	BR24L04-W BR24L08-W BR24L16-W	BR24L32-W BR24L64-W

The above numbers are maximum bytes for respective types. Any bytes below these can be written.

In the case of BR24L02-W, 1 page = 8 bytes, but the page write cycle write time is 5ms at maximum for 8byte bulk write.
It does not stand 5ms at maximum x 8 bytes = 40ms (Max.).

EEPROM timing is a standard I2C timing, in front of which has been mentioned in this reference is not tired, if you need detailed information, please go to the manual to find the data.

EEPROM流程图：



5.6 Infrared communication module

Infrared communication module Description: Infrared communication infra-red as a communications carrier, through infrared light spread in the air to transmit data, it is by infrared transmitter and infrared receiver to complete. In the transmitter, sending the digital signal through an appropriate modulation coding, the transformation into the electro-optical circuit, the infrared emission tube into infrared light pulses launched into the air; in the receiver, infrared receiver infrared docking Receiving light pulses to photovoltaic conversion, demodulation decoding recovery of the original signal. Infrared communication as a means of data transmission can be applied on many occasions, such as home appliances, entertainment facilities, infrared remote control, water, electricity and gas energy measurement, such as automatic meter reading.

Infrared communication in order to realize a thought: The next in the infrared receiver INTP2 mouth falling edge detection signal, if convinced, consider the position on the start bit, then the prohibition of INTP2 interrupted, started to do the ordinary I/O port, receive data, and its timing is achieved through the timer TM00, sender and recipient are in accordance with the timing TM00 agreed 833us timing started at the same time, the latter in every 833us, the the

data to send out one and receiver are received after the beginning of the signal in each receive a 833us period, when a byte of communications after the sender to send parity bit, the receiving party according to the agreement agreed to receive to determine parity bit to determine bytes received and sent from the same sender, and finally, sending side to send stop bit to tell the recipient, the end of the byte communication.

Infrared communication transmission byte format: one start bit, 8 data bits, 1 parity bit, 1 stop bit. Low the previous data, high in the post.

Infrared communication baud rate: 1200bps.

Baud rate calculation :

Pre-register sub-frequency mode PRM00 :

符号	7	6	5	4	3	2	1	0
PRM00	ES110	ES100	ES010	ES000	0	0	PRM001	PRM000
	ES110	ES100	TI010 引脚有效沿选择					
	0	0	下降沿					
	0	1	上升沿					
	1	0	禁止设置					
	1	1	上升沿和有效沿均为有效沿					
	ES010	ES000	TI000 引脚有效沿选择					
	0	0	下降沿					
	0	1	上升沿					
	1	0	禁止设置					
	1	1	上升沿和有效沿均为有效沿					
	PRM001	PRM000	计数时钟选择					
	0	0	f_{XP} (10 MHz)					
	0	1	$f_{XP}/2^2$ (2.5 MHz)					
	1	0	$f_{XP}/2^8$ (39.06 kHz)					
	1	1	TI000 引脚有效沿 ^{注*}					

备注 1. f_{XP} : 供给外围设备的时钟振荡频率
 2. (): $f_{XP} = 10 \text{ MHz}$

注 外部时钟要求一个比两个内部计数时钟(f_{XP})周期长的脉冲。

16-bit timer/capture compare register CR000 : CR000 is a 16-bit register, used for comparison here Register, CR000 settings with 16-bit timer/counter value of the TM00 constantly compared, when the value of equal generated interrupt request (INTTM000), at any time to respond to infrared transceiver service program byte frames.

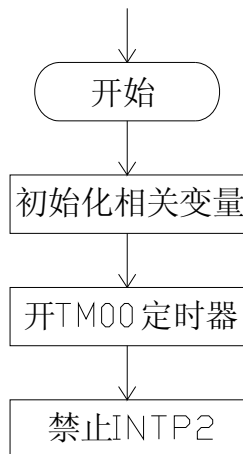
PRM00 = 0X01; settings TM00 count clock counter for 8MHz / 4 = 2 MHz, the cycle is 1 / 2 = 0.5us;

CR000 number will be able to let the baud rate to 1200bps it? TM00 timing means that the number of time periods, the communication of data 1, the baud rate for 1200 is 1 seconds to

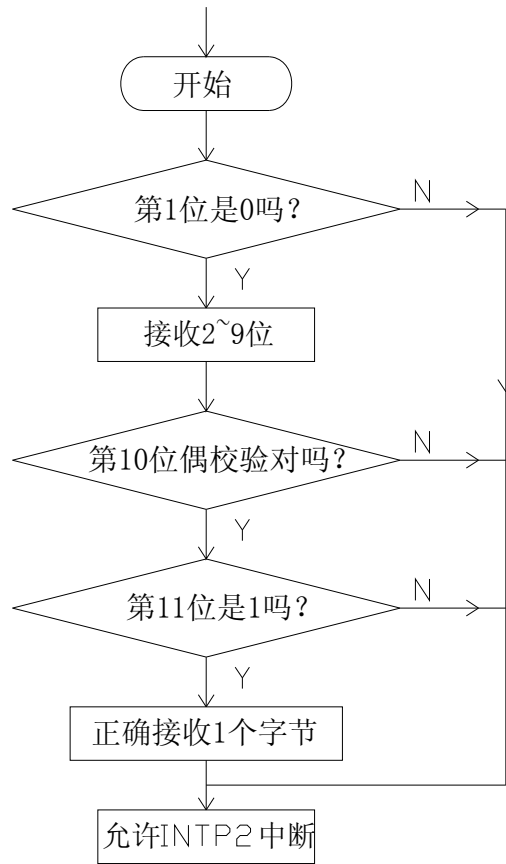
communications 1200, then used a communication 1/1200 seconds, that is 833us, so, TM00 timing period of 833 us, therefore, CR000 = $833/0.5 = 1666 = 682H$.

Infrared communication flow chart :

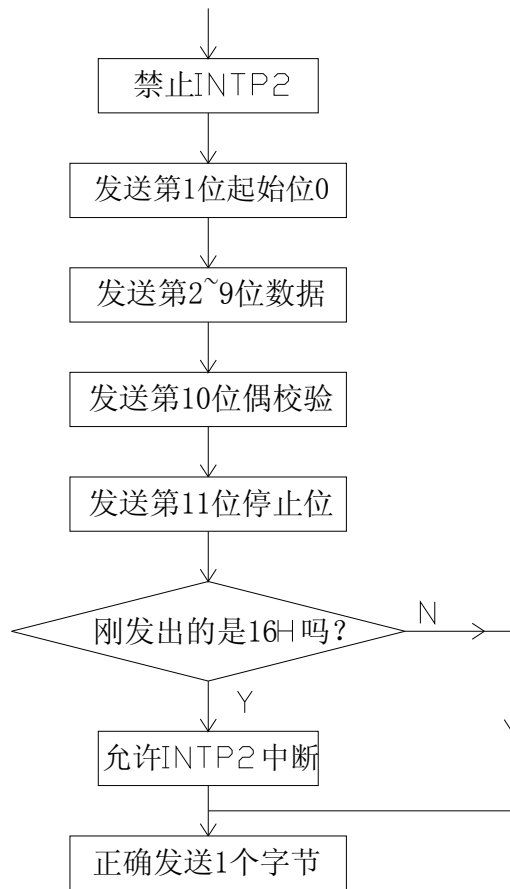
INTP2 红外中断口:



TM00 定时器中断口：接收数据



TM00 定时器中断口：红外发送数据



5.7 485 Communication Module

485 Communication Module Description: asynchronous serial communication widely applied to industry, the majority of RS-232 communications. 232 short communication distance, about ten meters, for long-distance communications, 232 through 485 interface circuit 485 is converted to the TTL-level, this can be achieved long-range communications (less than 1200 meters), so the use of 485 watt-hour meter. Communications prior to the relevant register in accordance with the communication byte

transmission format is configured so that data can begin to send and receive work. Its communication rate can be adjusted through programming. The entire communication process is through receive buffer register 6 (RXB6) and send the buffer register 6 (TXB6) to achieve, and the asynchronous serial interface reception error status register 6 (ASIS6) at all times to monitor the received data accuracy, asynchronous string line interface to send status register 6 (ASIF6) at all times to monitor the status of data distribution.

485 communication bytes transmission format: one start bit, 8 data bits, 1 parity bit, 1 stop bit. Low the previous data, high in the post. Here through the asynchronous serial interface operation mode register 6 (ASIM6) configured to be realized.

Infrared communication baud rate: 2400bps .

Baud rate calculation: Here we have adopted on-chip baud rate generator, it is necessary to register a choice of baud rate configurations. External hardware clock frequency of the shocks F_{xp} , through the clock selection register 6 (CKSR6) for sub-frequency reference clock generated F_{xclk6} , through F_{xclk6} reference clock baud rate generator control register 6 (BRGC6) set the UART serial port 8-bit counter sub - frequency value, to generate a clock frequency, the frequency is 2 times the baud rate.

Therefore, the formula for calculating the baud rate as follows :

$$\text{波特率} = \frac{f_{xp}}{2^n \times K}$$

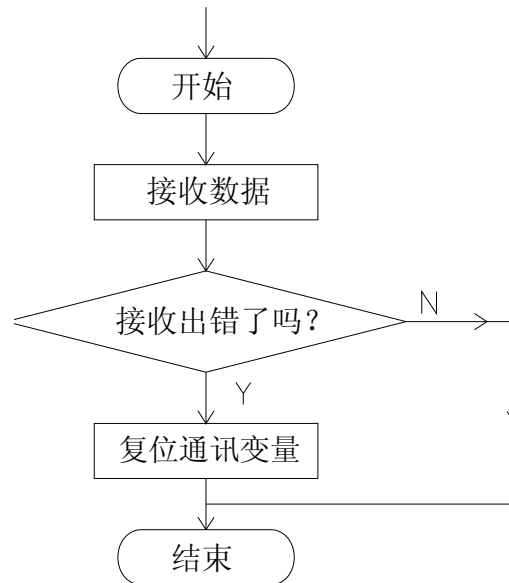
F_{xp}: external hardware clock frequency of concussion; clock generator configuration: Here is the processor clock control register PCC and pre-processor clock control register is configured to become a full-PPCC after zero, F_{xp} = internal high-speed clock concussion F_x (8MHZ) here F_{xp} = 8 MHZ, that is, the system clock .

2ⁿ: it is by the clock selection register 6 (CKSR6) configuration, where CKSR6 = 0x05; determine the n value of 5 .

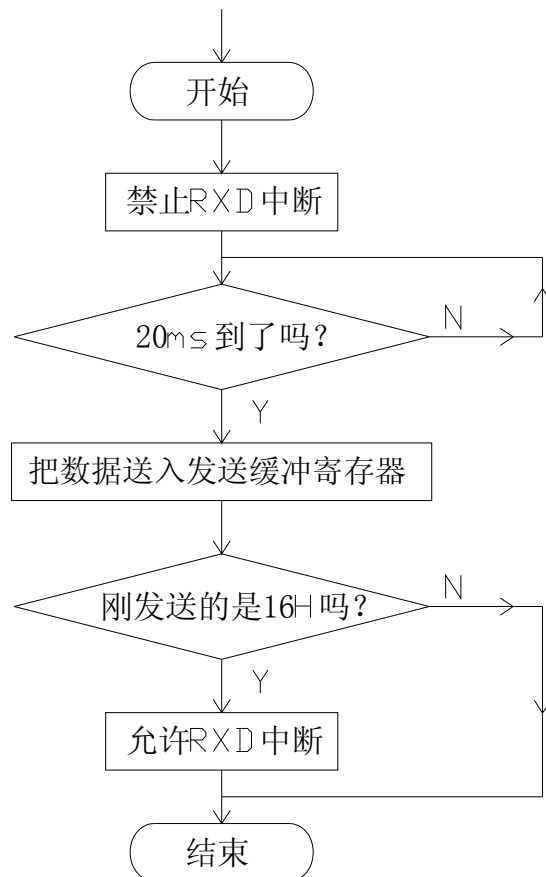
K: It is by the baud rate generator control register 6 (BRGC6) configuration, where BRGC6 = 52 hours, through the above formula and determine the relevance of the variable's value, you can calculate the baud rate = 2400.

485 communication flow chart:

RXD 中断口: 485接收数据



485发送数据:



5.8 Frame communication module

Communication module frame Description: 645 in the new statute, the definition of a data as follows :

Head er	Contro l code	Length L	DI0、 DI1、 DI2、 DI3 Data	Checkout & CS	The end of FU 16H
------------	------------------	-------------	----------------------------	------------------	----------------------

Header: 68 A0 A1 A2 A3 A4 A5 68

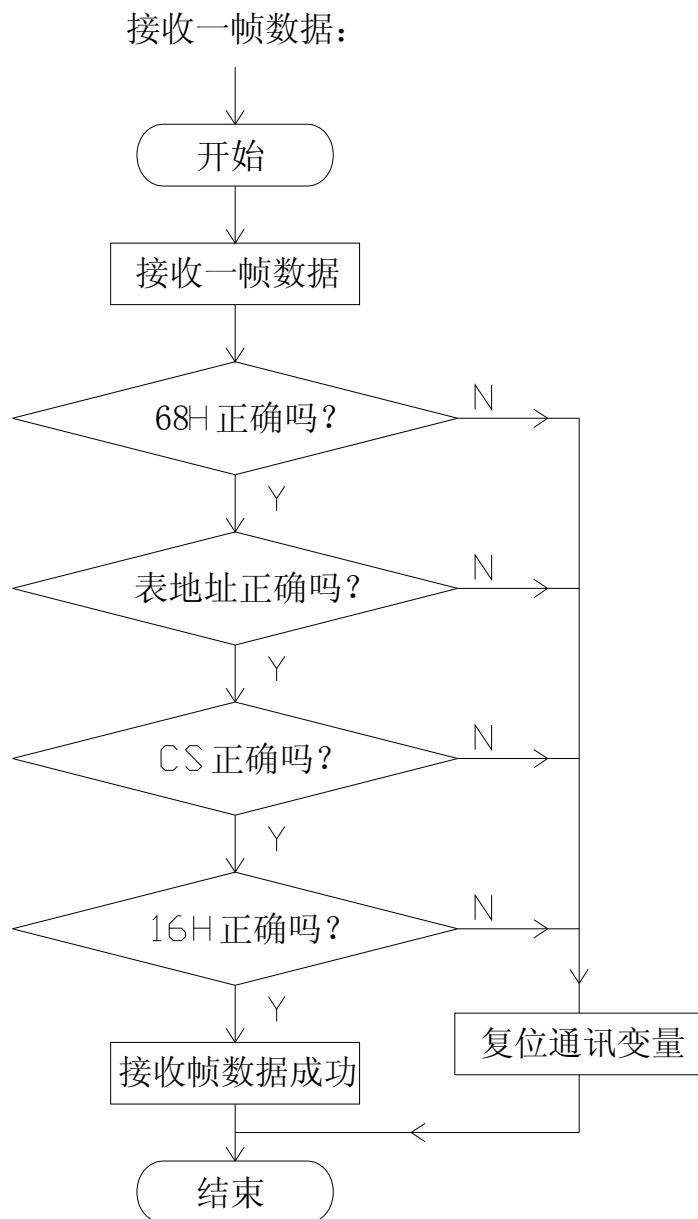
A0-A5 for meter code .

To receive data in a process: in receiving pre-FEH byte, if received by the first 68H, began to receive the Bureau meter number (address), close enough after seven bytes to determine the first 8 bytes whether it is the second 68H, if correct, we can continue to receive control code, and data length, the length of the data checksum CS can determine the location of CS in the admission before the end after all the data on these data checksum calculation, when the calculation of CS and CS received the same, it can be identified in front of all the data received is correct, simply click again to judge the end of the last address is 16H, if it is, this frame to receive all correct.

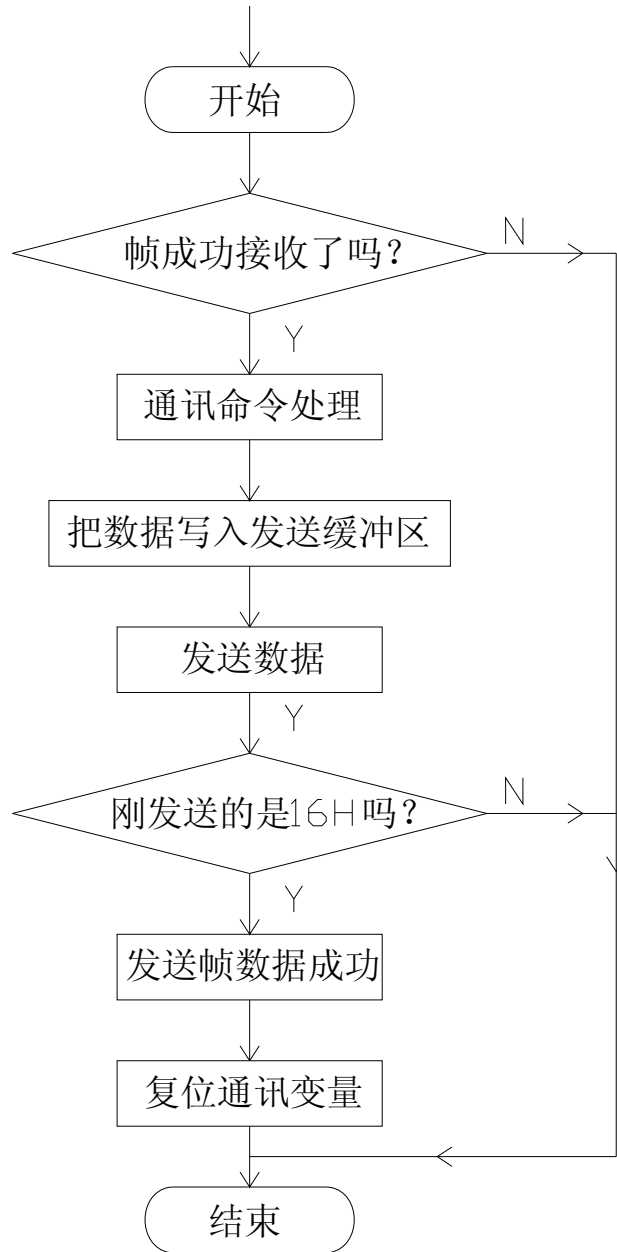
Preparation of data: When the implementation of the command after the completion of treatment, it is necessary to prepare relevant data, and placed in the send buffer.

Sending a data process: first send a preamble be FEH PC wake-up call, and then prepare to send the buffer zone where good data delayed by 20 milliseconds to send sent. When 16H sent after the reset communication variables.

Frame communication diagram



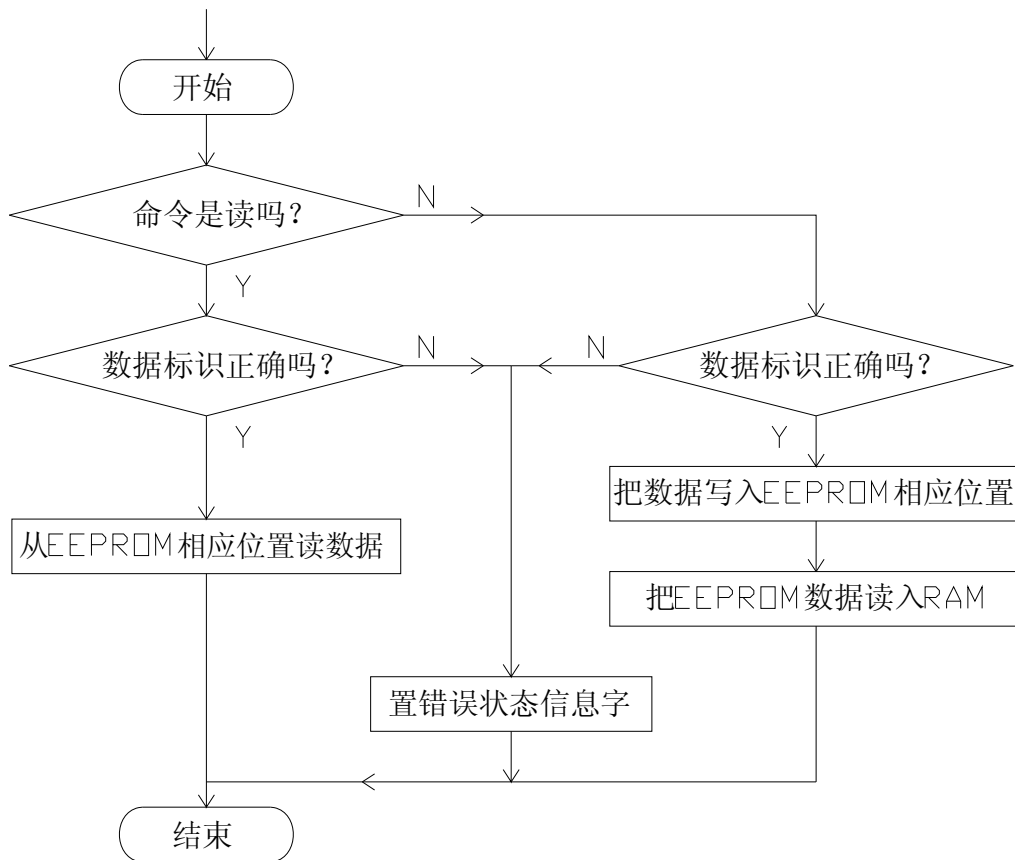
发送一帧数据：



5.9 Order processing module

Order processing module: the receiving module to receive a data Add to the receiving buffer, the program first to determine the authenticity of the address table, and then to determine the correct control code to determine the nature of the orders, if the order is written order, but also to judge the correctness of the password and hardware programming whether I shorted, only the password is correct and programming I shorted only permit-related events programming, event data is written into the use of first EEPROM, then read the data in EEPROM out to the RAM area, the completion of the correct programming operation; if the password is incorrect or programming I have not shorted, the program of related events will not be programmed, at the same time to return the relevant error code, or no response. At this point the command to complete a deal.

Treatment order diagram



5.10 4ms timer TM80 interrupt regular processing module

4ms timer TM80 interrupt regular processing module

Description: The module is interrupted to realize once every 4ms interval interrupt service routine, the need to regularly do the work, such as keyboard scanning, power direction, energy constant, the occurrence of such signals seconds. Here are the relevant timer configuration :

8-bit timer mode control register 80 TMC80 :

(1) 8 位定时器模式控制寄存器 80 (TMC80)

TMC80 用来允许或停止 8 位定时器/计数器 80 (TMS0) 的操作, 并可用来设置 TMS0 的计数时钟。

该寄存器可用 1 位或 8 位存储操作指令进行设置。

复位寄存器值清零

图 7-4 8 位定时器模式控制寄存器 80 (TMC80) 的格式

地址: FFCCH 复位后: 00H 读/写

符号 <7> 6 5 4 3 2 1 0

TMC80	TCE80	0	0	0	0	TCL801	TCL800	0
-------	-------	---	---	---	---	--------	--------	---

TCE80	TMS0 的控制操作	
0	停止操作 (TMS0 被清零)。	
1	允许操作。	

TCL801	TCL800	8 位定时器 80 的计数时钟选择		
			$f_{\text{XP}} = 8.0 \text{ MHz}$	$f_{\text{XP}} = 10.0 \text{ MHz}$
0	0	$f_{\text{XP}}/2^4$	125 kHz	156.3 kHz
0	1	$f_{\text{XP}}/2^5$	31.25 kHz	39.06 kHz
1	0	$f_{\text{XP}}/2^{12}$	7.81 kHz	9.77 kHz
1	1	$f_{\text{XP}}/2^{14}$	0.12 kHz	0.15 kHz

注意事项 1 定时器操作停止后必须对 TMC80 重新设置。

 2 第 0 位和第 6 位必须清零。

TMC80=0X84;//enable count,interval is 1/7.81KHz=128us, 配置
定时器的计数时钟为 7.81KHz。

8-bit compare register 80 CR80 :

(1) 8 位比较寄存器 80 (CR80)

8 位比较寄存器 80 用来将其设定值与 8 位定时器/计数器 80 的值进行比较，当 8 位比较寄存器 80 的值与 8 位定时器/计数器 80 的值相等时，产生中断请求信号 (INTTMS0)。

CR80 可通过一个 8 位的存储操作指令来设置。其值可为 00H—FFH。

复位后寄存器值不确定。

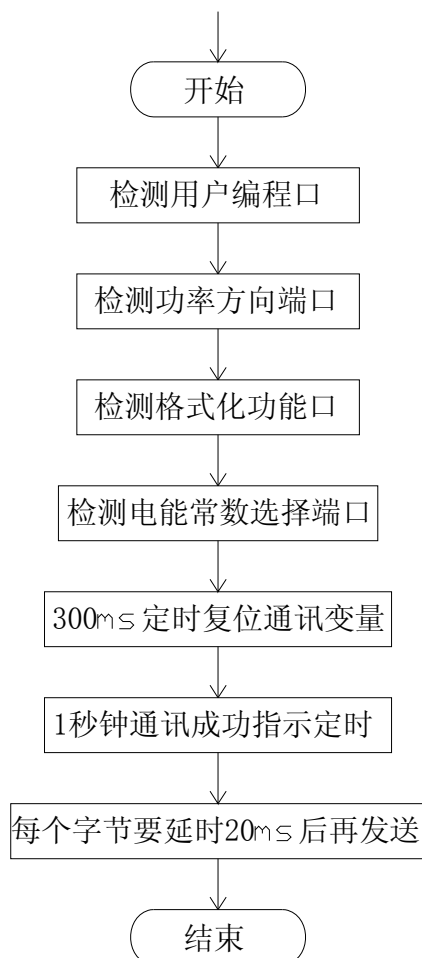
图 7-2 8 位比较寄存器 80 (CR80) 格式



注意事项 在定时器操作期间，不能改变 CR80 的值。如果在定时器操作期间改变 CR80 的值，则立刻产生中断请求信号。

CR80=0x20;//128us*32=4ms, TM80 configure the timing cycle for 4 ms.

4ms timer TM80 interrupt regular processing module flow chart:

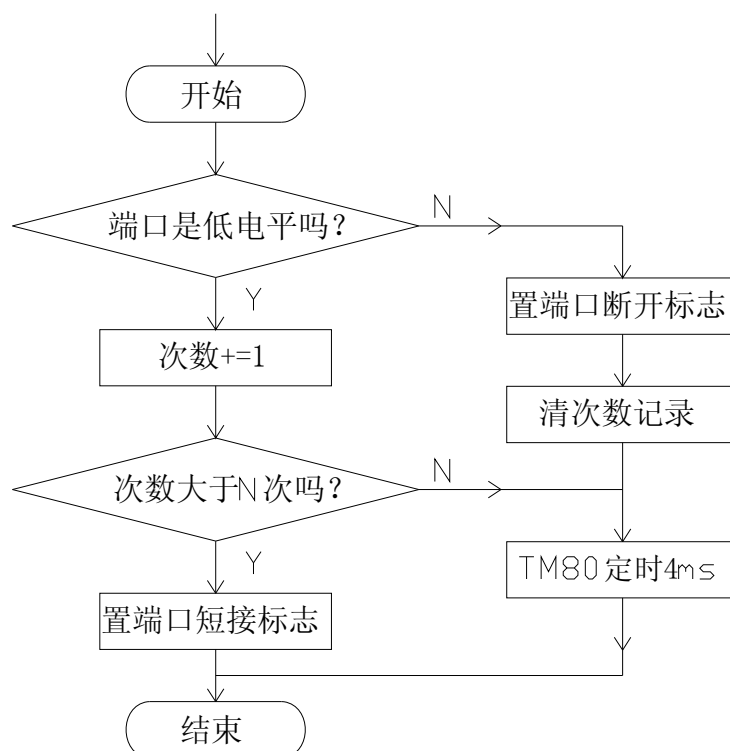


5.11 Port detection module

Port detection module Description: Detection of the substance of the port is the keyboard scanning, from time to time in order to achieve detection of a fracture state the purpose of the use of timer timing the interval between the completion of a period of time, so that might dispense with the software program code from time to time, and so in response to more timely, so simple and clear procedures.

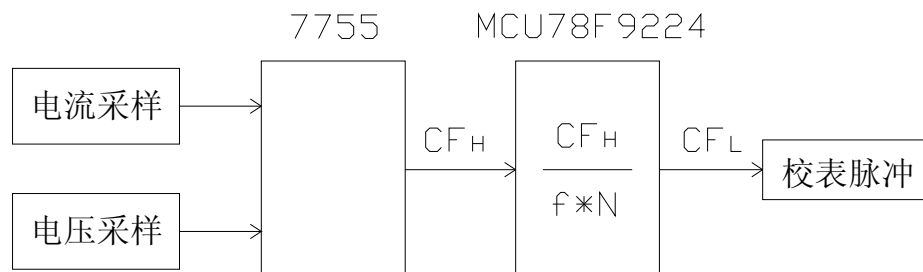
Port detection diagram :

TM80 定时4ms 中断入口:



5.12 Software School Table Module

Software School Table principle:



Automatic table functions: through infrared or 485 pairs of 7755 pulses of high frequency numerical adjustments, software school table.

Software on the school map is schematic form, the figure was 7755 of the CFH output high-frequency pulse, CFL is a single-chip microcomputer software school after the low-frequency pulses, namely, School Table pulse, f is the correction factor, N is equivalent to sub - frequency coefficient, the error in the test table for 0:00, the figure above correction factor $f = 1$, when the school for x when the error, $f = 1 + x$, x can be a positive number can also be negative. Software School table is calculated through the error correction coefficient, thereby changing the frequency coefficient, the realization of the frequency of CFL and standard tables are consistent.

Software form the formula for calculating school :

$$\text{div_CF_N} = \frac{10000 + \text{误差的整数} \times 100 + \text{误差的小数}}{10000} \times \text{div_CF_N0}$$

For example: error of 12.25, $\text{div_CF_N0} = 1122$,

$$\text{div_CF_N} = \frac{11225}{10000} \times 1122 = 1259.4450$$

Another example is: error is -12.25, $\text{div_CF_N0} = 1122$,

$$\text{div_CF_N} = \frac{8775}{10000} \times 1122 = 984.5550$$

As the single-chip does not support the 11225×1122 , so the calculation can only be carried out to large numbers into a smaller number, or the realization of multiplication into addition. See below formula:

$$\begin{aligned} \text{div_CF_N} &= 1122 + \frac{1200}{10000} \times 1122 + \frac{25}{10000} \times 1122 \\ &= 1122 + \frac{12}{100} \times 1122 + \frac{25}{10000} \times 1122 \\ &= 1122 + 134.\underline{64} \text{ (舍去)} + 2.\underline{8050} \text{ (舍去)} \\ &= 1258 \end{aligned}$$

As the MCU in FFFFH variable value is greater than 10000 in addition to computing an error, if error of the fractional part of a larger number, such as 85, then $85 \times 1122/10000$ can not be directly realized, therefore, divided by the operator, and than computing dividend minus the divisor can only be used many times to achieve.

The remainder will be discarded as a result of the loss of accuracy, resulting in software school table errors, so to calculate

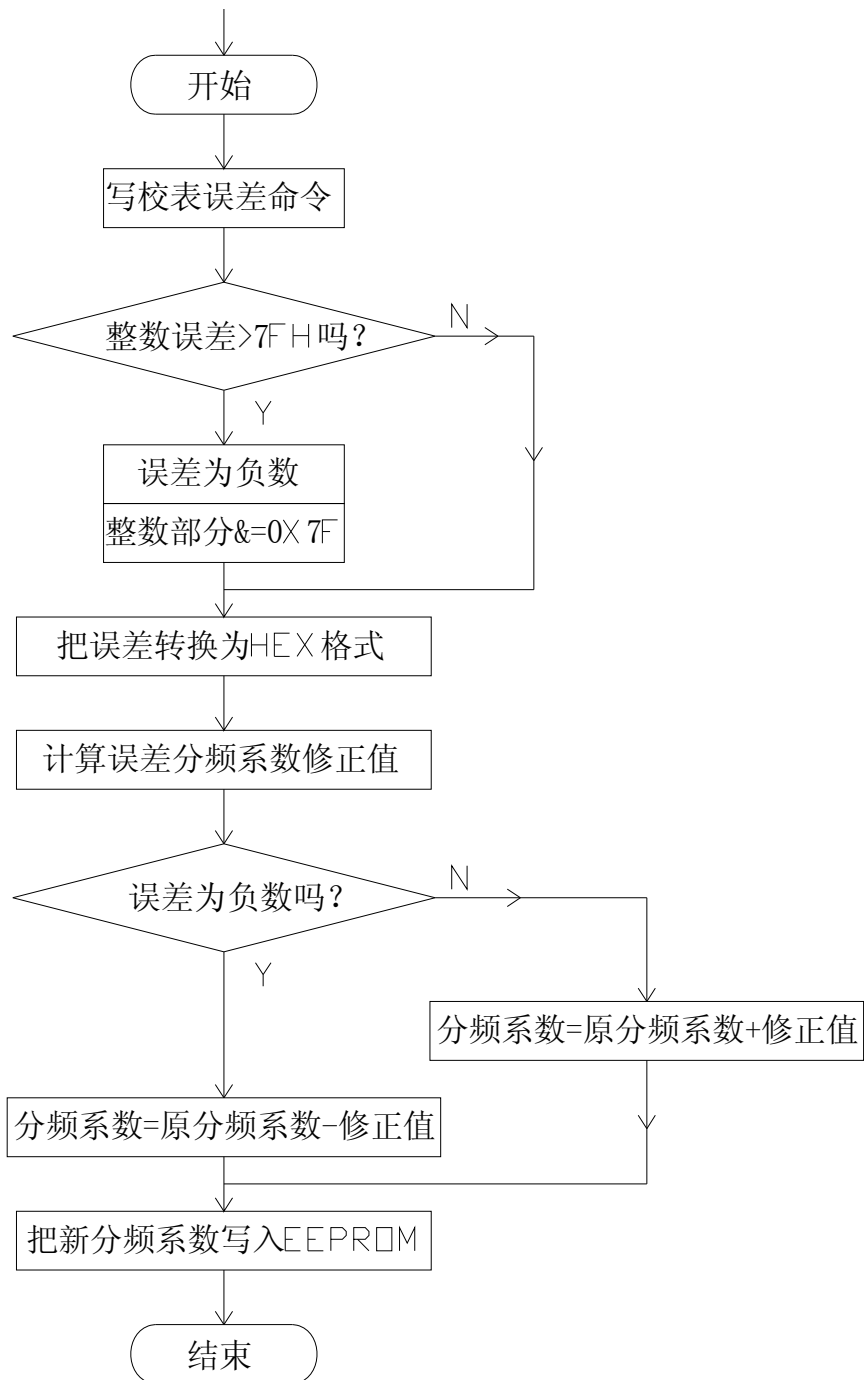
the balance, to achieve a one-off to a good error correction. The following formula shows this algorithm.

$$\begin{aligned} \text{div_CF_N} &= 1122 + 134.64 \langle \text{不舍去} \rangle + 2.8050 \langle \text{不舍去} \rangle \\ &= 1122 + 134 + 2 + \frac{6400 + 8500}{10000} \\ &= 1258 + 1.4900 \langle \text{四舍五入处理, 因为小于5000, 所以舍去} \rangle \\ &= 1259 \end{aligned}$$

School tables software error correction range: in the EEPROM format after less than $\pm 25.99\%$ in error, software, schools can form a good school; other cases, software can not guarantee the school table.

Software School Table error adjustment fineness: EEPROM in the format, the error of adjustment for fineness of 0.10%; other cases, regulation of uncertain size, but should be close to 0.10 percent.

School software program flow chart form:

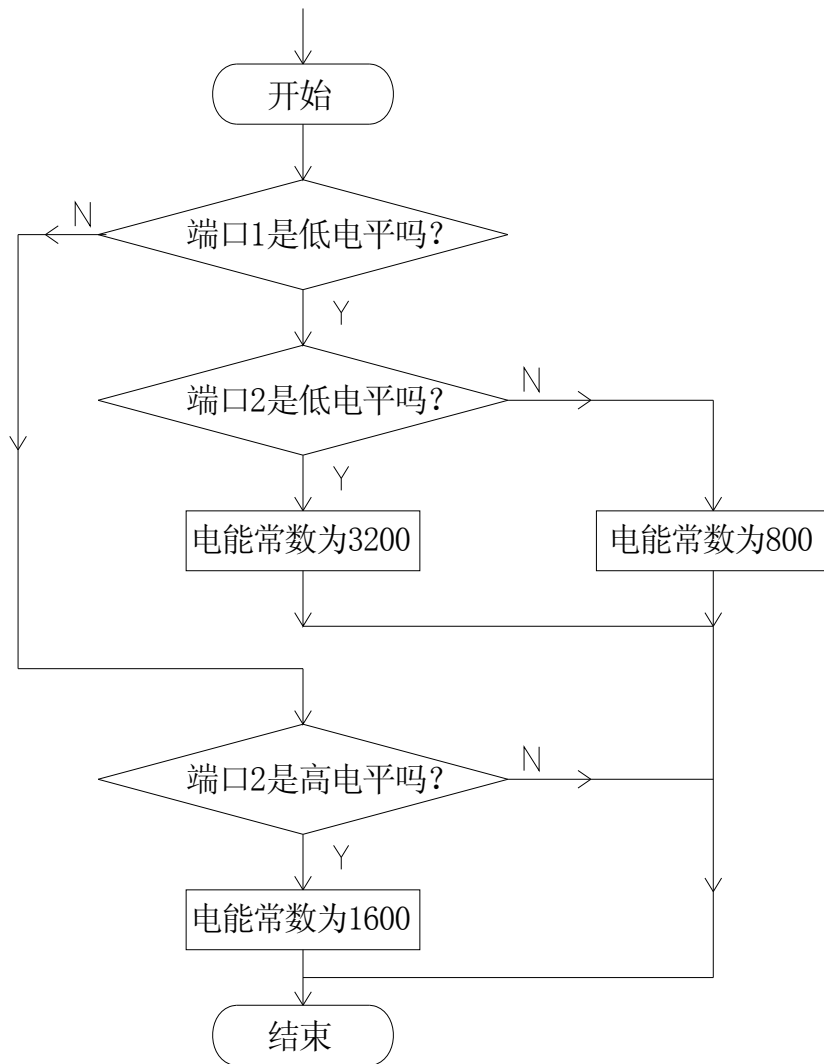


5.13 Constant power port detection module

Constant power port detection module Description: In order to achieve a common procedure, the way hardware configuration of the power energy meter constant, through the I/O port-level testing, to determine the current state of the corresponding energy constant, the measurement for the energy meter to provide standard scale. The module also used the substance to achieve TM80 regular 4ms interval scanning, real-time detection.

Constant power port detection diagram:

TM80 定时4ms 中断入口:

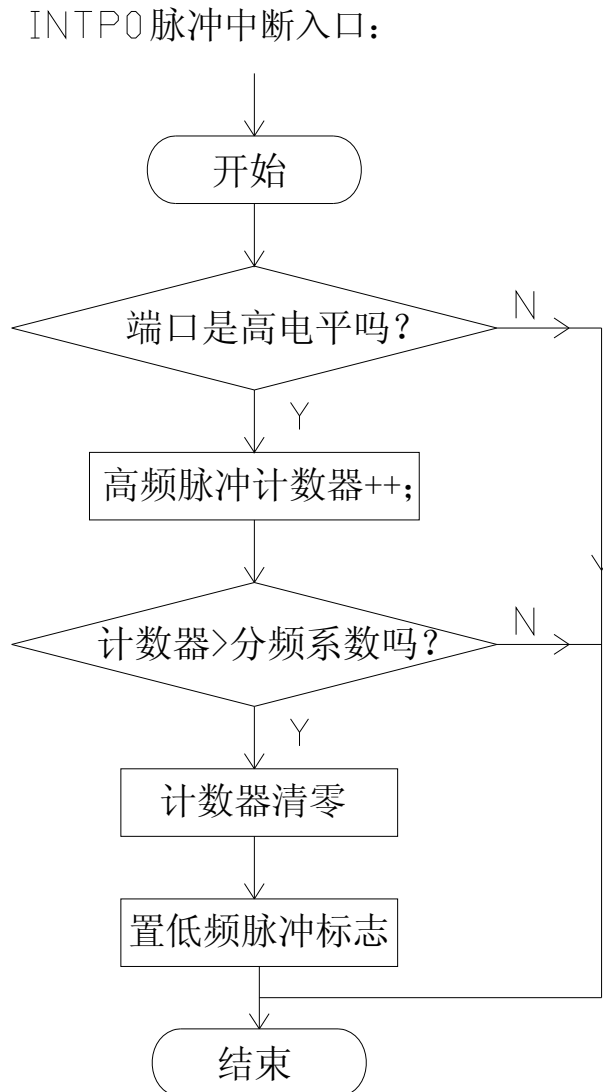


5.14 High-frequency pulse processing module

High-frequency pulse processing module port Description: Due to the high frequency of high-frequency pulse, pulse width of 18us, the way through the query easy to lose count of high-frequency pulse pulse, therefore, high-frequency sampling pulse interrupt mode to be adopted. When the high-frequency pulse count to the

frequency coefficient values, a low-frequency pulse will be generated.

Ports handle high-frequency pulse diagram:



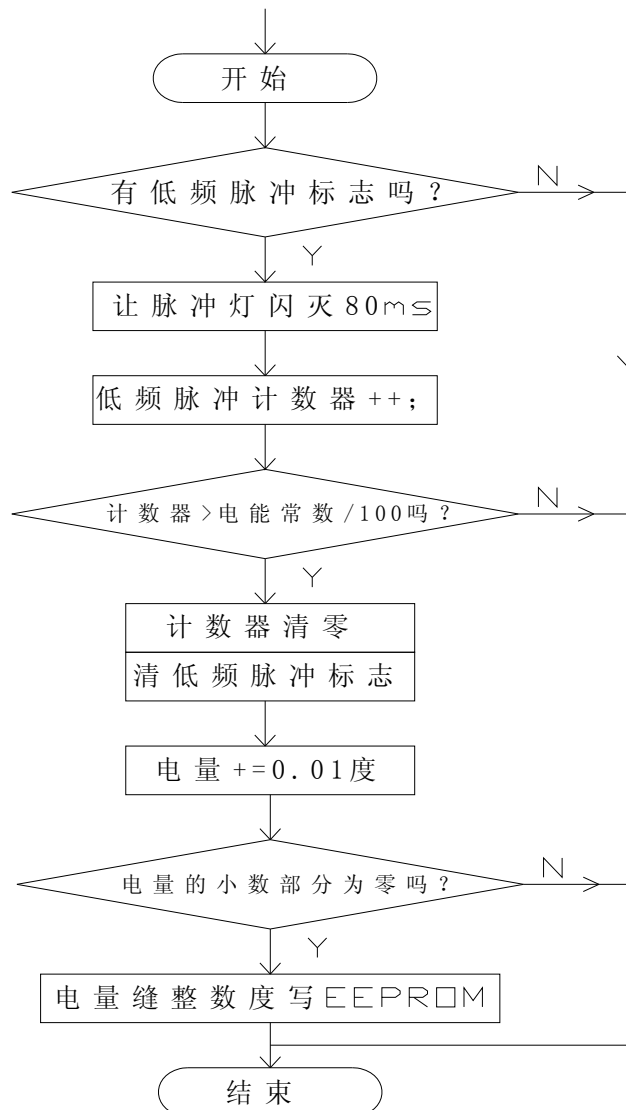
5.15 Low-frequency pulse processing module

Low frequency pulse treatment modules Description: After the arrival of low-frequency pulse, it is necessary to deal with it in real

time, using TM80 regular 4ms way to let the instructions of the pulse power lights flash out 80ms, to allow electricity to deal with some of the accumulated treatment, when the measurement of the binary, the to add the fractional part of 0.01 kWh, and then proceed to BCD code adjustment, part of the entire electricity consumption increased even moving, when the electricity to be binary integer, it is necessary to save on electricity raphe integer, write EEPROM.

Low frequency pulse treatment diagram :

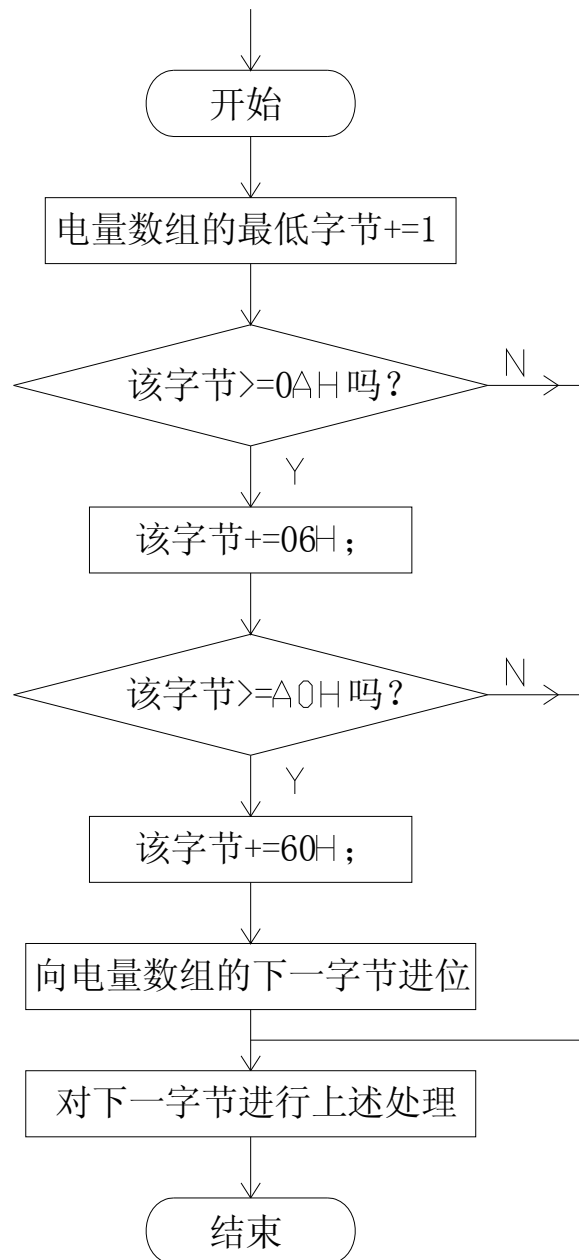
TM80定时4ms中断入口：



5.16 Power + = 0.01 degrees of the processing module

Power + = 0.01 degrees of the processing module Description:
The measurement of power is always part of the beginning of a few small, power-per-+ = 0.01 degrees, the decimal must be in accordance with the treatment algorithm, when the 10 o'clock to meet the seam on the hexadecimal A number of the system into one to achieve a few hexadecimal decimal algorithm.

Power + = 0.01 degrees handle diagram :



Chapter VI The list of programs

6.1 Variable naming rules

Software program naming a variety of variables, according to inspection, there is no naming convention for all the programmers agree that programming textbooks are generally not specified naming convention. Naming rules for software Products are not "the success or failure of death" thing, we do not spend too much energy trying to invent the world's best naming rules, but should develop a project to make the majority of members satisfied with the naming rules, and in project implementation.

Software program like this, single-chip process variable naming rules may even be impossible for the. But no matter how to rename the final text will be designed to look to know the meaning of the results, in order to ensure good readability of the procedure to facilitate maintenance.

This procedure is intended to comply with hope to know the principles of the text, in the procedures used English words or word the first few letters or letter combinations of words to name variables, and in proceedings related to the location of the Notes to be in English to ensure the readability of the program.

6.2 Variable list

Although the procedures are the explanatory notes in order to allow readers to better and faster understanding of variables, read the procedures to be here and then explaining the Chinese.

const unsigned char DI0_DI3_table [8] [5]; constant two-dimensional array form, used to store identification data and the corresponding data length.

const unsigned char address_table [8]; EEPROM data stored in the address table.

sreg struct serial_address s; structure variables, used to array or variable number of addresses to connect to together.

sreg unsigned char disp_buffer [10]; display buffer.

unsigned char received_data; used for temporary storage, or 485 to receive infrared data.

unsigned char id_error_num; password error number.

sreg unsigned char comm_err_msg; communications error status information word.

unsigned char clear_num; EEPROM cleared (that is formatted EEPROM) to detect low-level detection of port number.

unsigned char prog_num; programmed to detect low-level

detection of port number.

unsigned char power_dir_num; power port to detect the direction of detection of low frequency.

sreg unsigned char i_8bit; infrared transceiver needs a byte 11, 2 ~ 9 is the data bit, i_8bit on the data bit count.

sreg unsigned char i_11bit; infrared transceiver needs a byte 11, i_11bit this count to 11.

sreg unsigned char init_flags0; can be bit-addressable variables, used to store flag.

sreg unsigned char init_flags1; can be bit-addressable variables, used to store flag.

sreg unsigned char init_flags2; can be bit-addressable variables, used to store flag.

sreg unsigned char init_flags3; can be bit-addressable variables, used to store flag.

sreg unsigned char stage; to send and receive data in a count.

unsigned char datacounter; used to send and receive data in a CS positioning, addition and other features.

unsigned char byteinterval; in the communication process of

receiving, if the pause time between bytes is greater than 500ms, to give up receiving data, byteinterval for time 500 ms.

unsigned char sendbyteinterval; in communications send process, send interval is greater than 20 ms, sendbyteinterval for the 20 ms time.

unsigned char gotframe; to receive communications procedures to receive the return value, return value is 0, that receive an error for the one that received the N-byte, 2 received an express data.

unsigned char * dataptr; data pointer.

unsigned char irbyte; infrared transceiver buffer register.

sreg unsigned char datastring [30]; communication buffer.

unsigned long residue; more than a few, in the procedure to do summation using variables and then make dividend.

unsigned char energy_consant [2]; power constant.

unsigned int CFH_counter; high-frequency pulse counter.

unsigned int div_CF_N; sub-frequency coefficients.

unsigned char pulse_width_counter; low-frequency pulse width 80ms timer counters used.

unsigned char dispinterval; screen display interval of each variable.

unsigned char couter1pps; in seconds counter, for the time period-second count.

unsigned char screen; multi-screen display when the round screen

display counters, screen different values corresponding to different display content.

Etc.

6.3 Code

See program files <slightly>

- 本档所登载的内容有效期截止至 2009 年 12 月，信息先于产品的生产周期发布。将来可能未经预先通知而更改。在实际进行生产设计时，请参阅各产品最新的数据表或数据手册等相关资料以获取本公司产品的最新规格。
- 并非所有的产品和/或型号都向每个国家供应。请向本公司销售代表查询产品供应及其他信息。
- 未经本公司事先书面许可，禁止复制或转载本文件中的内容。否则因本档所登载内容引发的错误，本公司概不负责。
- 本公司对于因使用本文件中列明的本公司产品而引起的，对第三者的专利、版权以及其它知识产权的侵权行为概不负责。本文件登载的内容不应视为本公司对本公司或他人所有的专利、版权以及其它知识产权作出任何明示或默示的许可及授权。
- 本文件中的电路、软件以及相关信息仅用以说明半导体产品的运作和应用实例。用户如在设备设计中应用本文件中的电路、软件以及相关信息，应自行负责。对于用户或其他人因使用了上述电路、软件以及相关信息而引起的任何损失，本公司概不负责。
- 虽然本公司致力于提高半导体产品的质量及可靠性，但用户应同意并知晓，我们仍然无法完全消除出现产品缺陷的可能。为了最大限度地减少因本公司半导体产品故障而引起的对人身、财产造成损害（包括死亡）的危险，用户务必在其设计中采用必要的安全措施，如冗余度、防火和防故障等安全设计。
- 本公司产品质量分为：

“标准等级”、“专业等级”以及“特殊等级”三种质量等级。

“特殊等级”仅适用于为特定用途而根据用户指定的质量保证程序所开发的日电电子产品。另外，各种日电电子产品的推荐用途取决于其质量等级，详见如下。用户在选用本公司的产品时，请事先确认产品的质量等级。

“标准等级”： 计算机，办公自动化设备，通信设备，测试和测量设备，音频·视频设备，家电，加工机械以及产业用机器人。

“专业等级”： 运输设备（汽车、火车、船舶等），交通用信号控制设备，防灾装置，防止犯罪装置，各种安全装置以及医疗设备（不包括专门为维持生命而设计的设备）。

“特殊等级”： 航空器械，宇航设备，海底中继设备，原子能控制系统，为了维持生命的医疗设备、用于维持生命的装置或系统等。

除在本公司半导体产品的数据表或数据手册等资料中另有特别规定以外，本公司半导体产品的质量等级均为“标准等级”。如果用户希望在本公司设计意图以外使用本公司半导体产品，务必事先与本公司销售代表联系以确认本公司是否同意为该项应用提供支持。

（注）

- （1）本声明中的“本公司”是指日本电气电子株式会社（NEC Electronics Corporation）及其控股公司。
- （2）本声明中的“本公司产品”是指所有由日本电气电子株式会社开发或制造的产品或为日本电气电子株式会社（定义如上）开发或制造的产品。

详细信息请联系：

中国区

MCU 技术支持热线：

电话：+86-400-700-0606 (普通话)

服务时间：9:00-12:00, 13:00-17:00 (不含法定节假日)

网址：

<http://www.cn.necel.com/> (中文)

<http://www.necel.com/> (英文)

[北京]

日电电子(中国)有限公司

中国北京市海淀区知春路 27 号

量子芯座 7, 8, 9, 15 层

电话：(+86) 10-8235-1155

传真：(+86) 10-8235-7679

[深圳]

日电电子(中国)有限公司深圳分公司

深圳市福田区益田路卓越时代广场大厦 39 楼

3901, 3902, 3909 室

电话：(+86) 755-8282-9800

传真：(+86) 755-8282-9899

[上海]

日电电子(中国)有限公司上海分公司

中国上海市浦东新区银城中路 200 号

中银大厦 2409-2412 和 2509-2510 室

电话：(+86) 21-5888-5400

传真：(+86) 21-5888-5230

[香港]

香港日电电子有限公司

香港九龙旺角太子道西 193 号新世纪广场

第 2 座 16 楼 1601-1613 室

电话：(+852) 2886-9318

传真：(+852) 2886-9022

2886-9044

上海恩益禧电子国际贸易有限公司

中国上海市浦东新区银城中路 200 号

中银大厦 2511-2512 室

电话：(+86) 21-5888-5400

传真：(+86) 21-5888-5230

[成都]

日电电子(中国)有限公司成都分公司

成都市二环路南三段 15 号天华大厦 7 楼 703 室

电话：(+86)28-8512-5224

传真：(+86)28-8512-5334

[长春]

日电电子(中国)有限公司长春分公司

吉林省长春市朝阳区

西安大路 727 号中银大厦 A 座 1609 室

电话：(+86)431-8859-7533 / 8859-8533

传真：(+86)431-8680-2944

[大连]

日电电子(中国)有限公司长春分公司

大连市中山路 88 号天安国际大厦 2701 室

电话：(+86)411-8230-8815 / 8230-8825

传真：(+86)411-8230-8835

[青岛]

日电电子(中国)有限公司青岛分公司

中国山东青岛市宁夏路 288 号

G3 楼 607 室

电话：(+86)532-8872-7900 / 8872-7901

传真：(+86)532-8872-7902