# *KIT-V850E/PG2-IE*

**User's Manual (Rev.1.01)**

***RealTimeEvaluator***

## Software Version Up

* The latest RTE for Win32 (Rte4win32) can be down-loaded from following URL.
  http://www.midas.co.jp/products/download/english/program/rte4win_32.htm

## Notice



## Trademarks

# REVISION HISTORY

| | | |
|---|---|---|
| Rev.1.01 | Mar., 09, 2006 | 1st edition |

# CONTENTS

# 1. OVERVIEW

KIT-V850E/PG2-IE is a kit that performs in-circuit emulation for NEC RISC microprocessor V850E/PG2. Using a dedicated emulator chip in the kit has made it highly transparent, compact, and lightweight.

Connect the pod to the RTE-2000-TP or RTE-2000H-TP and use it. After this, by explanation which does not distinguish RTE-2000-TP and RTE-2000H-TP, these are named generically and it is described as RTE-2000(H)-TP.

This product comes with the following items:

1. V850E/PG2 pod : 1
2. RTE for Win32 setup disk : 1
3. User's Manual : 1
4. Power supply (RTE-PS04: +5 V/4.5 A) : 1
5. NQ Pack Set : 1 set
6. Support spacers and screws : 1 set

The main body which can use this product is as follows.

- RTE-2000-TP-x-x
- RTE-2000 H-TP-IF-IE80
- In the case of RTE-2000 H-TP other than RTE-2000 H-TP-IF-IE80
  Please use it after adding IF card (IF-IE80) of an option.

# 2. HARDWARE SPECIFICATIONS

Emulation

| | | | | |
|---|---|---|---|---|
| Target device | | | | V850E/PG2 (TQFP-100) |
| RTE-TP type to be used | | | | RTE-2000-TP, RTE-2000H-TP(with IF-IE80) |
| Emulation functions | | | | |
| | Operating frequency | | | 64 MHz (max.) |
| | Clock source | | | internal clock (4/5/8/16MHz) |
| | Internal ROM emulation capacity | | | 1 MB |
| | Internal RAM emulation capacity | | | 48KB |
| | Operation voltage | | | 3.3 V/+1.5V |
| Event function | | | | |
| | Number of events | | | |
| | | Setting of execution address | | 8 |
| | | Setting of data access | | 6 |
| | | | Address specification | Specifiable range |
| | | | Data specification | Maskable |
| | | | Status specification | Maskable |
| | | | Number of sequential unit stages | 4 |
| | | | Path counter | 12 bits |
| Break functions | | | | |
| | Hardware breakpoints | | | |
| | | Instruction/access breakpoints | | 2 |
| | | | Address specification | Maskable |
| | | | Data specification | Maskable |
| | | | Status specification | Maskable |
| | Software breakpoints | | | 100 |
| | Breaks that can be set using events | | | Supported |
| | Step breaks | | | Supported |
| | Manual breaks | | | Supported |
| | External breaks (High/Low edge) | | | Supported |
| Trace functions | | | | |
| | Trace data bus | | | 24 bits |
| | Trace memory | | | 24 bits × 256k words |
| | Trigger setting | | | |
| | | Trigger that can be set using an execution address | | Supported |
| | | Trigger setting by data access | | Supported |
| | | Trigger setting by event | | Supported |
| | | Trigger setting by external input | | Supported |
| | Start/stop specification (sub-switch) | | | Supported |
| | Trace delay | | | 0 - 3FFFF |
| | Time tag | | | 100 ns - 30 h |
| | Disassembled trace data display function | | | Provided |
| | Complete trace mode specification function (no real time) | | | Provided |
| Pin mask functions | | | | RESET- |

Host & interface blocks

| Item | Contents |
|---|---|
| Target host machine | DOS/V machine |
| Debug monitor | GreenHills Multi (Windows95/98/NT/2000) |
| Interface | PC-Card Type2 (PCMCIA Ver2.1/JEIDA Ver4.2 or later)<br>PCI bus<br>LAN/USB |
| Power supply | Dedicated power supply: RTE-PS04 (in: 100 V, out: +5 V, 4.5 A) |

# 3. INSTALLATION PROCEDURE

Install this product using the following procedure:

1. Installing the RTE-2000(H)-TP
   → Refer to the manual of the RTE-2000(H)-TP.
2. Connecting this product to the RTE-2000(H)-TP
   In the case of RTE-2000-TP
   →Connect the pod cable to the CPU-IF connector on the JTAG/N-Wire board module of the RTE-2000-TP.
   In the case of RTE-2000H-TP
   →Connect the pod cable to the ICE-IF(80) connector on the IF-IE80 board module of the RTE-2000H-TP.
3. A setup of SW on the pod
   → See Chapter 4 in this manual.
4. Connecting this product to a user system
   → See Chapter 5 in this manual.
5. Installing RTE for Win32
   → Refer to the manual of RTE for Win32.
6. Initializing RTE for Win32
   → See Chapter 6 in this manual.
7. Installing the debugger
   → Refer to the manual of the target debugger.

# 4. SETTING SWITCHES

SW1

| SW1 | Symbol | Function | Initial value |
|---|---|---|---|
| 1 | CKSEL | for a factory test(don't change) | OFF |
| 2 | PLLSEL1 | for a factory test(don't change) | ON |
| 3 | PLLSEL2 | for a factory test(don't change) | ON |
| 4 | CLK_HALF | for a factory test(don't change) | ON |

SW2

| SW2 | | | | Frequency of the clock inputted into CPU | The set value of the CKP register |
|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | | |
| OFF | OFF | OFF | OFF | Don't set up. | |
| ON | OFF | OFF | OFF | 4MHz | 1/1 |
| OFF | ON | OFF | OFF | 8MHz(initial value) | 1/2 |
| ON | ON | OFF | OFF | 16MHz | 1/4 |
| -- | -- | ON | OFF | Don't set up. | -- |
| OFF | ON | ON | ON | 5MHz | 1/2 |
| -- | | ON | ON | Don't set up. | -- |

**Don't set any values other than the combination of a table to the CKP register.**
**SW1 and 2 are the upper surface of a central board, and near the pod tip.**
**Please do not change a setup of those other than SW2.**

# 5. CONNECTING THIS PRODUCT TO THE USER SYSTEM

Connect this product to the user system using the following procedure.

Mounting the NQPACK

Solder NQPACK supplied with the product on the user system.

Turning the power on

1. Turn the power to the host personal computer on.
2. Turn the power to the RTE-2000(H)-TP on.
3. Turn the power to the V850E/PG2 pod on. (Connect the dedicated power supply Plug to the power supply jack.)
   Confirm that the LED_POWER indicating the power status of the pod comes on.
4. Turn the power to the user system on.
   Confirm that the LED_TON indicating the power status of the user system comes on.
5. Start up the debug monitor.

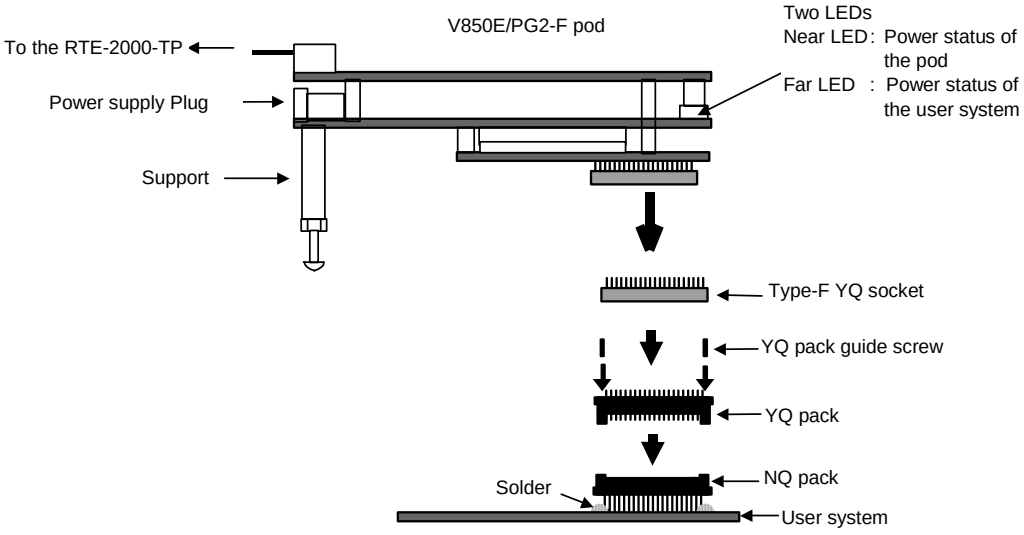
Turning the power off

1. Exit the debug monitor.
2. Turn the power to the user system off.
   Confirm that the LED indicating the power status of the user system goes out.
3. Turn the power to KIT-V850E/PG2-IE off. (Disconnect the dedicated power supply from the power supply jack.)
4. Turn the power to the RTE-2000(H)-TP off.
5. Turn the power to the host personal computer off.

[Caution]

When soldering the NQPACK on the board, be careful about the position of pin 1 because the orientation of the socket is determined. Use the ♦ mark.

The following figure shows how the V850E/PG2 pod is connected to the user system.



# 6. RTE for WIN32

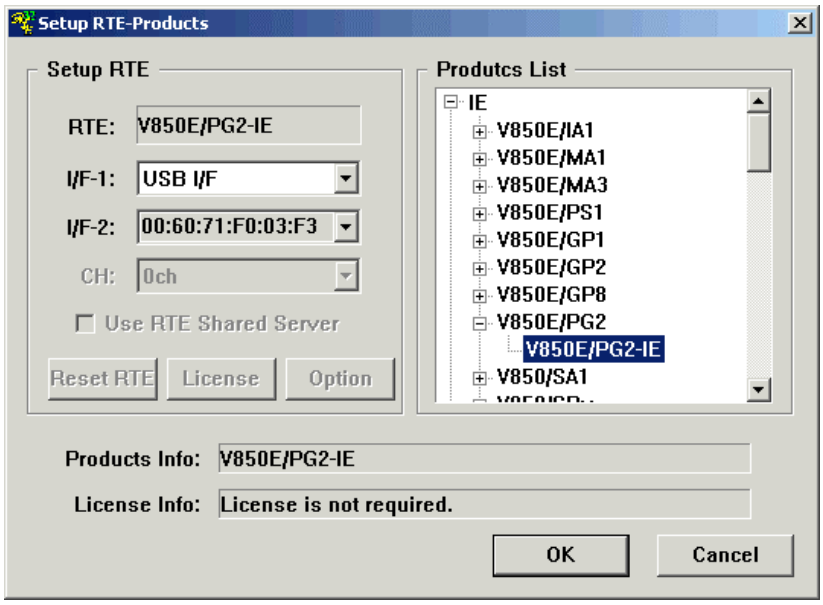
This chapter describes the setting of RTE for WIN32.

Invoking ChkRTE2.exe

After finishing to connect to the user system and apply the power supply for all equipments, invoke ChkRTE2.exe to set up the configuration of "RTE for WIN32".

Please set up the "RTE for WIN32" configuration at least one time for newly installed hardware.

<Setting up RTE-products>




<Selecting RTE>

From Product List, select the V850E/PG2-IE located beneath the IE tree.

<Selecting I/F-1, I/F-2>

Select and specify the host interface that suitable for your system from pull-down menu. (The display in example shows that USB-IF is assigned.)

**When you use it by RTE-2000H-TP, please use rte4win32 ver.6.00.xx or later.**

<Function test>

For the function test, RTE for WIN32 must properly be connected to the user system and capable of debugging. If you set up RTE and then perform a function test according to the screen instructions, the following dialog box appears upon the normal completion of the test. In this state, control from the debugger is possible.


**Perform the ChkRTE2.exe function test when the power to the user system is on if it is connected.**
**If the power is off, an error occurs.**

# 7. PRECAUTIONS

This chapter provides the precautions you should observe when using KIT-V850E/PG2-IE.

Precautions for connecting the user system

1) If the power to the user system is turned off in the break status, the ICE puts the CPU into the forced reset status and stops the output of the signal line to the user system. In this status, the user system cannot be controlled from the debugger. If you want to turn the power to the user system again, it is desirable to restart up this system from scratch in principle. To continue with debugging from necessity, turn the power to the user system on again and be sure to issue the initialize (init) command from the debugger. Then, set the CPU and debugger again. If the power to the target system is turned off, then on again after the debugger has started up, however, the debugger may hang up. In this case, restart up the system from scratch. Do not leave the RTE system with only the power to the user system turned off because this status may cause a failure in the user system or this product.

2) If the CPU in the user system fails to operate normally, the debugger may also fail to start up or hang up with specific commands.

Handling the pod

The entire circuit of the pod is exposed. Do not allow the circuit to come into contact with metals and others when it is energized. Otherwise, a failure may occur in the main unit.

Initializing the ASID register

Before using the emulator, set the value of the ASID register to 0x00 for future compatibility. If the emulator is used with the ASID register set to other than 0x00, a break function may be disabled.

Adjusting supports

The pod is designed so that supports can be mounted at its end. Adjust the supports so that the pod becomes parallel to the board on the user system when it is connected to the user system with the NQPACK.

**To adjust the height of a support, loosen the nut and slide the screw in or out.**
**After adjusting the height, tighten the nut to fix the screw position.**

The input of an external clock

A clock cannot be supplied from a user system.

Caution related to the delay time

Almost all signals are connected directly between the CPU in the pod and the user system. However, a delay of about 3 ns (typical) may occur due to the wiring length to the tip and the capacity, compared with direct CPU connection. Design the user system with accommodating this delay.

HALT instruction

When a break is made with the HALT instruction, the break address is the starting address of the instruction next to the HALT instruction.

Breakpoints

If a hardware breakpoint is set to the second instruction of an instruction string that simultaneously execute two instructions, it is invalid.

Measuring the execution time

The time command displays the execution time from the previous "execution to a break". The measurement value contains the overhead time (error of several CPU clocks). Note the following point:

→ If a breakpoint is set at the execution start address, the measurement error is doubled. To measure the execution time, remove the breakpoint at the execution start address.

The trace display under execution

A trace display is possible for the program executed in the space of internal ROM also in execution.

NQPACK set consumables

(1) 100-pin type-F YQ socket
YQS-100SDF

(2) 100-pin YQ pack
YQP-100SD with guide screws

(3) 100-pin NQ pack
NQP-100SD

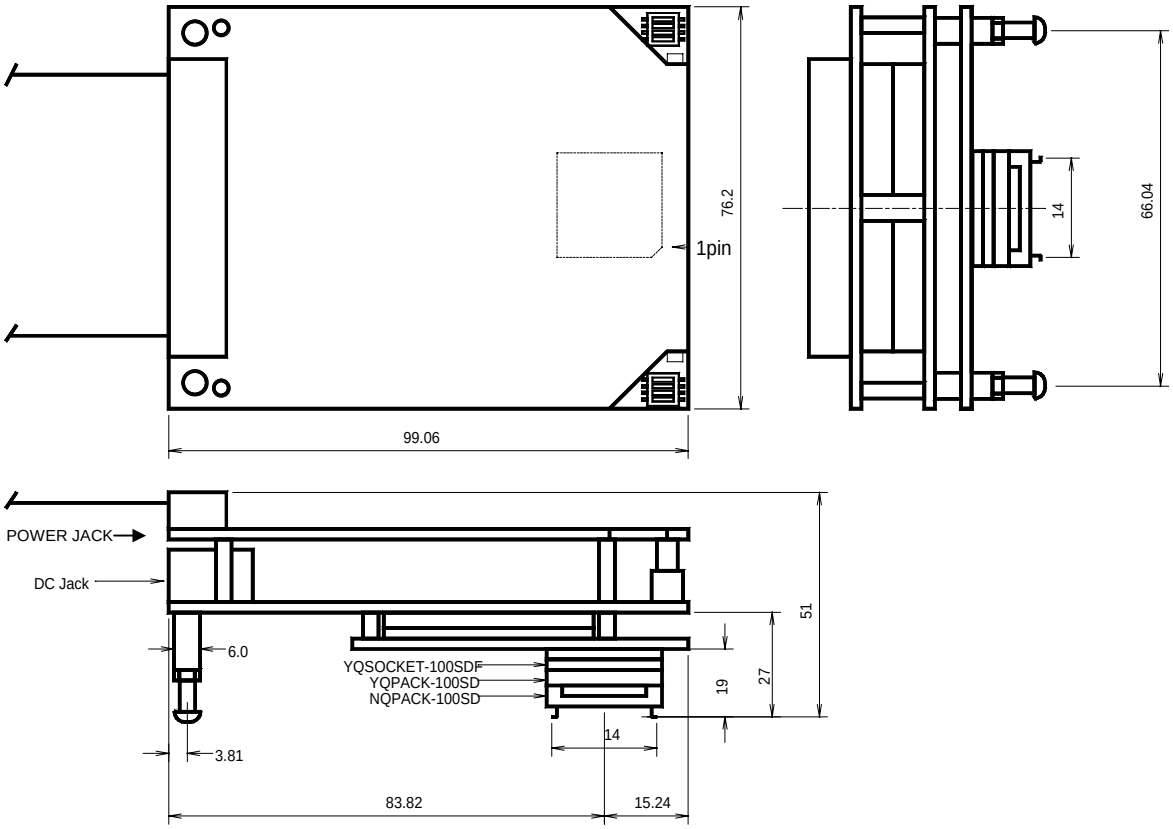
**[Remark]**

The sockets shown above are consumables. They should be replaced regularly, for example after about 50 cycles of insertion/removal. However, a soldered socket at the lower surface of the V850E/PG2 pod cannot be replaced. If it is expected that it is subjected to frequent insertion/removal, install a 208-pin YQ socket previously for protection purposes.

Other information

Be sure to refer to the Release Note and other manuals if provided.

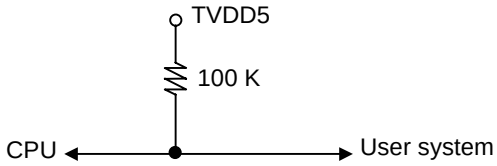
## APPENDIX A. PACKAGE DRAWING OF THE POD SECTION



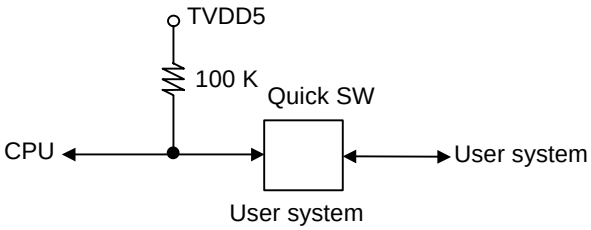

Unit: mm

## APPENDIX B. USER INTERFACE CIRCUITS

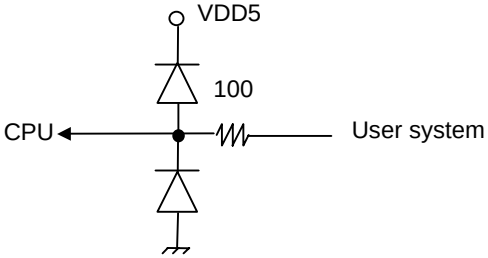
Port 0, Port 1, Port 2, Port 3, Port 5, Port 6



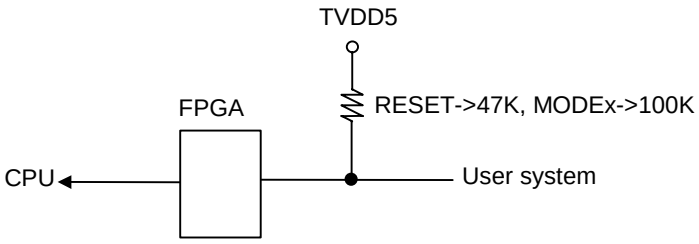

Port 4



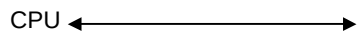

ANI001-ANI011, ANI101-ANI111



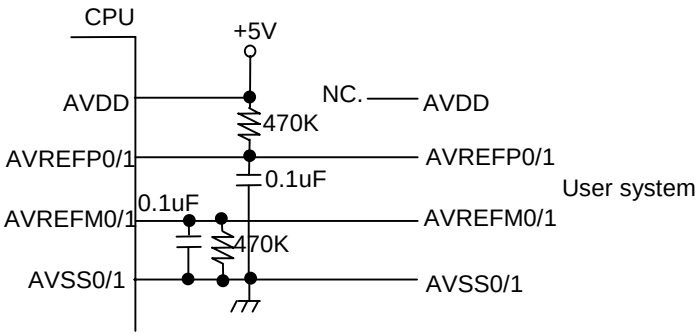

RESET-, MODEx



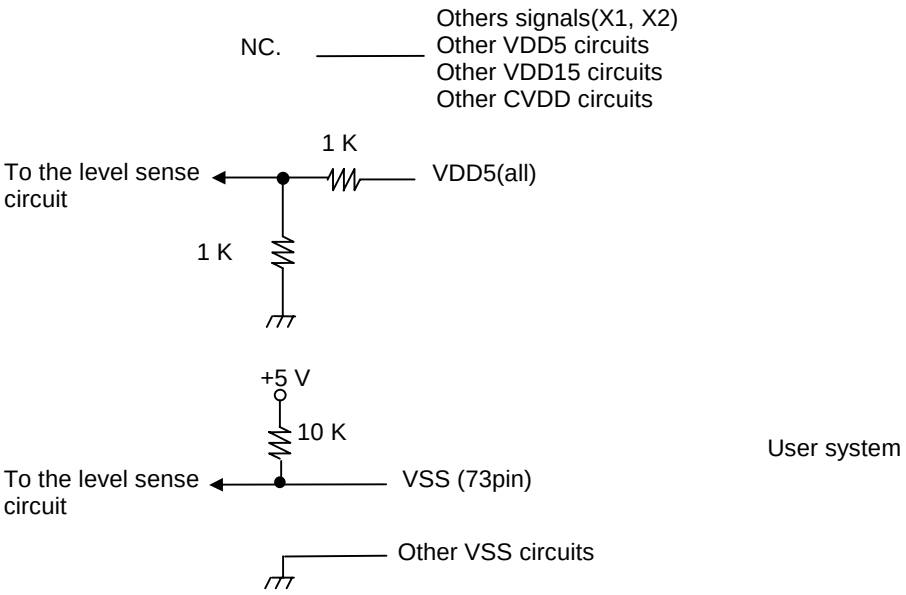
CLK_DBG




AVDD, AVREF0/1, AVSS0/1




VDD5, VDD15, VSS, and others




**Remark:** TVDD5 is an internal power supply equivalent to a 5-V power supply in the user system.

# APPENDIX C. DETAILS OF TRACE FUNCTIONS

This appendix describes the real-time trace function.

Overview of trace function

The real-time trace function writes the details of the execution (trace data) output from the CPU in the trace buffer in the ICE for each execution. You can check the data using the trace command.

You can set the trace mode, trace start condition, trigger condition, section condition, qualify condition, and other conditions to specify the loading of trace data.

For the flow of loading trace data, see Figures 1 and 2.

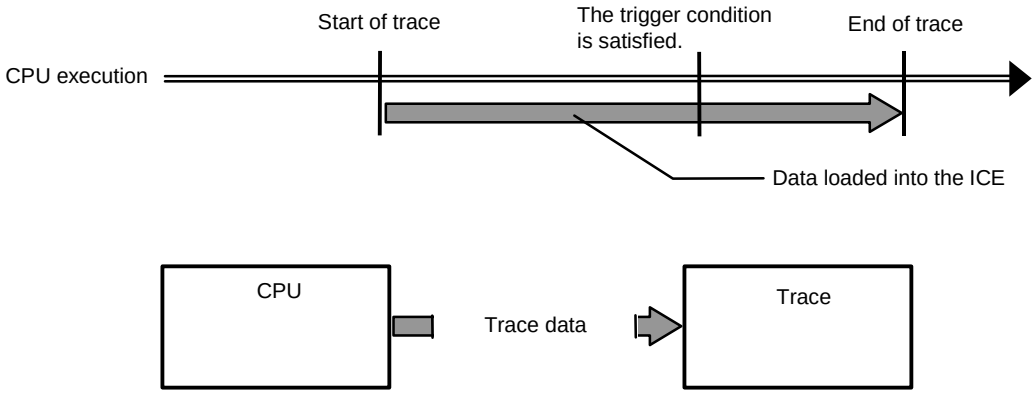



Figure 1 Flow of loading trace data

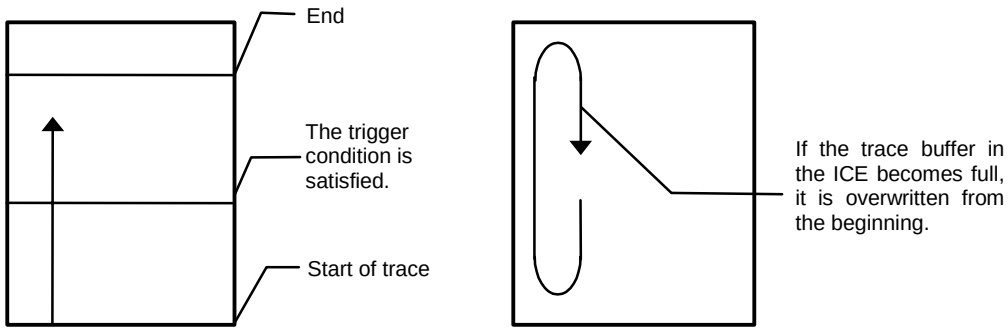



Figure 2 Trace data in ICE

Delay count

The delay count means the number of cycles in which trace data is to be loaded after the trigger condition is satisfied (Figure 3). The number of cycles differs depending on the type of CPU execution. One cycle is not one execution unit.

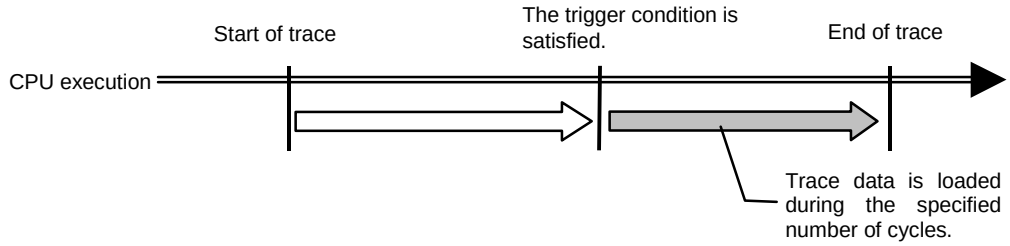



Figure 3 Flow of delay count

Trace execution mode

In **the real-time mode**, trace data is loaded with priority given to the CPU execution. If the trace buffer (FIFO) in the CPU becomes full, part of trace data may not be loaded (Figure 4).

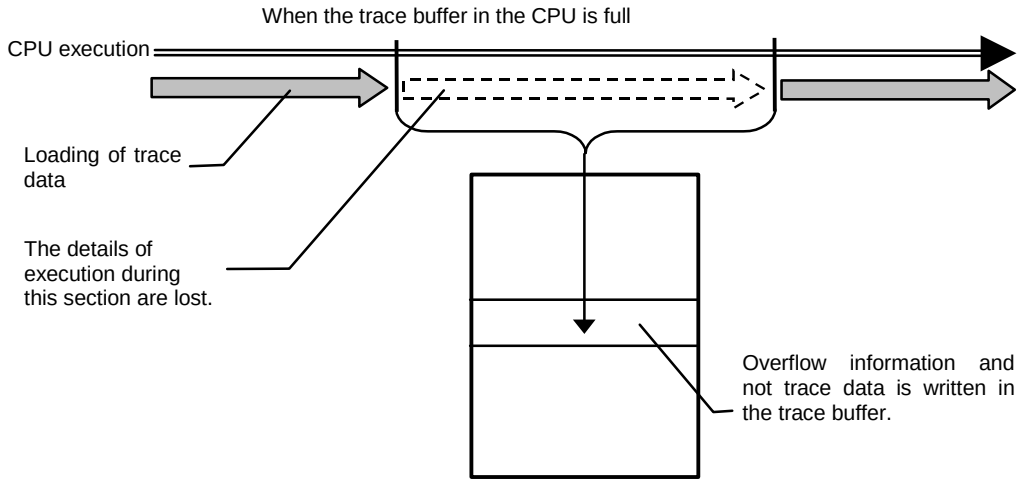



Figure 4 Real-time mode

In **the non-real-time mode**, all trace data can be loaded. If the trace buffer (FIFO) in the CPU becomes full in this mode, the CPU execution is temporarily stopped and is automatically restarted (Figure 5).

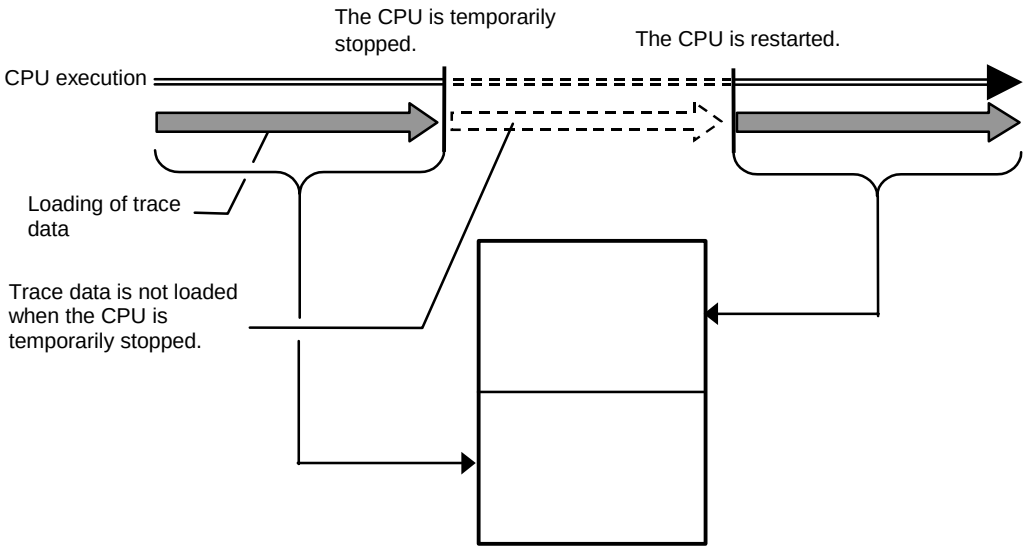



Figure 5 Non-real-time mode

Sub-switch, section, and qualify

The sub-switch indicates whether OR or AND (set by tenv [subor|suband]) of the section and qualify conditions are satisfied (on) or not (off). You can specify cycles in which trace data is to be loaded according to the on or off status (sswon/sswoff command). By specifying cycles in which trace data is to be loaded for sswon and nothing to be loaded for sswoff, the on/off status of this sub-switch corresponds to the start or stop of trace. (The initial value of the sswon/sswoff command is as described above. In the description below, these commands are assumed to be set to their initial value.)

You can specify a section using the tsp1 and tsp2 commands and evt secon and secoff parameters. Use tsp1 and secon to specify that a section is established (on) and tsp2 and secoff to specify that a section is not established (off).

The event condition specified for qualify in the evt command is used as a qualify condition. When the event condition is satisfied, the qualify condition is also satisfied.

Starting trace

To start loading trace data, the following methods are available: Forced start method (tron force) and the method using the status of the sub-switch according to the section and qualify setting. (Figure 6)

To set the loading condition using the sub-switch, use sswon and sswoff. Usually, specify cycles in which trace data is to be loaded for sswon and nothing to be loaded for sswoff. According to this setting, trace data is loaded in the sub-switch on state and the loading of trace data is stopped in the sub-switch off state.

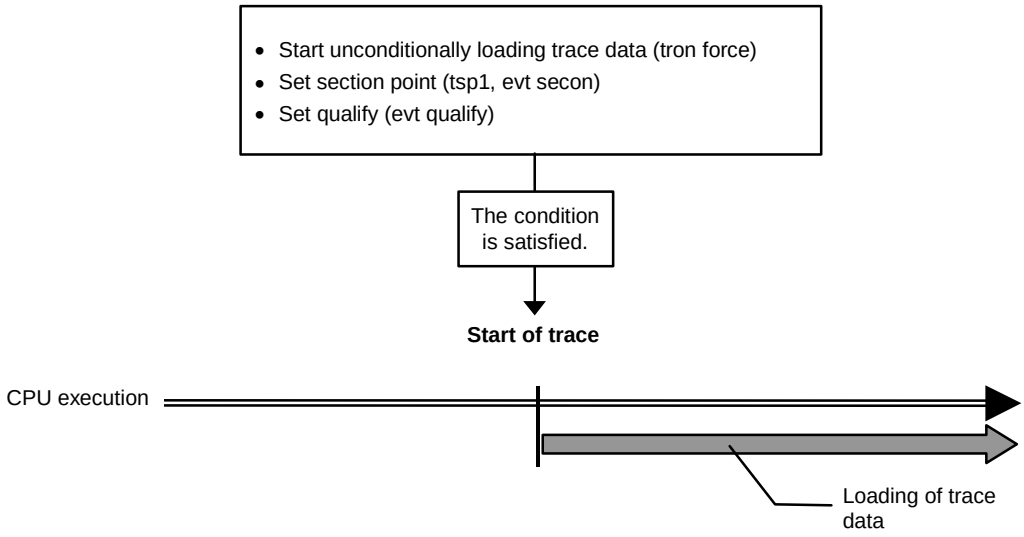



Figure 6 Starting trace

Trigger condition

A trigger condition is used as the start point of delay count (Figure 7). You can set a trigger condition to check the details of the execution before and after the trigger.

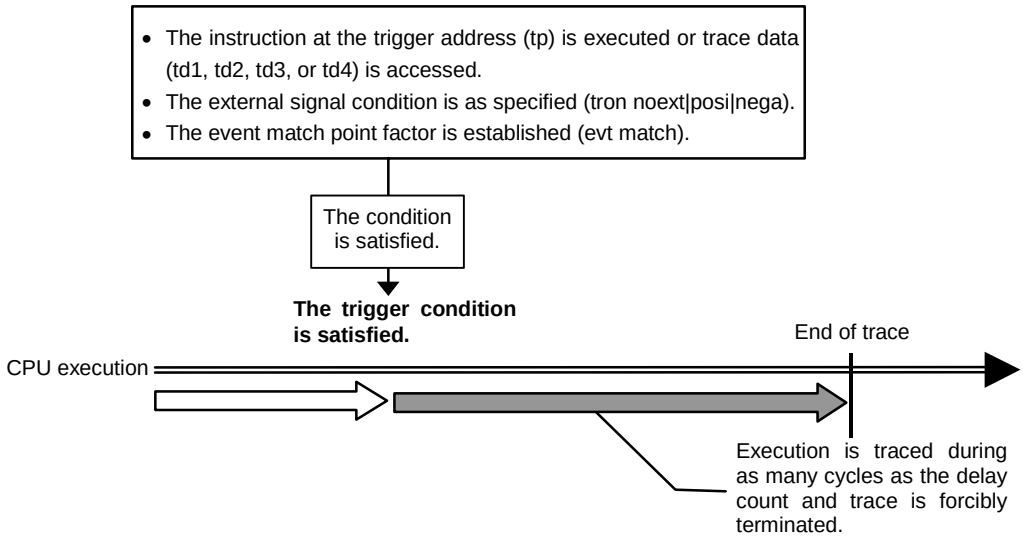



Figure 7 Trigger condition

Stopping trace

To stop loading trace data, use the status of the sub-switch according to the section and qualify setting. (Figure 8)

To set the loading condition using the sub-switch, use sswon and sswoff. Usually, specify cycles in which trace data is to be loaded for sswon and nothing to be loaded for sswoff. According to this setting, trace data is loaded in the sub-switch on state and the loading of trace data is stopped in the sub-switch off state.

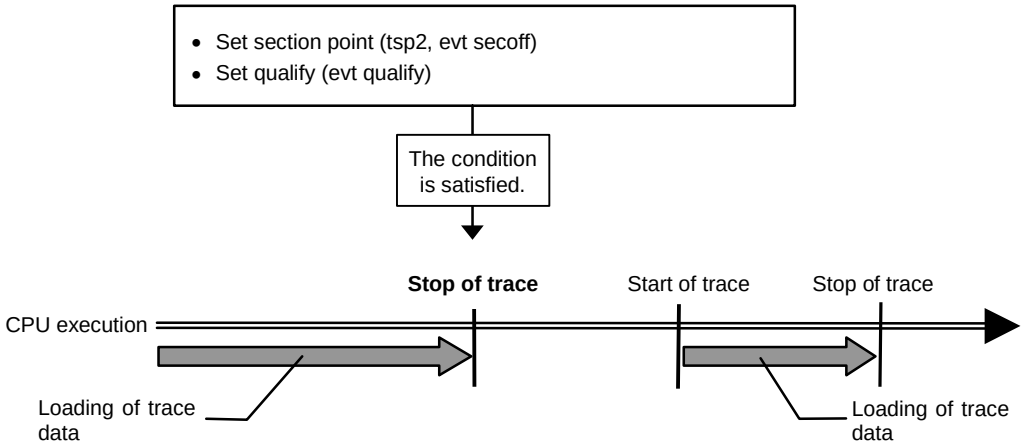



Figure 8 Stopping trace

Terminating trace

After trace is terminated, no more trace data is loaded.

When the end condition is satisfied, unlike the stop condition, trace is not restarted (Figure 9).

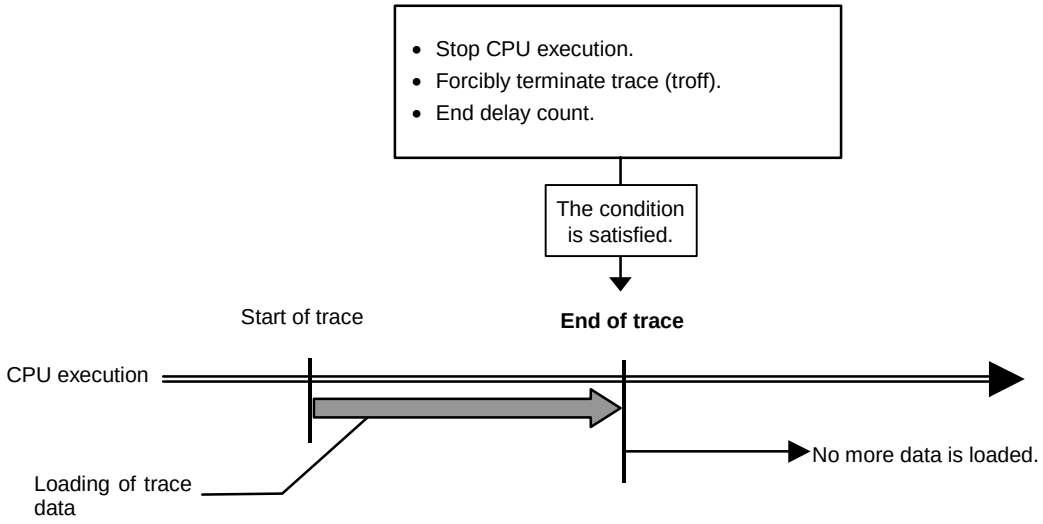



Figure 9 Terminating trace

Forced delay mode

In the forced delay mode, trace is forcibly terminated when trace data is loaded during the specified delay count (number of cycles) after the start of trace. In this mode, the trigger condition is ignored (Figure 10).

When CPU execution starts, trace is started in this mode.

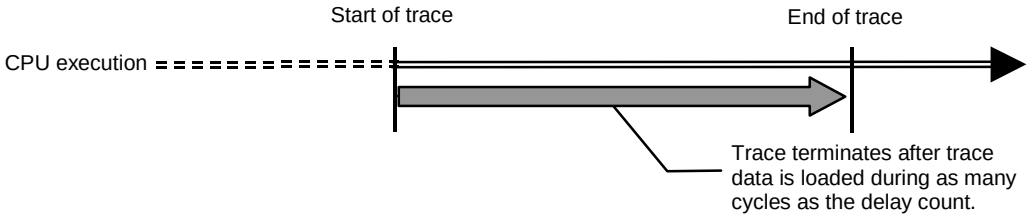



Figure 10 Forced delay mode