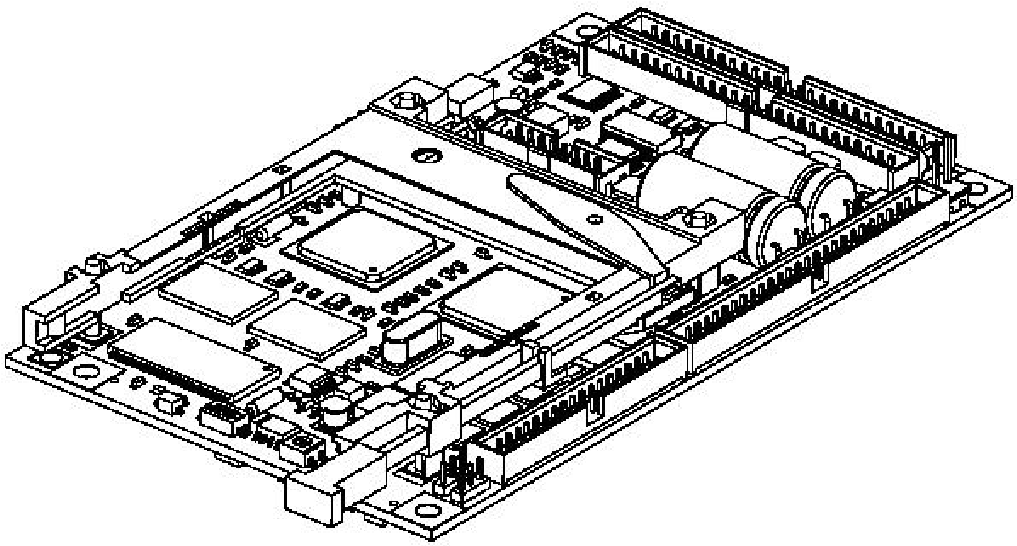
BitsyX
User's Manual



ADS document # 110115-00033, preliminary

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About the Cover Image

The cover image shows a Rev 2 BitsyX populated with the supercapacitor option.

Printing this Manual

This manual has been designed for printing on both sides of a 8.5x11 inch paper, but can be printed single-sided as well. It has also been optimized for use in electronic form with active cross-reference links for quick access to information.

Revision History

REV	DESCRIPTION	BY
1	Preliminary release	12/15/03 ak
1-2	Created from document 110114-10017-3 Incorporate doc. 110115-00031-1 changes: Change references to StrongARM SA-1110 to XScale PXA255 Add section about MMC controller (4.5.5) Add section for J7 (3.3.7) and note in 2.1.2 Update processor pin cross-reference table (4.1.6) with new PXA255 signals Update Serial section (4.5.1) with information about XScale serial control Update I^2C section (4.5.4) with information about XScale interface Rewrite section 5.2 to incorporate XScale Turbo mode Add notes about system wakeup by keypad in section 5.3.3 and [tbd]Revision History Update revision history for board revision 2	4/25/03 ak
1-3	Add 64 MiB flash and footnote about availability (1.2.3) Add section 5.3.3, *System Sleep* Add note about Vsleep and wakeup (5.3.4) Edit Note 4 about Vsleep (6.2.1) Correct Note 12 (6.2.2) to indicate that Vee and Vcon available concurrently Removed audio *Line Out* section (4.4.2) Remove Pvee parameter (6.2.2) Change DCIN_POS parameter to VBATT_POS, reduce minimum voltage from 6 to 5 V and add note 15 (6.2.4). Add sleep current notes 16 and 17 (6.2.4) Removed I^2C parameters with no values (6.2.6) Removed USB current control parameters (implemented on personality board) (6.2.8) Update drawings text to specify BitsyX Update codec drawing to 4202 (6.2.9)	4/28/03 ak

1-4	Condense PCMCIA/CF description (1.2.3) Correct PCMCIA misspelling Correct typo: LLD to LDD Change Compact Flash to CompactFlash; add trademark Footnote 4 Correct spacing before some parentheses Update USB feature description (1.2.4) Correct USB_PWR_SENSE description (4.5.2) Lower specification voltage for Vsleep (6.2.1) Add Vsleep,hyst parameter and note (6.2.1) Indicate that PD0 and PD1 are for dedicated functions and not available for general purpose use (3.3.9, 4.3.7) Widen this section (Document Revision History) Update cover image to rev. 2 BitsyX Update mechanical drawing and make note of slight mechanical changes between Bitsy Plus A and BitsyX 1(6.1.1, 7.2.2)	5/1/03 ak
1-5	Complete Revision History differences both from Bitsy Plus and BitsyX Update IRQ table (RqOnOff and IRQ1) (4.1.4) Add notes about EIOn digital I/Os (6.2.10) and remove EIOn notes from controller section (6.2.7). Update processor signal cross-reference with EIOn signals (4.1.6) Update LED control section to indicate that LED is driven by system controller, not CPU (3.1.2). Update system drawing to PXA255, change codec connection (1.3)	5/2/03 ak
2	Second preliminary release	5/2/03 ak
2-1	Update I^2C section (4.5.4) with architecture drawing and BitsyX architectural details; add I^2C specs for PXA255 (6.2.10)	5/12/03 ak
2-2	Update display 12-bit color mapping (4.6.4) Remove "ADSmartIO I^2C" from RTC section (4.2) Clarify that PC6 and PC7 are dedicated to I^2C, but that they can be configured as digital I/Os for custom applications (footnote 13)	5/13/03 ak
2-3	Correct Bitsy Personality Board part number in sections 4.5.2 and 5.5.3. Note in Revision History (7.2.2) that USB hardware change requires change in operating system driver	5/14/03 ak
2-4	Correct L_FCLK signal name (J1 and 4.1.6) Change LDDn signals to L_DDn Add mating connector and footnote for J7 (3.3.7) Add information about serial ports used as 3.3 V CMOS (4.5.1) Add LCD control signals to display cable section (4.6.4) Add section 6.1.4, *Production Options* Correct J3 changes in 7.2.2 ("Changes from BitsyX revision 1") Add note about MMC driver availability (4.5.5) Correct VDDI voltage range (6.2.4). Add notes about Vddi voltage scaling (5.2.2, 5.3.1) Correct Vddi label in power supply diagram (5.3.1) Add picture of typical development system (2.1.1)	6/17/03 ak
2-5	Add note that it's not recommended to use ADSmartIO I^2C for new designs (4.5.4)	6/20/30 ak
3	Third preliminary release	6/20/03 ak

Table of Contents

1 Introduction

1.1 Overview

The BitsyX is a full-featured single board computer using the PXA255 XScale RISC microprocessor and SA-1111 Companion Chip. The BitsyX is designed to meet the needs of embedded and graphical systems developers.

This manual applies to Revision A of the BitsyX. The revision history of the BitsyX is listed in chapter 7.

1.2 Features

1.2.1 Processor

- PXA255 32-bit XScale
- SA-1111 Companion Chip
- Clock rates up to 400 MHz
- Battery-Backed Real-Time Clock

1.2.2 Power Supply

- 6-15 V Input Range
- Battery Trickle Charger

1.2.3 Memory

- 16, 32, 64 or 128 [1] MiB[2] synchronous DRAM
- 8, 16, 32 or 64 [3] MiBFlash
- PCMCIA and CompactFlash[4] (CF), Type I and II, 3.3 and 5 V
- Supports CF cards with optional personality board

1.2.4 Communications

- USB 1.1 Host port (low 1.5 Mbit/s and full 12 Mbit/s speeds) and full speed Client port
- Three Serial Ports

  Serial 1: RS-232, 3.3V CMOS (9-wire)

  Serial 2: 3.3V CMOS (3-wire); IrDA and RS-232 with optional personality board

  Serial 3: RS-232, 3.3V CMOS (5-wire)

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[1] The BitsyX supports 128 MiB SDRAM. However, those components are not yet commercially available as of April 2003.

[2] MiB is the IEC abbreviation for mebibyte = 2^{20} byte = 1 048 576 byte. The kibi and mebi abbreviations are based on the 1998 IEC standard for binary multiples. For further reading, see the US NIST web site, http://physics.nist.gov/cuu/Units/binary.html

[3] The BitsyX supports synchronous and asynchronous flash. The 64 MiB flash option is available only in synchronous flash.

[4] CompactFlash is a trademark of the CompactFlash Association, http://www.compactflash.org/.

- 10/100BT Ethernet, RJ45 (with optional personality board)
- CompactFlash Interface (with optional personality board)

1.2.5 User Interface and Display

- Flat Panel Interface
- Software-Controlled VEE Generator for passive LCD contrast control
- Analog Touch Panel Interface (four- or five-wire options)
- External PS/2 Keyboard Support

1.2.6 I/O

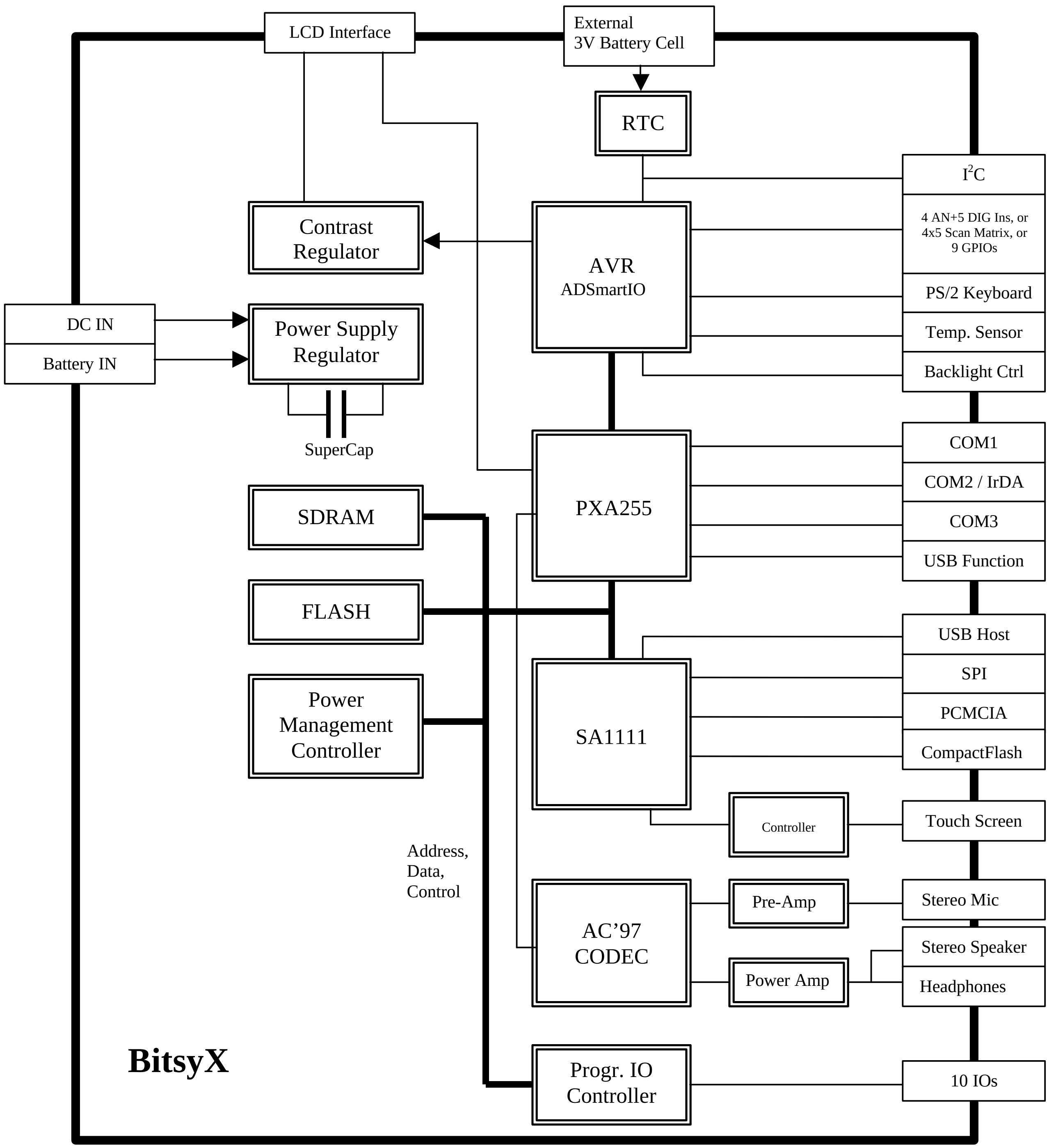
- Nine ADSmartIO™ ports configurable for digital I/O, A/D inputs (up to four) and/or up to 4x5 keypad
- Ten digital I/Os
- Backlight Control Signals for Intensity and On/off
- External Temperature Probe support

1.2.7 Audio Interface

- AC'97 Codec
- Stereo Microphone Input
- Stereo 1W Speaker Outputs
- Headphone Output

1.3 Block Diagram

The following diagram illustrates the system organization of the BitsyX.



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2 Getting Started

2.1 Development Systems

BitsyX boards are shipped as development systems designed to get the developer up and running quickly.

To use the system, simply plug power supply into the mini DIN-8 receptacle on the system.

If the screen does not display anything after five to ten seconds, check the *Frequently Asked Questions,* below. Most operating systems cold boot within twenty seconds.

2.1.1 System Components

A typical development system is shown at right. It consists of the following components:

- BitsyX single-board computer
- Bitsy Personality Board with CompactFlash or 10/100BT Ethernet
- Flat panel display and cable
- Backlight inverter and cable
- Touch screen and cable
- 120 VAC power adapter
- Plexiglas mounting
- Developer's Cable Kit including
  - Serial Port DB9 adapter (ADS cable #610111-80001)
  - DB9F/F null modem cable
- Operating system of your choice
- User's Guide (this document and operating system guide)

Please make sure you have received ***all*** the components before you begin your development.

2.1.2 BitsyX Personality Boards

The BitsyX often works in tandem with another board to add functionality and customize the system for its application. Personality boards can add custom circuits and locate connectors best suited for the application design.

In production volumes, the BitsyX can be built with interface connectors J1, J3, J9 and J10 on the underside of the board. This allows the BitsyX to rest above custom personality boards rather than below them. Note that J7 can only be populated on top side of the BitsyX.

At the time of writing, ADS supplies a reference design for personality board. Schematics are and user manuals available on the ADS support site. The ADS design can be populated as either a "CF" or "Ethernet" personality board.

ADS CF Personality Board

The CF Personality board breaks out signals from the BitsyX for a wide range of functions including USB, audio, keyboard, power, serial, LCD display, backlight, IrDA and touch screen. It also includes a reset button and CF socket.

For further details about this board, please consult the Personality Board user's manual, ADS document #110111-8001.

ADS Ethernet Personality Board

The Ethernet Personality Board uses the same circuit board as the ADS CF Personality Board. An RJ-45 jack replaces the CF socket, and the board adds an SMSC LAN91C111 10/100 Ethernet chip and associated line drivers. Otherwise, the board is identical to the CF Personality Board.

2.2 Frequently Asked Questions

The following are some of the most commonly asked questions for development systems:

Q: When I plug in power, my screen is white and nothing comes up on it.

A: Check the connector seating. The flat panel connector may have come loose in shipping. Press it firmly into the panel and reapply power to your system.

Q: When I plug in power, my screen stays black.

A: If your system has supercapacitors installed (section 5.3.3), your system may be asleep. Try waking up the system by shorting the wakeup signal (J3 pin 45) to ground. Development systems include a two-pin header on the personality board whose pins can be shorted together to wake the system. You may also press the reset button to fully restart the system.

Q: When I plug in power, the LED doesn't turn on.

A: Your system may still be booting. The LED is software controlled and is not necessarily turned on at boot.

Q: Do I have to turn off the system before I insert a PCMCIA or CompactFlash card?

A: No. The BitsyX supports hot-swapping of PCMCIA and CompactFlash cards. Consult the operating system documentation for details.

Q: Do I need to observe any ESD precautions when working with the system?

A: Yes. If possible, work on a grounded anti-static mat. At a minimum, touch an electrically grounded object before handling the board or touching any components on the board.

Q: What do I need to start developing my application for the system?

A: You will need a flash ATA card (16 MiB or larger, 32 MiB recommended) and the cables supplied with your system to interface your development station to the system. For further direction, consult the ADS guide for the installed operating system.

Q: Who can I call if I need help developing my application?

A: ADS provides technical support to get your development system running. For customers who establish a business relationship with ADS, we provide support to develop applications and drivers.

Q: Is there online support?

A: Yes. Information about the BitsyX hardware and software is available on the ADS support site at http://www.applieddata.net/support. See section 2.4 for further details.

Q: Can I upgrade the version of the operating system?

A: Yes. ADS provides regular operating system updates on its developers' web site. For operating systems not maintained by ADS, contact the operating system vendor.

Q: I would like to interface to a different display panel. How can I do this?

A: ADS may have already interfaced to the panel you are interested in. Consult ADS for availability.

2.3 Organization of this Manual

The manual organizes information in five key sections:

Introduction	Provides an overview of the functionality and organization of the BitsyX, as well as how to use this manual.
Hardware Reference	Describes the configuration settings and pinouts for all connectors and jumpers on the BitsyX.
Feature Reference	Gives details about the various subsystems of the BitsyX.
Power Management	Provides key information about power management, tips for system integration and electrical and mechanical interface specifications.
Specifications	Electrical and mechanical interface specifications.

To locate the information you need, try the following:

1. Browse the *Table of Contents.* Section titles include connector designators and their function.
2. Follow cross-references between sections.
3. View and search this manual in PDF format

2.4 Errata, Addenda and Further Information

Errata and addenda to this manual are posted on the ADS support forums along with the latest release of the manual. Consult the support forums any time you need further information or feel information in this manual is in error. You may access the forums from the ADS support site,

http://www.applieddata.net/Support

In addition to manuals, the support forums include downloads, troubleshooting guides, operating system updates and answers to hundreds of questions about developing applications for ADS products. You may also post questions you have about ADS products on the forums.

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3 Hardware Reference

This section gives an overview of the hardware features of the BitsyX. This overview includes a description of the switches, jumper settings, connectors and connector pinouts.

Many connectors and headers have a visible number or marking on the board that indicates pin 1. If that pin is not clearly marked, there are two other ways to locate pin 1:

1. The easiest method is to look at the underside of the board. The square pad is pin 1.

2. Download the mechanical drawing of the BitsyX available on the ADS Support site (section 2.4). The square or indicated pad on each connector is pin 1.

3.1 Switches and Indicators

3.1.1 S1: DIP Switch

S1 is a two-position DIP switch. When in the "ON" position, switches are closed and connect to ground. Otherwise they are pulled up.

DIP switch positions "1" and "2" connect to the SA-1111.

Most operating systems on the BitsyX reserve these switches for their use. Consult the operating system manual for details.

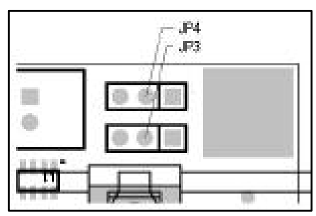
3.1.2 LED Indicator

The BitsyX has one onboard LED that turned on and off by the system controller. The LED is driven by the same buffers as the display driver data lines. The LED will be off when the display buffers are disabled (see power management section 5.3.2).

3.2 Jumper Settings

Jumpers on the BitsyX select a variety of operational modes. All use 2mm shorting blocks (shunts) to select settings. Make sure power is turned off to the BitsyX when changing the position of a shunt.

JP3 and JP4 are located at the corner of the board near the PCMCIA ejector as shown at right:



3.2.1 JP3: Flat Panel Power Select

Type: 3-post header, 2mm

This jumper selects the supply voltage for the flat panel. It is located near the PCMCIA ejector button.

Jumper setting	Voltage Selected
1-2	*Vddx (3.3 V)*
2-3	*Vcc (5.0 V)*

WARNING! Make sure you have selected the correct voltage before connecting the panel. Flat panels are notoriously sensitive to--and are often irreparably damaged by--incorrect voltages.

3.2.2 JP4: Vee Polarity Select

Type: 3-post header, 2mm

This jumper selects the polarity of Vee, the contrast control voltage for passive displays. Vee is controlled with a PWM signal from the ADSmartIO (section 4.3). See section 4.6.7 for further details about Vee.

Jumper setting	Vee
1-2	*positive*
2-3	*negative*
n/c	*no Vee*

3.3 Connector Pinouts

The following tables describe connector pinouts and the type of connector. At least one pin of every connector is labeled on the BitsyX. Pin 1 of the connector is also typically indicated by a square pad where the pin is soldered to the board.

2	4	6	8...
1	3	5	7...

As seen from the component side[5], double-row headers on the board are all numbered as shown in the figure to the right.

For information about the location of the connectors on the BitsyX, refer to section 6.1.1.

Legend:

n/c	Not connected
GND	BitsyX ground plane
(3.3)	Reference sections for signals
I	signal is an input to the system
O	signal is an output from the system
IO	signal may be input or output
P	power and ground
A	analog signals
OC	open collector output

[5] The "component side" of the BitsyX is the one on which the PCMCIA ejector is installed. As a factory option, some connectors may be installed on the "bottom side" of the BitsyX.

3.3.1 J1: LCD Panel Interface Connector

Board Connector: Samtec #STMM-117-02-T-D

Recommended Mating Cable: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-117-02-F-D-500)

The following table describes the signals on the LCD interface connector. Signal names shown are for TFT active matrix color LCDs at 16 bpp (bit-per-pixel). For other color depths and LCD technologies, consult the table in section 4.6.4. Signals from the XScale are buffered and RFI filtered before reaching J1. See section 4.6 for further details about displays.

Pin	**PXA255 Signal Name**	**Color Active TFT Display at 16bpp**	
		ADS Signal Name	**Description**
1		*PNL_VEE*	*V_{EE} (contrast); see JP4*
2		*GND*	*ground*
3	*L_PCLK*	*PNL_PIXCLK*	*Pixel Clock*
4	*L_LCLK*	*PNL_HSYNC*	*Horizontal Sync.*
5	*L_FCLK*	*PNL_VSYNC*	*Vertical Sync.*
6		*GND*	*ground*
7	*L_DD15*	*PNL_RED0*	*Red Bit 0*
8	*L_DD11*	*PNL_RED1*	*Red Bit 1*
9	*L_DD12*	*PNL_RED2*	*Red Bit 2*
10	*L_DD13*	*PNL_RED3*	*Red Bit 3*
11	*L_DD14*	*PNL_RED4*	*Red Bit 4*
12	*L_DD15*	*PNL_RED5*	*Red Bit 5*
13		*GND*	*ground*
14	*L_DD5*	*PNL_GREEN0*	*Green Bit 0*
15	*L_DD6*	*PNL_GREEN1*	*Green Bit 1*
16	*L_DD7*	*PNL_GREEN2*	*Green Bit 2*
17	*L_DD8*	*PNL_GREEN3*	*Green Bit 3*
18	*L_DD9*	*PNL_GREEN4*	*Green Bit 4*
19	*L_DD10*	*PNL_GREEN5*	*Green Bit 5*
20		*GND*	*ground*
21	*L_DD4*	*PNL_BLUE0*	*Blue Bit 0*
22	*L_DD0*	*PNL_BLUE1*	*Blue Bit 1*
23	*L_DD1*	*PNL_BLUE2*	*Blue Bit 2*
24	*L_DD2*	*PNL_BLUE3*	*Blue Bit 3*
25	*L_DD3*	*PNL_BLUE4*	*Blue Bit 4*
26	*L_DD4*	*PNL_BLUE5*	*Blue Bit 5*
27		*GND*	*ground*
28	*L_BIAS*	*PNL_LBIAS*	*Data_Enable*
29 *30*		*PNL_PWR*	*Vcc (5 V) or 3.3 V (JP3)*
31		*PNL_RL*	*Horizontal Mode Select (set by R22 or R87)*
32		*PNL_UD*	*Vertical Mode Select (set by R79 or R17)*
33	*ADSmartIO PD0*	*PNL_ENA*	*Panel enable signal*
34		*VCON*	*low-voltage adjust for contrast control of some displays (6.2.2) (zero to PNL_PWR volts)*

3.3.2 J2: PCMCIA

Integrated ejector: FCI #95620-050CA

The 68-pin PCMCIA socket conforms to the PCMCIA standard for 5V-tolerant Type II cards, and can also be run at 3.3 V. The socket is normally de-energized; the operating system is responsible for turning on the socket when a card is inserted and turning it off when the card is removed. Ejector hardware is standard.

Vpp (pins 18 and 52), which is 12 V in older PCMCIA implementations, is left unconnected in this implementation. See section 6.2.12for electrical specifications.

3.3.3 J3: Power, I/O, Serial 2 & 3, USB, Touch Screen and others

Board Connector : Samtec #STMM-125-02-T-D

Recommended Mating Connector: Samtec # TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-125-02-F-D-500)

Pin	Name	Pin	Type	Description		
1	*EIO9*		*IO*	*Digital I/Os (6.2.10)*		
	EIO8	*2*	*IO*			
3	*EIO7*		*IO*			
	GND	*4*	*P*	*ground*		
		6				
	VCC	*8*	*PO*	*+5 V*		
		10				
5	*TEMP_SENSOR _MINUS*		*AI*	*External Temperature Probe Connection (4.3.5)*		
7	*TEMP_SENSOR _PLUS*		*PO*			
9	*/IRDAON*		*O*	*External IRDA control output*		
11	*TSPX*		*AIO*	*right*	*UL*	*Touch screen (6.2.3)*
13	*TSMY*		*AIO*	*top*	*LR*	
15	*TSMX*		*AIO*	*left*	*LL*	
17	*TSPY*		*AIO*	*bottom*	*UR*	
	EIO5	*12*	*IO*	*Digital I/Os (6.2.10)*		
	EIO6	*14*	*IO*			
	BACKLIGHT PWM	*16*	*AO*	*Backlight Intensity (PWM) (4.6.6, 6.2.2)*		
	/BACKLIGHT ON	*18*	*OC*	*Backlight On/Off (open-collector) (4.6.6, 6.2.2)*		
19	*RXD2T*		*I*	*Serial 2 (3.3 V CMOS) (4.5.1)*		
	TXD2T	*20*	*O*			
21	*WIPER*		*AI*	*Touch screen wiper (optional 5-wire touch)*		
	CHARGE	*22*	*O*	*Charge Enable output (PB0 [6]) (5.3.7)*		
23	*GND*		*P*	*ground*		
	PE2	*24*	*O*	*Power Enable #2 for external devices (5.3.2)*		
25	*CTS3*		*I*	*Serial 3 (RS-232) (4.5.1)*		
	TXD3	*26*	*O*			
27	*RTS3*		*O*			
	RXD3	*28*	*I*			

[6] This output does not have any series resistance or ESD protection

<table>
<tr><th>Pin</th><th>Name</th><th>Pin</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td>29</td><td>USB+</td><td></td><td>IO</td><td colspan="2" rowspan="2">USB Client (4.5.2)</td></tr>
<tr><td></td><td>USB-</td><td>30</td><td>IO</td></tr>
<tr><td>31</td><td>GND</td><td></td><td>P</td><td colspan="2">Ground</td></tr>
<tr><td></td><td>HP_IN</td><td>32</td><td>I</td><td colspan="2">Headphone connected (4.4.2, 6.2.9)</td></tr>
<tr><td>33</td><td>USB_RECONN</td><td></td><td>0</td><td colspan="2">USB Client power management (4.5.2) [6]</td></tr>
<tr><td></td><td>GND</td><td>34</td><td>P</td><td colspan="2">connects to ground through R281(0W)</td></tr>
<tr><td></td><td>GND</td><td>36</td><td>P</td><td colspan="2">ground</td></tr>
<tr><td>35</td><td>STXD</td><td></td><td>O</td><td>MOSI</td><td rowspan="4">SPI signals (4.5.3)</td></tr>
<tr><td>37</td><td>SRXD</td><td></td><td>I</td><td>MISO</td></tr>
<tr><td>39</td><td>SCLK2</td><td></td><td>O</td><td>SCLK</td></tr>
<tr><td>43</td><td>SFRM2</td><td></td><td>O</td><td>SS</td></tr>
<tr><td rowspan="2"></td><td>VBATT_POS</td><td>38</td><td>PI</td><td colspan="2" rowspan="2">External Battery Input
(5.3.7)</td></tr>
<tr><td>VBATT_NEG</td><td>40</td><td>P</td></tr>
<tr><td>41</td><td>POWERENABLE</td><td></td><td>O</td><td colspan="2">Power Supply Control Output (5.3.2)</td></tr>
<tr><td></td><td>/PE1</td><td>42</td><td>O</td><td colspan="2">Power Enable #1 for external devices (5.3.2)</td></tr>
<tr><td rowspan="2"></td><td rowspan="2">DCIN_POS</td><td>44</td><td rowspan="2">PI</td><td colspan="2" rowspan="2">External Power Input
(also on J6)</td></tr>
<tr><td>48</td></tr>
<tr><td>45</td><td>/RQONOFF</td><td></td><td>I</td><td colspan="2">"Request On/Off" Switch Input
(5.3.3, 6.2.1)</td></tr>
<tr><td></td><td rowspan="3">GND</td><td>46</td><td rowspan="3">P</td><td colspan="2" rowspan="3">ground</td></tr>
<tr><td>47</td><td></td></tr>
<tr><td>49</td><td></td></tr>
<tr><td></td><td>BATPOS</td><td>50</td><td>PI</td><td colspan="2">Real-time clock backup battery (4.2, 6.2.4)</td></tr>
</table>

3.3.4 J4: Manufacturing Test Connector

Type: 2x3 header, 0.100-inch spacing

This header is used during manufacturing to load the ADSmartIO firmware. It is not supported for any other use.

3.3.5 J5: JTAG Connector

Type: 1x6 header, 0.100-inch spacing

This header is used during manufacturing to program the boot flash and onboard logic. It is intended for factory use.

3.3.6 J6: Input Power Connector

Board Connector: Molex #22-23-2021

Recommended mating connector: Molex 22-01-3027

These power inputs are also connected to J3. See Chapter 5 and section 6.2.3 for input power specifications.

Pin	Name	Type	Description
1	DCIN_POS	PI	DC Power Input
2	GND	P	Ground

3.3.7 J7: XScale I/O Signals

Board Connector : 2x8, 2mm spacing, Samtec STMM-108-02-G-D-SM

Recommended Board-to-Cable Connector: TCSD series

Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-108-02-F-D-450) [7]

This header supplies signals from the XScale that were not available on the StrongARM. These include I^2C and MMC interfaces as well as a number of processor pins that may be used as general-purpose I/Os (GPIOs) or for alternate, special-purpose functions.

Pin	Name	Type	Description	
1	*I2C_SCA*	*IO*	*I^2C (4.5.4)*	
	I2C_SCL	*IO*		
3	*GND*	*P*	*Ground*	
4		*P*		
5	*MMCCS0*	*O*	*Chip select 0*	*Multimedia Card (MMC) Controller (4.5.5)*
6	*MMCCS1*	*O*	*Chip select 1*	
7	*MMCMD*	*O*	*Command*	
8	*MMCDAT*	*IO*	*Data*	
9	*MMCCLK*	*O*	*Clock*	
10	*MMCCD*	*I*	*Card Detect*	
11	*VDDX*	*P*	*3.3 V*	
12	*VCC*	*P*	*5 V*	
13	*/CS_4 GPIO80*	*IO*	*Digital I/Os (6.2.10)*	
14	*/CS_5 GPIO33*	*IO*		
15	*CPLD_IO*	*IO*	*reserved*	
16	*n/c*		*unused*	

3.3.8 J9: External CompactFlash / Expansion Bus

Board Connector : Samtec #STMM-125-02-T-D

Recommended Mating Connector: Samtec TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-125-02-F-D-500)

The BitsyX makes its CompactFlash bus signals available on J9. These signals can be used to add a CompactFlash socket to a daughter board or to expand the capabilities of the BitsyX as a digital expansion bus. See section 4.1.5 for details.

Pin	Name	Pin	Type	Description
1	*GND*		*P*	*ground*
	/CARDBDET2	*2*	*I*	*Card Detect 2*
	/CARDB16	*4*	*I*	*16 Bit Access*
3	*PCBD10*		*IO*	*Data8-10*
5	*PCBD9*		*IO*	
7	*PCBD8*		*IO*	
	PCBD2	*6*	*IO*	*Data0-2*
	PCBD1	*8*	*IO*	
	PCBD0	*10*	*IO*	

[7] Note that the STMM header is 0.050-inch higher than the other 2mm headers on the board because it is a surface-mount part. Use a correspondingly shorter socket on mating boards.

Pin	Name	Pin	Type	Description
9	*CARDBSTSCHG*		*I*	*Status Change*
11	*CARDBSPK*		*I*	*Speaker Input*
13	*/CARDBREG*		*O*	*Register Access*
15	*VCC*		*PO*	*5 V*
17	*/CARDBWAIT*		*I*	*Wait*
19	*CARDBRES*		*O*	*Reset*
21	*/CARDBVS2*		*I*	*Voltage Sense 2 Input*
	PCBA0	*12*	*O*	*Address0-6*
	PCBA1	*14*	*O*	
	PCBA2	*16*	*O*	
	PCBA3	*18*	*O*	
	PCBA4	*20*	*O*	
	PCBA5	*22*	*O*	
	PCBA6	*24*	*O*	
23	*+3.3V*		*P0*	*+3.3 V*
25	*/CARDBON*		*O*	*5 V Power Control*
	CARDBVCC	*26*	*PI*	*External Switched CardB Power Input*
27	*CARDBIRQ*		*I*	*Interrupt Signal*
29	*/CARDBMWR*		*O*	*Memory Write*
31	*/CARDBIOWR*		*O*	*IO Write*
33	*/CARDBIORD*		*O*	*IO Read*
	PCBA7	*28*	*O*	*Address7-10*
	PCBA8	*30*	*O*	
	PCBA9	*32*	*O*	
	PCBA10	*36*	*O*	
	/CARDBMRD	*34*	*O*	*Memory Read*
35	*/CARDB_VS1*		*I*	*Voltage Sense 1 Input*
37	*/CARDBCE2*		*O*	*Low Byte Chip Select*
	/CARDBCE1	*38*	*O*	*High Byte Chip Select*
39	*PCBD15*		*IO*	*Data11-15*
41	*PCBD14*		*IO*	
43	*PCBD13*		*IO*	
45	*PCBD12*		*IO*	
47	*PCBD11*		*IO*	
	PCBD7	*40*	*IO*	*Data3-7*
	PCBD6	*42*	*IO*	
	PCBD5	*44*	*IO*	
	PCBD4	*46*	*IO*	
	PCBD3	*48*	*IO*	
49	*/CARDBDET1*		*I*	*Card Detect 1*
	/CARDBON_3P3V	*50*	*O*	*3.3 V Power Control*

3.3.9 J10: ADSmartIO, USB, Serial 1, Stereo Audio, I/Os

Board Connector : Samtec #STMM-125-02-T-D

Recommended Mating Connector: Samtec # TCSD Series
Recommended Board-to-Board Connector: ESQT series (e.g. ESQT-125-02-F-D-500)

Pin	Name	Pin	Type	Description	
1	*/EXT_IRQ1*		*I*	*External Interrupt 1 Input*	
3	*/EXT_IRQ2*		*I*	*External Interrupt 2 Input*	
5	*EIO4*		*IO*	*Digital I/Os (6.2.10)*	
	EIO3	*2*	*IO*		
	EIO2	*4*	*IO*		
	EIO1	*6*	*IO*		
	EIO0	*8*	*IO*		
7	*SIGPS2*		*IO*	*External PS/2 keyboard inputs*	
9	*CLKPS2*		*IO*		
	USB_PWR_SENSE	*10*	*I*	*Sense Input from external USB host power switch (4.5.2)*	
	USB_PWR_CTRL	*12*	*O*	*Discrete output to control external USB host power switch (4.5.2)*	
	USB_UDC-	*14*	*IO*	*USB Host (4.5.2)*	
	USB_UDC+	*16*	*IO*		
11	*SMTIO2*		*IO*	*PC6*	*I^2C [8]*
13	*SMTIO1*		*IO*	*PD1*	*Thermistor energize (4.3.5)*
15	*SMTIO0*		*IO*	*PD0*	*Passive panel enable (PNL_ENA)*
	SPKR_L-	*18*	*AO*	*Stereo Speaker, left channel (4.4.2)*	
	SPKR_L+	*20*	*AO*		
	SPKR_R-	*22*	*AO*	*Stereo Speaker, right channel (4.4.2)*	
	SPKR_R+	*24*	*AO*		
17	*ROW0*		*IO*	*PC0*	*ADSmartIO (see section 6.2.6)*
19	*ROW1*		*IO*	*PC1*	
21	*ROW2*		*IO*	*PC2*	
23	*ROW3*		*IO*	*PC3*	
25	*ROW4*		*IO*	*PC4*	
27	*COL0*		*IO*	*PA0*	
29	*COL1*		*IO*	*PA1*	
31	*COL2*		*IO*	*PA2*	
33	*COL3*		*IO*	*PA3*	
	RI1	*26*	*I*	*Serial 1 [9] (RS-232 with 3.3 V CMOS factory option) (4.5.1)*	
	DCD1	*28*	*I*		
	DSR1	*30*	*I*		
	DTR1	*32*	*O*		
	RXD1	*34*	*I*		
	TXD1	*36*	*O*		
	CTS1	*38*	*I*		
	RTS1	*40*	*O*		

[8] PC6 and PC7 are used for the I^2C bus master interface. See section 4.5.4 for details.

[9] Serial 1 signals RTS, CTS, DCD, DTR, DSR and RI are controlled by the StrongARM GPIO lines. See section 4.1.6 for details.

Pin	Name	Pin	Type	Description	
35	*/EXT_IRQ3*		*I*	*External Interrupt 3 Input*	
37	*VDDX*		*PO*	*3.3 V*	
39	*MIC_GND*		*P*	*Microphone ground*	
41					
	MIC_L	*42*	*AI*	*Stereo Microphone Input*	
	MIC_R	*44*	*AI*		
43	*VREF*		*AO*	*ADSmartIO A/D reference voltage*	
45	*/RESET_IN*		*I*	*External Reset Input (6.2.1)*	
47	*VDDX*		*PO*	*3.3 V*	
	VCC	*46*	*PO*	*5 V*	
		48			
49	*SMTIO3*		*IO*	*PC7*	*I^2C* [10]
	GND	*50*	*P*	*ground*	

[10] See footnote 8.

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4 Feature Reference

This chapter provides details about the architecture and many features of the BitsyX, and how they can fit together to create a system that meets your application needs.

4.1 System Architecture

4.1.1 Boot Code

The BitsyX uses the first block of onboard flash to store the boot code. At the factory, boot code is loaded using the JTAG interface (J6, section 3.3.5). Most ADS BitsyX boot loaders are field-upgradeable using a flash card on either the CompactFlash or PCMCIA port.

4.1.2 Synchronous DRAM

One bank of synchronous DRAM (SDRAM) can be populated for a system total of 16, 32, 64 or 128 MiB of RAM[11]. The data bus width is 32 bit.

The memory clock speed is one half the CPU core clock speed. Typical memory bus operation is at 99.5 MHz.

The self-refreshed RAM consumes most of the system sleep current. Sleep current increases roughly in direct proportion to the amount of RAM installed.

4.1.3 Non-Volatile Memory

There are several ways to store data on the BitsyX that will survive a power failure. Some devices can only be accessed through operating system drivers, and not all are available for application data storage.

Flash Memory

Flash memory is the primary site for non-volatile data storage. The BitsyX includes a bank of flash memory for non-volatile data storage. The board supports 8, 16 or 32 MiB of installed flash. The data bus width is 32 bit.

ADS systems store the operating system, applications and system configuration settings in the onboard flash. Most operating systems configure a portion of the flash as a flash disk, which acts like a hard disk drive.

ADSmartIO EEPROM

The ADSmartIO controller includes 256 bytes or more of EEPROM storage. ADS reserves a portion of this memory for future use. Drivers are not yet available for all operating systems.

CompactFlash and PCMCIA/ATA Cards

CF and ATA cards provide removable storage in a wide variety of capacities. These cards can be cost-effective means to expand system storage capacity for applications that provide access to the PCMCIA and CF slots. A CF slot must be placed on a daughter board, as it is not included on the BitsyX.

---

[11] 128 MiB SDRAM was not yet commercially available as of April 2003.

RTC NVRAM

The real-time clock chip includes 56 bytes of non-volatile RAM. The RAM is maintained as long as main or backup power is provided to the chip. Drivers are not yet available to access this feature. Contact ADS Sales if your application requires this feature.

4.1.4 Interrupts

The BitsyX includes several sources for external interrupts. The following table summarizes the external interrupt sources and the devices to which they are connected.

Interrupt Signal	Pin	IRQ Handler
/RqOnOff	*J3.45*	*PXA255, GP 0 (via CPLD &ADSmartIO)*
CARDBIRQ	*J9.27*	*SA-1111*
/EXT_IRQ1	*J10.1*	*PXA255, GP 27*
/EXT_IRQ2	*J10.3*	*SA-1111, GPIO_B<4>*
/EXT_IRQ3	*J10.35*	*PXA255, GP 10*

Your operating system may not include drivers for all interrupt sources.

4.1.5 CompactFlash / Expansion Bus

The BitsyX makes its CompactFlash bus signals available on J9. These signals can be used to add a CompactFlash socket to a daughter board or to expand the capabilities of the BitsyX as a digital expansion bus. The voltage of the bus signals are set by the CardBVcc voltage (3.3 V or 5 V).

The ADS Bitsy CF and Ethernet Personality Boards use this bus for CF and digital expansion, respectively. The schematic (ADS document number 640111-8000, available on the ADS Support Forums) illustrates how to use this bus both ways.

4.1.6 PXA255 GPIO Cross-Reference

The following table describes how the BitsyX utilizes the XScale GPIO lines (*GPn*). They are offered for reference purposes only. Most operating systems make this information transparent to developers.

GP	Signal Name	Type	Function (connector, section)
0	*WAKE_UP*	*I*	*wakeup from ADSmartIO*
1	*SA1111_IRQ*	*I*	*SA-1111 interrupt*
2	*EXT_IRQ3*	*I*	*External interrupt 3 (4.1.4)*
3	*EIO0*	*IO*	*Digital I/O (J10, 3.3.9)*
4	*EIO1*	*IO*	
5	*IRQ_SSP*	*I*	*ADSmartIO interrupt*
6	*MMCCLK*	*O*	*MMC clock (J7, 3.3.7)*
7	*EIO2*	*IO*	*Digital I/O (J10, 3.3.9)*
8	*MMCCS0*	*O*	*MMC chip select 0 (J7, 3.3.7)*
9	*MMCCS1*	*O*	*MMC chip select 1 (J7, 3.3.7)*
10	*EIO3*	*IO*	*Digital I/O (J10, 3.3.9)*
11	*3.6MHZ GPIO_11*	*IO*	*GPIO11, alt. function 3.6MHz oscillator out*
12	*MMCCD*	*O*	*MMC card detect (J7, 3.3.7)*
13	*GPIO13*	*I*	*SA-1111 Memory Request*
14	*GPIO14*	*O*	*SA-1111 Memory Request Bus Grant*
15	*/CS1*	*O*	*Asynchronous flash chip select*

GP	Signal Name	Type	Function (connector, section)
16	*EIO4*	*IO*	*Digital I/O (J10, 3.3.9)*
17	*GPIO17*	*O*	*Reset SA-1111*
18	*RDY*	*O*	*CPU ready*
19	*EIO5*	*IO*	*Digital I/O (J3, 3.3.3)*
20	*EIO6*	*IO*	
21	*EIO7*	*IO*	
22	*EIO8*	*IO*	
23	*SCLK-C*		*SSP*
24	*SFRM-C*		
25	*TXD-C*		
26	*RXD-C*		
27	*GPIO27*	*O*	*Reset ADSmartIO controller*
28	*BITCLK*		*AC97 Codec*
29	*SDATA_IN0*		
30	*SDATA_OUT*		
31	*SYNC*		
32	*EIO9*	*IO*	*Digital I/O (J3, 3.3.3)*
33	*/CS_5 GPIO33*	*IO*	*GPIO33, alt. function external chip select (J7, 3.3.7)*
34	*FF_RXD*	*I*	*Serial 1 (J10, 4.5.1)*
35	*FF_CTS*	*I*	
36	*FF_DCD*	*I*	
37	*FF_DSR*	*I*	
38	*FF_RI*	*I*	
39	*FF_TXD*	*O*	
40	*FF_DTR*	*O*	
41	*FF_RTS*	*O*	
42	*BT_RXD*	*I*	*Serial 3 (J3, 4.5.1)*
43	*BT_TXD*	*O*	
44	*BT_CTS*	*I*	
45	*BT_RTS*	*O*	
46	*IR_RXD*	*I*	*Serial 2 (J3, 4.5.1)*
47	*IR_TXD*	*O*	
48	*/POE*		*PCMCIA/CF Card interface*
49	*/PWE*		
50	*/PIOR*		
51	*/PIOW*		
52	*/PCE1*		
53	*/PCE2*		
54	*PSKTSEL*		
55	*/PREG*		
56	*/PWAIT*		
57	*/IOIS16*		
58	*L_DD0*	*O*	*LCD display (J1)*
59	*L_DD1*	*O*	
60	*L_DD2*	*O*	
61	*L_DD3*	*O*	
62	*L_DD4*	*O*	
63	*L_DD5*	*O*	
64	*L_DD6*	*O*	
65	*L_DD7*	*O*	

GP	Signal Name	Type	Function (connector, section)
66	*L_DD8*	*O*	*LCD display (J1)*
67	*L_DD9*	*O*	
68	*L_DD10*	*O*	
69	*L_DD11*	*O*	
70	*L_DD12*	*O*	
71	*L_DD13*	*O*	
72	*L_DD14*	*O*	
73	*L_DD15*	*O*	
74	*L_FCLK*	*O*	
75	*L_LCLK*	*O*	
76	*L_PCLK*	*O*	
77	*L_BIAS*	*O*	
78	*CS2*	*O*	*CPLD chip select*
79	*CS3*	*O*	*SA-1111 chip select*
80	*/CS_4 GPIO80*	*IO*	*GPIO80, alt. function external chip select (J7, 3.3.7)*

4.2 Real-Time Clock (RTC)

The BitsyX uses the DS1307 real-time clock chip to maintain the system date and time when the system is powered down. The operating system typically reads the RTC on boot and wakeup, and sets the RTC when the system time or date is changed.

The RTC is powered from the BATPOS input. Connect a long-life 3 V battery to the BATPOS input (J3 pin 50) to maintain the system time.

The system communicates with the RTC on the I^2C bus (section 4.5.4). See section 6.2.4 for electrical specifications.

4.3 ADSmartIO

ADSmartIO™ is a RISC microcontroller on the BitsyX that is programmed with ADS firmware. This device provides additional I/O functionality for specialized tasks. Your application software can configure the standard ADSmartIO for a variety of functions, such as digital I/O, PWM, A/D, I^2C, keypad scan and PS/2 keyboard operation.

4.3.1 Overview

The ADSmartIO controller has four, eight-pin I/O ports named PA, PB, PC and PD. Some of these ports' pins are used internally, while others are available for user applications. See the signal cross-reference in section 4.3.7 for details.

Generally, ADSmartIO ports are referenced by port and pin number (e.g. PA2), but I/O signals may go by several names based on its functionality. See the connector pinouts to cross-reference ADSmartIO signal names.

Electrical specifications for the ADSmartIO are listed in section 6.2.6. The *ADSmartIO Programmer's Reference* (ADS document 110110-4004) gives information about how to use the ADSmartIO features.

4.3.2 ADSmartIO Features

The following are some of the functions that the ADSmartIO can perform. The functions actually implemented depend on the firmware loaded on your system:

- General purpose digital I/O and A/D
- Keypad scan (section 4.3.6)
- PS/2 keyboard input
- Backlight on/off and brightness control (section 4.6.6)
- Contrast control for display (enabled only when pixel clock is running) (section 4.6.7)
- Read/set real-time clock (RTC) (section 4.2)
- Wakeup via RQONOFF signal (section 5.3.3)
- Trickle-charge a battery (section 5.3.7)
- Read a temperature sensor (section 4.3.5)
- Monitor system power
- Reset CPU

4.3.3 Digital I/Os

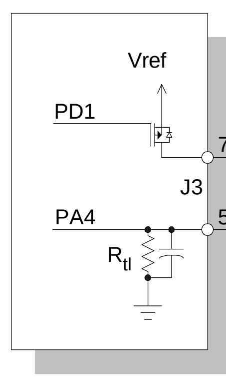
All available ports on the ADSmartIO controller can be individually configured as inputs or outputs. If you write a "1" to an I/O port when it is configured as an input, it enables a pull-up resistor. Electrical specifications are listed in section 6.2.6.

4.3.4 Analog Inputs (A/D)

Each of the Port A I/Os (PA0-PA7) includes an analog-to-digital (A/D) converter. The converters give full-scale readings when the input voltage is equal to voltage reference Vref (e.g. V=Vref•reading/1023). Not all ports are available for external A/D use; see section 4.3.7 for port assignments. Electrical specifications are listed in section 6.2.6.

4.3.5 Temperature Sensing

The BitsyX ADSmartIO can read the temperature of an external thermistor connected across pins 5 and 7 of J3. The ADSmartIO controller drives a transistor to energize the thermistor, then reads the result through the voltage divider created by the thermistor (R_{th}) and an internal resistor (R_{tl}). The thermistor circuit is shown at right.



Electrical specifications for the temperature sensing circuit are listed in section 6.2.6.

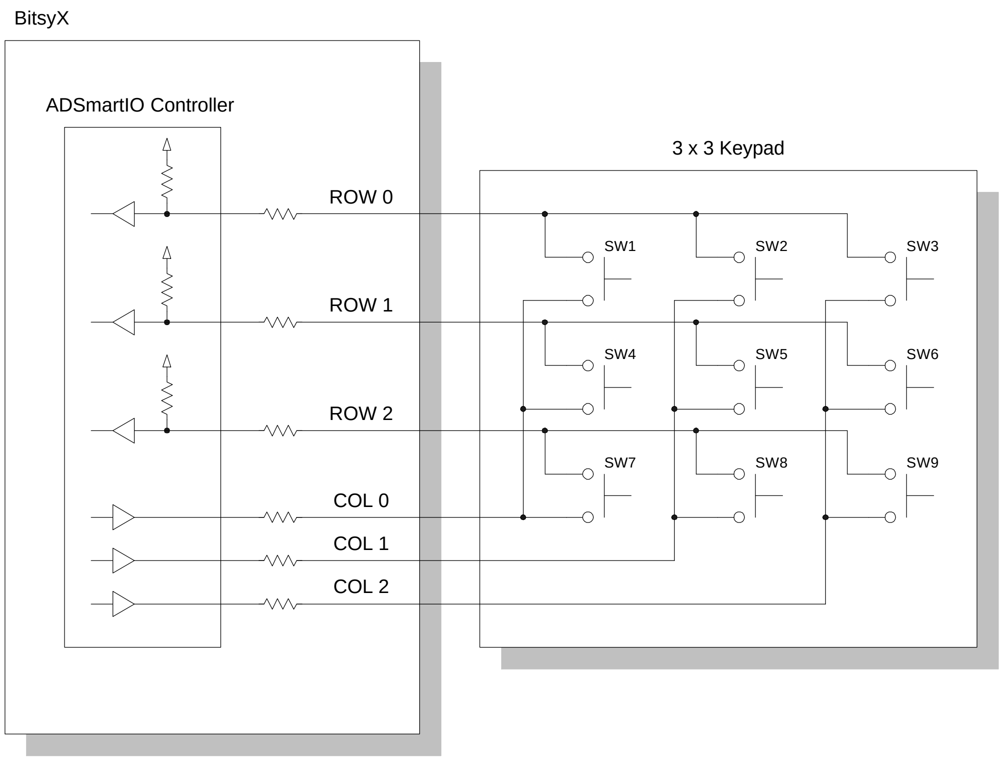
4.3.6 Keypad Scan

The ADSmartIO can scan a matrix keypad up to four by five keys in size. Matrix keypads are simpler and cost less than full keyboards and can be easily customized for your application. You can also create a keypad matrix from a collection of normally-open switches.

When configured to scan a keypad, the ADSmartIO configures the ROWn lines as inputs with software pull-ups enabled and configures the COLn lines as outputs set to "1"(high). For the scan, the keypad scanner sets successive COLn outputs to "0"(low), then looks for a "0" on one of the ROWn inputs. The scanner re-reads the pressed key after a delay to debounce the key press.

Unused row and column lines can be used for general purpose I/O or A/D.

The following diagram illustrates how to connect a 3x3 keypad matrix. The pull-ups are the software-activated internal resistors of the ADSmartIO, while the series resistors are part of the BitsyX.



4.3.7 ADSmartIO Signal Cross-Reference

The ADSmartIO microcontroller serves many functions in the BitsyX. The following table illustrates how the microcontroller ports are utilized for ADSmartIO functionality on the BitsyX.

Entries in parentheses indicate indirect connections to the listed pin (e.g. through voltage dividers or additional circuits). Signals with conventional protection circuits are considered directly connected. I=input, O=output.

Port	Pin	Type	Function
PA0	*J10.27*	*IO*	*Keypad, A/D or digital I/O*
PA1	*J10.29*	*IO*	
PA2	*J10.31*	*IO*	
PA3	*J10.33*	*IO*	
PA4	*J3.5*	*AI*	*Thermistor reading*
PA5	-	*I*	*DC_GOOD*[12]
PA6	-	*O*	*Reset CPU*
PA7	*(J3.38)*	*AI*	*VBATT_POS divided by 7.2*

[12] DC_GOOD is an internal digital signal that goes low when the input voltage drops below Vsleep (6.2.1).

Port	Pin	Type	Function	
PB0	*J3.22*	*O*	*Battery charger*	
PB1	*-*	*I*	*System Power enable*	
PB2	*-*	*O*	*Wake up CPU*	
PB3	*-*	*O*	*IRQ to CPU*	
PB4	*-*		*SSP_SFRM*	*SSP communication with CPU*
PB5	*-*		*SSP RX (MOSI)*	
PB6	*-*		*SSP TX (MISO)*	
PB7	*-*		*SSP CLK*	
PC0	*J10.17*	*IO*	*Keypad, A/D or digital I/O*	
PC1	*J10.19*	*IO*		
PC2	*J10.21*	*IO*		
PC3	*J10.23*	*IO*		
PC4	*J10.25*	*IO*		
PC5	*(J1.3)*	*I*	*Pixel clock*	
PC6	*J10.11*	*IO*	I^2C [13]	
PC7	*J10.49*	*IO*		
PD0	*J10.15*	*O*	*Passive panel enable (PNL_ENA)*	
PD1	*J10.13*	*O*	*Thermistor energize (4.3.5)*	
PD2	*J10.9*	*IO*	*PS/2 Clock*	
PD3	*J3.45*	*I*	*wakeup signal from CPLD*	
PD4	*(J1.1)*	*O*	*Vee PWM*	
PD5	*(J3.16)*	*O*	*Backlight PWM*	
PD6	*J10.7*	*IO*	*PS/2 Data*	
PD7	*(J3.18)*	*O*	*Backlight on/off*	

4.4 Audio

The BitsyX includes an AC97 codec for stereo audio input and output. Electrical specifications for the audio system are listed in section 6.2.9.

4.4.1 Microphone Pre-amps

The BitsyX supports the connection of a stereo electret microphone to the MIC_R and MIC_L inputs on J10. The audio signals run through pre-amplifiers that low-pass filter and boost the signal before being passed on to the audio codec.

When connecting external electret microphones to the BitsyX, use the MIC_GND analog ground plane for improved signal-to-noise ratio. The BitsyX includes pull-ups to power electret microphones.

4.4.2 Audio Outputs: Speakers and Headphones

The BitsyX audio amplifier supports both differential and single-ended output devices. Differential (or "bridge") drive delivers greater output power and is suitable for speakers, which

[13] PC6 and PC7 are used for the I^2C bus master interface. See section 4.5.4 for details. These pins can be reconfigured as digital I/Os for custom production applications.

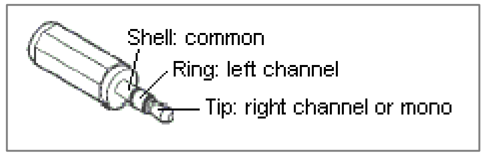
can be wired independently from each other. Single-ended mode is used for devices like headphones, which have a common ground between output channels.

The HP_IN input (J3.32) determines the output mode of the amplifier: When HP_IN is high, the audio output drive is single-ended, when HP_IN is low, the output drive is differential. An on-board pull-up normally keeps HP_IN high.

Connecting Speakers

When using the BitsyX to drive speakers, short the HP_IN signal to ground. This places the output amplifier in differential mode. Connect speakers to the SPKR_L and SPKR_R outputs on J10.

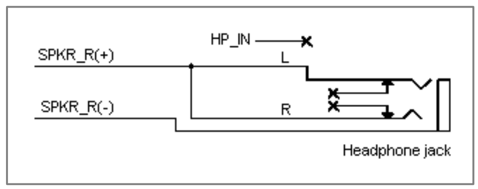
Connecting Headphones



Standard headphones use a plug wired as shown at right. Three rings on the plug provide right and left channels and a common return. Mono headphones do not include the center ring.

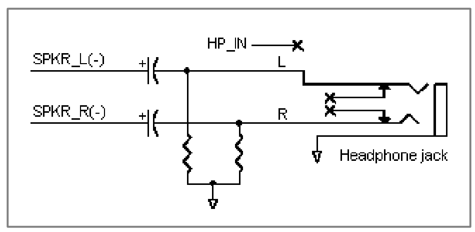
The mating headphone jacks include spring contacts to make an electrical connection with the headphone and to mechanically hold the plug in place. Some jacks include a mechanical switch suitable for use with the HP_IN signal that is activated when a plug is inserted into the jack.

Mono Headphones



You can connect mono headphones directly to the BitsyX as shown at right. Keep in mind that the resulting impedance of the parallel-connected headphone speakers is half that of a single headphone speaker. See the audio driver specifications in section 6.2.9 for details about the minimum impedance an audio output channel can drive.

Stereo Headphones



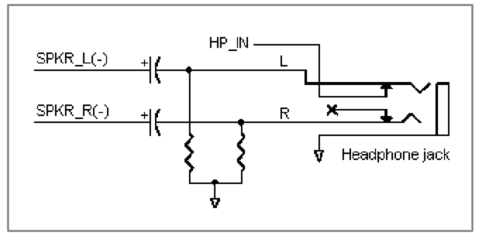
When wiring for stereo headphones, wire blocking capacitors in series with the BitsyX SPKR- signals as shown at right. These capacitors block the DC component of the audio signal and complete the conversion from differential to single-ended output drive. Leave the HP_IN signal pulled high to enable headphone output.

Select blocking capacitor size based on the lowest frequency your application will need to play out. Larger capacitors give improved bass response (lower frequency cutoff), but are physically larger and cost more. The corner frequency for the low-pass filter created by the capacitor and the headphone speaker is calculated as $fo=1/(2\pi R_L C)$. A 330 uF capacitor into a 32 ohm headphone speaker will give a low cutoff frequency of 15 Hz. Use electrolytic capacitors rated for at least 6.3 V.

The pull-down resistors shown in the diagram drain any charge that builds up on the headphone outputs when headphones are not connected. Use 1 kΩ resistors.

Using Stereo Headphones and Speakers in the Same System

Some applications use both headphones and speakers. You can wire the headphone jack to automatically switch the amplifier to single-ended mode when a headphone plug is inserted in the jack. This will disable the drive to any speakers that are wired into the system.



Most headphone jacks include mechanical switches that indicate when a headphone plug has been inserted. The diagram at right shows a circuit that pulls down the HP_IN signal when a headphone plug is removed.

For this circuit to work reliably in differential mode, the HP_IN signal must remain below V_{HP_IN} through the largest output voltage swings of SPKR_L. Use of 1 kΩ resistors meets this requirement.

4.5 Buses and Data Communications

The BitsyX has several built-in channels for communication with peripheral and peer devices. These include RS-232 and logic-level serial, USB host and client ports, SPI bus and I^2C.

4.5.1 Serial Ports

The BitsyX has three XScale serial ports configured as follows:

Port	# signals	Connector	Standard	Factory options
Serial 1	9-wire	J10	RS-232 (9-wire)	3.3 V CMOS
Serial 2	3-wire	J3	3.3 V CMOS	(none)
Serial 3	5-wire	J3	RS-232	3.3 V CMOS

The XScale standard serial ports (Serial 2 and 3) supply two or four signals: Serial 2 uses TX and RX ("three-wire serial", counting GND), while Serial 3 adds RTS and CTS. Serial 1 uses the XScale "full-featured serial port," which adds four more signals (DTR, DSR, DCD and RI) to supply the full complement of modem control signals.

The XScale can configure Serial 2 as an IrDA port . IrDA should be used in conjunction with the IrDAOn signal (J3), which enables the IrDA transmitter. IrDA transceivers can be panel mounted or placed on a personality board.

Ports that are configured for 3.3 V CMOS operation go directly to the XScale and should be treated electrically as GPIOs. See section 6.2.10for electrical specifications.

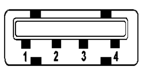
4.5.2 USB

The BitsyX includes signals for USB 1.1 Host and Client ports. The USB Host (downstream) functionality is driven by the SA-1111 companion chip, while the USB Client ("Function" or upstream) port is managed by the PXA255 processor. The BitsyX can be configured as a self-powered hub, with one Host and one Client port

To create a USB connection, you must wire a standard USB socket as described in the following sections. For each type of connector, pin numbering is as follows:

Pin	USB signal
1	*USB_PWR*
2	*USB -*
3	*USB +*
4	*GND*

USB Host



The BitsyX USB Host port allows you to connect one USB device to the BitsyX. USB mouse and keyboard are the most common client devices, but you can connect any USB function device that has USB drivers installed on the BitsyX.

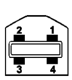
Use a Type A connector for the host signals on J10 pins 14 and 16 (section 3.3.9). The mating face of such a socket is shown at left. The USB standard also permits directly wiring the USB signals to the target USB device (e.g. USB mouse). To connect more than one USB client device to the BitsyX, use a USB hub.

The USB protocol allows client devices to negotiate the power they need from 100 mA to 500 mA in 100 mA increments. The BitsyX supplies 5 V power through the USB_PWR pin. Make sure to account for power used through USB in your BitsyX power budget (section 5.4.1). It is recommended that you use a power switch.

The BitsyX supports two power control signals on J10. USB_PWR_SENSE is an input that detects over-current conditions. USB_PWR_CTRL an output that controls power to the USB port. See the BitsyX CF Personality Board (ADS p/n 640111-8000) for an example of how to use these signals. Electrical specifications are in section 6.2.8.

USB Client

The BitsyX includes a USB Client (or "Function") port. This interface allows the BitsyX to appear as a client device to USB Host devices such as desktop and laptop computers.



The USB Client signals are available on connector J3, pins 29 and 30. Connect these signals to a USB client Type B socket (mating face shown at left). The USB standard also permits directly wiring the USB signals to the host or to a host connector (e.g. USB mouse).

The BitsyX supports the full USB connection speed (12 Mbit/s), so you must tie a 1.5 kΩ pull-up to the USB+ signal to indicate this capability to host hardware.

USB_PWR is power supplied from the host computer. Since the BitsyX is self-powered (not powered by the USB cable), USB_PWR is not needed as a power input. However, USB_PWR is useful for sensing when a USB cable is connected and for powering the 1.5kΩ pull-up resistor that indicate to the host that the device supports 12Mbps. The Bitsy CF Personality Board reference design (ADS p/n 640111-8000) for an example of such an application.

Revision 2 of the BitsyX add the USB_RECONN signal to J3, pin 33. This signal interrupts power to the 1.5kΩ pull-up, simulating a cable disconnection to the USB host controller. This signal can be used to force the host to re-enumerate the BitsyX (e.g. after wakeup).

4.5.3 SPI Bus

Overview

The SPI Bus (Serial Peripheral Interface) is a full-duplex, synchronous serial protocol developed by Motorola that can support multiple bus masters. The bus consists of a clock line, transmit and receive lines, ground and one or more device selects. Each device on the bus requires its own select line. A key feature of SPI is that data is clocked in both directions at the same time, providing full-duplex data flow.

To clarify direction of the signals, the SPI bus master transmit line (STXD) is also known as MOSI (Master Out, Slave In), while its receive line is known as MISO (Master In, Slave Out). The Slave Select (SS) signal, which enables the slave device's transmitter, is also known as SFRM2 on the BitsyX.

SPI on the BitsyX

The BitsyX has two SPI channels. The XScale PXA255 SPI port is used to communicate with the ADSmartIO controller. The signals for that port are brought out to J4 for ADSmartIO in-system programming, but the port is not otherwise available for external use.

The SA-1111 supplies the second SPI port. The BitsyX uses this port as an SPI bus master to communicate with the touch panel controller. This SPI bus can also communicate with an external device using signals are available on J3.

The BitsyX system controller de-multiplexes the SPI SS line to select either the touch panel controller or the external SPI device. SFRM2 on J3 pin 43 is the external SPI device select. The BitsyX drives the SPI clock and does not support external bus masters.

Electrical specifications for the SPI bus are listed in section 6.2.12. Consult the operating system references for details about how to use the SPI bus for external devices.

Alternate uses of the SPI Port

The SA-1111 SPI port has a great deal of flexibility. If a touch panel is not used, the SA-1111 SPI port can be configured to make use of one or more of the following features:

- Data widths from four to sixteen bits
- 16-entry transmit and receive FIFOs with burst-mode data transfers to/from RAM
- Adjustable FIFO threshold interrupts
- Bit clock speeds up to 1.84 MHz
- Support for Microwire (a National Semiconductor standard) and SSP (Synchronous Serial Port, a TI standard)

Contact ADS Sales of your application will require a driver to make use of these features.

4.5.4 I²C Bus Master and SMBus

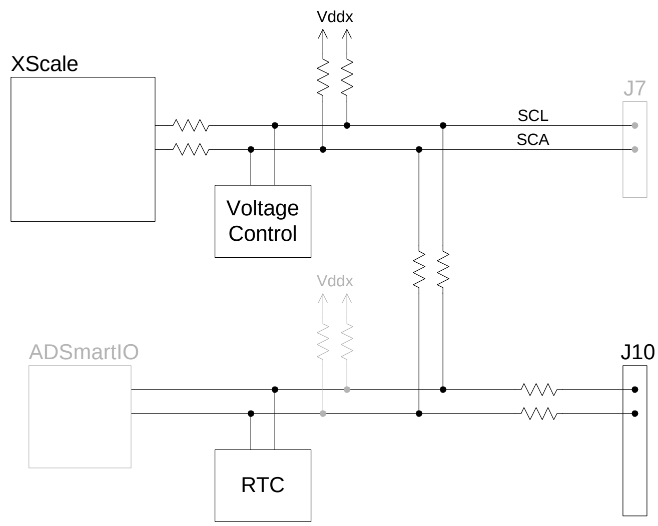
I²C (Inter-IC) Bus is a multi-master, "two-wire" synchronous serial bus developed by Philips for communications between integrated circuits (ICs). The bus master addresses devices using the data line and provides a synchronous clock for reading and writing devices. Client devices respond only when queried by the master device. Philips has developed many I²C devices, but other organizations have adopted I²C as a convenient means for addressing peripherals in a system.

I²C on the BitsyX

The BitsyX can support two, independent I²C interfaces. The first is provided by the XScale processor; the second by the ADSmartIO controller. Standard BitsyX systems use only the XScale controller as a bus master, but the ADSmartIO can become a second I²C bus master for custom applications.

The BitsyX uses the I²C interface to communicate with the real-time clock (section 4.2) and the CPU core voltage controller. I²C can also be used to communicate with external devices.

The following diagram illustrates the I²C architecture on BitsyX.



XScale I²C

The BitsyX XScale I²C signals are available on connector J7 (or J10). Specifications are listed in section 6.2.10.

ADSmartIO I²C

The ADSmartIO emulates an I²C bus master using PC6 as SCL and PC7 as SDA. These signals are available on J10 (or J7) for expansion to off-board devices. Specifications are listed in section 6.2.6.

The ADSmartIO is connected to the I²C bus for backward compatibility with the Bitsy Plus, but is not recommended for new designs. To indicate this status, ADSmartIO I²C is "grayed-out" in the diagram above. Use the XScale I²C controller for new applications.

SMBus

SMBus (System Management Bus) is a protocol developed by Intel that is similar to I^2C. Some laptop and desktop computers use SMBus to manage system power using the ACPI standards.[14] A subset of SMBus, the Smart Battery protocol, uses SMBus to communicate with "intelligent" batteries and chargers.[15]

Key differences[16] between I^2C and SMBus include:

- Bus speed:
  The SMBus clock rate must be between 10 kHz and 100 kHz while I^2C can run between DC and 400 kHz.
- Timeout
  SMBus slave devices time out and reset their communication interfaces if there is more than a 35 ms delay in the clock. I^2C doesn't have a timeout.
- Current draw on bus
  SMBus devices must draw between 100 and 350 µA; I^2C devices can draw up to 3 mA.

The BitsyX implementation of I^2C will work with most SMBus devices. The most likely point of conflict is in the BitsyX I^2C bus current draw (see the pull-up resistor specifications in section 6.2.6 and 6.2.10). If your configuration will use I^2C as an SMBus controller, contact ADS Sales to discuss the BitsyX configuration you'll require.

4.5.5 Multimedia Card (MMC) Controller

The XScale MMC controller provides a serial interface to MMC cards. The controller supports up to two cards in either MMC or SPI modes with serial data transfers up to 20 Mbps. The MMC controller has FIFOs that support DMA access to and from memory.

This interface can also be used to access Secure Digital (SD) Memory Cards and Secure Digital I/O (SDIO) cards. See Intel Application Note 278533 for details and pitfalls.

Signals for the MMC Controller are brought out to header J7. See the XScale Developer's Manual for details about how to use the MMC interface.

Drivers for MMC may not be available for all operating systems. Contact ADS for driver availability for the operating system you are using.

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[14] ACPI: Advanced Configuration and Power Interface, http://www.acpi.info

[15] Smart Battery Implementers Forum:,http://www.sbs-forum.org/

[16] Maxim application note 356, http://dbserv.maxim-ic.com/appnotes.cfm?appnote_number=356

4.6 Displays

The BitsyX uses the integrated XScale display controller to drive liquid crystal displays (LCDs). Connector J1 supplies the power and data signals needed to drive LCDs, while backlight and touch panel control signals are located on connector J3.

4.6.1 Display Types Supported

ADS has configured the BitsyX for a wide variety of display types and sizes. Consult the ADS support site (section 2.4) for the latest list of displays supported by ADS. If a display isn't on the list, contact ADS Sales for information about ADS' panel configuration service.

The XScale controller uses system memory for the display frame buffer, and can drive VGA (640x480) and SVGA (800x600) displays easily. Larger displays will work with the XScale, with some constraints imposed by the controller architecture. The ADS Support Forums provide details about the design tradeoffs that are required to support larger displays.[17]

The BitsyX can drive LVDS displays using an ADS adapter circuit.

4.6.2 Panel Voltages

The BitsyX supplies 3.3 V or 5 V power to the LCD display via J1. Select this voltage with JP3 (section 3.2.1). Please observe the cautions listed with the JP3 settings.

4.6.3 Display Signals

XScale display signals *L_DD0* through *L_DD15*--as well as the pixel clock, vertical sync and horizontal sync--are all buffered at a factory-set voltage. See section 6.2.2 for full specifications.

The *PNL_RL* and *PNL_UD* signals are for active (TFT) displays that support changing the scan direction. This feature allows the display to be flipped right-to-left (*RL*) or up-and-down (*UD*) by changing the voltage on these signals. See section 6.2.2 for full specifications.

[17] Currently posted at http://www.applieddata.net/forums/topic.asp?topic_id=580

4.6.4 Creating Display Cables

ADS has designed cables for a wide variety of displays. See the list of supported displays on the ADS support forums. Cable drawings for supported displays are available on request.

While ADS does not provide support to customers to create their own cables, designers with LCD display experience may be able to design their own. For those that do so, a key point to keep in mind is that the PXA255 LCD interface maps its display controller pins differently based on LCD technology and color palette size. The following table illustrates how they are mapped for some of the more common technologies. Consult the PXA255 User's Manual for more information.

<table>
<tr><th rowspan="2">XScale [18]
Signal Name</th><th colspan="2">Color Active</th><th colspan="3">Color Passive</th><th colspan="4">Mono Passive</th></tr>
<tr><th>16-bit</th><th>12-bit</th><th colspan="2">Dual</th><th>Single</th><th colspan="2">Dual</th><th>Single DPD[19]</th><th>Single</th></tr>
<tr><td>L_DD0</td><td>B0</td><td>B0</td><td>DU0</td><td rowspan="8">top</td><td>D0</td><td>DU0</td><td rowspan="4">top</td><td>D0</td><td>D0</td></tr>
<tr><td>L_DD1</td><td>B1</td><td>B1</td><td>DU1</td><td>D1</td><td>DU1</td><td>D1</td><td>D1</td></tr>
<tr><td>L_DD2</td><td>B2</td><td>B2</td><td>DU2</td><td>D2</td><td>DU2</td><td>D2</td><td>D2</td></tr>
<tr><td>L_DD3</td><td>B3</td><td>B3</td><td>DU3</td><td>D3</td><td>DU3</td><td>D3</td><td>D3</td></tr>
<tr><td>L_DD4</td><td>B4</td><td></td><td>DU4</td><td>D4</td><td>DL0</td><td rowspan="4">bottom</td><td>D4</td><td rowspan="4">not used</td></tr>
<tr><td>L_DD5</td><td>G0</td><td>G0</td><td>DU5</td><td>D5</td><td>DL1</td><td>D5</td></tr>
<tr><td>L_DD6</td><td>G1</td><td>G1</td><td>DU6</td><td>D6</td><td>DL2</td><td>D6</td></tr>
<tr><td>L_DD7</td><td>G2</td><td>G2</td><td>DU7</td><td>D7</td><td>DL3</td><td>D7</td></tr>
<tr><td>L_DD8</td><td>G3</td><td>G3</td><td>DL0</td><td rowspan="8">bottom</td><td colspan="5" rowspan="8">not used</td></tr>
<tr><td>L_DD9</td><td>G4</td><td></td><td>DL1</td></tr>
<tr><td>L_DD10</td><td>G5</td><td></td><td>DL2</td></tr>
<tr><td>L_DD11</td><td>R0</td><td>R0</td><td>DL3</td></tr>
<tr><td>L_DD12</td><td>R1</td><td>R1</td><td>DL4</td></tr>
<tr><td>L_DD13</td><td>R2</td><td>R2</td><td>DL5</td></tr>
<tr><td>L_DD14</td><td>R3</td><td>R3</td><td>DL6</td></tr>
<tr><td>L_DD15</td><td>R4</td><td></td><td>DL7</td></tr>
<tr><td>L_PCLK</td><td colspan="2">PCLK</td><td colspan="7">PCLK</td></tr>
<tr><td>L_LCLK</td><td colspan="2">HSYNC</td><td colspan="7">LCLK</td></tr>
<tr><td>L_FCLK</td><td colspan="2">VSYNC</td><td colspan="7">FCLK</td></tr>
<tr><td>L_BIAS</td><td colspan="2">DE</td><td colspan="7">LBIAS</td></tr>
</table>

4.6.5 Developing Display Drivers

The XScale has a bank of registers (LCCR0 through LCCR3) that define the timing for displays. In addition, the operating system must define the region of memory for the frame buffer(s).

ADS provides display timings for supported displays on request. For displays not yet supported, ADS has a panel configuration service to creates panel timings and cable drawings. Contact ADS Sales for further details.

[18] Intel. PXA255 Processor: Developer's Manual. Order number 278693-001, March 2003. pp. 7-20 to 7-22.

[19] Double pixel data (DPD) mode = 1

4.6.6 Brightness Control (Backlight)

Most LCD displays include one or more cold-cathode fluorescent lamp (CCFL) tubes to backlight the displays. Some LCDs, such as passive transflective displays, can be viewed in daylight without backlighting.

Panel backlights are driven by backlight inverters. These circuits are typically external to the display and generate the several hundred volts required to drive the CCFL tubes. Backlights can easily become the greatest source of power consumption in a portable system. Fortunately, most backlight inverters include control signals to dim and turn off the backlight.

The BitsyX supplies two signals for backlight control: BacklightPWM (J3.16) and /BacklightOn (J3.18). BacklightPWM is a filtered PWM signal that supplies an analog output voltage to control the intensity of the backlight. The /BacklightOn signal is an open-collector output to turn the backlight on and off. The ADSmartIO controller drives these signals. See section 6.2.2 for electrical specifications.

4.6.7 Contrast Control (Vee and Vcon)

Vee and Vcon are used to control the contrast of passive panels. Many passive panels require a positive or negative bias voltage in the range of fifteen to thirty volts to bias the passive LCD display.

Some displays include a Vee generator and simply require a low-voltage analog signal to control the contrast. The Vcon output is a PWM-controlled output that can be used for this purpose. Electrical specifications for Vee and Vcon are listed in section 6.2.2.

4.6.8 Touch Panel

The BitsyX supports four and five-wire analog resistive touch panels (five-wire control is a factory option). Connect the touch panel to the inputs on connector J3. The touch panel controller can wake the system from sleep (section 5.3.3) Electrical details are listed in section 6.2.3.

4.7 EMI/RFI and ESD Protection

The BitsyX board incorporates a number of industry-leading features that protect it from electrostatic discharge (ESD) and suppress electromagnetic and radio-frequency interference (EMI/RFI). Transient voltage suppressors, EMI fences, filters on I/O lines and termination of high-frequency signals are included standard on all systems. For details, see electrical specifications for subsystems of interest.

4.7.1 Agency Certifications

Many products using ADS single-board computers have successfully completed FCC and CE emissions testing as a part of their design cycle. Because ADS supplies only the single-board computer and not fully integrated systems, ADS cannot provide meaningful system-level emissions test results.

See the crystal frequencies (section 6.2.11) and electrical specifications for information that may be helpful during agency certifications.

4.7.2 Protecting the Power Supply Inputs

It is the responsibility of the designer or integrator to provide surge protection on the input power lines. This is especially important if the power supply wires will be subject to EMI/RFI or ESD.

5 Power and Power Management

Power management is especially critical in portable and handheld applications where battery power is at a premium. The BitsyX includes advanced power management features, including the low power XScale CPU, partitioned power distribution and ability to run from several types of DC power inputs. The BitsyX can also operate as a conventional single-board computer, taking advantage of the inherently low power consumption of the system.

This chapter describes the architecture of the BitsyX power supply, factors affecting power consumption and reference designs to get you started. For information about how much power the BitsyX consumes, consult the electrical specifications in section 6.2.5.

5.1 Determining the Features You Need

Not all designs with the BitsyX need to be optimized for lowest power consumption. Consider the following types of typical system configurations to determine the topics of interest to your application.

Relevant Topics / Features Required	"Line" power (5.3.1)	Control ext power supply (5.3.2)	Sleep/ wakeup button (5.3.3)	Backlight power control (5.3.6)	System battery (5.3.1)	Battery charging (5.3.7 and 5.5.3)	Supercapacitors (5.3.5)	RTC battery (4.2 nd 5.5.1)
System is On All the Time	✓							
System Power Supply Turned Off to Shut Down System		✓					✓	
System Should "Turn Off" when not in use	✓	✓	✓	✓				
Battery-Operated, Minimum Power Consumption					✓	✓		
"Pulled-Plug"/Brownout Protection			✓		✓	✓	✓	
Must Preserve Time and Date Under All Circumstances			✓		✓			✓

5.2 Power Management Modes

Handheld and portable systems available today never really turn "off." They make use of power management algorithms that cycle the electronics into "standby" and "sleep" modes, but never fully remove power from the full system.

This section describes the various power management modes of the XScale processor and how the BitsyX makes use of them.

5.2.1 XScale Power Management Modes

The XScale PXA255 processor supports four operational modes: Turbo, Run, Idle, and Sleep.

- Sleep mode uses the least amount of electrical power. The processor core is powered off and only a few processor peripherals (RTC, I/Os and interrupt control) remain active. The transition back to Run mode may take a few hundred milliseconds, as clocks must stabilize and hardware that was powered off must be reinitialized.
- Idle mode reduces power consumption by pausing the processor core clock. Processor peripherals remain enabled. This mode is used for brief periods of inactivity and offers a quick transition back to Run mode.
- Run mode is the standard mode used when applications are running. It offers the best MIPS/mW (performance vs. power) performance when running applications from RAM.
- Turbo mode runs the processor core at up to three times the Run mode speed. Since external memory fetches are still performed at the memory bus frequency, Turbo mode is best used when running the application entirely from cache.

5.2.2 Power Management on the BitsyX

The BitsyX can actively be configured to be in XScale Run or Sleep modes. Turbo and Idle modes are controlled by the operating system and is typically transparent to the application.

In Turbo, Run and Idle modes, the power supplies are in their standard, full-power state and applications run normally on the system. Specific subsystems (as described in section 5.3.2) may be selectively disabled to conserve power during these states. The operating system is responsible for adjusting the core voltage (Vddi) for optimal power consumption in each mode.

In Sleep mode, sometimes called "Suspend" mode, the processor puts the SDRAM in a low-power, self-refresh mode, the processor core shuts off, most peripheral sub-systems are shut down and the power supplies drop into low-power states or turn off entirely (see the diagram in section 5.3.2 for details). In this state, the BitsyX consumes very little power, most of which is dedicated to the maintenance of the RAM (see section 6.2.5 for specifications). The system can be "awakened" and returned to the Run state by initiating a system wakeup using one of the methods described in section 5.3.3.

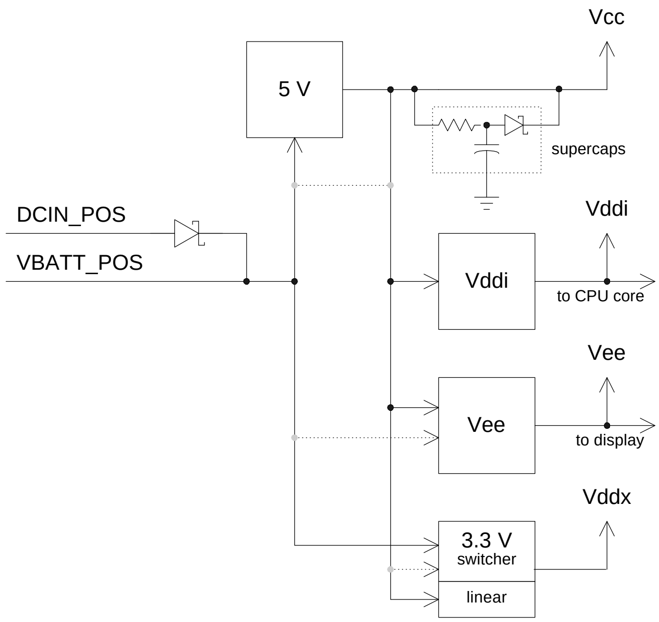
If Main Power (DC_IN or VBATT_POS) drops below the power supply trip point (section 6.2.2), the BitsyX automatically goes in Sleep mode. The transition time from Run mode to Sleep mode is a function of the operating system. System Sleep can also be initiated programmatically.

5.3 *Architectural Overview and Power Management Features*

This section provides an overview of the architecture of the BitsyX power supply and a description of the various features of the BitsyX power management systems.

5.3.1 Power Supply Architecture

The BitsyX power supply is laid out as shown in the following diagram. Incoming DC power is regulated to 5 and 3.3 V. Other system voltages are derived from these power supplies.



DC_IN and VBATT voltages are mixed using a diode with a low forward voltage. This allows a battery and DC power supply to be connected at the same time. If only one power supply is used for your system, use the VBATT_POS input. See sections 5.3.7 and 5.5.3 for examples.

Vddi is a variable-voltage power supply controlled by the XScale I^2C bus (4.5.4). This voltage scaling feature allows the operating system to manage power consumption over the full range of CPU clock rates.

Several factory options are available and are indicated by dashed lines in the diagram above. The supercapacitors (section 5.3.5) are a typical factory option. The other options are available for production customers, but are outside the scope of this manual. Contact your ADS sales representative if you believe one or more of these options is required for your application.

Specifications for the BitsyX power supply are listed in section 6.2.4.

5.3.2 Subsystem Partitioning

The BitsyX can selectively turn off power to subsystems on the board. This load-shedding feature can extend battery life and significantly increase the amount of time the supercapacitors will hold up system power. Applications and the operating system determines how selective power management is utilized.

BitsyX systems that can be selectively disabled include the following:

- LCD display (panel power and signal buffers)
- Vee (contrast control)
- Audio output amplifier
- Audio codec and microphone pre-amps
- Serial 1 and 3 RS-232 buffers
- External device 1 (/PE1, J3.42)
- External device 2 (PE2, J3.24)

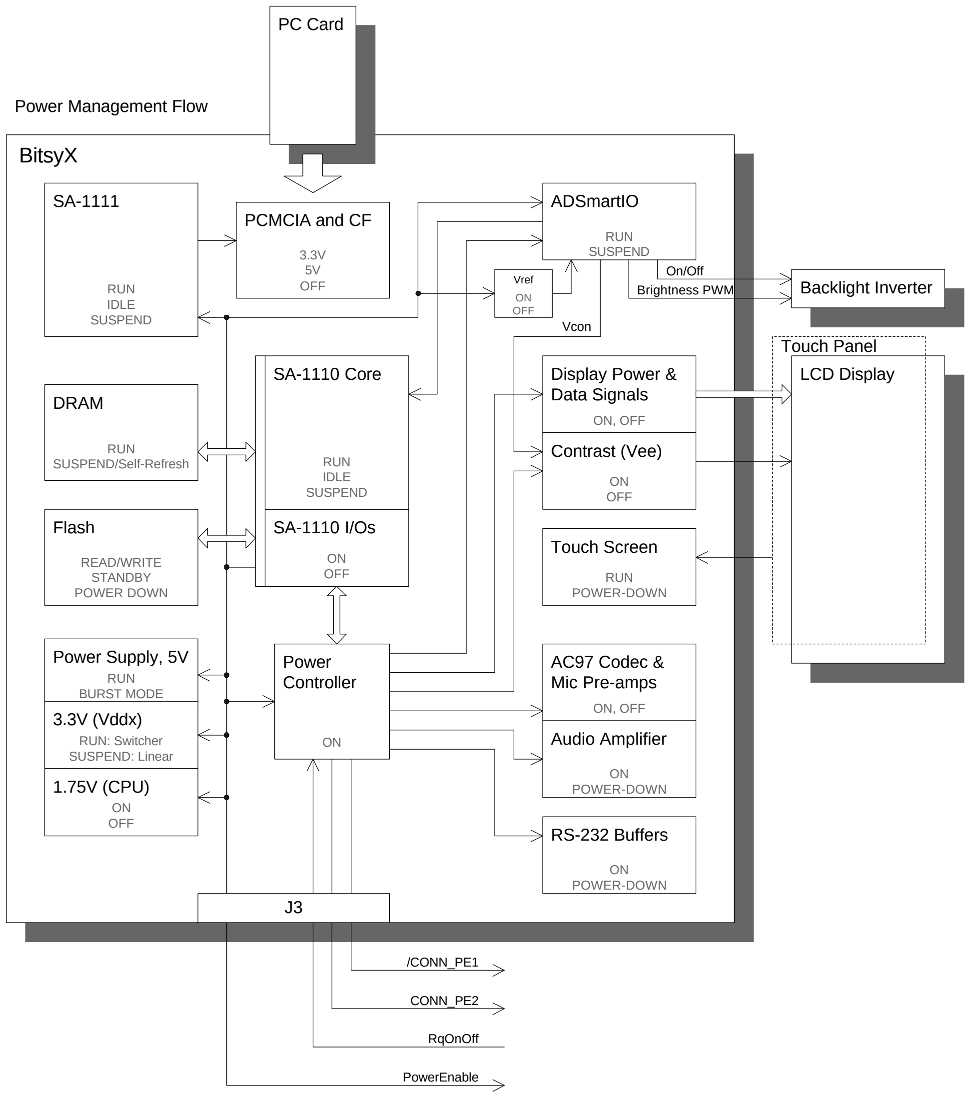
In addition, the BitsyX also controls its core power supplies to support sleep operation:

- Vcc (5 V) supply
- Vddx (3.3 V) Vddi (processor core) supplies

The following diagram illustrates the architecture of the BitsyX power management system. At the heart of the system is a power controller that controls the state of the various power subsystems of the BitsyX. Under control of the XScale processor, this controller can manage most of the power distribution of the board. The XScale PowerEnable signal controls the rest of the subsystems.[20]

[20] The controller inverts the PowerEnable signal for use with some subsystems. This details is not shown in the diagram.

In the diagram, the power management modes of each of the subsystems is indicated in gray. Arrows indicate the direction of both signal flow and of power management.



5.3.3 System Sleep

This section describes several methods for putting the system into Sleep mode.

Power Failure Interrupt

When the input voltage falls below Vsleep (section 6.2.2), the system generates a in internal power failure interrupt (the DC_GOOD signal goes low). This interrupt gives the operating system early warning of an impending power failure, allowing the system to drop into low-power Sleep mode before power has failed completely.

Systems that have supercapacitors benefit from this feature by going to sleep before they begin drawing down energy stored in the capacitors. This prolongs the amount of time the system can maintain the contents of RAM.

Operating systems may allow the option to ignore power-failure interrupts. This allows systems to run with lower input voltages without going to sleep. However, note that if the system does go to sleep, it will not be able to wake until the input voltage is above Vsleep (see section 5.3.4 for details).

RQOnOff Input

Operating systems and applications can configure the /RQONOFF signal (J3.45) to put the system to sleep. In conjunction with the wakeup function (section 5.3.4, below), the RQONOFF input can be used as an "on/off" button for some systems. Electrical specifications are listed in section 6.2.7.

Software Control

Applications can put the system to sleep programmatically. Operating systems may also put the system to sleep if the system has not been used for a certain amount of time or for other reasons. In remote, battery-powered applications, software Sleep can be used in conjunction with the Timed Wakeup feature (section 5.3.4) for minimum power consumption.

5.3.4 System Wakeup

This section describes several mechanisms for waking a BitsyX system from Sleep mode. The system will resume operation in Run mode unless the power supply voltage is lower than Vsleep (section 6.2.1). If the input voltage is too low, the system will not wake under any circumstances. This protects the RAM from getting corrupted by an undervoltage condition.

RQOnOff Input

Shorting the /RQONOFF signal (J3.45) to ground will wake the system. The signal is connected to the system controller. Electrical specifications are listed in section 6.2.7.

Touch Panel

The touch panel controller interrupts the processor when touch panel events occur. Before going to sleep, the processor can place the controller in a low-power sleep mode from which the controller generates a wakeup interrupt when a touch event occurs.

Timed Wakeup

The XScale can wake up at a predetermined time. This feature is controlled by software.

ADSmartIO/Keypad

The ADSmartIO controller controls the wakeup signal to the StrongARM. For production applications, ADS can configure the ADSmartIO to wake up the system on specific events (e.g. the BitsyX adds a factory option to wake upon keypad activity). Contact ADS Sales if your application requires a special wakeup event.

5.3.5 Supercapacitors (factory option)

Supercapacitors (sometimes known as "ultracapacitors") are energy storage devices that combine the quick charge/discharge characteristics of capacitors with the higher energy density of batteries. "Supercaps," as they are called, are useful for maintaining power when changing batteries or for riding out power failures.

Supercaps are a factory option for the BitsyX and must be requested when you place your order. Supercaps are the two large cylinders mounted between the PCMCIA header and 50-pin headers J9 and J10.

Charging

There are two important factors related to the charging phase of the capacitors. The first is how long it takes to fully charge the capacitors. The second is the added load on the power supply it takes to charge the capacitors. Both are important to effectively use the supercaps.

Charge time for capacitive circuits is typically measured in "time constants," the product of the charging resistance, R and the capacitance, C. It takes three time constants (3RC) to charge fully-discharged supercaps to 95% of their target voltage. For example, a system with 44 ohm charging impedance and 1.65 F supercaps has a time constant of 73 seconds. Allow at least five minutes to recharge the capacitors after the board has been disconnected from power. Charge time is shorter if the supercaps aren't completely discharged.

The charging current for the supercaps starts out high and diminishes exponentially as the capacitors reach full charge. Make sure to account for this current in your power budget (section 5.4.1). The charge current is calculated as

$$i(t) = \frac{V_t - V_i}{R}\ e^{-t/RC}$$

where

V_t	is the charging/final voltage of the capacitor (assume 5.0 V unless the capacitor is not charged completely),
V_i	is the initial charge voltage of the capacitor, and
t	is the time in seconds

Use the maximum current (time=0, V_i=0, $i(0)=i_{max}=V_t/R$) in your power budget.

Discharging

When power fails on a system equipped with supercaps, the operating system shuts off all power to the board and puts the system to sleep. When power is restored, the system remains asleep until either the system is awakened (J3.45) or is reset (J10.45).

The amount of time that a system can remain asleep using only supercap power depends primarily on how quickly external power drops off and how quickly the operating system can put the board to sleep.

If the operating system can shut down the system before the power supply drops below the supercap charge level, you will get significantly longer sleep time from your supercaps. You can calculate how much time the system will have to go to sleep based on (1) how quickly your power supply will fall when main power fails and (2) the trip point of the BitsyX power fail circuit (section 6.2.1). When possible, put the system to sleep with software if a power failure condition is expected (e.g. changing a battery).

The supercaps discharge linearly from the constant-current drain during sleep according to the equation

$$t = \frac{(V_i - V_f - 0.2) * C * Eff}{I_{sleep}}$$

where

t	is the duration the system can sleep, in seconds;
V_i	is the initial charge voltage of the capacitor;
V_f	is the supercap voltage at which onboard systems will fail (assume 3.2 V);
C	is the capacitance of the supercaps, in Farads;
Eff	is the efficiency of power delivery; 85-90% is a safe value to use;
I_{sleep}	is the amount of current the system consumes while in sleep mode.

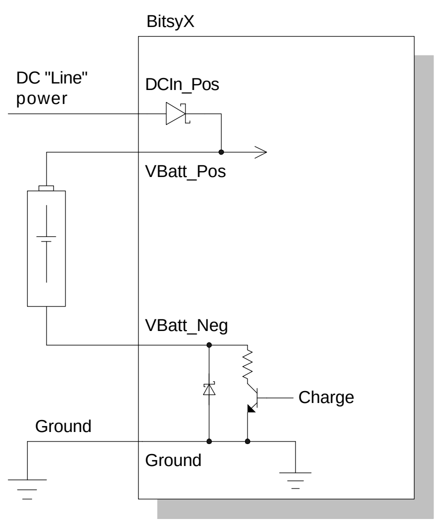
For example, a system with fully charged 1.65 F supercaps and a sleep current of 4 mA can expect to run for up to ten minutes after a power failure. Consult the electrical specifications of section 6.2.4 and power consumption specifications of 6.2.5 for the values to use in your calculations.

5.3.6 Backlight Power

The BitsyX provides software control of Backlight Intensity and On/Off using the ADSmartIO controller. Power for the backlight is not routed through the board, and must be supplied to the backlight separately from the BitsyX. This provides the greater flexibility when selecting backlight inverters for an application. See section 4.6.6 for further details about backlight control.

5.3.7 Battery Trickle Charger (factory option)

The BitsyX includes a trickle charger for basic charging of external batteries. The following diagram illustrates the charging circuit and a standard means of combining it with DC line power.



The Charge signal comes from the ADSmartIO controller (port PB0) and is also available on J3 pin 22 for external use. Writing a logic "1" to PB0 turns on the trickle charging. It is up to the application to manage battery charging.

The diode on the negative terminal of the battery allows the battery to power the BitsyX at any time, but prevents the battery from being charged by a DC voltage on the DCIN_Pos input. The charge current is calculated as follows:

$$I_{charge} = \frac{DCIN\_Pos - (2 * 0.2) - V_{batt}}{R}$$

where

Vbatt is the battery voltage (Vbatt_pos-Vbatt_neg), and

R is the charge resistor (section 6.2.4).

While standard systems include the charging circuit, the charge resistors must be selected for effective charging of specific batteries to be used. Select a resistor value that will provide the desired charge current but not exceed the power rating of the resistor. Since $P=I^2R$,

$$I_{charge,\ max} = \sqrt{P_{ch} / R}$$

where P_{ch} is the maximum power the charge resistor can support. Consult the electrical specifications in section 6.2.2 for the values populated on standard systems.

5.3.8 Power Supply Efficiency

The BitsyX power supply achieves high efficiency through several means. First, it utilizes high-efficiency switching regulators. These regulators use conventional step-down switchers under operating load conditions, but are configured by the system for linear and "burst" mode[21] operation during low-load conditions that occur during system sleep. Additionally, there is only one level of cascaded regulation, reducing the losses that multiply through each stage.

5.4 Designing for Optimal Power Management

Designing a system for optimal power management requires careful attention to many details. This section provides some guidelines and tips for best power management.

5.4.1 Create a Power Budget for Peripherals

Embedded system designers using the BitsyX should have a clear understanding of how power usage will be allocated in the system they design. Designers should create a power budget that takes into account the types of devices that are expected to be used with the BitsyX.

The following lists detail some of the typical external loads that can be placed the BitsyX power supplies. Baseline power consumption of the BitsyX is listed in section 6.2.5.

3.3 V Loads

Typical external loads on the 3.3 V power supply include the following:

- Display
- Personality Board
- CF and some PCMCIA cards

[21] "Burst mode" in this context is a registered trademark of Linear Technology Corporation

5 V Loads

5 V loads come from both onboard and external devices:

External:

- Display
- Backlight
  Only if powered by 5 V BitsyX power supply
- Most PCMCIA cards
- USB devices
- PS/2 keyboard
- Speaker(s)
  Assume 80% efficiency

Onboard:

- 3.3 V Supply
  Multiply by 115% to account for 3.3 V power supply efficiency
- Supercaps
  Use peak inrush current in your budget

Loads on Main Supply

The main power supply (DCIN_Pos or VBatt_Pos) is loaded by the 5 V and 3.3 V supplies as indicated in the diagram of section 5.3.1. Assume 85% efficiency for external loads that cascade through the 5 V supply. Consider these loads when creating your power budget.

5.4.2 Power Loads During Sleep

When designing systems for minimal power consumption during Sleep mode, make sure to consider DC losses to external connections. The following are a few of the ways your system may "leak" when asleep:

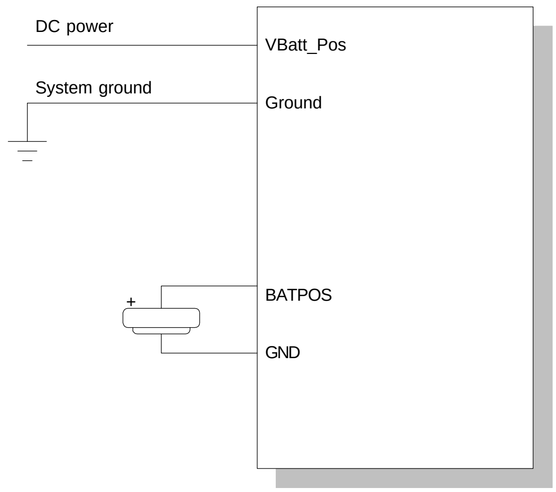
- PCMCIA and CF cards
  Cards in place when the system is asleep can drain power through the Card Detect and Voltage Sense lines. Assume that all four lines ground the BitsyX PCMCIA pull-ups (section 6.2.12) while the card is inserted.
- Digital I/Os
  Review digital I/O connections for potential voltage differences from external connections when the BitsyX is asleep.
- USB
  Depending on how USB devices are powered and how the operating system handles USB, USB devices may draw power during Sleep.

5.5 *Power Supply Examples*

The following are basic examples of how to configure power supplies for the BitsyX.

5.5.1 Basic DC Supply

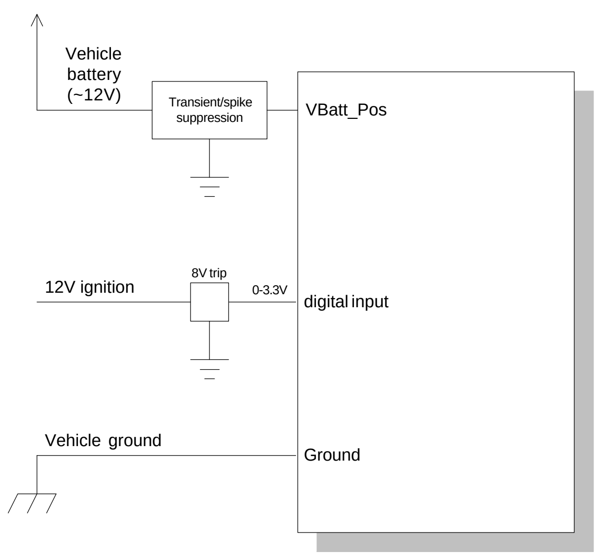
The simplest way to power the BitsyX is to supply DC power to the VBatt_Pos input, as shown below.



This diagram also illustrates how to connect a coin cell to the RTC circuit for systems that require the RTC to be maintained under all power conditions.

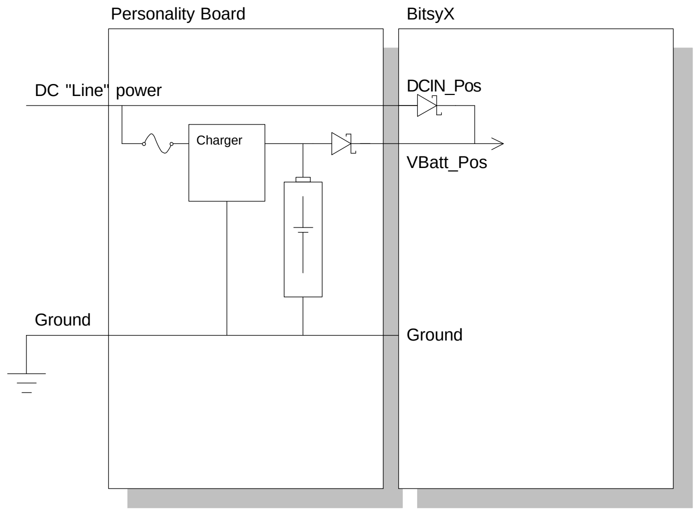
5.5.2 Automotive System

This system connects the BitsyX directly to the vehicle battery, but polls a sense line on the ignition to put the system to sleep when the vehicle is turned off.



5.5.3 Line Power and Battery with External Charger

You may choose to use an off-board battery charger for a specific battery chemistry or voltage. The following diagram illustrates one way to include a charger on your own personality board.



In this example, DC "Line" power may come from a DC power supply, battery or other DC power source.

The Bitsy Personality Board (ADS p/n 640111-8000) includes an external battery charger using a design similar to the one depicted above.

For an illustration of how to use the onboard BitsyX trickle charger in conjunction with line power, see the diagram in section 5.3.7.

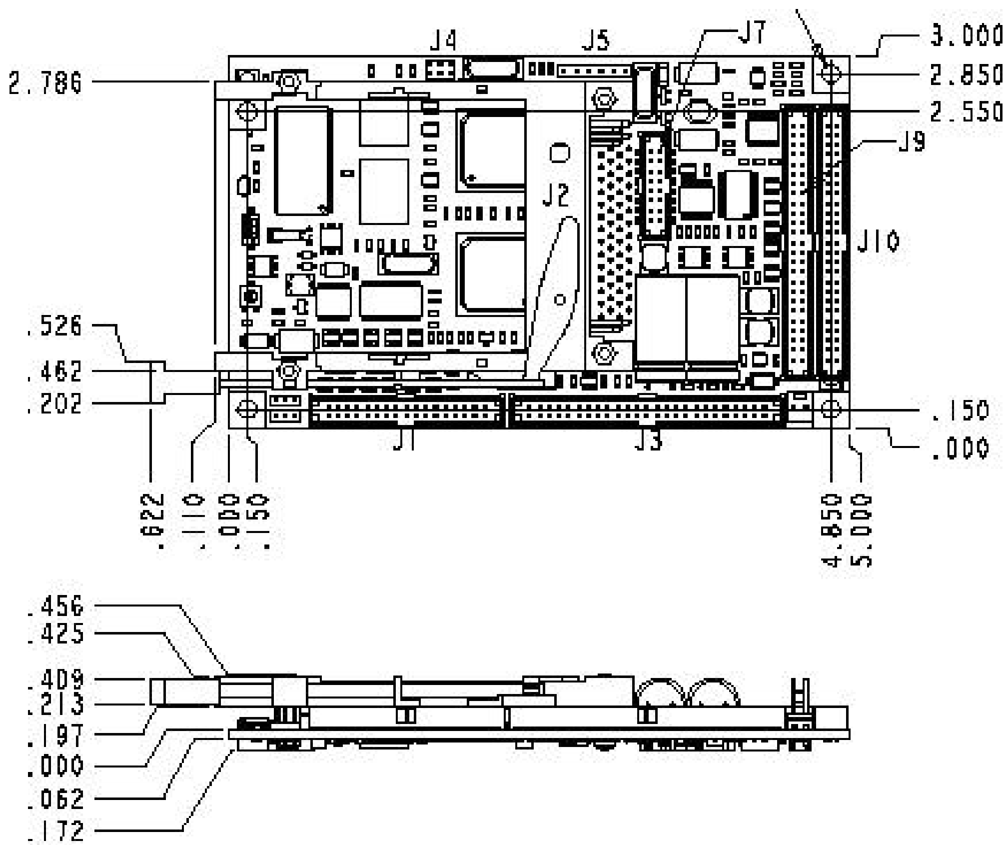
6 System Specifications

6.1 Mechanical Specifications

The BitsyX is 3.0 inches by 5.0 inches in size. This section describes the component dimensions and mounting of the board. Detailed drawings are available on the support forums (section 2.4), and 3D models are available from ADS in electronic format for production customers.

6.1.1 Mechanical Drawing

The following mechanical drawing of the BitsyX specifies the dimensions of the BitsyX, as well as locations of key components on the board. The PCMCIA ejector is integrated into the design and is not removable. All dimensions are in inches. This image is an excerpt from the full mechanical drawings, ADS document number 630115-00003.



6.1.2 Mounting Holes

Four holes are provided, one on each corner, for mounting. The diameter of the holes is 0.138-in. Mounting holes are plated through and connected to the BitsyX ground plane.

For reliable ground connections, use locking washers (star or split) when securing a BitsyX in an enclosure. Make sure that washers do not extend beyond the limits of the pads provided.

6.1.3 Clearances

The BitsyX has a low profile. It can fit in an enclosure with inside dimensions as thin as 0.728 inch (18.5 mm). Key clearances are as follows:

- Highest component: 0.456 inch (11.6 mm), top
  0.110 inch (2.79 mm), bottom
- Board thickness: 0.062 inch (1.57 mm)
- Clearance over top/bottom: 0.05 inch (1.3 mm)

Note: Selection of connectors and wiring harnesses will determine height of final assembly.

6.1.4 Production Options

The BitsyX has a number of production options detailed throughout this manual. This section describes options that most significantly affect the mechanical design of the board. These options are generally available only for volume production orders.

Mating Headers on Underside of Board

The four system signal headers—J1, J3, J9 and J10—can be mounted on the underside of the BitsyX. This allows the BitsyX to sit on top of another board.

Important! When the headers are placed on the underside of the board, the pin numbers will not correspond to the signals as described in this manual. Lay out the mating board with this in mind.

Supercapacitors

Section 5.3.5 describes the supercapacitor option. The capacitors are two large cylinders mounted between the PCMCIA header and header J9. When they are not populated, there is a conspicuously open space marked on the board where they would have been placed.

Removal of PCMCIA Header

Systems can be produced without the PCMCIA header. However, since most ADS operating system ports rely on the header for file updates, this option is not recommended. A special operating system build may be needed if the PCMCIA header is removed.

Connector Plating

Connectors on the BitsyX come standard with tin plating, which is suitable for most applications. For applications where the headers will go through many insertion/removal cycles, ADS can populate headers with gold or other suitable platings. The PCMCIA header comes standard with gold plating.

6.2 Electrical Specifications

6.2.1 Temperature, Reset, Sleep, Wakeup

Absolute Maximum Ratings

Reset Input (RESET_IN) ....3.6 V (note 1)

Wakeup Input (/RqOnOff) ....5.5 V (note2)

Symbol	Parameter	Min	Typ.	Max	Units
Temperature					
Trun	operating temperature	-40		+85	°C
Reset_In (J10.45)					
Vrst	trigger voltage (Note 3)		2.7		V
Vprst	pull-up voltage		Vddx		V
Rprst	pull-up resistance		47		kΩ
Sleep (5.3.3)					
Vsleep	Sleep trigger voltage (Note 4)	5.4		5.8	V
Vsleep,hyst	Sleep trigger release hysteresis (Note 5)	0.06		0.25	V
Wakeup: RqOnOff (J3.45)					
trq	wakeup pulse duration (Note 6)	100			ms
Vprq	pull-up voltage		Vddx		V
Rprq	pull-up resistance		11		kΩ

Notes:

1. The reset controller can support operating voltages up to 10 VDC. However, such high voltages on Vddx through the pull-up resistor may damage the system.
2. The RqOnOff signal is connected to the system controller, which determines this rating (see section 6.2.7).
3. Short /Reset_In to GND to reset system
4. This is the voltage at VBATT_POS at which the DC_GOOD signal (4.3.7) changes from high to low, which can trigger the system to go into Sleep mode. Sleep trigger at DCIN_POS is Vsleep+Vdin (6.2.4).
5. **Important!** Once Vsleep has been triggered, the input voltage must rise at least Vsleep,hyst above Vsleep before the voltage detector will restore the DC_GOOD signal. Make sure that your input voltage is designed to always run above Vsleep+Vsleep,hyst, or systems that go to sleep may not be able to wake again.
6. Short /RqOnOff to GND to for at least trq to wake up system. A low-level voltage on /RqOnOff initiates wakeup.

6.2.2 Display

LCD display panels have a wide range of voltage and data requirements. The BitsyX has a number of adjustable voltages to support these requirements, as well as controls for brightness (backlight) and contrast (passive panels only). See section 4.5.5 for further details.

Symbol	Parameter	Min	Typ.	Max	Units
LCD (4.6.2)					
V pnl	Display power supply (note 7)	3.3		5.0	V
P pnl_pwr	Display power (note 8)			2	W
V pnl_data	Panel data voltage (note 9)	3.3	3.3	5.0	V
Scan direction (active displays) (4.6.3)					
R pnl_rl	Pull-up/down resistance		4.7		kΩ
R pnl_ud	Pull-up/down resistance		4.7		kΩ
V pnl_rl	(note 10)	0	V pnl	V pnl	V
V pnl_ud	(note 11)	0	V pnl	V pnl	V

Symbol	Parameter	Min	Typ.	Max	Units
Contrast Control (passive displays) (3.2.2, 4.6.7)					
Vee(-)	Contrast adjust, R_L=5kΩ, JP4: 1-2	-30		-15	V
Vee(+)	Contrast adjust, R_L=5kΩ, JP4: 2-3	15		30	V
Vcon	Low-voltage contrast adjust (note 12)	0		Vddx	V
Brightness Control (backlight, 4.6.6)					
R backlightOn	Pull-up (factory option, note 13)		10		kΩ
V backlightOn	Pull-up installed (note 13)		5		V
	No pull-up			30	V
V backlightPWM	PWM (note 14)	0		3.3	V
R backlightPWM	PWM series resistance (note 14)		1.2		kΩ

Notes:

7. JP3 selects the display voltage.
8. Total power available depends on system power budget.
9. Systems are configured at the factory with buffers for 3.3 or 5 V panel data. R289 selects 5 V power for the buffers while R288 selects 3.3 V power (they're located under the opening for the PCMCIA header about 1cm from the right, ejector corner of the board). 5 V displays with Vih <= 0.6•Vpnl_pwr (3.0 V) will work reliably with 3.3 V data.
10. PNL_RL is pulled up with R87 or pulled down with R22.
11. PNL_UD is pulled up with R79 or pulled down with R17.
12. Vcon is the low-voltage PWM signal used to control Vee. It can be used directly with some passive displays to control contrast.
13. A pull-up resistor (R116) can be installed on the BacklightOn signal as a factory option. If the pull-up is not installed, maximum voltage is limited by the transistor ratings.
14. The backlight on/off and PWM outputs are driven by the ADSmartIO controller

6.2.3 Touch Panel Controller

The BitsyX uses touch panel controllers from Burr Brown. It uses the ADS7846 to support four-wire analog-resistive touch panels and the ADS7845 to support five-wire panels. The system is factory-configured for use with four-wire panels. All touch-panel signals are ESD and RF protected. The touch panel controller is powered during sleep mode and can generate an interrupt to wake the system.

Symbol	Parameter	Min	Typ.	Max	Units
Vdd	Supply voltage		Vddx		V
---	A/D sample resolution		12		bit

6.2.4 Power Supply

Absolute Maximum Ratings

Supply Voltage (DCIN_POS).................................... 18 V

Symbol	Parameter		Min	Typ.	Max	Units
System Power						
VBATT_POS	BitsyX supply voltage (Note 15)		5	12	15	V
Vdin	Diode drop from DCIN_POS to VBATT_POS at 130 mA			0.35	0.4	V
VDDI	Processor core voltage (6.2.10)		0.85	1.0	1.3	V
VDDX	3.3 V onboard supply	Run	3.1	3.3	3.5	V
		Sleep		3.15		V
VCC	5.0 V onboard supply		4.75	5.0	5.25	V

I (Vcc)	5 V available for display, PCMCIA, USB, J9.15, J10.48, etc. (Note 16)	Run			500	mA
		Sleep				
I (Vddx)	3.3 V available for display, PCMCIA, J9.23, J10.47, etc. (Note 17)	Run			700	mA
		Sleep			100	mA
Supercapacitor Option (section 5.3.3)						
C	Capacitance			1.65		F
Vcap	Charge voltage			Vcc		V
Rcap	Series charge resistance			44		Ω
tc	Charging time from full discharge		5			min
RTC Backup Power (4.2)						
V BATPOS	real-time clock battery backup		2.2	3.0	3.6	V
I BATPOS	RTC current (note 18)			300	500	nA
Battery Trickle Charger (section 5.3.7)						
Rch	Charger series resistance			37.5		Ω
Pch	Charge resistor power rating				0.25	W

Notes:

15. The system can operate down to the minimum voltage shown, but the DC_GOOD signal may cause the system to go to sleep when running at that voltage. See *Power Failure Interrupt* in section 5.3.3 for details. The power failure feature can be overridden.
16. LTC 1771 "Burst" mode, used when the BitsyX is in Sleep mode, is more efficient at low currents. However, it is electrically noisier and can cause significantly greater EMI/RFI at higher current draws.
17. During Sleep mode, Vddx is powered by a linear regulator, which draws from the 5V supply.
18. Vddx=0V, Vbatpos=3.2 V (source: DS1307 data sheet)

6.2.5 Power Consumption

The following table lists typical power consumption for the BitsyX with varying input voltage and activity levels. Run mode efficiency of the power supply decreases slightly with higher input voltage.

Power consumption varies based on peripheral connections, components populated on the system and the LCD panel connected. Input voltage, temperature and the level of processor activity affect power consumption to a lesser extent.

LCD displays and backlights add significantly to the total power consumption of a system. ADS Development systems include the Sharp LQ64D343 5V TFT VGA display, which draws about one watt, and the Xentek LS520 backlight inverter, which draws about six watts at full intensity.

Note: The following measurements are based on preliminary measurements from pre-production systems and are not official product specifications. [TBD]

Test Condition	**VBATT_POS**							
	6.5 V		**9 V**		**12 V**		**15 V**	
Sleep mode	4.3	28	3.3	30	2.7	32	2.4	36
CPU idle (note 19)	140	900	105	900	85	1000	70	1100
CPU at max (note 20)				[TBD]				
Units	mA	mW	mA	mW	mA	mW	mA	mW

Notes: Power consumption was measured under the following conditions:

19. Fully populated 64 MiB BitsyX with no peripheral connections. System running only the Windows CE desktop (predominantly in Idle mode; <5% CPU utilization)
20. Fully populated 64 MiB BitsyX with no peripheral connections. Full (95-100%) processor utilization achieved by running multiple instances of a graphical application

6.2.6 ADSmartIO Controller

The ADSmartIO Controller is a second RISC microcontroller on the BitsyX designed to handle I/O functions autonomously. The BitsyX communicates with the ADSmartIO controller using the PXA255 SPI bus. On the BitsyX, ADSmartIO is implemented with the Atmel AVR 8535 microcontroller, which has 512 bytes EEPROM.

Absolute Maximum Ratings

Input voltage, any pin .... 3.8 V

Symbol	Parameter	Min	Typ.	Max	Units
Vdd	ADSmartIO supply voltage		3.3		V
Rs	Series resistance (note 21)		1		kΩ
Vprot	(note 21)				V
Digital Outputs (4.3.3)					
Vol				0.5	V
Voh		2.3	3.3		V
I sink	(see notes 21, 22)			20	mA
I source	(see notes 21, 22)			12	mA
Digital Inputs (4.3.3)					
Vih		0.6			Vdd
Vil				0.3	Vdd
R	Software-selectable pull-ups to 3.3 V (see note 23)	35		120	kΩ
A/D Inputs (4.3.4)					
n	resolution (note 24)		8	10	bit
Rin			100		MΩ
Vref	A/D reference voltage (note 25)		2.5		V
Ivref	Current drain from ref voltage			100	uA
Vin	valid A/D input voltage range	0		Vref	V
I (Vref)	J10.43			100	µA
Temperature Sensing (4.3.5)					
Rth	external thermistor resistance @ 25C		33		kΩ
Vt	thermistor excitation voltage		Vref		V
Rtl	lower voltage divider		47		kΩ
I2C Bus (4.5.4, note 26)					
	Bus clock		50		kHz
	input buffer size			32	byte
	packet size			32	byte
Vi/o	I/O voltages	see digital I/Os, above			V
Rbus	pull-up on SDA, SCK		4.7		kΩ
Vbus			3.3		V

Notes:

21. Row and column I/Os have series resistance and overvoltage protection to ground. The series resistance limits the dc current that any one pin can source or sink.
22. SMTIO0-3 are directly connected to I/O controller without external protection.
23. Control pull-up resistors by writing to bits of IO port when the port is configured as a digital input (bit mask 1=enable, 0=disable).
24. Digital noise on the board may degrade analog performance under some conditions.
25. Vref turns off when the system is in Sleep mode (section 5.3.2).
26. Specifications based on ADSmartIO release 1010 rev 2 (ADS release #700114-10102)

6.2.7 System Controller

A Xilinx XC3064 CPLD on the BitsyX manages the RqOnOff, CONN_PE1/PE2 (5.3.2) and other system control signals. It is programmed at the factory using the JTAG interface (3.3.5).

Absolute Maximum Ratings

Input voltage, digital I/O pins ....-0.5 to 5.5 V

Output current, continuous,
digital I/O pins ....-100 to 100 mA

Symbol	Parameter	Min	Typ.	Max	Units
Vdd	Supply voltage		3.3		V
Digital Outputs					
Vol		0		0.4	V
Voh		2.4			V
Digital Inputs					
Vil		0		0.8	V
Vih		2.0		3.5	V

6.2.8 USB

The BitsyX supports USB operation as described in section 4.5.2. The USB_PWR_SENSE and USB_PWR_CTRL lines are SA-1111 control lines. See section 6.2.12 for their electrical characteristics.

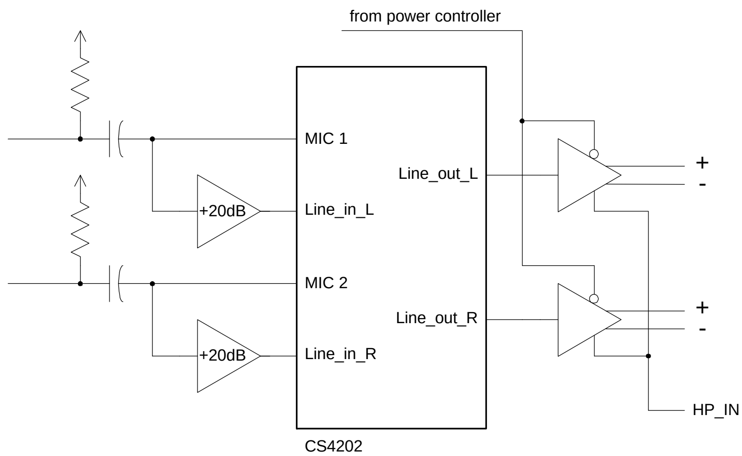
Symbol	Parameter	Min	Typ.	Max	Units
Host Port					
R_pwr_sense	USB_PWR_SENSE Pull-up to Vddx		47		kΩ

6.2.9 Audio

For its audio sub-system the BitsyX uses the Crystal CS4201 or CS4202, AC'97 stereo codecs with dual audio input and output channels. The BitsyX adds an output power amplifier (National LM4863LQ) and a microphone pre-amp with power for electret microphones.

The output amplifier supports differential and single-ended modes. When the HP_IN signal is greater than V(HP_IN), the amplifier is in single-ended mode; when lower, it is in differential mode.

The following diagram illustrates the relationship of the BitsyX signal amplifiers to the codec:



The BitsyX microphone circuitry can be factory configured to support "line in" inputs (1 Vrms with no electret pull-ups) and different input gain and filtering. If a special configuration needed for your project, consult ADS Sales with information about your requirements.

Absolute Maximum Ratings

Vin_mic .... 5 Vdc

Symbol	Parameter	Min	Typ.	Max	Units
DVdd	codec digital supply voltage		3.3		V
Avdd	codec analog supply voltage		5.0		V
fso	sample rate, output		48		kHz
fsi	sample rate, input (note 27)	8		44.1	kHz
Audio Input					
Vin_mic	signal input voltage		100		mV_{rms}
Gain_mic	pre-amp gain		20		dB
fo_mic	pre-amp low-pass cutoff (note 28)		3.4		kHz
Rin_mic	input impedance		12.5		kΩ
Cin_mic	DC blocking capacitor		1		µF
Vmicpwr	microphone power (MIC_L/R+)		5		V
Rmicpwr	microphone power, series resistance			3.2	kΩ
Audio Output					
Rl	speaker load	4	8		Ω
Vout	Zspkr=4Ω, differential mode			3.7	V_{rms}
Vdc	DC bias, differential mode		0.5		Avdd
Pspkr	output power, ea. channel (note 29)				
	differential, THD+N 1%, Rl 4Ω		1.0	2.2	W
	differential, THD+N 10%, Rl 4Ω		1.0	2.7	W
	differential, THD+N 1%, Rl 32Ω		1.0	0.34	W
	single-ended, THD+N 0.5%, Rl 32Ω		75	85	mW
	single-ended, THD+N 1%, Rl 8Ω			340	mW
	single-ended, THD+N 10%, Rl 8Ω			440	mW
R HP_IN	pull-up to Vcc			100	kΩ
V HP_IN	threshold voltage		4		V

Notes:

27. The output sample rate is fixed, but the input sample rate can be set to 8, 11.025, 22.05 or 44.1 kHz.
28. Pre-amp anti-aliasing filter rolls off at 3dB/octave (first-order filter)
29. Typical values are guaranteed to National Semiconductor's AOQL (Average Outgoing Quality Level) Operating above typical values for a sustained period of time may result in thermal shutdown of the amplifier.

6.2.10 PXA255 Processor

The XScale PXA255 core can change system voltage Vddi (6.2.4) dynamically to achieve lower power consumption at high clock rates. It uses voltage Vddx to power its interface I/Os. The EIOn digital I/Os include series resistance and ESD protection.

Serial ports configured for 3.3 V CMOS operation run directly to the processor (section 4.5.1). These lines should be treated as digital I/Os and protected for over-current and over-voltage accordingly.

Absolute Maximum Ratings

Input voltage, digital I/O pins .... 3.6 V

Symbol	Parameter	Min	Typ.	Max	Units
Digital Outputs					
Vol			0		V_{ddx}
Voh			1.0		V_{ddx}
Io		-2		2	mA

Symbol	Parameter	Min	Typ.	Max	Units
Digital Inputs					
Vil				0.2	V_{ddx}
Vih		0.8			V_{ddx}
EIOn Digital I/Os (J3 3.3.3 and J10 3.3.9)					
Reio	EIOn series resistance		1		kΩ
I2C Bus (4.5.4)					
	bus clock (note 30)	100		400	kHz
	buffer size			1	byte
Rbus	pull-up on SDA, SCK		4.7	4.99	kΩ
Vbus			3.3		V

Notes:

30. The PXA255 supports "standard" and "fast" I2C speeds of 100 and 400 kHz.

6.2.11 Crystal Frequencies

Agencies certifying the BitsyX for compliance for radio-frequency emissions typically need to know the frequencies of onboard oscillators. The following table lists the frequencies of all crystals on the BitsyX.

Note that the frequency of the StrongARM crystal X4 is multiplied internally by 4n, where n is a value from 4 to 14, to achieve the processor core frequency. The system bus runs at half the processor's core frequency.

Crystal	Device	Typ.	Units
X1	RTC	32.768	kHz
X2	ADSmartIO microcontroller	3.6864	MHz
X3	StrongARM RTC	32.768	kHz
X4	Strong ARM core	3.6864	MHz
X5	Codec	24.576	MHz

6.2.12 SA-1111 Companion Chip

The SA-1111 is a companion to the XScale PXA255. It provides a number of features that supplement the core processor. These include a USB Host Controller, PCMCIA/CF control logic and buffers, interface to an AC'97 codec, DMA controllers and an interrupt controller, among others.

On the BitsyX, the CompactFlash (CF) port can be used as a digital expansion bus. Signals for PCMCIA, CF and the expansion bus are listed in a separate section, below.

Absolute Maximum Ratings

Input voltage, digital I/O pins .... 3.8 V

Input voltage, CF port I/O pins.................................. 5.5 V

Symbol	Parameter	Min	Typ.	Max	Units
V_{ddx}	SA-1111 I/O voltage		3.3		V
V_{ccb}	CARDBVcc: CF port voltage (note 31)	3.3	5.0	5.0	V
Digital Outputs					
Vol			0		V_{ddx}
Voh			1.0		V_{ddx}
Digital Inputs					
Vil	Vddx=3.3 V			0.2	V_{ddx}
Vih	Vddx=3.3 V	0.8			V_{ddx}
SPI Bus (section 4.5.3)					
	Bit rate		460	1840	kHz

Notes:

31. The CF port voltage is selected programmatically with the SA-1111. The socket is keyed for 5V-tolerant CF cards.

PCMCIA, CompactFlash Port and Expansion Bus

The CompactFlash bus can be used as a digital expansion port on the BitsyX. The following are specifications for the CF port used as an expansion bus.

Symbol	Parameter	Min	Typ.	Max	Units
I 3.3V	3.3 V socket current			2	W
I 5V	5 V socket current			2	W
Rp pcmcia	Card detect (1 & 2) and voltage sense (VS1 & 2) pull-ups (note 32)		100		kΩ
Vp pcmcia	Card detect and voltage sense pull-up voltage (note 33)	Vddx	Vcc	Vcc	V
Digital Outputs					
Vol			0		V_{ccb}
Voh			1.0		V_{ccb}
I sink					mA
I source				4	mA
Digital Inputs					
Vil	V_{ccb}=3.3 V			0.325	V_{ccb}
	V_{ccb}=5.0 V			0.8	V
Vih	V_{ccb}=3.3 V	0.475			V_{ccb}
	V_{ccb}=5.0 V	2.4			V

Symbol	Parameter	Min	Typ.	Max	Units
Timing (note 34)					
t mem	system memory clock		9.7		us
t setup1	address setup to command, first access	2		97	t mem
t setup2	address setup to command, second access	1		64	t mem
t access	nRD/WR duration, first access	3		97	t mem

Notes:

32. Each card inserted in a PCMCIA or CF slot can drain up to 10 mW when the system is in Sleep mode (4 * (Vcc^2/Rpcmcia)).
33. The PCMCIA/CF voltage is software-selectable. External implementations of the CF bus (i.e. on a Personality Board) can hard-wire the voltage to Vddx or to Vcc.
34. The PXA255 MECR register independently sets timings for the attribute, IO and memory spaces of the CF bus in 32 steps. Values shown assume 206 MHz CPU clock. Min values are with Fast bit=1, max values are with Fast bit=0.

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7 Board Revision History

7.1 Identifying the board revision

The product revision number of the BitsyX is etched on the underside of the printed circuit board. That number is 170115-0000x, where "x" is the board revision.

7.2 Revision History

7.2.1 Revision 1

Initial release. If you are using a BitsyX as a replacement for the Bitsy Plus, please note these differences from revision 2 of the Bitsy Plus:

New Features

XScale PXA255 processor replaces StrongARM SA-1110

Dynamically scalable core voltage power supply

J7 connector for PXA255 I/Os

Factory option to wake system with keypad activity (section 5.3.3)

I2C bus from XScale processor

Enhancements

Improved audio amplifier SNR

Changes

Signals on J3 change as follows:

Pin	From	To
33	*n/c*	*LEDOUT0*

Different XScale signals used for internal system control functions (section 4.1.6)

7.2.2 Revision 2

Revision 2 incorporates many of the changes made in the Bitsy Plus design between revisions 2 and A. Differences between BitsyX revision 2 and Bitsy Plus revision A are listed first, followed by a detailed list of the changes that occurred since BitsyX revision 1

Differences from Bitsy Plus revision A

New Features

PXA255 XScale processor replaces StrongARM SA-1110

Adds connector J7

LED controlled by system controller, not by CPU

Other Key Differences

EIOn I/Os driven by CPU, not CPLD

AC97 Codec is driven by XScale, not SA-1111

Height profile is slightly different

Polarity of 3.3V PCMCIA power enable signal is active low (same as 5V enable)

Changes from BitsyX revision 1

New Features

Production option to bypass audio amplifier

Can turn off ADSmartIO analog voltage reference (Vref) as part of subsystem partitioning

ADSmartIO now can monitor the DC_GOOD signal (VBATT_NEG is a production option).

Enhancements

Expanded backlight PWM voltage range from 3.3 V to 5 V (option for 3.3 V)

Codec reset control (PXA255 GP11)

Reduced sleep mode current

Improved touch panel operation (lower noise)

Improved audio codec operation through additional power and ground partitioning

[tbd] R_{tl} (thermistor base resistor) changed from 3.3kΩ to 47kΩ to improve temperature resolution (-40 to +85C).

Reduced sleep current

Adds support for CS4202 audio codec

Improved Vddx performance with 5V-only systems

Changes

Internal USB control signals have changed. Requires different operating system drivers from revision 1.

J7 change from 24 to 16 pins; pinout is different

Signals on J3 change as follows:

Pin	From	To
33	*LEDOUT0*	*USB_Reconn*

EIOn I/Os driven by CPU, not CPLD

AC97 Codec is driven by XScale, not SA-1111

Height profile is slightly different

Flash reset now controlled by system reset. Resolves condition under which system will sometimes not reboot from hard reset.

PCMCIA power control updated to allow full cut-off of power

PCMCIA 3.3V power control enable signal has inverse polarity

RqOnOff signal management now handled by CPLD and not AVR.

EXT_IRQ1 goes to CPU, not to SA-1111 (4.1.4)

System can wake up after a touch screen event

Polarity of audio amplifier power enable is inverted; allows full-shutdown of amplifier

ADSmartIO voltage reference turns off when system is asleep

LED is driven by CPLD, not CPU GP 20

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