USER MANUAL

Accessory 24P

Axis Expansion Board (New Version)

3Ax-602192-xUx2

October 15, 2003

Single Source Machine Control *Power // Flexibility // Ease of Use*
21314 Lassen Street Chatsworth, CA 91311 // Tel. (818) 998-2095 Fax. (818) 998-7807 // www.deltatau.com

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To report errors or inconsistencies, call or email:

Delta Tau Data Systems, Inc. Technical Support
Phone: (818) 717-5656
Fax: (818) 998-7807
Email: support@deltatau.com
Website: http://www.deltatau.com

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INTRODUCTION

Overview

The ACC-24P Axis Expansion Board provides four or eight channels of PMAC(1)-style servo interface circuitry for PMAC and Turbo PMAC controllers. One ACC-24P board can be connected to a single (non-Turbo) PMAC board, providing up to eight additional channels of servo interface circuitry. Up to four ACC-24P boards can be connected to one Turbo PMAC board, providing up to 32 additional channels of servo interface circuitry.

The ACC-24P is a 2/3-sized PC expansion card. It has an ISA bus connector, so it can be mounted in an ISA expansion slot. The ACC-24P does not communicate over the bus; the bus connector is just a convenience for mounting the board near the Turbo PMAC.

The ACC-24P board contains no processor; it has 1 or 2 highly integrated 4-channel PMAC(1)-style "Servo ICs" with the buffering circuitry and connectors around them.

Compatibility

The ACC-24P can be used with any regular (non-Turbo) PMAC(1) or PMAC2 board, interfacing through the expansion port. (It is electrically and software compatible with the PMAC(1)-VME and PMAC2-VME, but of course special mounting would be required.) PMAC(1) controllers have full software support for use of the ACC-24P. PMAC2 controllers do not have I-variables for the automatic setup of ACC-24P registers, and they cannot use the flags on ACC-24P as automatic servo flag inputs and outputs.

The ACC-24P board can be used with any Turbo PMAC(1) or Turbo PMAC2 board, interfacing through the Expansion port. (It is electrically and software compatible with Turbo PMAC(1)-VME and Turbo PMAC2-VME, but of course special mounting would be required.) Note that even if the Turbo PMAC itself is a PMAC2 with the PMAC2-style Servo ICs and interface circuitry, the ACC-24P with its PMAC(1)-style Servo ICs and interface circuitry can be connected to it, with full software support for using its features.

Board Configuration

Base Version

The base version of the ACC-24P provides a 2/3-slot board with:

- 4 channels axis-interface circuitry, each including:
  - 16-bit +/-10V analog output
  - 3-channel differential/single-ended encoder input
  - 4 optically isolated input flags, 2 optically isolated output flags
  - Interface to external 16-bit serial ADC
- 60-pin IDC servo connector
- Expansion port connector to PMAC/Turbo PMAC CPU
- Auxiliary port connector for PMAC hardware clock signals
- On-board hardware clock generation circuitry

Option 1

ACC-24P can be expanded past the standard four channels of axis-interface circuitry by factory configuration, with the order of Option 1.

- Option 1 provides an additional 4 channels of axis interface circuitry with a 60-pin connector, identical to the first four channels. The key components are a "DSPGATE" Servo IC in U38 and a connector in J7.

Hardware Updates

Significant upgrades were made to the ACC-24P board in the 602192-103 version. This new version replaces earlier versions of the ACC-24P board, bringing important improvements, which include:

- **Surface-Mount Technology**: Most components are surface mounted for higher reliability and greater long-term part availability.
- **Raised Bottom Edge**: The bottom edge of the board has been raised so that it can clear high-profile parts on the PC mother board – up to 25 mm (1 inch) high
- **On-Board Clock Generation Circuitry**: This eliminates the need to bring a 2-strand cable from the PMAC-PC or PMAC-Lite J6 to ACC-24P J5 or J6 to provide the hardware clock signals for the encoder inputs and DAC outputs.
- **Daisychain Capability for Turbo PMAC**: Up to four of the new ACC-24P boards may be connected to a single Turbo PMAC CPU on a daisychain expansion port connector using the new S1 addressing DIP-switch bank.
- **Individual Amplifier Enable Polarity Control**: New jumpers E17A-E17H permit individual high-true/low-true control of the 8 amplifier enable signals. Existing jumper E17 can invert the polarity of all amplifier enable signals.
- **24V Amplifier Enable Capability**: New Jumper E100 permits use of up to 24V supply for the amplifier, compared to a maximum of 15V on the older version.
- **Sinking or Sourcing Input Flags**: The new ACC-24P permits the use of either sinking or sourcing input flags (home, limits, fault); the old ACC-24P permitted only sinking input flags.
- **Voltage Interlock Circuit**: The new ACC-24P has an interlock circuit that shuts down the analog outputs if it detects anything wrong with the power supply, preventing runaway on partial supply loss.
- **Buffered, Isolated Compare Outputs**: The new J9 10-pin header provides optically isolated outputs for the position compare function for each encoder with outputs rated to 24V and 100mA.

Compatibility Issues:

The new ACC-24P can be operated in a manner that is 100% compatible with the old ACC-24P. The board is shipped from the factory with settings for 100% compatible operation. To ensure your operation is compatible, double-check the following settings:

- **Clock Generation Circuitry**: If you desire to bring the hardware clock signals from the PMAC J6 connector as before, there must be a jumper on E38A, a jumper on E98C, and no jumpers on E34A, E34, E35, E36, E37, E38, E98A, or E98B. If you desire to use the on-board clock signals which provide 100% operational compatibility, there must be a jumper on only one of the set {E34A, E34, E35, E36, E37, E38} which select the frequency exactly as they do on PMAC. There must be a jumper on only one of the set {E98A, E98B}, where E98A selects the same frequency as PMAC E98 pins 1 and 2, and E98B selects the same frequency as PMAC E98 pins 2 and 3; there must be no jumper on E38A or E98C.

- **Daisychain Capability**: To use the ACC-24P with a "non-Turbo" PMAC-PC or PMAC-Lite, DIP-switches S1-1, S1-2, S1-3 and S1-4 must be in the OFF position.
- **Amplifier Enable Polarity**: For jumper E17 to control the high-true/low-true polarity of all of the amplifier enable outputs as before, all jumpers E17A – E17H must be OFF.
- **24V Amplifier Enable Capability**: In order for the amplifier enable outputs to use the +12V to +15V analog supply voltage for a high-side clamping supply, jumper E100 must connect pins 1 and 2.
- **Sinking/Sourcing Input Flags**: To use sinking input flags, simply connect the flags as you have done before.

Documentation Note:

Because multiples of the new ACC-24P can be used with a single Turbo PMAC, the channel numbers for the ACC-24P on the new documentation are referred to as Channels 1 – 8, instead of 9 – 16 in the documentation for the old version. An individual channel in the system is referred to by both board number and channel number. When a single ACC-24P is used with a regular (non-Turbo) PMAC, its Channels 1 – 8 map into PMAC channels 9 – 16, respectively.

HARDWARE SETUP

Output Flag Driver ICs

The output flags on the ACC-24P – both the amplifier-enable (AENA) signals and the position compare (EQU) signals – are driven by socketed ICs. Either sinking driver ICs or sourcing driver ICs may be installed in these sockets. Component U11 contains the driver for the first four channels; if Option 1 is ordered, component U12 contains the driver for the second four channels.

ULN2803A or equivalent sinking driver ICs are installed at the factory. These can be changed in the field to UDN2981A or equivalent sourcing driver ICs. If the ICs are changed, it is essential to change the configuration jumpers: E101 and E102 for U11; E103 and E104 for U12 (see *Output Flag Configuration Jumpers*, below).

Switch Configuration

Address DIP Switch S1

S1 is a 4-point DIP switch that determines whether the ACC-24P is to be connected to a "regular" (non-Turbo) PMAC, or a Turbo PMAC. Switches S1-1, S1-2, S1-3 and S1-4 must be OFF on an ACC-24P to enable addressing of the board by an non-Turbo PMAC. This setting is equivalent to operation of the older versions of the ACC-24P board without S1.

Switches S1-3 and S1-4 must be ON on an ACC-24P to enable addressing of multiple boards by a Turbo PMAC. If they are OFF (or an older version of the board is used with a Turbo PMAC), the board will respond to any of the four possible addresses, so no more than one board may be connected to a Turbo PMAC.

Additionally, S1 sets up the address of the ACC-24P in Turbo PMAC's memory and I/O map. The setting of these DIP switches must match the addresses used by Turbo PMAC; and no two ACC-24P boards connected to the same Turbo PMAC may have the same DIP switch settings, or there will be an addressing conflict.

The settings of switches S1-1 and S1-2 define the address of the board in Turbo PMAC's address space. This in turn defines the "number" of the Servo IC(s) on the board, and the I-variable numbers in the Turbo PMAC that configure the IC(s). The following table lists the possible settings:

S1-1	S1-2	Board No.	1ST IC NO.	2ND IC NO.	1st Ic I-Var. Range	2nd Ic I-Var. Range	1st Ic Base Address	2nd Ic Base Address
ON	ON	1ST	2	3	I7200-I7299	I7300-I7399	$078200	$078300
OFF	ON	2ND	4	5	I7400-I7499	I7500-I7599	$079200	$079300
ON	OFF	3RD	6	7	I7600-I7699	I7700-I7799	$07A200	$07A300
OFF	OFF	4TH	8	9	I7800-I7899	I7900-I7999	$07B200	$07B300

It is suggested, but not required, that the boards be assigned in order. That is, if there are two ACC-24P boards in the system, the one closest to the Turbo PMAC be set up as the "1st" board, and the next one be set up as the "2nd" board.

Jumper Configuration

DAC/ADC Clock Signal Source

Jumper E98C must be ON in order to accept the DCLK clock signal for the D/A converters and A/D converters for the ACC-24P from the PMAC through J5 pin 9. (On older versions of the ACC-24P, this was the only way to provide the DCLK signal.) The signal comes from the comparable pin on PMAC's JXIO connector.

If Jumper E98C is OFF, the DCLK signal must come from the ACC-24P's own clock generation circuitry. This configuration is strongly recommended to simplify system wiring and to provide more noise immunity. It is completely operationally compatible with the older external clock-source configuration. This internal clock-source configuration is required if there is more than one ACC-24P connected to a single Turbo PMAC.

If the internal clock-source configuration is chosen, the signal must come through either jumper E98A or E98B. If E98A is ON (default), the 2.45 MHz frequency is selected. If E98B is ON, the 1.22 MHz frequency is selected. This lower frequency improves the operation of ACC-28 A/D converter boards connected to the ACC-24P. The DCLK frequency on the ACC-24P should be the same as that on the PMAC itself, which is selected by PMAC's E98 jumper.

Only one of the jumpers E98A, E98B, and E98C should be ON at one time.

Encoder Clock Signal Source

Jumper E38A must be ON in order to accept the SCLK clock signal for the encoder circuits on the ACC-24P from the PMAC through J5 pin 10. (On older versions of the ACC-24P, this was the only way to provide the SCLK signal.) The signal comes from the comparable pin on PMAC's JXIO connector.

If Jumper E38A is OFF, the SCLK signal must come from the ACC-24P's own clock generation circuitry. This configuration is strongly recommended to simplify system wiring and to provide more noise immunity. It is completely operationally compatible with the older external clock-source configuration. This internal clock-source configuration is required if there is more than one ACC-24P connected to a single Turbo PMAC.

If the internal clock-source configuration is chosen, the signal must come through one of the jumpers E34(A) through E38. If E34 is ON (default), the 9.83 MHz frequency is selected. The SCLK frequency on the ACC-24P does not have to be the same as that on the PMAC itself, which is selected by PMAC's E34A to E38(A) jumper bank. The following table lists the frequency selected by each jumper:

E34A	19.66 MHz	**E36**	2.45 MHz
E34	9.83 MHz	**E37**	1.22 MHz
E35	4.92 MHz	**E38**	(External)

Only one of the jumpers E34A through E38A should be ON at one time.

Encoder Input Signal Configuration

Jumpers E27 through E24 control the open-circuit voltage of the complementary input lines A/, B/, and C/ for Encoders 1 through 4, respectively. If Option 1 is ordered, jumpers E21 through E18 do the same for Encoders 5 through 8.

These are 3-point jumpers. If pins 1 and 2 are connected (default), the complementary lines are held at 2.5V if not driven by an input. If pins 2 and 3 are connected, these lines are pulled to 5V if not driven. The main signal lines are always pulled up to 5V if not driven.

For single-ended encoders, these jumpers must connect pins 1 and 2. For differential line-driver encoders, the setting does not matter; most users leave the jumpers in the default setting of 1-2. The only reasons to change the setting is to connect to complementary open-collector drivers (now nearly obsolete), or if external exclusive-or if circuitry is used to detect loss of encoder.

Analog Circuit Isolation

The analog circuitry on the ACC-24P can be isolated from the digital circuitry, or both circuits can be tied to a common reference voltage. It is strongly recommended in actual industrial application that isolation be maintained between the two circuits. To do this, jumpers E85, E87, and E88 must be OFF, and separate power supplies must be used for the two circuits.

To tie both circuits to a common reference, jumpers E85, E87, and E88 should be ON. A common power supply may be used for both circuits in this configuration.

Input Flag Supply

There are several possibilities for supplying the power to the input flag (HMFL, -LIM, +LIM, FAULT) circuits. Most commonly, the same +15V supply that is used for the analog output circuitry is used for the input flags. In this configuration, jumper E89 should be ON, and jumper E90 should connect pins 1 and 2. This is the default configuration, and it supports sinking drivers only.

A separate supply can be brought in on Pin 9 of J9, or, if Option 1 is ordered, on Pin 59 of J7. For sinking drivers, this can be a +12V to +24V supply; for sourcing drivers, this is the 0V return of the supply. In this configuration, jumper E89 should be OFF, and jumper E90 should connect pins 1 and 2.

It is also possible to use the +12V digital supply from the P1 ISA bus connector or the TB1 terminal block. This configuration defeats the optical isolation of the flag receivers and is not recommended for industrial systems. It may be useful for desktop demonstration systems. In this configuration, jumper E90 should connect pins 2 and 3.

Output Flag Supply

There are two possibilities for supplying power to the output flag (AENA, EQU) circuits. Most commonly, the same +15V supply that is sued for the analog output circuitry is used for the output flags. In this configuration, jumper E100 should connect pins 1 and 2. This is the default configuration.

A separate supply can be brought in on Pin 9 of J9, or, if Option 1 is ordered, on Pin 59 of J7. This can be a +12V to +24V supply. In this configuration, jumper E100 should connect pins 2 and 3.

Output Flag Signal Configuration

The output flags (AENA and EQU) on the ACC-24P can use either sinking or sourcing drivers. Component U11 drives the flags for the first four channels; if Option 1 is ordered, U12 drives the flags for the last four channels. ULN2803A or equivalent sinking driver ICs are installed at the factory in the sockets for these components; these may be replaced with UDN2981A or equivalent sourcing drivers.

CAUTION

Incorrect settings of these jumpers can permanently damage the driver ICs.

If a sinking driver IC is installed in U11, jumper E101 should connect pins 1 and 2; jumper E102 should connect pins 1 and 2. If a sourcing driver IC is installed in U11, jumper E101 should connect pins 2 and 3; jumper E102 should connect pins 2 and 3.

If a sinking driver IC is installed in U12, jumper E103 should connect pins 1 and 2; jumper E104 should connect pins 1 and 2. If a sourcing driver IC is installed in U12, jumper E103 should connect pins 2 and 3; jumper E104 should connect pins 2 and 3.

Resistor Pack Configuration

Termination Resistors

The ACC-24P provides sockets for termination resistors on differential input pairs coming into the board. As shipped, there are no resistor packs in these sockets. If these signals are brought long distances into the ACC-24P board and ringing at signal transitions is a problem, SIP resistor packs may be mounted in these sockets to reduce or eliminate the ringing.

All termination resistor packs are the type that has independent resistors (no common connection) with each resistor using 2 adjacent pins. The following table shows which packs are used to terminate each input device:

Input	Pack	Pack Size
Encoder 1	RP14	6-pin
Encoder 2	RP15	6-pin
Encoder 3	RP16	6-pin
Encoder 4	RP17	6-pin
Encoder 5	RP33	6-pin
Encoder 6	RP34	6-pin
Encoder 7	RP35	6-pin
Encoder 8	RP36	6-pin

Connections

Mounting

The ACC-24P can be mounted in one of two ways: in the ISA bus, or using the standoffs.

- ISA bus: To mount in the ISA bus, simply insert the P1-ISA card-edge connector into the ISA socket. If there is a standard PC-style housing, a bracket at the end of the ACC-24P board can be used to screw into the housing to hold the board down firmly.
- Standoffs: At each of the 4 corners of the ACC-24P board, there are mounting holes that can be used to mount the board on standoffs.

Note:

The ACC-24P board does not do any communications through the bus connector; the connector is simply used for mounting, and probably for power supply. Even in standalone applications, passive backplane boards can be very useful for mounting and power supply.

Power Supply Connection

The ACC-24P requires 5V power for its digital circuits: 1A in a 4-channel configuration, 2A in an 8-channel configuration (with Option 1). It also requires a +/-12V to +/-15V supply for the analog output circuits, 150 mA each in a 4-channel configuration, 300 mA each in an 8-channel configuration. The positive analog supply can also power the flags; alternately, a separate +12V to +24V supply may be used.

The digital 5V (regulated, +/-5%) power can be provided through one of three paths:

- Bus connector: If the ACC-24P is mounted in an electrically active ISA bus slot, it automatically draws its 5V power from the bus.

- Terminal block: The TB1 terminal block can be used to bring in 5V power, especially in standalone applications. Point 1 is GND; Point 2 is +5V.
- JMACH connectors: Up to 2A may be brought in through each 60-pin JMACH connector from an ACC-8 board or its equivalent, provided the cable is 500 mm (20 in) or less in length.

The analog +/-12V to +/-15V supply can be provided through one of three paths:

- Bus connector: If the ACC-24P is mounted in an electrically active ISA bus slot, it can draw +/-12V power from the bus if jumpers E85, E87, and E88 are all ON. This configuration defeats the optical isolation on the ACC-24P.
- Terminal block: The TB1 terminal block can be used to bring in +/-12V power, especially in standalone applications if jumpers E85, E87, and E88 are all ON. This configuration defeats the optical isolation on the ACC-24P. Point 1 is GND; Point 3 is +12V; Point 4 is -12V.
- JMACH connectors: +/-15V supplies may be brought in on pins 58, 59, and 60 of the 60-pin J8 (JMACH1) connector from an ACC-8 board or its equivalent. If this is from a supply isolated from the 5V digital supply, optical isolation can be maintained by making sure jumpers E85, E87, and E88 are all OFF.

The flag +12V to +24V supply can be provided through one of several paths:

- JMACH1 connector: The +12V to +15V provided on pin 59 of the J8 (JMACH1) connector is also the input flag supply if jumper E89 is ON and E90 connects pins 1 and 2. It is the output flag supply if E100 connects pins 1 and 2.
- JMACH2/JEQU connector: A +12V to +24V supply brought in on pin 59 of the J7 (JMACH2) connector, or on pin 9 of the J9 (JEQU) connector, can be used as the input flag supply for sinking flag drivers if E89 is OFF and E90 connects pins 1 and 2. The 0V return line of the supply can be connected to this pin through the same jumpers for sourcing flag drivers. The +12V to +24V supply can be used as the output flag supply if E100 connects pins 2 and 3.
- TB1/ISA connector: The +12V provided on point 3 of TB1 or through the P1 ISA-bus connector can be used as the input flag supply if E90 connects pins 2 and 3. This defeats isolation of the input flags, and generally should only be used for demonstration systems. This +12V can also be used to supply the output flag drivers if E100 connects pins 2 and 3. E87 must also be ON, defeating the isolation between the digital and analog circuits.

Expansion Port Connection to PMAC

The ACC-24P connects to the PMAC through the 50-pin J1 header on the ACC-24P. A short flat cable connects this to the JEXP header on the PMAC. If multiple ACC-24 boards are connected to a single PMAC board, they must be connected on a single daisy-chain cable. Total length of this cable should not exceed 300mm (12 in).

Clock Port Connection to PMAC

The J6 (JXIO) connector is a 10-pin IDC header on the ACC-24P. It can be used to bring in the SCLK encoder clock signal and the DCLK DAC/ADC clock signal from the PMAC's matching J6 JXIO connector. A short cable with two 10-pin connectors and 4 strands is provided with the ACC-24P. This port can also be used to send one or two position-compare signals, as selected by E54 – E65, back to PMAC's interrupt controller to interrupt the host computer.

It is strongly recommended that the ACC-24P's internal clock generation circuitry be used. If this circuitry is used (as set by jumpers E34A – E38A and E98A – E98C) and there is no need to send back position-compare interrupt signals, this connector does not need to be used. If the

connector is used for the position-compare interrupts, the ACC-24P's internal clock generation circuitry can still be used as set by the jumpers.

Machine Port Connections

ACC-24P has one (standard) or two (with Option 1) 60-pin IDC headers for each set of four servo interface channels. Through this connector, all of the digital signals pass to and from the amplifier, encoder, and flags for the channels. Typically, this header is connected with a matching Delta Tau ACC-8 family PMAC(1)-style 4-channel breakout board or equivalent through a provided 60-pin flat cable.

The machine port connectors are:

- J8 (JMACH1) Board Channels 1 – 4
- J7 (JMACH2) Board Channels 5 – 8

ACC-28 / Alternate Port Connections

ACC-24P has one (standard) or two (with Option 1) 16-pin headers that provide connection for A/D-converter signals, as well as alternate pinout for several signals associated with each quartet of servo interface channels.

The main use of the alternate port connector is to provide an interface to an ACC-28A or ACC-28B A/D converter board. The ACC-28 boards can be connected directly to this connector on the ACC-24P through a 16-pin flat cable provided with the ACC-28.

The A/D port connectors are:

- JS1 Board Channels 1 – 4
- JS2 Board Channels 5 – 8

PMAC SOFTWARE SETUP

Use of the ACC-24P requires the proper setup of several I-variables on the regular (non-Turbo) PMAC. These settings are discussed in this section. See the PMAC Software Reference for more detailed descriptions of the variables.

Note:

This manual refers to the 8 servo interface channels on the ACC-24P as Channels 1 – 8. When connected to a PMAC, these channels map into PMAC as PMAC channels 9 – 16, respectively.

Channel Setup I-Variables

Each channel on the ACC-24P has four setup I-variables. The following table lists the I-variable numbers for each channel:

ACC-24P Channel #	1	2	3	4	5	6	7	8
PMAC Channel #	9	10	11	12	13	14	15	16
Encoder Decode I-Var	I940	I945	I950	I955	I960	I965	I970	I975
Filter Disable I-Var	I941	I946	I951	I956	I961	I966	I971	I976
Capture Control I-Var	I942	I947	I952	I957	I962	I967	I972	I977
Flag Select I-Var	I943	I948	I953	I958	I963	I968	I973	I978

The setup variables work exactly the same on an ACC-24P as they do on the PMAC(1) itself. The variables are:

- **Encoder I-Variable 0:** **Encoder Decode Control**: This variable is typically set to 3 or 7 for "x4" quadrature decode, depending on which way is "up".
- **Encoder I-Variable 1:** **Encoder Filter Disable**: This variable is typically set to 0 for digital encoder inputs to keep the filter active, or to 1 when the channel is used with an analog encoder interpolator such as the ACC-8D Opt 8, to disable the filter and synchronize the quadrature and fractional count data.
- **Encoder I-Variable 2:** **Capture Control**: This variable determines whether the encoder index channel, an input flag, or both, are used for the capture of the encoder position.
- **Encoder I-Variable 3:** **Capture Flag Select**: This variable determines which input flag is used for encoder capture, if one is used.

Encoder Conversion Table Entries

To use feedback or master position data from an ACC-24P, entries must be added to the encoder conversion table (ECT) to address and process this data. The default conversion table in the PMAC does not contain these entries.

The position data obtained through an ACC-24P board is usually an incremental encoder feedback, and occasionally an A/D converter feedback from an ACC-28A/B board connected through the ACC-24P.

The ECT entries for ACC-24P incremental encoder channels are shown in the following table:

ACC-24P Channel #	**PMAC Channel #**	**ECT Entry**	**ACC-24P Channel #**	**PMAC Channel #**	**ECT Entry**
1	9	$m0C020	5	13	$m0C030
2	10	$m0C024	6	14	$m0C034
3	11	$m0C028	7	15	$m0C038
4	12	$m0C02C	8	16	$m0C03C

The first hexadecimal digit in the entry, represented by 'm' in the table, is a '0' for the most common 1/T timer-based extension of digital incremental encoders; it is an '8' for the parallel-data extension of analog incremental encoders; it is a 'C' for no extension of an incremental encoder.

The ECT entries for ACC-28B A/D converters read through an ACC-24P are shown in the following table:

ACC-24P Channel #	PMAC Channel #	ECT Entry	ACC-24P Channel #	PMAC Channel #	ECT Entry
1	9	$mnC026	5	13	$mnC036
2	10	$mnC027	6	14	$mnC037
3	11	$mnC02E	7	15	$mnC03E
4	12	$mnC02F	8	16	$mnC03F

The first hexadecimal digit of the entry, represented by 'm' in the above table, is a '1' if the ADC data is processed directly, without integration; it is a '5' if the data is integrated in the conversion. If the entry integrates the data, there is a second line in the entry (another I-variable) that specifies the bias of the A/D converter.

The second hexadecimal digit of the entry, represented by 'n' in the above table, is a '0' if the ACC-28A with signed data is used; it is an '8' if the ACC-28B with unsigned data is used.

Motor Addressing I-Variables

For a PMAC motor to use the servo interface circuitry of the ACC-24P, several of the addressing I-variables for the motor must contain the addresses of registers in the ACC-24P, or the addresses of encoder conversion table registers containing data processed from the ACC-24P. These I-variables can include:

- **Ix02:** **Motor x Command Output Address**: Ix02 tells PMAC where to write its command outputs for Motor x. If ACC-24P is to create the command signals, Ix02 must contain the address of the register. The following table shows the address of the DAC output register for each channel of each ACC-24P. These addresses can be used for single analog outputs or double analog outputs.

ACC-24P Channel #	PMAC Channel #	Ix02 Value	ACC-24P Channel #	PMAC Channel #	Ix02 Value
1	9	$C023	5	13	$C033
2	10	$C022	6	14	$C032
3	11	$C02B	7	15	$C03B
4	12	$C02A	8	16	$C03A

When using a pair of DACs for sine-wave outputs, Ix02 contains the address of the higher-numbered DAC of the pair (the lower address).

- **Ix03:** **Motor x Position-Loop Feedback Address**
- **Ix04:** **Motor x Velocity-Loop Feedback Address**
- **Ix05:** **Motor x Master Position Address**

  Usually the Ix03, Ix04, and Ix05 variables contain the address of a processed position value in the encoder conversion table, even when the raw data comes from the ACC-24P.

- **Ix10:** **Motor x Power-On Position Address:** Ix10 tells the Turbo PMAC where to read absolute power-on position, if any. Typically, the only times Ix10 will contain the

address of an ACC-24P register is if the position is obtained from an A/D converter on an ACC-28A/B connected through the ACC-24P.

The following table shows the possible values of Ix10 for ACC-28 A/D converters:

ACC-24P Channel #	PMAC Channel #	Ix10 Value	ACC-24P Channel #	PMAC Channel #	Ix10 Value
1	9	$m1C023	5	13	$m1C033
2	10	$m1C022	6	14	$m1C032
3	11	$m1C02B	7	15	$m1C03B
4	12	$m1C02A	8	16	$m1C03A

The first hexadecimal digit of the variable, represented by 'm' in the above table, is a '3' if the ACC-28B, which provides unsigned data, is used; it is a 'B' if ACC-28A, which provides signed data, is used.

- **Ix25: Motor x Flag Address:** Ix25 tells PMAC where to access its flag data for Motor x. If ACC-24P is interface to the flags, Ix25 must contain the address of the flag register in ACC-24P. The following table shows the address of the flag register for each channel of each ACC-24P:

ACC-24P Channel #	PMAC Channel #	Ix25 Value	ACC-24P Channel #	PMAC Channel #	Ix25 Value
1	9	$mnC020	5	13	$mnC030
2	10	$mnC024	6	14	$mnC034
3	11	$mnC028	7	15	$mnC038
4	12	$mnC02C	8	16	$mnC03C

The first two digits of Ix25 represented by 'm' and 'n' in the above table, control how the flags at the specified address are used. Refer to the PMAC Software Reference for details.

- **Ix81: Motor x Power-On Phase Position Address:** Ix81 tells PMAC where to read absolute power-on position for motor phase commutation if any. Typically, it will contain the address of an ACC-24P register for only two types of absolute phasing sensors. The hall-effect commutation sensors (or their optical equivalents) connected to the U, V, and W input flags on an ACC-24P channel, or the encoder counter filled by simulated quadrature from a Yaskawa absolute encoder connected to the ACC-24P through an ACC-8D Option 9 board.

  The following table contains the possible settings of Ix81 for hall sensor absolute position with an ACC-24P:

ACC-24P Channel #	PMAC Channel #	Ix81 Value	ACC-24P Channel #	PMAC Channel #	Ix81 Value
2	10	$mnC024	6	14	$mnC034
4	12	$mnC02C	8	16	$mnC03C

  The following table contains the possible settings of Ixx81 to read the encoder counters for Yaskawa absolute encoders:

ACC-24P Channel #	PMAC Channel #	Ix81 Value	ACC-24P Channel #	PMAC Channel #	Ix81 Value
1	9	$58C021	5	13	$58C031
2	10	$58C025	6	14	$58C035
3	11	$58C029	7	15	$58C039
4	12	$58C02D	8	16	$58C03D

- **Ix83: Motor xx Phase Position Address:** Ix83 tells Turbo PMAC where to get its commutation position feedback every phase update cycle. Usually, this contains the address of an encoder "phase position" register.

  The following table shows the possible values of Ix83 for ACC-24P encoder phase position registers:

ACC-24P Channel #	PMAC Channel #	Ix83 Value	ACC-24P Channel #	PMAC Channel #	Ix83 Value
1	9	$C021	5	13	$C031
2	10	$C025	6	14	$C035
3	11	$C029	7	15	$C039
4	12	$C02D	8	16	$C03D

TURBO PMAC SOFTWARE SETUP

Use of the ACC-24P requires the proper setup of several I-variables on the Turbo PMAC. These settings are discussed in this section. See the PMAC Software Reference for more detailed descriptions of the variables.

System Configuration I-Variables

Turbo PMAC variable I65 tells the controller which external devices containing Servo ICs, such as the ACC-24P, are present in the system. I65 is a 4-bit value, with each bit representing 1 of the 4 possible devices that can be connected to a Turbo PMAC. The bit must be set to 1 to the Turbo PMAC software that the device is present.

- Bit 0, with a value of 1, specifies whether the 1st device is present
- Bit 1, with a value of 2, specifies whether the 2nd device is present
- Bit 2, with a value of 4, specifies whether the 3rd device is present
- Bit 3, with a value of 8, specifies whether the 4th device is present

An ACC-24P can be either the 1st, 2nd, 3rd, or 4th device, depending on the setting of DIP switches S1-1 and S1-2.

Normally these external devices are added in order, so I65 takes one of 4 values:

- 1st external device alone: I65=1
- 1st and 2nd external devices: I65=3
- 1st, 2nd, and 3rd external devices: I65=7
- 1st, 2nd, 3rd, and 4th external devices: I65=15

Turbo PMAC variable I66 tells the controller which type of IC is present on a given external device. I66 is a 4-bit value, with each bit representing 1 of the 4 possible devices that can be connected to a Turbo PMAC. The bit is set to 0 if the device contains “Type 0” PMAC(1)-style DSPGATE Servo ICs; it is set to 1 if the device contains “Type 1” PMAC2-style DSPGATE1 Servo ICs.

The ACC-24P contains the PMAC(1)-style Servo ICs, so the bit of I66 for the ACC-24P must be set to 0 for proper operation.

- Bit 0, with a value of 0, is set to 1 if the 1st ACC-24P is present
- Bit 1, with a value of 0, is set to 1 if the 2nd ACC-24P is present
- Bit 2, with a value of 0, is set to 1 if the 3rd ACC-24P is present
- Bit 3, with a value of 0, is set to 1 if the 4th ACC-24P is present

If only ACC-24P boards are present on the Expansion port, I66 is left at the default value of 0.

Servo IC Configuration I-Variables

Turbo PMAC I-variables in the range I7000 – I7999 control the configuration of the Servo ICs. The hundred's digit represents the number of the Servo IC (0 to 9) in the system. Servo ICs 0 and 1 are (or can be) on board the Turbo PMAC board itself. Servo ICs 2 through 9 are (or can be) on external devices such as the ACC-24P.

Servo IC Numbering

The number 'm' of the Servo IC on the ACC-24P board is dependent on the addressing of the board with DIP switches S1-1 and S1-2, which place the board as the 1st, 2nd, 3rd, or 4th external device:

- 1st ACC-24P: Servo IC 2 (Standard); Servo IC 3 (Option 1)
- 2nd ACC-24P: Servo IC 4 (Standard); Servo IC 5 (Option 1)
- 3rd ACC-24P: Servo IC 6 (Standard); Servo IC 7 (Option 1)
- 4th ACC-24P: Servo IC 8 (Standard); Servo IC 9 (Option 1)

The "Standard" Servo IC on an ACC-24P occupies Channels 1 – 4 on the board, using connectors JMACH1 and JS1. The "Option 1" Servo IC on an ACC-24P occupies Channels 5 – 8 on the board, using connectors JMACH2 and JS2.

For example, the "Standard" Servo IC on the first ACC-24P is Servo IC 2 to Turbo PMAC and is configured by variables I7200 – I7299.

Servo Channel Numbering

Each Servo IC has 4 channels of servo interface circuitry. The ten's digit 'n' of the I-variable configuring the IC represents the channel number on the IC (n = 1 to 4). For example, Channel 1 of the "Standard" Servo IC on the 1st ACC-24P is configured by variables I7210 – I7219. These channel-specific I-variables are represented generically as I7mn0 – I7mn9, where 'm' represents the Servo IC number (0 – 9) and 'n' represents the IC channel number (1 – 4).

The Channels 1 – 4 on the "Standard" Servo IC of an ACC-24P correspond to Channels 1 – 4, respectively, on the ACC-24P board itself. The Channels 1 – 4 on the "Option 1" Servo IC on an ACC-24P correspond to Channels 5 – 8, respectively, on the ACC-24P board.

Single-Channel I-Variables

The single-channel setup I-variables for Channel 'n' of Servo IC 'm' work exactly the same on an ACC-24P as they do on a Turbo PMAC(1) itself. These are:

- **I7mn0:** **Servo IC m Channel n Encoder Decode Control**: I7mn0 is typically set to 3 or 7 for "x4" quadrature decode, depending on which way is "up".
- **I7mn1:** **Servo IC m Channel n Encoder Filter Disable**: I7mn1 is typically set to 0 for digital encoder inputs to keep the filter active, or to 1 when the channel is used with an analog encoder interpolator such as the ACC-8D Opt 8, to disable the filter and synchronize the quadrature and fractional count data.
- **I7mn2:** **Servo IC m Channel n Capture Control**: I7mn2 determines whether the encoder index channel, an input flag, or both, are used for the capture of the encoder position.
- **I7mn3:** **Servo IC m Channel n Capture Flag Select**: I7mn3 determines which input flag is used for encoder capture, if one is used.

Encoder Conversion Table I-Variables

To use feedback or master position data from an ACC-24P, entries must be added to the encoder conversion table (ECT) using I-variables I8000 – I8191 to address and process this data. The default conversion table in the Turbo PMAC does not contain these entries.

The position data obtained through an ACC-24P board is usually an incremental encoder feedback, and occasionally an A/D converter feedback from an ACC-28A/B board connected through the ACC-24P.

The ECT entries for ACC-24P incremental encoder channels are shown in the following table:

Encoder Channel #	1st ACC-24P	2nd ACC-24P	3rd ACC-24P	4th ACC-24P
Channel 1	$mF8200	$mF9200	$mFA200	$mFB200
Channel 2	$mF8204	$mF9204	$mFA204	$mFB204
Channel 3	$mF8208	$mF9208	$mFA208	$mFB208
Channel 4	$mF820C	$mF920C	$mFA20C	$mFB20C
Channel 5	$mF8300	$mF9300	$mFA300	$mFB300
Channel 6	$mF8304	$mF9304	$mFA304	$mFB304
Channel 7	$mF8308	$mF9308	$mFA308	$mFB308
Channel 8	$mF830C	$mF930C	$mFA30C	$mFB30C

The first hexadecimal digit in the entry, represented by 'm' in the table, is a '0' for the most common 1/T timer-based extension of digital incremental encoders; it is an '8' for the parallel-data extension of analog incremental encoders; it is a 'C' for no extension of an incremental encoder.

The ECT entries for ACC-28B A/D converters read through an ACC-24P are shown in the following table:

Register	1st ACC-24P	2nd ACC-24P	3rd ACC-24P	4th ACC-24P
ADC 1	$mn8206	$mn9206	$mnA206	$mnB206
ADC 2	$mn8207	$mn9207	$mnA207	$mnB207
ADC 3	$mn820E	$mn920E	$mnA20E	$mnB20E
ADC 4	$mn820F	$mn920F	$mnA20F	$mnB20F
ADC 5	$mn8306	$mn9306	$mnA306	$mnB306
ADC 6	$mn8307	$mn9307	$mnA307	$mnB307
ADC 7	$mn830E	$mn930E	$mnA30E	$mnB30E
ADC 8	$mn830F	$mn930F	$mnA30F	$mnB30F

The first hexadecimal digit of the entry, represented by 'm' in the above table, is a '1' if the ADC data is processed directly, without integration; it is a '5' if the data is integrated in the conversion. If the entry integrates the data, there is a second line in the entry (another I-variable) that specifies the bias of the A/D converter.

The second hexadecimal digit of the entry, represented by 'n' in the above table, is a '7' if the ACC-28A with signed data is used; it is an 'F' if the ACC-28B with unsigned data is used.

Motor Addressing I-Variables

For a Turbo PMAC motor to use the servo interface circuitry of the ACC-24P, several of the addressing I-variables for the motor must contain the addresses of registers in the ACC-24P, or the addresses of encoder conversion table registers containing data processed from the ACC-24P. These I-variables can include:

- **Ixx02: Motor xx Command Output Address**: Ixx02 tells Turbo PMAC where to write its command outputs for Motor xx. If ACC-24P is to create the command signals, Ixx02 must contain the address of the register. The following table shows the address of the DAC output register for each channel of each ACC-24P. These addresses can be used for single analog outputs or double analog outputs.

ACC-24P Register: Board No. & Channel	Address / Ixx02 Value	PMAC Default for:	ACC-24P Register: Board No. & Channel	Address / Ixx02 Value	PMAC Default for:
1st ACC-24P DAC1	$078203	I902	3rd ACC-24P DAC1	$07A203	I2502
1st ACC-24P DAC2	$078202	I1002	3rd ACC-24P DAC2	$07A202	I2602
1st ACC-24P DAC3	$07820B	I1102	3rd ACC-24P DAC3	$07A20B	I2702
1st ACC-24P DAC4	$07820A	I1202	3rd ACC-24P DAC4	$07A20A	I2802
1st ACC-24P DAC5	$078303	I1302	3rd ACC-24P DAC5	$07A303	I2902
1st ACC-24P DAC6	$078302	I1402	3rd ACC-24P DAC6	$07A302	I3002
1st ACC-24P DAC7	$07830B	I1502	3rd ACC-24P DAC7	$07A30B	I3102
1st ACC-24P DAC8	$07830A	I1602	3rd ACC-24P DAC8	$07A30A	I3202
2nd ACC-24P DAC1	$079203	I1702	4th ACC-24P DAC1	$07B203	--
2nd ACC-24P DAC2	$079202	I1802	4th ACC-24P DAC2	$07B202	--
2nd ACC-24P DAC3	$07920B	I1902	4th ACC-24P DAC3	$07B20B	--
2nd ACC-24P DAC4	$07920A	I2002	4th ACC-24P DAC4	$07B20A	--
2nd ACC-24P DAC5	$079303	I2102	4th ACC-24P DAC5	$07B303	--
2nd ACC-24P DAC6	$079302	I2202	4th ACC-24P DAC6	$07B302	--
2nd ACC-24P DAC7	$07930B	I2302	4th ACC-24P DAC7	$07B30B	--
2nd ACC-24P DAC8	$07930A	I2402	4th ACC-24P DAC8	$07B30A	--

- **Ixx03: Motor xx Position-Loop Feedback Address**
- **Ixx04: Motor xx Velocity-Loop Feedback Address**
- **Ixx05: Motor xx Master Position Address**

Usually, the Ixx03, Ixx04, and Ixx05 variables contain the address of a processed position value in the encoder conversion table, even when the raw data comes from the ACC-24P.

- **Ixx10: Motor xx Power-On Position Address:** Ixx10 tells the Turbo PMAC where to read absolute power-on position, if any. Typically, the only times Ixx10 will contain the address of an ACC-24P register is if the position is obtained from an A/D converter on an ACC-28A/B connected through the ACC-24P.

The following table shows the possible values of Ixx10 for ACC-28 A/D converters:

Ixx10 Values for PMAC(1)-Style ADC Registers
(Ixx95=$310000 for ACC-28A; =$B10000 for ACC-28B)

Register	1st ACC-24P	2nd ACC-24P	3rd ACC-24P	4th ACC-24P
ADC 1	$078206	$079206	$07A206	$07B206
ADC 2	$078207	$079207	$07A207	$07B207
ADC 3	$07820E	$07920E	$07A20E	$07B20E
ADC 4	$07820F	$07920F	$07A20F	$07B20F
ADC 5	$078306	$079306	$07A306	$07B306
ADC 6	$078307	$079307	$07A307	$07B307
ADC 7	$07830E	$07930E	$07A30E	$07B30E
ADC 8	$07830F	$07930F	$07A30F	$07B30F

- **Ixx24: Motor xx Flag Mode:** Ixx24 tells Turbo PMAC how to read and use the flags for Motor xx that are in the register specified by Ixx25. Ixx24 is a set of independent control bits. There are two bits that must be set correctly to use a flag set on an ACC-24P.

  Bit 0 of Ixx24 must be set to 0 to tell the Turbo PMAC that this flag set is in a "Type 0" PMAC(1)-style Servo IC. Bit 18 of Ixx24 must be set to 0 to tell the Turbo PMAC that this flag set is *not* transmitted over a MACRO ring. Other bits of Ixx24 may be set as desired for a particular application.

- **Ixx25: Motor xx Flag Address:** Ixx25 tells Turbo PMAC where to access its flag data for Motor xx. If ACC-24P is interface to the flags, Ixx25 must contain the address of the flag register in ACC-24P. The following table shows the address of the flag register for each channel of each ACC-24P.

ACC-24P Register: Board No. & Channel	Address / Ixx25 Value	PMAC Default for:	ACC-24P Register: Board No. & Channel	Address / Ixx25 Value	PMAC Default for:
1st ACC-24P/V Flag Set 1	$078200	I925	3rd ACC-24P/V Flag Set 1	$07A200	I2525
1st ACC-24P/V Flag Set 2	$078204	I1025	3rd ACC-24P/V Flag Set 2	$07A204	I2625
1st ACC-24P/V Flag Set 3	$078208	I1125	3rd ACC-24P/V Flag Set 3	$07A208	I2725
1st ACC-24P/V Flag Set 4	$07820C	I1225	3rd ACC-24P/V Flag Set 4	$07A20C	I2825
1st ACC-24P/V Flag Set 5	$078300	I1325	3rd ACC-24P/V Flag Set 5	$07A300	I2925
1st ACC-24P/V Flag Set 6	$078304	I1425	3rd ACC-24P/V Flag Set 6	$07A304	I3025
1st ACC-24P/V Flag Set 7	$078308	I1525	3rd ACC-24P/V Flag Set 7	$07A308	I3125
1st ACC-24P/V Flag Set 8	$07830C	I1625	3rd ACC-24P/V Flag Set 8	$07A30C	I3225
2nd ACC-24P/V Flag Set 1	$079200	I1725	4th ACC-24P/V Flag Set 1	$07B200	--
2nd ACC-24P/V Flag Set 2	$079204	I1825	4th ACC-24P/V Flag Set 2	$07B204	--
2nd ACC-24P/V Flag Set 3	$079208	I1925	4th ACC-24P/V Flag Set 3	$07B208	--
2nd ACC-24P/V Flag Set 4	$07920C	I2025	4th ACC-24P/V Flag Set 4	$07B20C	--
2nd ACC-24P/V Flag Set 5	$079300	I2125	4th ACC-24P/V Flag Set 5	$07B300	--
2nd ACC-24P/V Flag Set 6	$079304	I2225	4th ACC-24P/V Flag Set 6	$07B304	--
2nd ACC-24P/V Flag Set 7	$079308	I2325	4th ACC-24P/V Flag Set 7	$07B308	--
2nd ACC-24P/V Flag Set 8	$07930C	I2425	4th ACC-24P/V Flag Set 8	$07B30C	--

- **Ixx81: Motor xx Power-On Phase Position Address:** Ixx81 tells Turbo PMAC where to read absolute power-on position for motor phase commutation if any. Typically, it will contain the address of an ACC-24P register for only two types of absolute phasing sensors. The hall-effect commutation sensors (or their optical equivalents) connected to the U, V, and W input flags on an ACC-24P channel, or the encoder counter filled by simulated quadrature from a Yaskawa absolute encoder connected to the ACC-24P through an ACC-8D Option 9 board.

  The following table contains the possible settings of Ixx81 for hall sensor absolute position with an ACC-24P:

Turbo PMAC Ixx81 ACC-24P Hall Phasing Settings
(Ix91=$800000 - $FF0000)

Hall Flag Channel #	1st ACC-24P	2nd ACC-24P	3rd ACC-24P	4th ACC-24P
Channel 2	$078204	$079204	$07A204	$07B204
Channel 4	$07820C	$07920C	$07A20C	$07B20C
Channel 6	$078304	$079304	$07A304	$07B304
Channel 8	$07830C	$07930C	$07A30C	$07B30C

  The following table contains the possible settings of Ixx81 to read the encoder counters for Yaskawa absolute encoders:

Turbo PMAC Ixx81 ACC-24P Encoder Register Settings
(Ix91=$480000 - $580000)

Encoder Register Channel #	1st ACC-24P	2nd ACC-24P	3rd ACC-24P	4th ACC-24P
Channel 1	$078201	$079201	$07A201	$07B201
Channel 2	$078205	$079205	$07A205	$07B205
Channel 3	$078209	$079209	$07A209	$07B209
Channel 4	$07820D	$07920D	$07A20D	$07B20D
Channel 5	$078301	$079301	$07A301	$07B301
Channel 6	$078305	$079305	$07A305	$07B305
Channel 7	$078309	$079309	$07A309	$07B309
Channel 8	$07830D	$07930D	$07A30D	$07B30D

- **Ixx83: Motor xx Phase Position Address:** Ixx83 tells Turbo PMAC where to get its commutation position feedback every phase update cycle. Usually this contains the address of an encoder "phase position" register.

The following table shows the possible values of Ixx83 for ACC-24P encoder phase position registers:

Turbo PMAC Ixx83 ACC-24P Encoder Register Settings

Encoder Register Channel #	**1st ACC-24P**	**2nd ACC-24P**	**3rd ACC-24P**	**4th ACC-24P**
Channel 1	$078201	$079201	$07A201	$07B201
Channel 2	$078205	$079205	$07A205	$07B205
Channel 3	$078209	$079209	$07A209	$07B209
Channel 4	$07820D	$07920D	$07A20D	$07B20D
Channel 5	$078301	$079301	$07A301	$07B301
Channel 6	$078305	$079305	$07A305	$07B305
Channel 7	$078309	$079309	$07A309	$07B309
Channel 8	$07830D	$07930D	$07A30D	$07B30D

ACC-24P JUMPER AND SWITCH DESCRIPTION

S1: Board Addressing DIP Switch Bank

Switch	Location	Description	Default
S1-1		Use S1-1 and S1-2 select Acc-24P address on Turbo PMAC's expansion port according to the following table: Set S1-1, S1-2, S1-3, S1-4 to OFF position when connecting to regular (non-Turbo) PMAC.	ON
S1-2		Use S1-1 and S1-2 select Acc-24P address on Turbo PMAC'S expansion port according to the following table: Set S1-1, S1-2, S1-3, S1-4 to OFF position when connecting to regular (non-Turbo) PMAC.	ON
S1-3		Board expansion port address enable: Set S1-3 to ON position when connecting to Turbo PMAC/PMAC2; enables addressing of multiple Acc-24 boards Set S1-1, S1-2, S1-3, S1-4 to OFF position when connecting to regular (non-Turbo) PMAC.	ON
S1-4		Board expansion port address enable: Set S1-3 to ON position when connecting to Turbo PMAC/PMAC2; enables addressing of multiple Acc-24 boards Set S1-1, S1-2, S1-3, S1-4 to OFF position when connecting to regular (non-Turbo) PMAC.	ON

Addressing of ACC-24 Boards For Turbo PMAC

S1-1	S1-2	S1-3	S1-4	Board No.	1ST IC No.	2ND IC No.	1ST IC Base Address	2ND IC Base Address
ON	ON	ON	ON	1ST	2	3	$078200	$078300
OFF	ON	ON	ON	2ND	4	5	$079200	$079300
ON	OFF	ON	ON	3RD	6	7	$07A200	$07A300
OFF	OFF	ON	ON	4TH	8	9	$07B200	$07B300

E17: Global Amplifier Enable/Direction Polarity Control

E Point & Physical Layout	Location	Description	Default
E17 		Jump pins 1-2 for conducting-on-enable AENA signals when channel-specific jumpers E17A-H are OFF (default); for non-conducting-on-enable signals when E17A-H are ON. Remove jumper for non-conducting-on-enable AENA signals when channel-specific jumpers E17A-H are OFF (default); for conducting-on-enable AENA signals when E17A-H are ON.	Jumper installed
Note: The default ULN2803A sinking drivers have a low output voltage when conducting and can pull high when not conducting. The optional UDN2981A sourcing drivers have a high output voltage when conducting and can pull low when not conducting.			

E17A-D: Individual Amplifier Enable/Direction Polarity Control

E Point & Physical Layout	Location	Description	Default
E17A 		Jump pins 1-2 for non-conducting-on-enable AENA1 when global jumper E17 is ON (default); for conducting-on-enable AENA1 when E17 is OFF. Remove jumper for conducting-on-enable AENA1 when global jumper E17 is ON (default); for non-conducting-on-enable AENA1 when E17 is OFF.	No jumper installed
E17B 		Jump pins 1-2 for non-conducting-on-enable AENA2 when global jumper E17 is ON (default); for conducting-on-enable AENA2 when E17 is OFF. Remove jumper for conducting-on-enable AENA2 when global jumper E17 is ON (default); for non-conducting-on-enable AENA2 when E17 is OFF.	No jumper installed
E17C 		Jump pins 1-2 for non-conducting-on-enable AENA3 when global jumper E17 is ON (default); for conducting-on-enable AENA3 when E17 is OFF. Remove jumper for conducting-on-enable AENA3 when global jumper E17 is ON (default); for non-conducting-on-enable AENA3 when E17 is OFF.	No jumper installed
E17D 		Jump pins 1-2 for non-conducting-on-enable AENA4 when global jumper E17 is ON (default); for conducting-on-enable AENA4 when E17 is OFF. Remove jumper for conducting-on-enable AENA4 when global jumper E17 is ON (default); for non-conducting-on-enable AENA4 when E17 is OFF.	No jumper installed
Note: The default ULN2803A sinking drivers have a low output voltage when conducting and can pull high when not conducting. The optional UDN2981A sourcing drivers have a high output voltage when conducting and can pull low when not conducting.			

E17E-H: Individual Amplifier Enable/Direction Polarity Control (Option 1 Required)

E Point & Physical Layout	Location	Description	Default
E17E 		Jump pins 1-2 for non-conducting-on-enable AENA5 when global jumper E17 is ON (default); for conducting-on-enable AENA5 when E17 is OFF. Remove jumper for conducting-on-enable AENA5 when global jumper E17 is ON (default); for non-conducting-on-enable AENA5 when E17 is OFF.	No jumper installed
E17F 		Jump pins 1-2 for non-conducting-on-enable AENA6 when global jumper E17 is ON (default); for conducting-on-enable AENA6 when E17 is OFF. Remove jumper for conducting-on-enable AENA6 when global jumper E17 is ON (default); for non-conducting-on-enable AENA6 when E17 is OFF.	No jumper installed
E17G 		Jump pins 1-2 for non-conducting-on-enable AENA7 when global jumper E17 is ON (default); for conducting-on-enable AENA7 when E17 is OFF. Remove jumper for conducting-on-enable AENA7 when global jumper E17 is ON (default); for non-conducting-on-enable AENA7 when E17 is OFF.	No jumper installed
E17H 		Jump pins 1-2 for non-conducting-on-enable AENA8 when global jumper E17 is ON (default); for conducting-on-enable AENA8 when E17 is OFF. Remove jumper for conducting-on-enable AENA8 when global jumper E17 is ON (default); for non-conducting-on-enable AENA8 when E17 is OFF.	No jumper installed
Note: The default ULN2803A sinking drivers have a low output voltage when conducting and can pull high when not conducting. The optional UDN2981A sourcing drivers have a high output voltage when conducting and can pull low when not conducting.			

E18 - E21: Encoder Single-Ended/Differential Control (Option 1 Required)

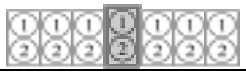
E Point & Physical Layout	Location	Description	Default
E18 		ENC 8 through 5: Jump pin 1 to 2 to tie complementary encoder inputs to 2.5V.	1-2 Jumper installed for E18 - E21.
E19 		Jump pin 2 to 3 to tie complementary encoder inputs to 5V. For no encoder connection: Jump pin 1 to 2.	E18: ENC 8 E19: ENC 7 E20: ENC 6 E21: ENC 5
E20 		For single-ended encoders: Jump pin 1 to 2. For differential line-driver encoders: Don't care.	
E21 		For complementary open-collector encoders: Jump pin 2 to 3.	

E24 - E27: Encoder Single-Ended/Differential Control

E Point & Physical Layout	Location	Description	Default
E24 		ENC 4 through 1: Jump pin 1 to 2 to tie complementary encoder inputs to 2.5V.	1-2 Jumper installed for E24 - E27.
E25 		Jump pin 2 to 3 to tie complementary encoder inputs to 5V. For no encoder connection: Jump pin 1 to 2.	E24: ENC 4 E25: ENC 3 E26: ENC 2 E27: ENC 1
E26 		For single-ended encoders: Jump pin 1 to 2. For differential line-driver encoders: Don't care.	
E27 		For complementary open-collector encoders: Jump pin 2 to 3.	

E34 - E38: Encoder Sampling Clock Frequency Control

Jumpers E34 - E38 control the encoder sampling clock (SCLK) used by the gate array ICs. No more than 1 of these 7 jumpers may be on at a time.

							SCLK Clock Frequency	Default & Physical Layout
E36	**E35**	**E34A**	**E34**	**E37**	**E38**	**E38A**		**E36 E35 E34A E34 E37 E38 E38A** 
OFF	OFF	ON	OFF	OFF	OFF	OFF	19.6608 MHz	
OFF	OFF	OFF	ON	OFF	OFF	OFF	9.8304 MHz	E34 ON
OFF	ON	OFF	OFF	OFF	OFF	OFF	4.9152 MHz	
ON	OFF	OFF	OFF	OFF	OFF	OFF	2.4576 MHz	
OFF	OFF	OFF	OFF	ON	OFF	OFF	1.2288 MHz	
OFF	OFF	OFF	OFF	OFF	ON	OFF	External Clock 1 to 30 MHz maximum input on CHC4 & CHC4/	
OFF	OFF	OFF	OFF	OFF	OFF	ON	Clock from PMAC, input on J5 OR J6 PIN 9 from PMAC	

E54-E57: Position Compare Channel Interrupt Select

E Point & Physical Layout	Location	Description	Default
E54 		Jump pin 1 to pin 2 to connect EQU8 to J5 pin 8 for possible PMAC interrupt.	No jumper
E55 		Jump pin 1 to pin 2 to connect EQU4 to J5 pin 8 for possible PMAC interrupt.	No jumper
E56 		Jump pin 1 to pin 2 to connect EQU4 to J5 pin 8 for possible PMAC interrupt.	No jumper
E57 		Jump pin 1 to pin 2 to connect EQU3 to J5 pin 7 for possible PMAC interrupt.	No jumper

E60-E65: Position Compare Channel Interrupt Select

E Point & Physical Layout	Location	Description	Default
E60 		Jump pin 1 to pin 2 to connect EQU6 to J5 pin 8 for possible PMAC interrupt.	No jumper
E61 		Jump pin 1 to pin 2 to connect EQU2 to J5 pin 8 for possible PMAC interrupt.	No jumper
E64 		Jump pin 1 to pin 2 to connect EQU5 to J5 pin 8 for possible PMAC interrupt.	No jumper
E65 		Jump pin 1 to pin 2 to connect EQU1 to J5 pin 7 for possible PMAC interrupt.	No jumper

E85: Host-Supplied Analog Power Source Enable

E Point & Physical Layout	Location	Description	Default
E85 		Jump pin 1 to pin 2 to allow A+14V to come from PC bus (ties amplifier and PMAC-Lite power supply together. Defeats OPTO coupling.) Note that if E85 is changed, E88 and E87 must also be changed. Also, see E90.	No jumper

E87 - E88: Host-Supplied Analog Power Source Enable

E Point & Physical Layout	Location	Description	Default
E87 		Jump pin 1 to pin 2 to allow AGND to come from PC bus (ties amplifier and PMAC-Lite GND together. Defeats OPTO coupling.) Note that if E87 is changed, E85 and E88 must also be changed Also, see E90.	No jumper
E88 		Jump pin 1 to pin 2 to allow A-14V to come from PC bus (ties amplifier and PMAC-Lite power supply together. Defeats OPTO coupling.) Note that if E88 is changed; E87 and E85 must also be changed. Also, see E90.	No jumper

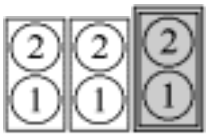
E89: Analog Supply for Input Flag Select

E Point & Physical Layout	Location	Description	Default
E89 		Jump pin 1 to 2 to use A+15V on J8 (JMACH1) pin 59 as supply for input flags. Remove jumper to use A+15V/OPT+V from J7 pin 59 as supply for input flags.	Jumper installed
Note: This jumper setting is only relevant if E90 connects pin 1 to 2.			

E90: Input Flag Supply Select

E Point & Physical Layout	Location	Description	Default
E90 		Jump pin 1 to 2 to use A+15V from J8 pin 59 as supply for input flags (E89 ON) {flags should be tied to AGND} or A+15V/OPT+V from J8 pin 11 as supply for input flags (E89 OFF) {flags should be tied to separate 0V reference}. Jump pin 2 to 3 to use +12V from PC bus connector P1-pin B09 as supply for input flags {flags should be tied to GND}. See also E85, E87, E88 and PMAC Opto-isolation diagram	1-2 Jumper installed

E98A-C: DAC/ADC Clock Frequency Control

E Point & Physical Layout	Location	Description	Default
 **E98C E98B E98A**		Jump E98A pins 1-2 to provide an internally generated 2.45 MHz DCLK signal to DACs and ADCs. Jump E98B pins 1-2 to provide an internally generated 1.22 MHz DCLK signal to DACs and ADCs. Important for high accuracy A/D conversion on ACC-28A. Jumper E98C pins 1-2 to provide PMAC's DCLK signal through J5 or J6 pin 10 to DACs and ADCs. Not recommended. Do not use if more than one ACC-24P connected to PMAC	1-2 Jumper installed

E100: Output Flag Supply Select

E Point & Physical Layout	Location	Description	Default
E100 		Jump pin 1 to 2 to apply analog supply voltage A+15V to "U54" flag output driver IC. Jump pin 2 to 3 to apply flag supply voltage OPT+V to "U54" flag output driver IC.	1-2 Jumper installed

E101 – E102: Output Flag Supply Voltage Configure

E Point & Physical Layout	Location	Description	Default
E101  		**CAUTION** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply +V (12V to 24V) to pin 10 of "U11" (should be ULN2803A for sink output configuration) for AENA1-4 and EQU1-4 flag outputs. Jump pin 2 to 3 to apply AGND to pin 10 of "U11" (should be UDN2981A for source output configuration) for AENA1-4 and EQU1-4 flag outputs.	1-2 Jumper installed
E102  		**CAUTION** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to AGND to pin 9 of "U11" (should be ULN2803A for sink output configuration) for AENA1-4 and EQU1-4 flag outputs. Jump pin 2 to 3 to apply +V (12V to 24V) to pin 9 of "U11" (should be UDN2981A for source output configuration) for AENA1-4 and EQU1-4 flag outputs.	1-2 Jumper installed

E103 – E104: Output Flag Supply Voltage Configure 1 required)

E Point & Physical Layout	Location	Description	Default
E103  		**CAUTION:** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply +V (12V to 24V) to pin 10 of "U74" (should be ULN2803A for sink output configuration) for AENA1-4 and EQU1-4 flag outputs. Jump pin 2 to 3 to apply AGND to pin 10 of "U74" (should be UDN2981A for source output configuration) for AENA1-4 and EQU1-4 flag outputs.	1-2 Jumper installed
E104  		**CAUTION:** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to AGND to pin 9 of "U74" (should be ULN2803A for sink output configuration) for AENA1-4 and EQU1-4 flag outputs. Jump pin 2 to 3 to apply +V (12V to 24V) to pin 9 of "U74" (should be UDN2981A for source output configuration) for AENA1-4 and EQU1-4 flag outputs.	1-2 Jumper installed

CONNECTOR DESCRIPTIONS

J1: Expansion Port Connector

J1 is a 50-pin IDC header that provides the connection to PMAC's JEXP Expansion Port. Contact the factory if pinout information is required.

JS1

This connector contains miscellaneous I/O signals related to the first DSPGATE on Acc-24p. Typically, it is used for direct connection to ACC-28 (analog-to-digital converter board).

JS1 (16 Pin Header)

Pin #	Symbol	Function	Description	Notes
1	DCLK	Output	D to A, A to D Clock	DAC & ADC clock for v 9, 10, 11, 12
2	BDATA1	Output	D to A Data	DAC data for Channel 9, 10, 11, 12
3	ASELO/	Output	Chan Select Bit 0	Select for Channel 9, 10, 11, 12
4	ASEL1/	Output	Chan Select Bit 2	Select for Channel 9, 10, 11, 12
5	CONVERT 01	Output	A to D Convert	ADC convert signal Channel 9, 10, 11, 12
6	ADCIN1	Input	A to D Data	ADC data for Channel 9, 10, 11, 12
7	OUT1/	Output	Amp Enable/Dir	Amp Enable/Direction for Channel 9
8	OUT2/	Output	Amp Enable/Dir	Amp Enable/Direction for Channel 10
9	OUT3/	Output	Amp Enable/Dir	Amp Enable/Direction for Channel 11
10	OUT4/	Output	Amp Enable/Dir	Amp Enable/Direction for Channel 12
11	HF41	Input	Amp Fault	Amp Fault input for Channel 9
12	HF42	Input	Amp Fault	Amp Fault input for Channel 10
13	HF43	Input	Amp Fault	Amp Fault input for Channel 11
14	HF44	Input	Amp Fault	Amp Fault input for Channel 12
15	+5V	Output	+5V Supply	Power Supply out
16	GND	Common	PMAC Common	

Miscellaneous I/0 – Typically, this connector is used for direct connection to ACC-23 or ACC-28 (the analog-to-digital converter boards)

JS2

This connector contains miscellaneous I/O signals related to the second DSPGATE on ACC-24P. Typically, it is used for direct connection to ACC-28 analog-to-digital converter board).

JS2 (16 Pin Header)				
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	DCLK	Output	D to A, A to D Clock	DAC and ADC clock for Channel 13, 14,15,16
2	BDATA2	Output	D to A Data	DAC data for Channel 13,14,15,16
3	ASEL2/	Output	Chan. Select Bit 2	Select for Channel 13,14,15,16
4	ASEL3/	Output	Chan. Select Bit 3	Select for Channel 13,14,15,16
5	CONVERT 23	Output	A to D Convert	ADC convert signal Channel 13,14,15,16
6	ADCIN2	Input	A to D Data	ADC data for Channel 13,14,15,16
7	OUT5/	Output	Amp Enable/Dir	Amp Enable/Direction for Channel 13
8	OUT6/	Output	Amp Enable/Dir	Amp Enable/Direction for Channel 14
9	OUT7/	Output	Amp Enable/Dir	Amp Enable/Direction for Channel 15
10	OUT8/	Output	Amp Enable/Dir	Amp Enable/Direction for Channel 16
11	HF45	Input	Amp Fault	Amp fault input for Channel 13
12	HF46	Input	Amp Fault	Amp fault input for Channel 14
13	HF47	Input	Amp Fault	Amp fault input for Channel 15
14	HF48	Input	Amp Fault	Amp fault input for Channel 16
15	+5V	Output	+5V Supply	Power Supply out
16	GND	Common	PMAC Common	
Miscellaneous I/O. Typically, this connector is used for direct connection to ACC-23 or ACC-28 (the analog-to-digital converter boards).				

J5

This connector brings in the required DSPGATE clock signals from PMAC's J6 (JXIO) connector. In addition, two (jumper selectable) Compare-Equal signals are sent back for PMAC's use (possibly for host interrupts). A 10-pin flat cable is provided for this purpose. For proper operation of ACC-24P**,** J5 must be connected to PMAC's J6 (JXIO).

J5				
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	CHA1	N.C.		
2	CHB1	N.C.		
3	CHC1	N.C.		
4	CHA3	N.C.		
5	CHB3	N.C.		
6	CHC3	N.C.		
7	IR5	Output[1]	Interrupt IR5	Interrupt from expansion board (See E point listing (E54 to E65)
8	IR6	Output[2]	Interrupt IR6	Interrupt from expansion board (See E point Listing (E54 to E65)
9	SCLK	Input	System Clock	Servo-encoder timing
10	DCLK	Input	D to A, A to D Clock	
[1] Jumper selector to EQU 9, or EQU 11, or EQU 13, OR EQU 15 [2] Jumper selector to EQU 10, or EQU 12, or EQU 14, or EQU 16 This connector must be connected to PMAC's JxIO (J6) via the supplied cable				

J6

This connector brings in two channels of converted resolver inputs from ACC-14D.

J6				
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	CHA9	Input	Enc. 9 Chan. A	Resolver input
2	CHB9	Input	Enc. 9 Chan. B	Resolver input
3	CHC9	Input	Enc. 9 Chan. C	Resolver input
4	CHA11	Input	Enc. 11 Chan. A	Resolver input
5	CHB11	Input	Enc. 11 Chan. B	Resolver input
6	CHC11	Input	Enc. 11 Chan. C	Resolver input
7	IR5	Output[1]	Interrupt IR5	Interrupt from expansion board (See E point listing (E54 to E65)
8	IR6	Output[2]	Interrupt IR6	Interrupt from expansion board (See E point listing E54 to E65)
9	SCLK	Output	System Clock	Servo-Encoder timing
10	DCLK	Output	D to A, A to D Clock	

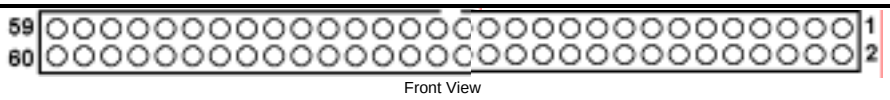
Typically, this connector is used for connection to ACC-14D in order to bring in two channels of resolver inputs via the iSBX connectors on ACC-14D

1 Jumper selector to EQU 9, or EQU 11, or EQU 13, OR EQU 15

2 Jumper selector to EQU 10, or EQU 12, or EQU 14, or EQU 16

J7 (JMACH2): Second Machine Port Connector

J7 JMACH2 (60-Pin Header)



Front View

Pin #	Symbol	Function	Description	Notes
1	+5V	Output	+5V Power	For encoders, 1
2	+5V	Output	+5V Power	For encoders, 1
3	GND	Common	Digital Common	
4	GND	Common	Digital Common	
5	CHC7	Input	Encoder C Ch. Pos.	2
6	CHC8	Input	Encoder C Ch. Pos.	2
7	CHC7/	Input	Encoder C Ch. Neg.	2,3
8	CHC8/	Input	Encoder C Ch. Neg.	2,3
9	CHB7	Input	Encoder B Ch. Pos.	2
10	CHB8	Input	Encoder B Ch. Pos.	2
11	CHB7/	Input	Encoder B Ch. Neg.	2,3
12	CHB8/	Input	Encoder B Ch. Neg.	2,3
13	CHA7	Input	Encoder A Ch. Pos.	2
14	CHA8	Input	Encoder A Ch. Pos.	2
15	CHA7/	Input	Encoder A Ch. Neg.	2,3
16	CHA8/	Input	Encoder A Ch. Neg.	2,3
17	CHC5	Input	Encoder C Ch. Pos.	2
18	CHC6	Input	Encoder C Ch. Pos.	2
19	CHC5/	Input	Encoder C Ch. Neg.	2,3
20	CHC6/	Input	Encoder C Ch. Neg.	2,3
21	CHB5	Input	Encoder B Ch. Pos.	2
22	CHB6	Input	Encoder B Ch. Pos.	2
23	CHB5/	Input	Encoder B Ch. Neg.	2,3
24	CHB6/	Input	Encoder B Ch. Neg.	2,3
25	CHA5	Input	Encoder A Ch. Pos.	2
26	CHA6	Input	Encoder A Ch. Pos.	2
27	CHA5/	Input	Encoder A Ch. Neg.	2,3
28	CHA6/	Input	Encoder A Ch. Neg.	2,3
29	DAC7	Output	Analog Out Pos.	4
30	DAC8	Output	Analog Out Pos.	4
31	DAC7/	Output	Analog Out Neg.	4,5
32	DAC8/	Output	Analog Out Neg.	4,5
33	AENA7/DIR7	Output	Amp-Ena/Dir.	6
34	AENA8/DIR8	Output	Amp-Ena/Dir.	6
35	FAULT7	Input	Amp-Fault	7
36	FAULT8	Input	Amp-Fault	7
37	+LIM7	Input	Neg. End Limit	8,9
38	+LIM8	Input	Neg. End Limit	8,9
39	-LIM7	Input	Pos. End Limit	8,9
40	-LIM8	Input	Pos. End Limit	8,9
41	HMFL7	Input	Home-Flag	10
42	HMFL8	Input	Home-Flag	10
43	DAC5	Output	Analog Out Pos.	4
44	DAC6	Output	Analog Out Pos.	4
45	DAC5/	Output	Analog Out Neg.	4,5
46	DAC6/	Output	Analog Out Neg.	4,5

47	AENA5/DIR5	Output	Amp-Ena/Dir.	6
48	AENA6/DIR6	Output	Amp-Ena/Dir.	6
49	FAULT5	Input	Amp-Fault	7
50	FAULT6	Input	Amp-Fault	7
51	+LIM5	Input	Neg. End Limit	8,9
52	+LIM6	Input	Neg. End Limit	8,9
53	-LIM5	Input	Pos. End Limit	8,9
54	-LIM6	Input	Pos. End Limit	8,9
55	HMFL5	Input	Home-Flag	10
56	HMFL6	Input	Home-Flag	10
57	ORST/	Output	Reset Out	Indicator/Driver
58	AGND	Input	Analog Common	
59	A+15V/OPT+V	Input	Analog +15V Supply	
60	A-15V	Input	Analog -15V Supply	

The J7 connector is used to connect ACC-24P to its second 4 channels (Channels 5, 6, 7, and 8) of servo amps, flags, and encoders. From a non-Turbo PMAC, these would be considered Channels 13, 14, 15, and 16. It is only present if Option 1 has been ordered for the ACC-24P.

Note 1: In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry. However, if a terminal block is available on your version of PMAC, it is preferable to bring the +5V power in through the terminal block.

Note 2: Referenced to digital common (GND). Maximum of ± 12V permitted between this signal and its complement.

Note 3: Leave this input floating if not used (i.e. digital single-ended encoders). In this case, jumper (E18 - 21, E24 - 27) for channel should hold input at 2.5V.

Note 4: ± 10V, 10mA max, referenced to analog common (AGND).

Note 5: Leave floating if not used; do not tie to AGND. In this case, AGND is the return line.

Note 6: Functional polarity controlled by jumper(s) E17. Choice between AENA and DIR use controlled by Ix02 and Ix25.

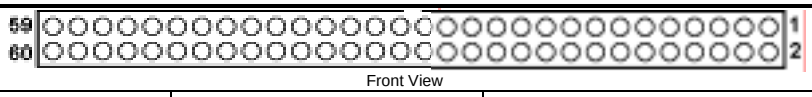
Note 7: Functional polarity controlled by variable Ix25. Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software. Automatic fault function can be disabled with Ix25.

Note 8: Pins marked -LIMn should be connected to switches at the positive end of travel. Pins marked +LIMn should be connected to switches at the negative end of travel.

Note 9: Must be conducting to 0V (usually AGND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.

Note 10: Functional polarity for homing or other trigger use of HMFLn controlled by Encoder/Flag Variable 2 (I902, I907, etc.) HMFLn selected for trigger by Encoder/Flag Variable 3 (I903, I908, etc.). Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software.

J8 (JMACH1): First Machine Port Connector

J8 JMACH1 (60-Pin Header)		 Front View		
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	+5V	Output	+5V Power	For encoders, 1
2	+5V	Output	+5V Power	For encoders, 1
3	GND	Common	Digital Common	
4	GND	Common	Digital Common	
5	CHC3	Input	Encoder C Ch. Pos.	2
6	CHC4	Input	Encoder C Ch. Pos.	2
7	CHC3/	Input	Encoder C Ch. Neg.	2,3
8	CHC4/	Input	Encoder C Ch. Neg.	2,3
9	CHB3	Input	Encoder B Ch. Pos.	2
10	CHB4	Input	Encoder B Ch. Pos.	2
11	CHB3/	Input	Encoder B Ch. Neg.	2,3
12	CHB4/	Input	Encoder B Ch. Neg.	2,3
13	CHA3	Input	Encoder A Ch. Pos.	2
14	CHA4	Input	Encoder A Ch. Pos.	2
15	CHA3/	Input	Encoder A Ch. Neg.	2,3
16	CHA4/	Input	Encoder A Ch. Neg.	2,3
17	CHC1	Input	Encoder C Ch. Pos.	2
18	CHC2	Input	Encoder C Ch. Pos.	2
19	CHC1/	Input	Encoder C Ch. Neg.	2,3
20	CHC2/	Input	Encoder C Ch. Neg.	2,3
21	CHB1	Input	Encoder B Ch. Pos.	2
22	CHB2	Input	Encoder B Ch. Pos.	2
23	CHB1/	Input	Encoder B Ch. Neg.	2,3
24	CHB2/	Input	Encoder B Ch. Neg.	2,3
25	CHA1	Input	Encoder A Ch. Pos.	2
26	CHA2	Input	Encoder A Ch. Pos.	2
27	CHA1/	Input	Encoder A Ch. Neg.	2,3
28	CHA2/	Input	Encoder A Ch. Neg.	2,3
29	DAC3	Output	Analog Out Pos.	4
30	DAC4	Output	Analog Out Pos.	4
31	DAC3/	Output	Analog Out Neg.	4,5
32	DAC4/	Output	Analog Out Neg.	4,5
33	AENA3/DIR3	Output	Amp-Ena/Dir.	6
34	AENA4/DIR4	Output	Amp-Ena/Dir.	6
35	FAULT3	Input	Amp-Fault	7
36	FAULT4	Input	Amp-Fault	7
37	+LIM3	Input	Neg. End Limit	8,9
38	+LIM4	Input	Neg. End Limit	8,9
39	-LIM3	Input	Pos. End Limit	8,9

40	-LIM4	Input	Pos. End Limit	8,9
41	HMFL3	Input	Home-Flag	10
42	HMFL4	Input	Home-Flag	10
43	DAC1	Output	Analog Out Pos.	4
44	DAC2	Output	Analog Out Pos.	4
45	DAC1/	Output	Analog Out Neg.	4,5
46	DAC2/	Output	Analog Out Neg.	4,5
47	AENA1/DIR1	Output	Amp-Ena/Dir.	6
48	AENA2/DIR2	Output	Amp-Ena/Dir.	6
49	FAULT1	Input	Amp-Fault	7
50	FAULT2	Input	Amp-Fault	7
51	+LIM1	Input	Neg. End Limit	8,9
52	+LIM2	Input	Neg. End Limit	8,9
53	-LIM1	Input	Pos. End Limit	8,9
54	-LIM2	Input	Pos. End Limit	8,9
55	HMFL1	Input	Home-Flag	10
56	HMFL2	Input	Home-Flag	10
57	ORST/	Output	Reset Out	Indicator/Driver
58	AGND	Input	Analog Common	
59	A+15V/OPT+V	Input	Analog +15V Supply	
60	A-15V	Input	Analog -15V Supply	

The J8 connector is used to connect ACC-24P to its first 4 channels (Channels 1, 2, 3, and 4) of servo amps, flags, and encoders. On a non-Turbo PMAC, these would be considered Channels 9, 10, 11, and 12.

Note 1: In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry. However, if a terminal block is available on your version of PMAC, it is preferable to bring the +5V power in through the terminal block.

Note 2: Referenced to digital common (GND). Maximum of ± 12V permitted between this signal and its complement.

Note 3: Leave this input floating if not used (i.e. digital single-ended encoders). In this case, jumper (E18 - 21, E24 - 27) for channel should hold input at 2.5V.

Note 4: ± 10V, 10mA max, referenced to analog common (AGND).

Note 5: Leave floating if not used; do not tie to AGND. In this case, AGND is the return line.

Note 6: Functional polarity controlled by jumper(s) E17. Choice between AENA and DIR use controlled by Ix02 and Ix25.

Note 7: Functional polarity controlled by variable Ix25. Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software. Automatic fault function can be disabled with Ix25.

Note 8: Pins marked *-LIMn* should be connected to switches at the *positive* end of travel. Pins marked *+LIMn* should be connected to switches at the *negative* end of travel.

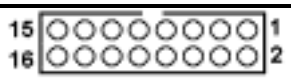
Note 9: Must be conducting to 0V (usually AGND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.

Note 10: Functional polarity for homing or other trigger use of HMFLn controlled by Encoder/Flag Variable 2 (I902, I907, etc.) HMFLn selected for trigger by Encoder/Flag Variable 3 (I903, I908, etc.). Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software.

J9 (JEQU) Position Compare Output Connector

J9 (JEQU)				
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	EQU1/	Output	Encoder 1 COMP-EQ	Low is TRUE
2	EQU2/	Output	Encoder 2 COMP-EQ	Low is TRUE
3	EQU3/	Output	Encoder 3 COMP-EQ	Low is TRUE
4	EQU4/	Output	Encoder 4 COMP-EQ	Low is TRUE
5	EQU5/	Output	Encoder 5 COMP-EQ	(1) Low is TRUE
6	EQU6/	Output	Encoder 6 COMP-EQ	(1) Low is TRUE
7	EQU7/	Output	Encoder 7 COMP-EQ	(1) Low is TRUE
8	EQU8/	Output	Encoder 8 COMP-EQ	(1) Low is TRUE
9	+V	Supply	Positive Supply	+5V to +24V
10	GND	Common	Digital Ground	
This connector provides the position-compare outputs for the eight encoder channels. (1). These signals only provided if Option 1 is ordered.				

JS1: First A/D Port Connector

JS1 (16-Pin Header)			 Front View	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	DCLK	Output	D to A, A to D Clock	DAC and ADC clock for Chan. 1, 2, 3, 4
2	BDATA1	Output	D to A Data	DAC Data for Chan. 1, 2, 3, 4
3	ASEL0/	Output	Chan. Select Bit 0	Select for Chan. 1, 2, 3, 4
4	ASEL1/	Output	Chan. Select Bit 1	Select for Chan. 1, 2, 3, 4
5	CNVRT01	Output	A to D Convert	ADC convert sig Chan. 1, 2, 3, 4
6	ADCIN1	Input	A to D Data	ADC data for Chan. 1, 2, 3, 4
7	OUT1/	Output	Amp Enable/Dir	Amp Enable input for Chan. 1
8	OUT2/	Output	Amp Enable/Dir	Amp Enable input for Chan. 2
9	OUT3/	Output	Amp Enable/Dir	Amp Enable input for Chan. 3
10	OUT4/	Output	Amp Enable/Dir	Amp Enable input for Chan. 4
11	HF41	Input	Amp Fault	Amp Fault input for Chan. 1
12	HF42	Input	Amp Fault	Amp Fault input for Chan. 2
13	HF43	Input	Amp Fault	Amp Fault input for Chan. 3
14	HF44	Input	Amp Fault	Amp Fault input for Chan. 4
15	+5V	Output	+5V Supply	Power supply out
16	GND	Common	PMAC Common	
ACC-28A/B connection; digital amplifier connection.				

JS1: Second A/D Port Connector (Option 1 required)

JS1 (16-Pin Header)			 Front View	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	DCLK	Output	D to A, A to D Clock	DAC and ADC clock for Chan. 5, 6, 7, 8
2	BDATA5	Output	D to A Data	DAC data for Chan. 5, 6, 7, 8
3	ASEL0/	Output	Chan. Select Bit 0	Select for Chan. 5, 6, 7, 8
4	ASEL1/	Output	Chan. Select Bit 1	Select for Chan. 5, 6, 7, 8
5	CNVRT05	Output	A to D Convert	ADC convert sig. Chan 5, 6, 7, 8
6	ADCIN5	Input	A to D Data	ADC data for Chan. 5, 6, 7, 8
7	OUT5/	Output	Amp Enable/Dir	Amp Enable/Dir for Chan. 5
8	OUT6/	Output	Amp Enable/Dir	Amp Enable/Dir for Chan. 6
9	OUT7/	Output	Amp Enable/Dir	Amp Enable/Dir for Chan. 7
10	OUT8/	Output	Amp Enable/Dir	Amp Enable/Dir for Chan. 8
11	HF45	Input	Amp Fault	Amp Fault input for Chan. 5
12	HF46	Input	Amp Fault	Amp Fault input for Chan. 6
13	HF47	Input	Amp Fault	Amp Fault input for Chan. 7
14	HF48	Input	Amp Fault	Amp Fault input for Chan. 8
15	+5V	Output	+5V Supply	Power supply OUT
16	GND	Common	PMAC Common	
ACC-28A/B connection; digital amplifier connection.				

P1: ISA Bus Connector

P1 is the standard 62-tooth card-edge ISA connector. If the ACC-24P is plugged into an ISA socket using this connector, only the power and return pins are used.

TB1: Standalone Power Supply Terminal Block

This terminal block can be used to provide the input for the power supply for the circuits on the ACC-24P board when it is not in a bus configuration. When the ACC-24P is in a bus configuration, these supplies automatically come through the bus connector from the bus power supply; in this case, this terminal block should not be used.

Pin #	Symbol	Function	Description	Notes
1	GND	Common	Reference Voltage	
2	+5V	Input	Digital Supply Voltage	Supplies all PMAC digital circuits
3	+12V	Input	Analog Positive Supply Voltage	E85, E87, E88 must be ON; no isolation from digital
4	-12V	Input	Analog Negative Supply Voltage	E85, E87, E88 must be ON; no isolation from digital