HI5905EVAL2 Evaluation Board User's Manual

Application Note | January 1999 | AN9785

Description

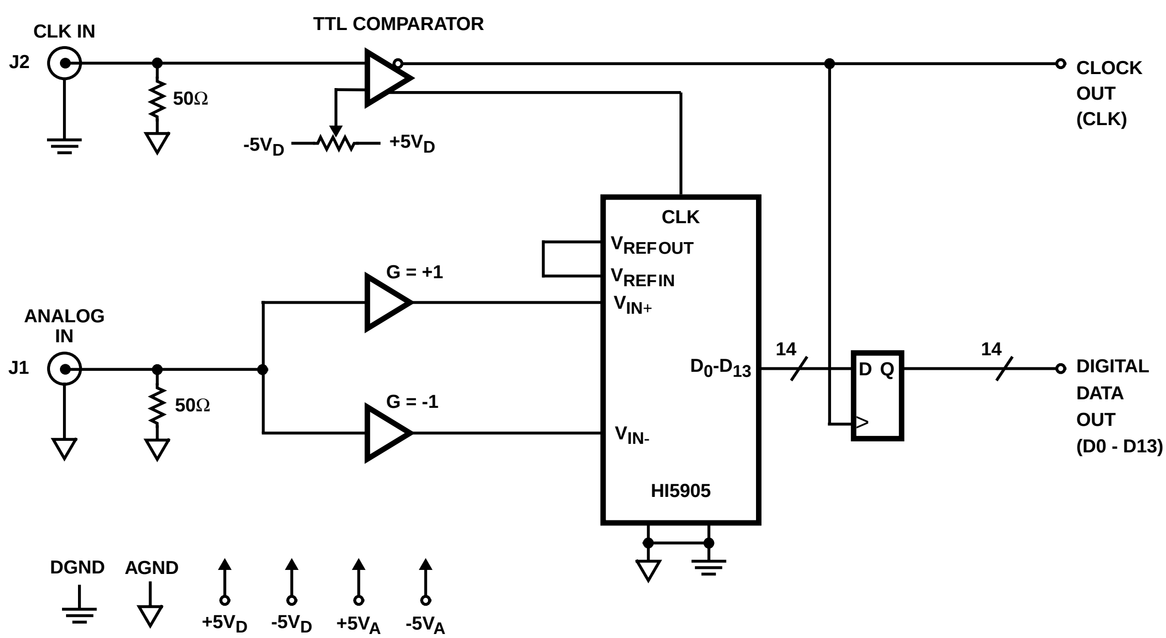
The HI5905EVAL2 evaluation board allows the circuit designer to evaluate the performance of the Intersil HI5905 monolithic 14-bit, 5MSPS analog-to-digital converter (ADC). As shown in the Evaluation Board Functional Block Diagram, the evaluation board includes sample clock generation circuitry, a single-ended to differential analog input amplifier configuration and digital data output latches/buffers. The buffered digital data outputs are conveniently provided for easy interfacing to a ribbon connector or logic probes. In addition, the evaluation board includes some prototyping area for the addition of user designed custom interfaces or circuits.

The sample clock generator circuit accepts the external sampling signal through an SMA type RF connector, J2. This input is AC-coupled and terminated in 50Ω allowing for connection to most laboratory signal generators. In addition, the duty cycle of the clock driving the A/D converter is adjustable by way of a potentiometer. This allows the effects of sample clock duty cycle on the HI5905 to be observed.

The analog input signal is also connected through an SMA type RF connector, J1, and applied to a single-ended to differential analog input amplifier. This input is AC-coupled and terminated in 50Ω allowing for connection to most laboratory signal generators. Also, provisions for a differential RC lowpass filter is incorporated on the output of the differential amplifier to limit the broadband noise going into the HI5905 converter.

The digital data output latches/buffers consist of a pair of 74ALS574A D-type flip-flops. With this digital output configuration the digital output data transitions seen at the I/O connector are essentially time aligned with the rising edge of the sampling clock.

Evaluation Board Functional Block Diagram



Reference Generator, V_{ROUT} and V_{RIN}

The HI5905 has an internal reference voltage generator, therefore no external reference voltage is required. The eval board, however, offers the ability to use the internal or an external reference. V_{ROUT} must be connected to V_{RIN} when using the internal reference. Internal to the converter, two reference voltages of 1.3V and 3.3V are generated making for a fully differential analog input signal range of ±2V.

The HI5905 can be used with an external reference. The converter requires only one external reference voltage connected to the V_{RIN} pin with V_{ROUT} left open. The evaluation board is configured with V_{ROUT} connected to V_{RIN} through a 0Ω resistor, R4. If it is desired to evaluate the performance of the converter utilizing an externally provided reference voltage, R4 can be removed and the alternate reference voltage can be brought in through twisted pair wire or coaxial cable. The latter would be the recommended method since it would provide the greatest immunity to externally coupled noise voltages. In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference input pin, V_{RIN}.

Analog Input

The fully differential analog input of the HI5905 A/D can be configured in various ways depending on the signal source and the required level of performance.

Differential Analog Input Configuration

A fully differential connection (Figure 1) will yield the best performance from the HI5905 A/D converter. Since the HI5905 is powered off a single +5V supply, the analog input must be biased so it lies within the analog input common mode voltage range of 1.0V to 4.0V. Figure 2 illustrates the differential analog input common mode voltage range that the converter will accommodate. The performance of the ADC does not change significantly with the value of the common mode voltage.

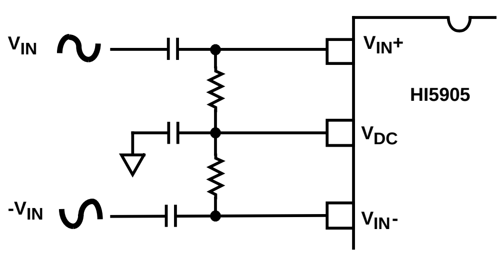


FIGURE 1. AC COUPLED DIFFERENTIAL INPUT

A 2.3V DC bias voltage source, V_{DC}, half way between the top and bottom internally generated reference voltages, is made available to the user to help simplify circuit design when using a differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the analog input common mode voltage range over temperature. The DC voltage source has a temperature coefficient of about +200ppm/^{o}C.

The difference between the converter's two internally generated voltage references is 2V. For the AC coupled differential input (Figure 1), if V_{IN} is a $2V_{P-P}$ sinewave with $-V_{IN}$ being 180 degrees out of phase with V_{IN}, the converter will be at positive full scale when the $V_{IN}+$ input is at V_{DC} + 1V and the $V_{IN}-$ input is at V_{DC} - 1V ($V_{IN}+$ - $V_{IN}-$ = +2V). Conversely, the ADC will be at negative full scale when the $V_{IN}+$ input is equal to V_{DC} - 1V and $V_{IN}-$ is at V_{DC} + 1V ($V_{IN}+$ - $V_{IN}-$ = -2V).

It should be noted that overdriving the analog input beyond the ±2.0V fullscale input voltage range will not damage the converter as long as the overdrive voltage stays within the converters analog supply voltages. In the event of an overdrive condition the converter will recover within one sample clock cycle.

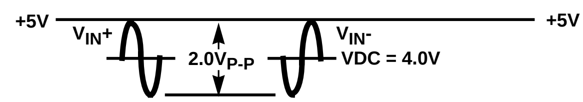


FIGURE 2A.

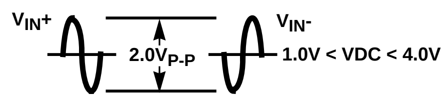


FIGURE 2B.

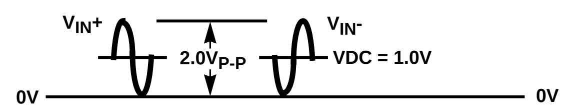


FIGURE 2C.

FIGURE 2. DIFFERENTIAL ANALOG INPUT COMMON MODE VOLTAGE RANGE

Evaluation Board Layout and Power Supplies

The HI5905 evaluation board is a four layer board with a layout optimized for the best performance of the ADC. This application note includes an electrical schematic of the evaluation board, a component parts list, a component placement layout drawing and reproductions of the various board layers used in the board stack-up. The user should feel free to copy the layout in their application. Refer to the component layout and the evaluation board electrical schematic for the following discussions.

The HI5905 monolithic A/D converter has been designed with separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The evaluation board provides separate low impedance analog and digital ground planes on layer 2. Since the analog and digital ground planes are connected together at a single point where the power supplies enter the board, **DO NOT** tie them together back at the power supplies.

The analog and digital supplies are also kept separate on the evaluation board and should be driven by clean linear regulated supplies. The external power supplies are hooked up with the twisted pair wires soldered to the plated through holes marked +5VAIN, +5VAIN1, -5VAIN, +5VDIN, +5VD1IN, +5VD2IN, -5VDIN, AGND and DGND near the analog prototyping area. +5VDIN, +5VD1IN, +5VD2IN and -5VDIN are digital supplies and are returned to DGND. +5VAIN, +5VAIN1 and -5VAIN are the analog supplies and are returned to AGND. Table 1 lists the operational supply voltages, typical current consumption and the evaluation board circuit function being powered. Single supply operation of the converter is possible but the overall performance of the converter may degrade.

TABLE 1. HI5905EVAL2 EVALUATION BOARD POWER SUPPLIES

POWER SUPPLY	NOMINAL VALUE	CURRENT (TYP)	FUNCTION(S) SUPPLIED
+5VAIN	5.0V ±5%	80mA	Op Amps, A/D AV_{CC}
-5VAIN	-5.0V ±5%	30mA	Op Amps
+5VDIN	5.0V ±5%3	60mA	CLK Comparator, Inverter D0-D13 D-FF's
+5VD1IN	5.0V ±5%	14mA	A/D DV_{CC1}
+5VD2IN	5.0V ±5%	6mA	A/D DV_{CC2}
-5VDIN	-5.0V ±5%	3mA	CLK Comparator

Sample Clock Driver, Timing and I/O

In order to ensure rated performance of the HI5905, the duty cycle of the sample clock should be held at 50% ±5%. It must also have low phase noise and operate at standard TTL levels.

A voltage comparator (U3) with TTL output levels is provided on the evaluation board to generate the sampling clock for the HI5905 when a sinewave (< ±3V) or squarewave clock is applied to the CLK input (J2) of the evaluation board. A potentiometer (VR1) is provided to allow the user to adjust the duty cycle of the sampling clock to obtain the best performance from the ADC and to allow the user to investigate the effects of expected duty cycle variations on the performance of the converter. The HI5905 clock input trigger level is approximately 1.5V. Therefore, the duty cycle of the sampling clock should be measured at this 1.5V trigger level. Test point TP2 provides a convenient point to monitor the sample clock duty cycle and make any required adjustments.

Figure 3 shows the sample clock and digital data timing relationship for the evaluation board. The data corresponding to a particular sample will be available at the digital data outputs of the HI5905 after the data latency time, t_{LAT}, of 4 sample clock cycles plus the HI5905 digital data output delay, t_{OD}. Table 2 lists the values that can be expected for the indicated timing delays. Refer to the HI5905 data sheet for additional timing information.

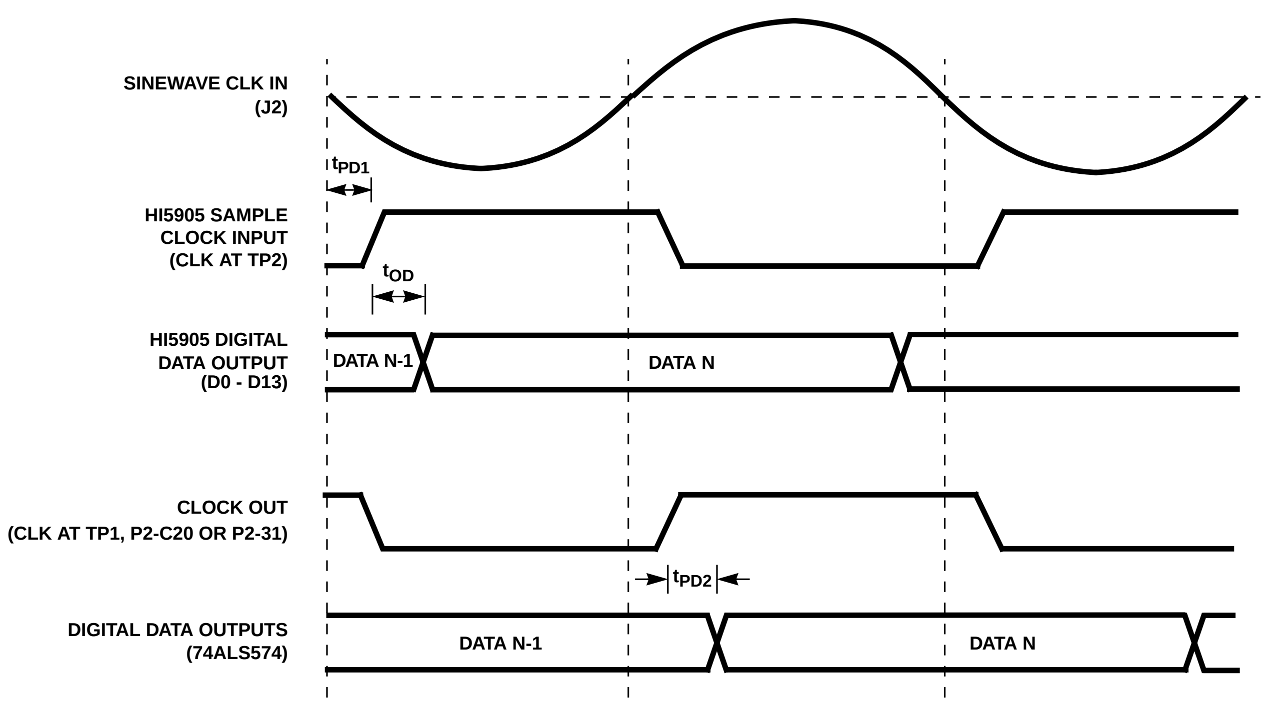


FIGURE 3. EVALUATION BOARD CLOCK AND DATA TIMING RELATIONSHIPS

TABLE 2. TIMING SPECIFICATIONS

PARAMETER	DESCRIPTION	TYP
t_{OD}	HI5905 Digital Output Data Delay	50ns
t_{PD1}	U4 Prop Delay	4.5ns
t_{PD2}	U2/3 Prop Delay	9ns

The sample clock and digital output data signals are made available through two connectors contained on the evaluation board. The line buffering provided by the data output latches allows for driving long leads or analyzer inputs. These data latches are not necessary for the digital output data if the load presented to the converter does not exceed the data sheet load limits of 100µA and 15pF. The P2 I/O connector allows the evaluation board to be interfaced to the DSP evaluation boards available from Intersil. Alternatively, the digital output data and sample clock can also be accessed by clipping the test leads of a logic analyzer or data acquisition system onto the I/O pins of connector header P1.

HI5905 Performance Characterization

Dynamic testing is used to evaluate the performance of the HI5905 A/D converter. Among the tests performed are Signal-to-Noise and Distortion Ratio (SINAD), Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD), Spurious Free Dynamic Range (SFDR) and InterModulation Distortion (IMD).

Figure 4 shows the test system used to perform dynamic testing on high-speed ADCs at Intersil. The clock (CLK) and analog input (V_{IN}) signals are sourced from low phase noise HP8662A synthesized signal generators that are phase locked to each other to ensure coherence. The output of the signal generator driving the ADC analog input is bandpass filtered to improve the harmonic distortion of the analog input signal. The comparator on the evaluation board will convert the sine wave CLK input signal to a square wave at TTL logic levels to drive the sample clock input of the HI5905. The ADC data is captured by a logic analyzer and then transferred over the GPIB bus to the PC. The PC has the required software to perform the Fast Fourier Transform (FFT) and do the data analysis.

Coherent testing is recommended in order to avoid the inaccuracies of windowing. The sampling frequency and analog input frequency have the following relationship: $F_I/F_S = M/N$, where F_I is the frequency of the input analog sinusoid, F_S is the sampling frequency, N is the number of samples, and M is the number of cycles over which the samples are taken. By making M an integer and odd number (1, 3, 5, ...) the samples are assured of being nonrepetitive.

Refer to the HI5905 data sheet for a complete list of test definitions and the results that can be expected using the evaluation board with the test setup shown. Evaluating the part with a reconstruction DAC is only suggested when doing bandwidth or video testing.

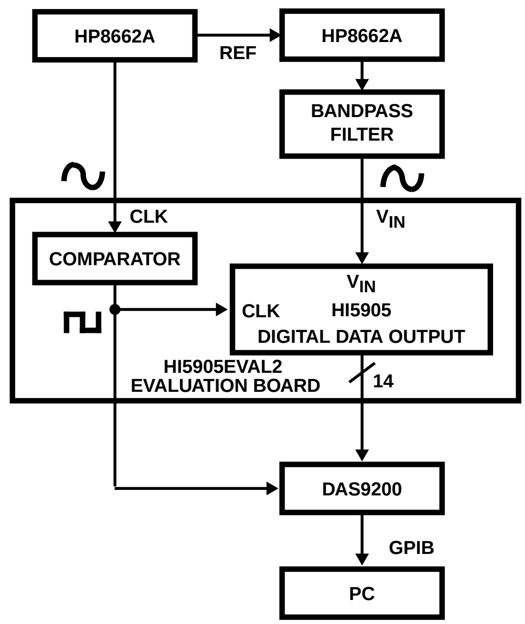


FIGURE 4. HIGH-SPEED A/D PERFORMANCE TEST SYSTEM

HI5905EVAL2 Typical Performance (Input Amplitude at -0.5dBFS)

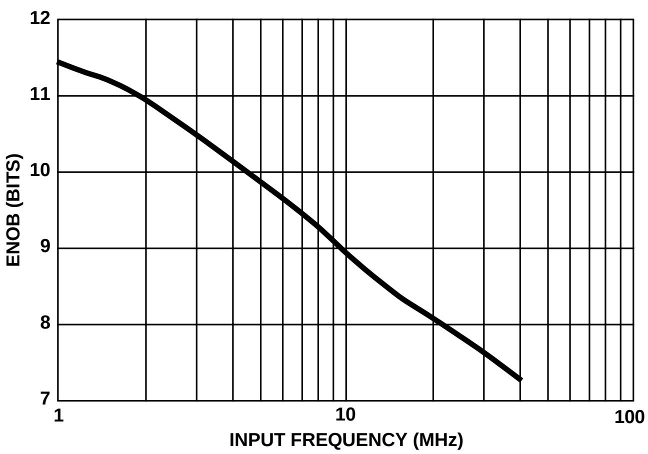


FIGURE 5. EFFECTIVE NUMBER OF BITS (ENOB) vs INPUT FREQUENCY

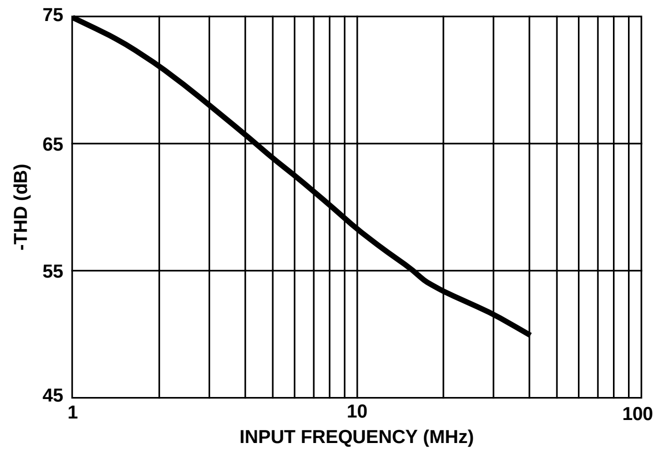


FIGURE 6. TOTAL HARMONIC DISTORTION (THD) vs INPUT FREQUENCY

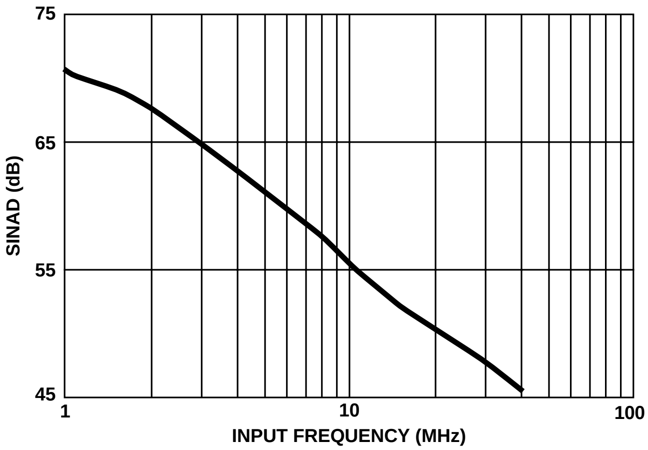


FIGURE 7. SINAD vs INPUT FREQUENCY

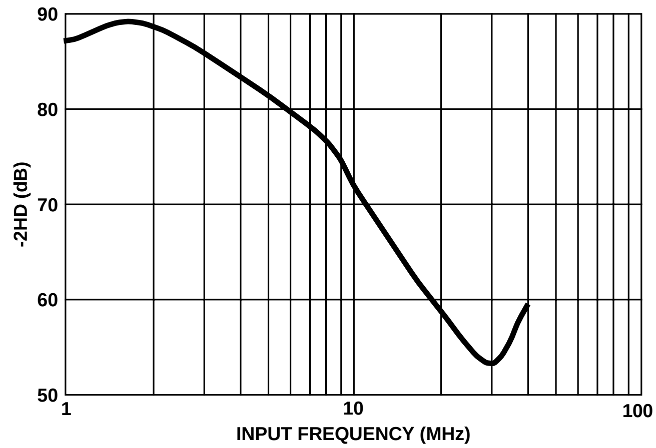


FIGURE 8. SECOND HARMONIC DISTORTION (2HD) vs INPUT FREQUENCY

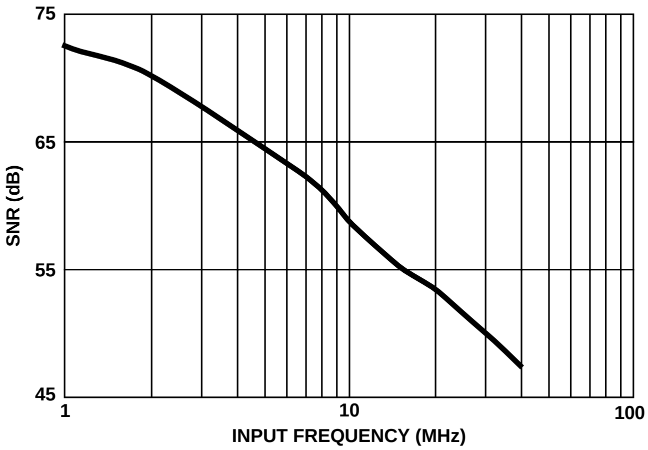


FIGURE 9. SNR vs INPUT FREQUENCY

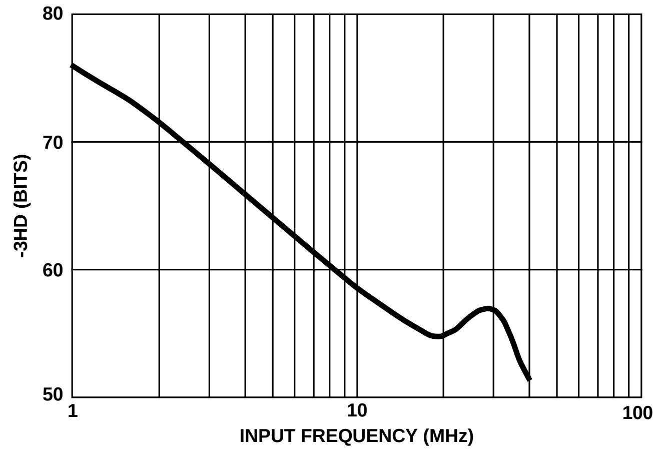


FIGURE 10. THIRD HARMONIC DISTORTION (3HD) vs INPUT FREQUENCY

Appendix A Board Layout

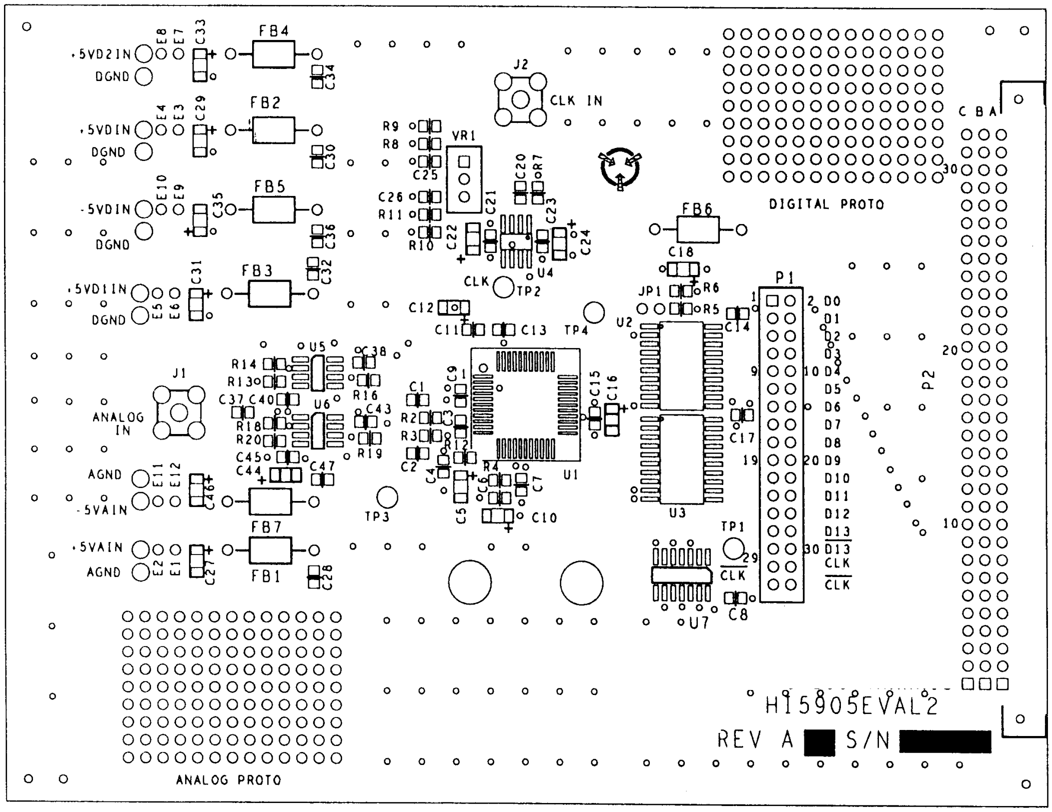


FIGURE 11. HI5905EVAL2 EVALUATION BOARD PARTS LAYOUT (NEAR SIDE)

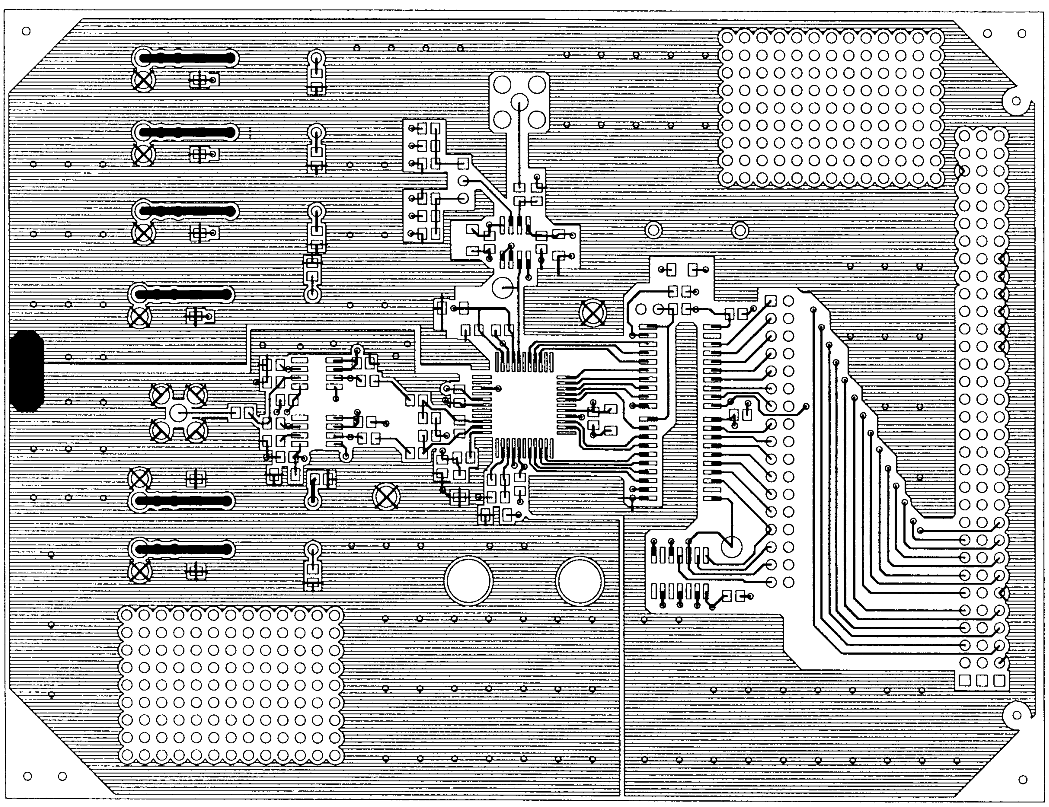


FIGURE 12. HI5905EVAL2 EVALUATION BOARD COMPONENT NEAR SIDE (LAYER 1)

Appendix A Board Layout (Continued)

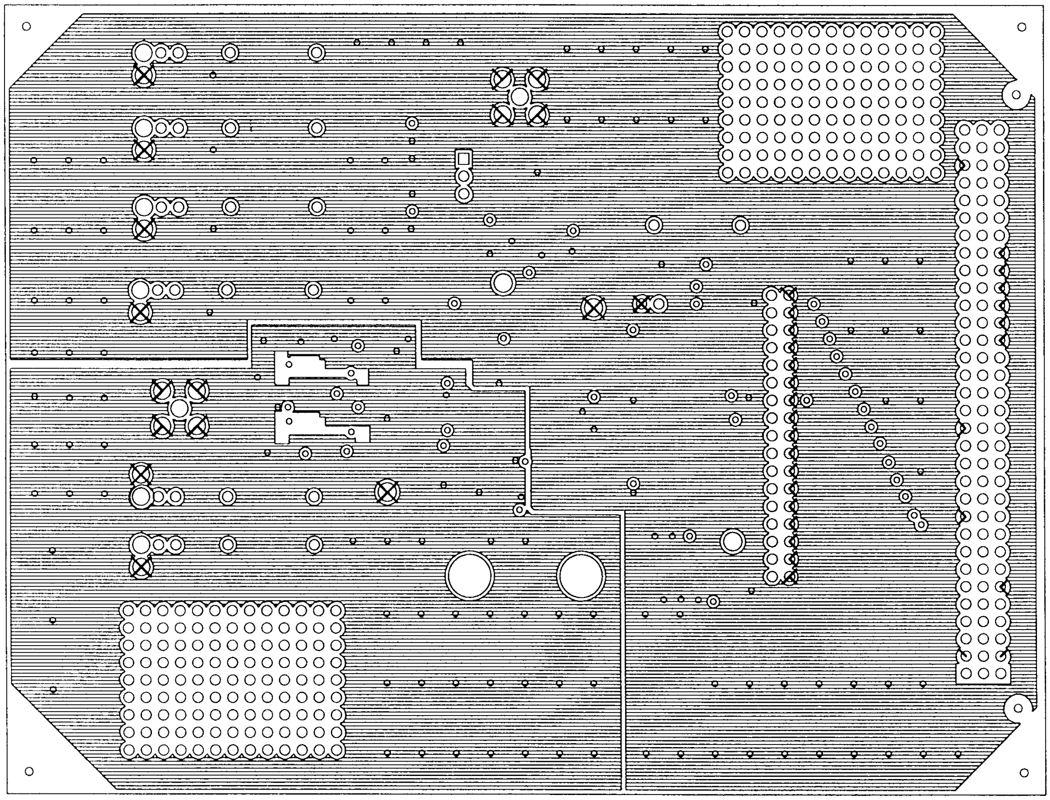


FIGURE 13. HI5905EVAL2 EVALUATION BOARD GROUND PLANE LAYER (LAYER 2)

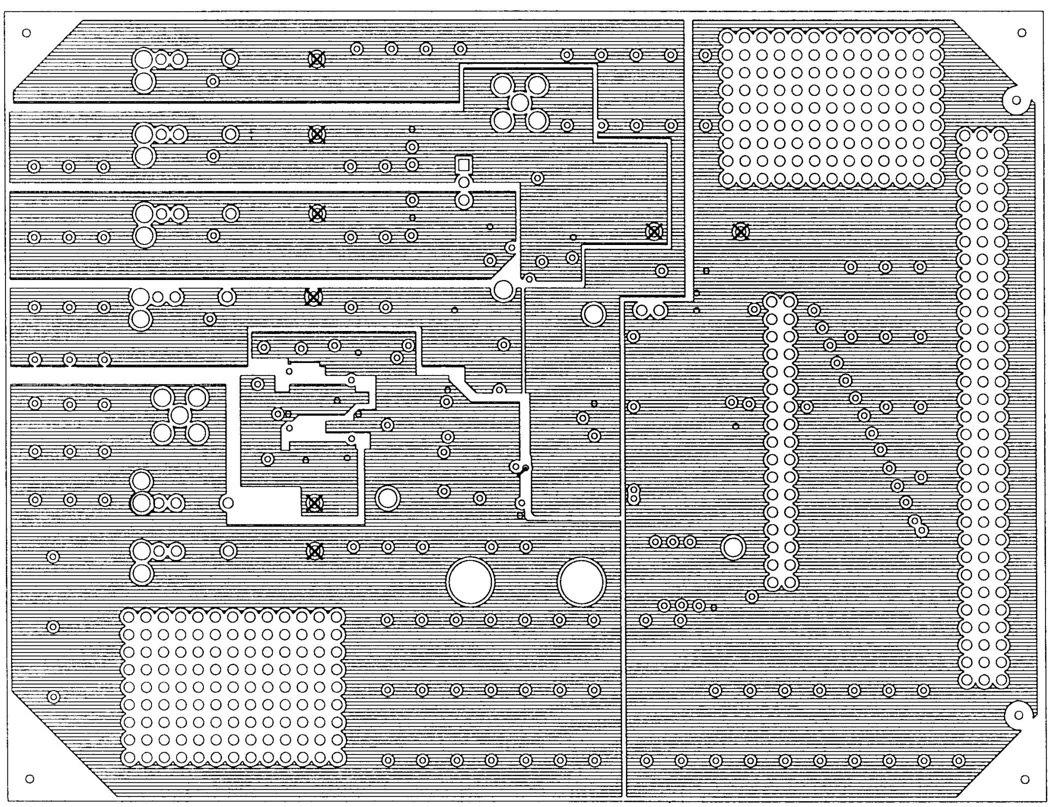


FIGURE 14. HI5905EVAL2 EVALUATION BOARD POWER PLANE LAYER (LAYER 3)

Appendix A Board Layout (Continued)

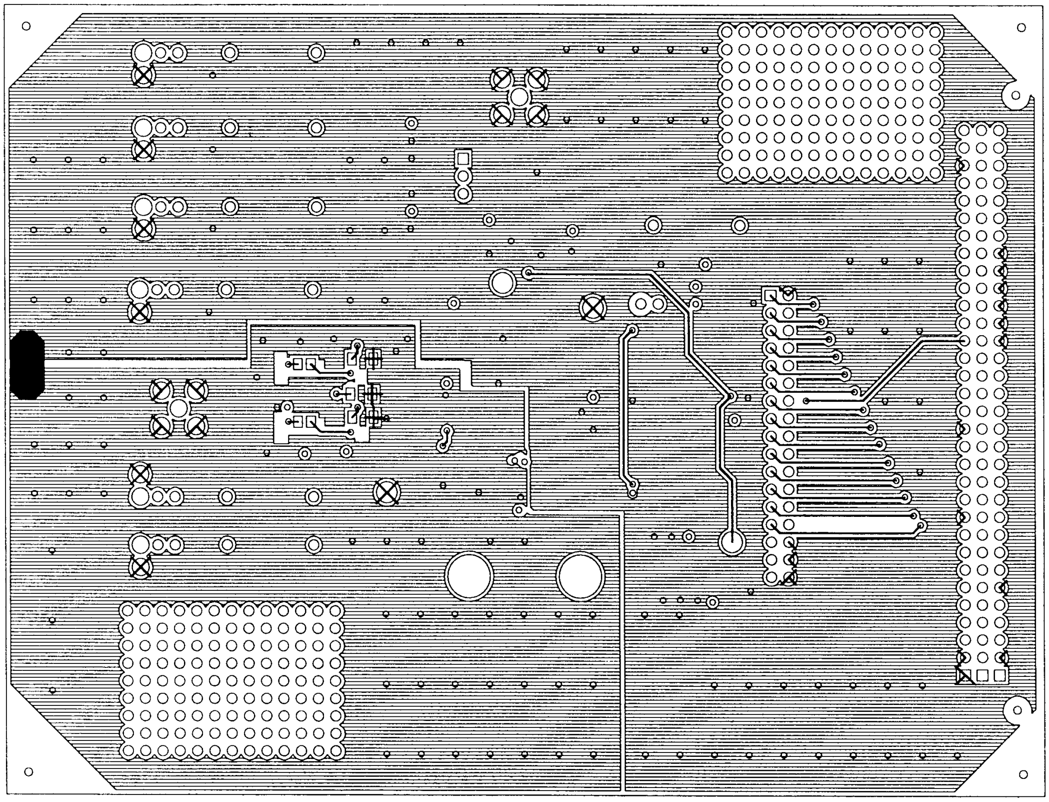


FIGURE 15. HI5905EVAL2 EVALUATION BOARD COMPONENT FAR SIDE (LAYER 4)

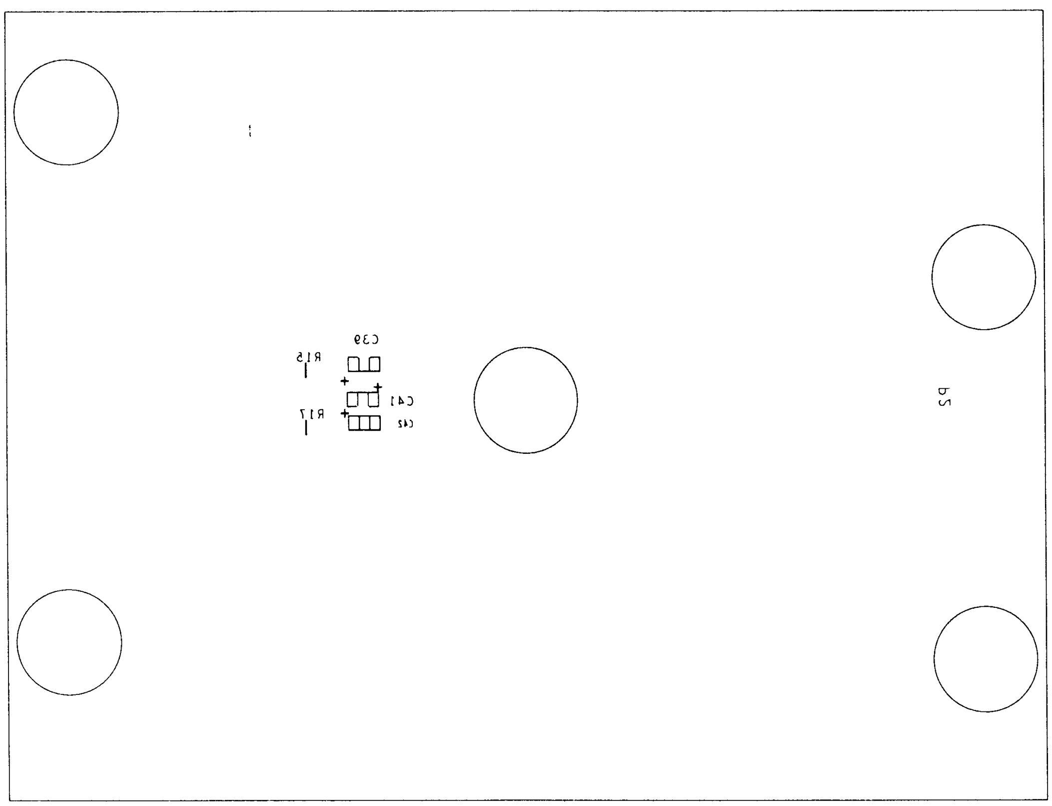
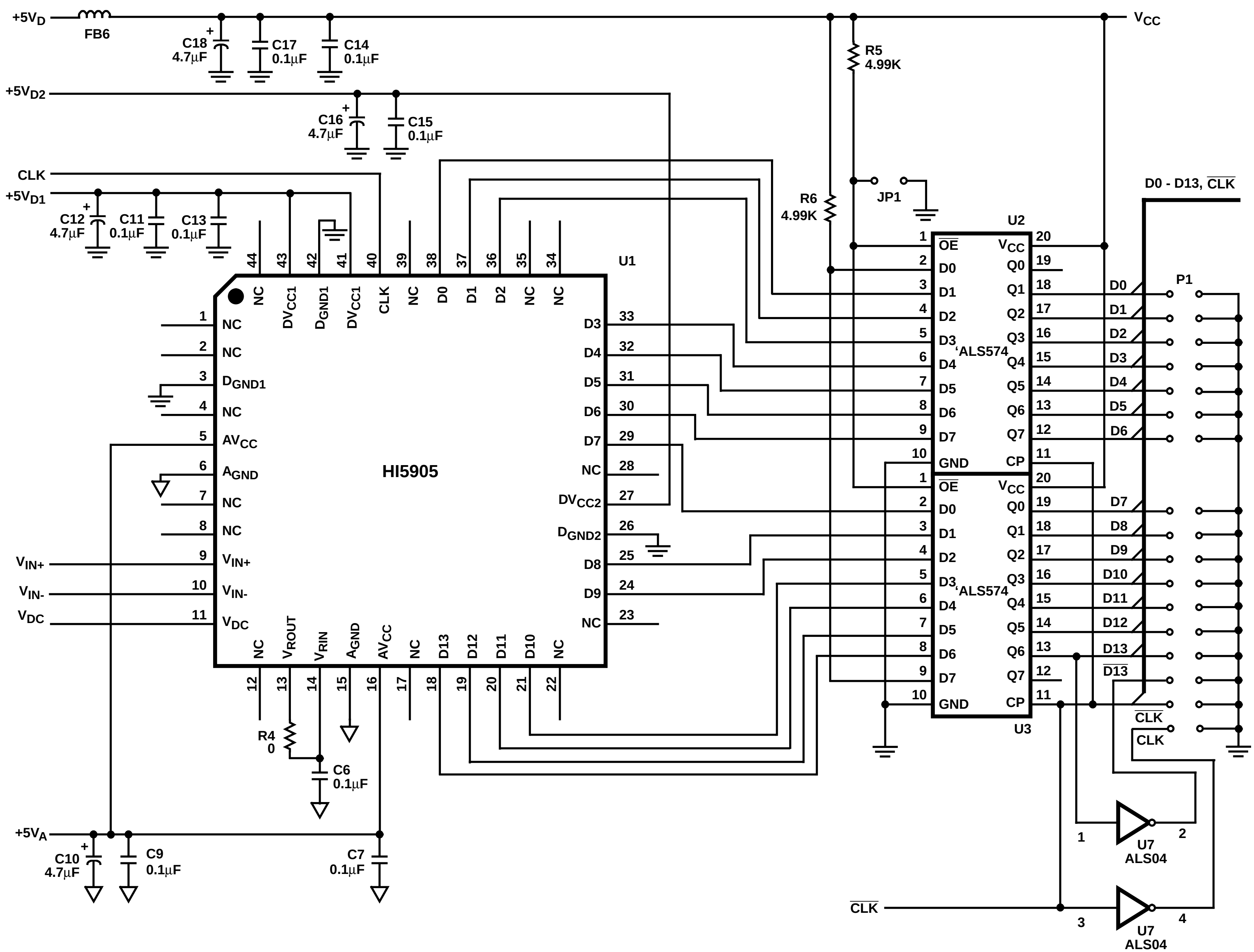
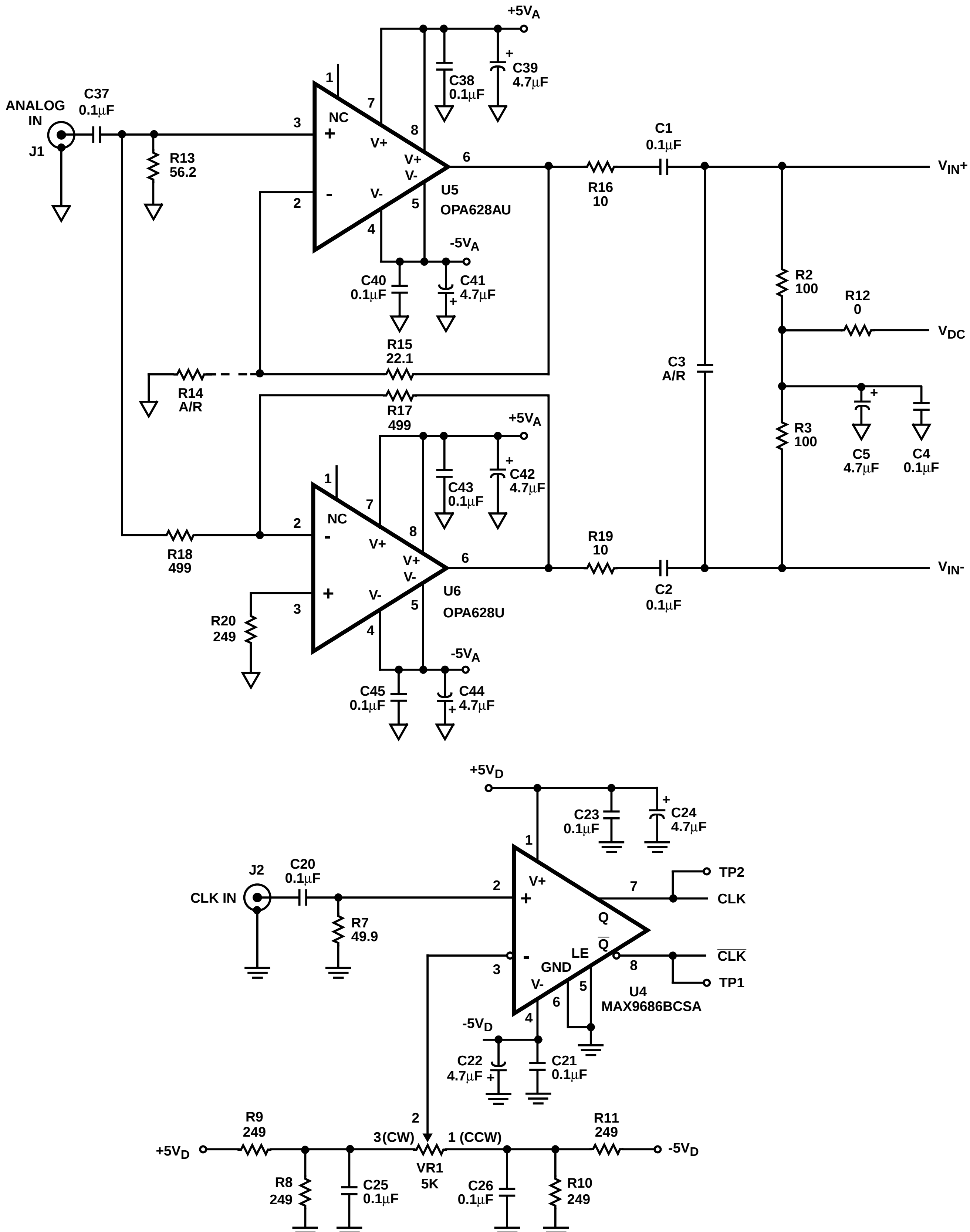


FIGURE 16. HI5905EVAL2 EVALUATION BOARD PARTS LAYOUT (FAR SIDE)

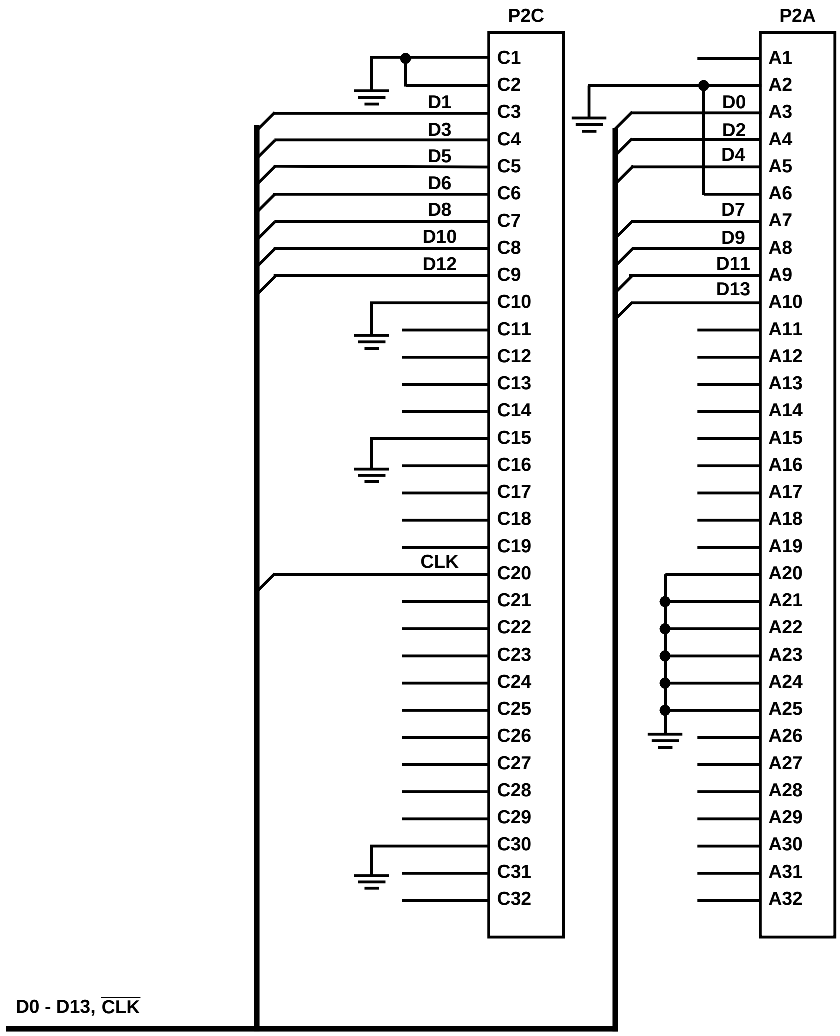
Appendix B Schematic Diagrams

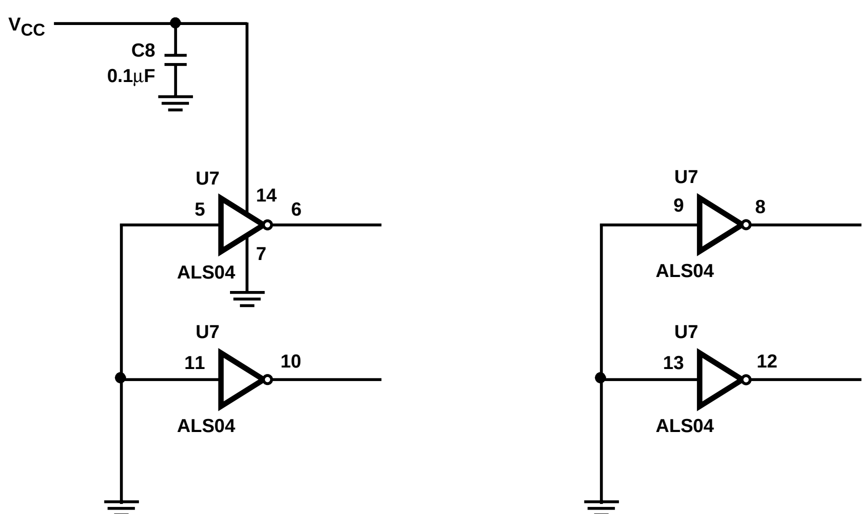


Appendix B Schematic Diagrams (Continued)

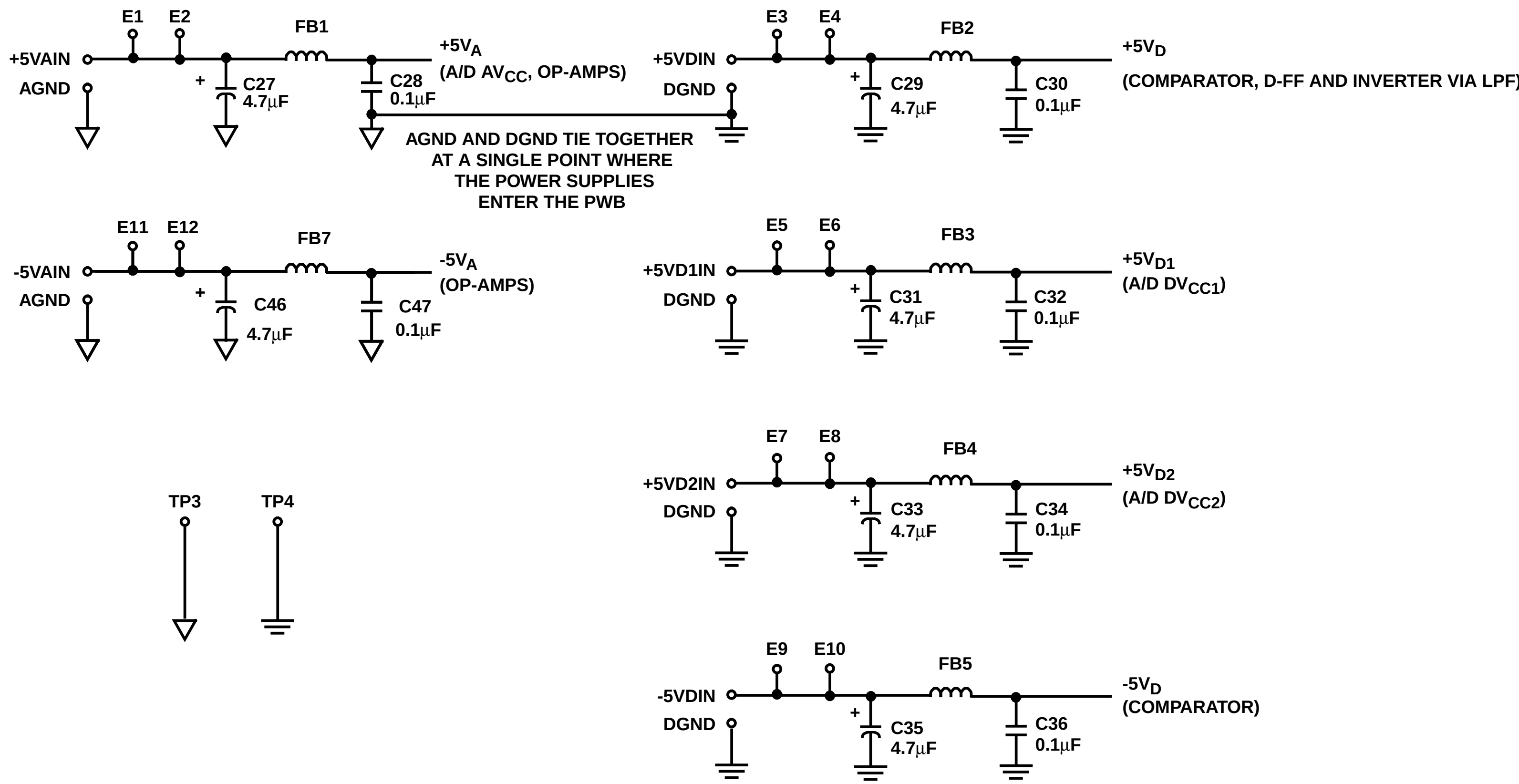


Appendix B Schematic Diagrams (Continued)





Appendix B Schematic Diagrams (Continued)



Appendix C Parts List

REFERENCE DESIGNATOR	QTY	DESCRIPTION
-	**1**	Printed Wiring Board
R16, R19	2	10Ω, 1/10W 805 Chip, 1%
R17, R18	2	499Ω, 1/10W 805 Chip, 1%
R13	1	56.2Ω, 1/10W 805 Chip, 1%
R14	1	A/RΩ, 1/10W 805 Chip, 1%
R15	1	22.1Ω, 1/10W 805 Chip, 1%
R2, R3	2	100Ω, 1/10W 805 Chip, 1%
R4, R12	2	0.0Ω, 1/4W 805 Chip, 5%
R5, R6	2	4.99kΩ, 1/10W 805 Chip, 1%
R7	1	49.9Ω, 1/10W 805 Chip, 1%
R8, R9, R10, R11, R20	5	249Ω, 1/10W 805 Chip, 1%
VR1	1	5kΩ Trim Pot
C5, C10, C12, C16, C18, C22, C24, C27, C29, C31, C33, C35, C39, C41, C42, C44, C46	17	4.7µF Chip Tant Cap, 10WVDC, 20%, EIA Case A
C1, C2, C4, C6, C7, C8, C9, C11, C13, C14, C15, C17, C20, C21, C23, C25, C26, C28, C30, C32, C34, C36, C37, C38, C40, C43, C45, C47	28	0.1µF Cer Cap, 50WVDC, 10%, 805 Case, Y5V Dielectric
C3	1	A/R pF Cer Cap, 50WVDC, 10%, 805 Case
FB1-7	7	10µH Ferrite Bead
J1, J2	2	SMA Straight Jack PCB Mount
-	5	Protective Bumper
JP1	1	1x2 Header
JPH1	1	1x2 Header Jumper
P1	1	2x17 Header
TP1, 2, 3, 4	4	Test Point
U1	1	Intersil HI5905IN, 14-Bit 5 MSPS A/D Converter
U4	1	Ultrafast Voltage Comparator
U2, U3	2	Octal D-type Flip-flop
U5, U6	2	Op-amp
U7	1	Hex Inverter
P2		64-Pin Eurocard RT Angle Receptacle

Appendix D HI5905 Theory of Operation

The HI5905 is a 14-bit fully differential sampling pipelined A/D converter with digital error correction. Figure 17 depicts the internal circuit for the converters front-end differential-in-differential-out sample-and-hold (S/H). The sampling switches are controlled by internal sampling clock signals which consist of two phase non-overlapping clock signals, $\phi 1$ and $\phi 2$, derived from the master clock (CLK) driving the converter. During the sampling phase, $\phi 1$, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of $\phi 1$ the input analog signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, $\phi 2$, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op amp output nodes. The charge then redistributes between C_S and C_H, completing one sample-and-hold cycle. The output of the sample-and-hold is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function, but can also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of the switches and C_S. The relatively small values of these components result in a typical full power input bandwidth of 100MHz for the converter.

As illustrated in the HI5905 Functional Block Diagram and the timing diagram contained in Figure 18, three identical pipeline subconverter stages, each containing a four-bit flash converter, a four-bit digital-to-analog converter and an amplifier with a voltage gain of 8, follow the S/H circuit with the fourth stage being only a 4-bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual sub-converter clock signal is offset by 180 degrees from the previous stage clock signal, with the result that alternate stages in the pipeline will perform the same operation. The output of each of the three identical four-bit subconverter stages is a four-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal clock. The function of the digital delay line is to time align the digital outputs of the three identical four-bit subconverter stages with the corresponding output of the fourth stage flash converter before inputting the sixteen bit result into the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final fourteen-bit digital data output (D0-D14) of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is presented on the digital data output bus on the 4th cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding analog sample is output on the following clock pulse. The output data is synchronized to the external sampling clock with a data latch and is presented in offset binary format.

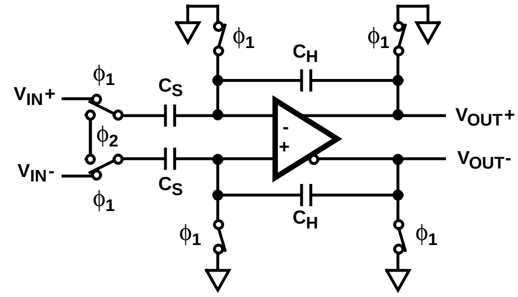
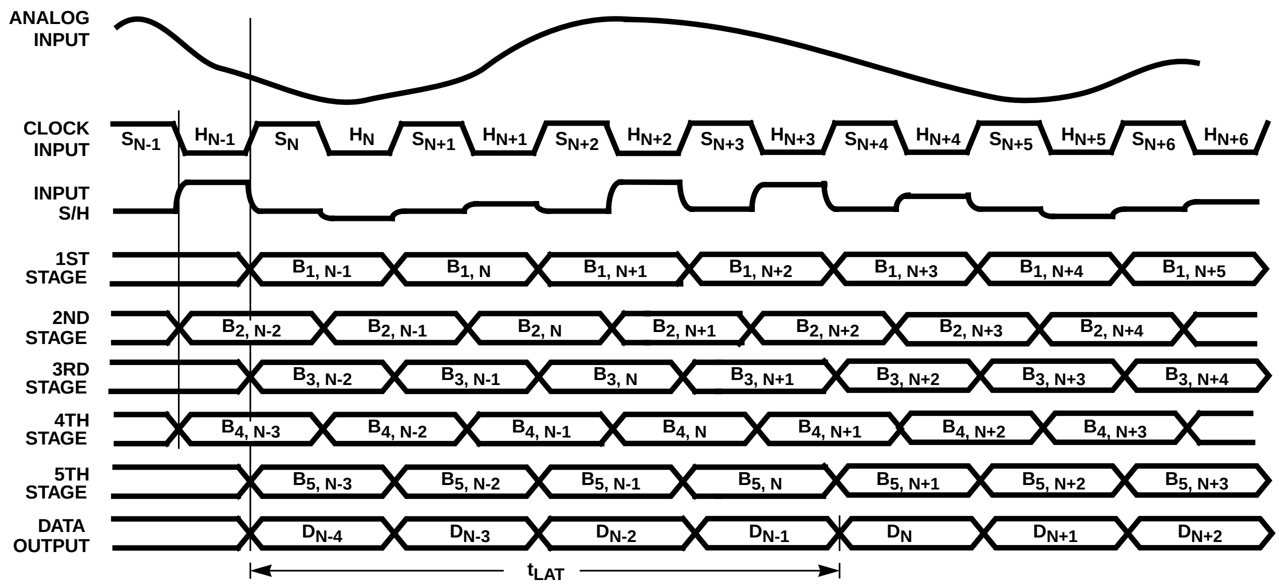


FIGURE 17. ANALOG INPUT SAMPLE-AND-HOLD

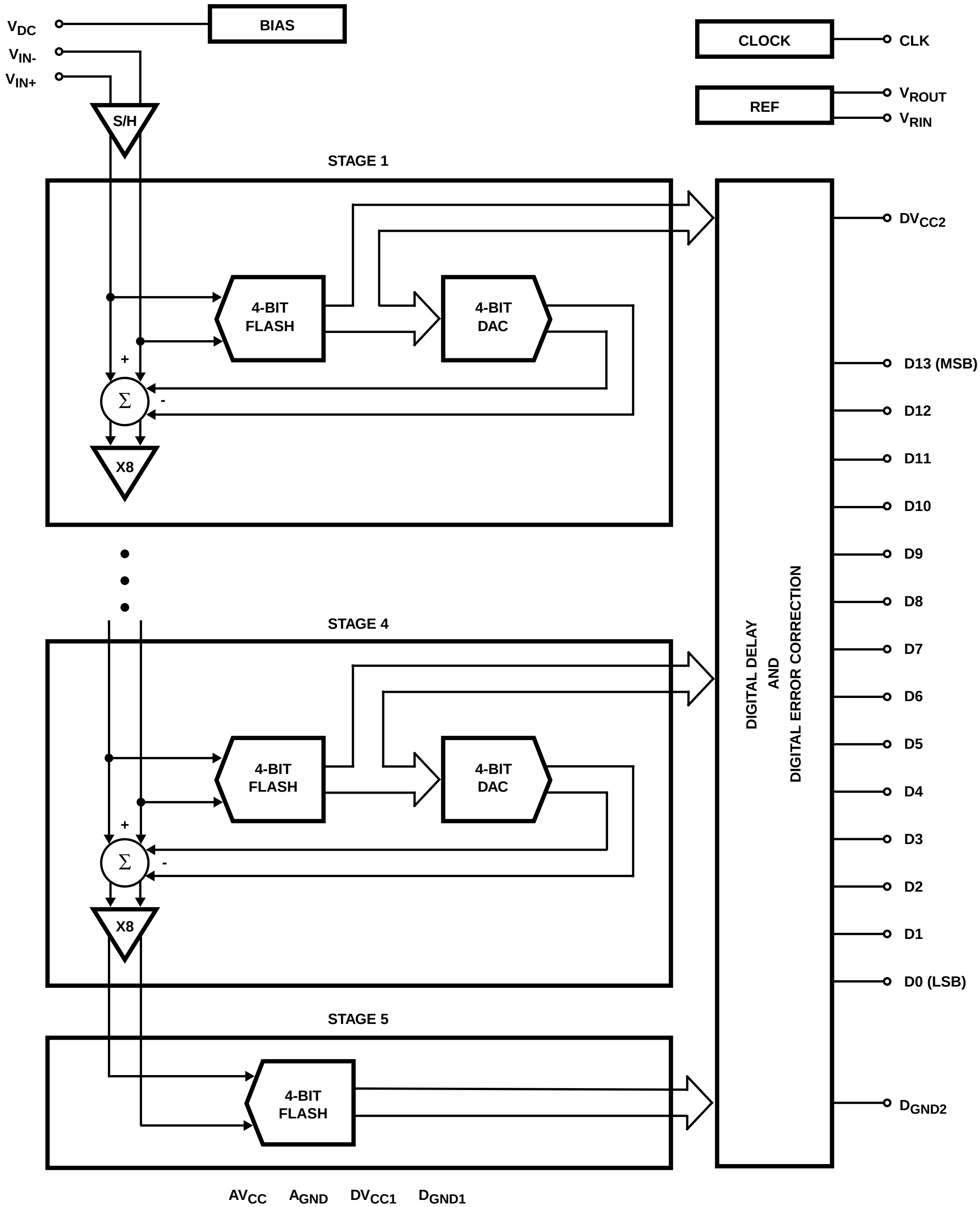


NOTES:

1. S_N: N-th sampling period.
2. H_N: N-th holding period.
3. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
4. D_N: Final data output corresponding to N-th sampled input.

FIGURE 18. HI5905 INTERNAL CIRCUIT TIMING

HI5905 Functional Block Diagram



Appendix E Pin Descriptions

PIN #	NAME	DESCRIPTION
1	NC	No Connection
2	NC	No Connection
3	D_{GND1}	Digital Ground
4	NC	No Connection
5	AV_{CC}	Analog Supply (5.0V)
6	A_{GND}	Analog Ground
7	NC	No Connection
8	NC	No Connection
9	$V_{IN}+$	Positive Analog Input
10	$V_{IN}-$	Negative Analog Input
11	V_{DC}	DC Bias Voltage Output
12	NC	No Connection
13	V_{ROUT}	Reference Voltage Output
14	V_{RIN}	Reference Voltage Input
15	A_{GND}	Analog Ground
16	AV_{CC}	Analog Supply (5.0V)
17	NC	No Connection
18	D13	Data Bit 13 Output (MSB)
19	D12	Data Bit 12 Output
20	D11	Data Bit 11 Output
21	D10	Data Bit 10 Output
22	NC	No Connection

PIN #	NAME	DESCRIPTION
23	NC	No Connection
24	D9	Data Bit 9 Output
25	D8	Data Bit 8 Output
26	D_{GND2}	Digital Ground
27	DV_{CC2}	Digital Supply (5.0V)
28	NC	No Connection
29	D7	Data Bit 7 Output
30	D6	Data Bit 6 Output
31	D5	Data Bit 5 Output
32	D4	Data Bit 4 Output
33	D3	Data Bit 3 Output
34	NC	No Connection
35	NC	No Connection
36	D2	Data Bit 2 Output
37	D1	Data Bit 1 Output
38	D0	Data Bit 0 Output (LSB)
39	NC	No Connection
40	CLK	Input Clock
41	DV_{CC1}	Digital Supply (5.0V)
42	D_{GND1}	Digital Ground
43	DV_{CC1}	Digital Supply (5.0V)
44	NC	No Connection