Series PMC408 PCI Mezzanine Card
32-Channel Digital I/O Module

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The PCI Mezzanine Card (PMC) Series PMC408 is a 32-channel combination digital input/output board. This model supports both 0 to 60V DC inputs, and 60VDC low-side switch outputs, in any combination up to 32 channels. As a combination input/output module, input channels on this model can be used for “loopback” monitoring of the output channel states. Up to 8 input channels can be programmed to generate Change-Of-State (COS), Low, or High level transition interrupts. The PMC408 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its high channel density and is an ideal choice for a wide range of industrial control and monitor applications that require high-density, high-reliability, and high-performance at a low cost.

The PMC408 module is available in standard and extended temperature ranges as follows;

MODEL	OPERATING TEMPERATURE RANGE
PMC408	**0 to +70°C**
PMC408E	**-40 to +85°C**

KEY PMC408 FEATURES

- **High Channel Count** - Interfaces with up to 32 input/output points. Input and output channels may be intermixed in any combination. The input circuitry of a single channel can also be used to monitor the output state of the same channel to efficiently implement “loopback” output control.
- **TTL-Compatible Input Threshold** - Input threshold is at TTL levels and includes hysteresis.
- **Input Hysteresis** - Buffered inputs include hysteresis for increased noise immunity.
- **Programmable Change-of-State/Level Interrupts -** Interrupts are software programmable for any bit Change-Of-State or level on up to 8 channels.
- **Loopback Output Control & Fault Diagnostics** - Input and output circuitry is connected in tandem to each I/O channel, making it directly compatible for “loopback monitoring” of the output channel states. This feature can also be used to

implement self-test or fault diagnosis, since inherent loopback can be used to detect open output switches or shorts.

- **High Voltage Inputs & Outputs** - Inputs and outputs are rated to 60VDC. I/O channels are non-isolated and share a common connection.
- **High Impedance Inputs** - High impedance inputs minimize loading of the input source and input current.
- **No Configuration Jumpers or Switches** - All configuration is performed through software commands with no internal jumpers to configure or switches to set.
- **Power Up & System Reset is Failsafe** - For safety, the outputs are always OFF upon power-up and cleared after a system reset. Unlike some competitive units, output gate pulldowns are included to ensure that the outputs do not turn on momentarily when output load power is applied with no power to the IP module.
- **True Logic** - Outputs operate using True-Logic (1=ON/SWITCH CLOSED, 0=OFF/SWITCH OPEN).
- **Low R_{dsON} (0.2Ω Maximum)-** Low output drain-to-source ON resistance ensures TTL logic-low compatibility at high currents and reduces power dissipation.
- **High Output Current** - individual output channels may sink up to 1A DC continuous (up to 10A total, all channels combined), or 312mA DC (with all 32 channels ON). No deration of maximum output current is required at elevated ambient temperatures.

PCI MEZZANINE CARD INTERFACE FEATURES

- **High density -** Single-width PMC Target module.
- **Field Connections –** All digital inputs/outputs (channels 0 – 31) and common connections are made through a single 50-pin SCSI-2 front panel I/O connector.
- **16-bit I/O** - Channel register Read/Write is performed through through 32-bit, 16-bit or 8-bit data transfer cycles in the PCI memory space.
- **Compatibility** – IEEE P1386.1 compliant PMC module which complies to PCI Local Bus Specification Revision 2.2. Provides one multifunction interrupt. 5V signaling compliant and 3.3V signaling tolerant.

SIGNAL INTERFACE PRODUCTS
(See Appendix for more information on compatible products)

This PMC Module will mate directly to any standard PMC carrier/CPU board that supports one single width PMC mezzanine module. Once connected, the module is accessed via a 50 pin front panel connector.

The cables and termination panels, described in the following paragraphs, are also available. For optimum performance with the PMC408 digital I/O module, use of the shortest possible length of shielded I/O cable is recommended.

Cables:

Model 5025-187 (SCSI-2 to Flat Ribbon Cable, Shielded): A round 50 conductor shielded cable with a male SCSI-2 connector at one end and a flat female ribbon connector at the other end. The cable is used for connecting the PMC408 module to Model 5025-552 termination panels.

Termination Panel:

Model 5025-552: DIN-rail mountable panel provides 50 screw terminals for universal field I/O termination. Connects to Acromag PMC408, via SCSI-2 to Flat Ribbon Cable, Shielded (Model 5028-187).

PMC MODULE ActiveX CONTROL SOFTWARE

Acromag provides a software product (sold separately) consisting of PMC module ActiveX (Object Linking and Embedding) controls for Windows 98, 95®, ME, 2000 and Windows NT® compatible application programs (Model PMCSW- ATX, MSDOS format). This software provides individual controls that allow Acromag PMC modules to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Microsoft® Office® 97 applications and others. The ActiveX controls provide a high-level interface to PMC modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the ActiveX controls. These functions consist of an ActiveX control for each Acromag PMC module.

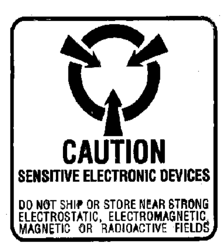
PMC MODULE VxWORKS SOFTWARE

Acromag provides a software product (sold separately) consisting of PMC module VxWorks® libraries. This software (Model PMCSW-API-VXW, MSDOS format) is composed of VxWorks® (real time operating system) libraries for all Acromag PMC modules. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PMC modules.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.



For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the PMC modules to the carrier/CPU board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing PMC modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-859 and your PMC module documentation for configuration and assembly instructions. Model PMC408 I/O Boards have no jumpers or switches to configure--interrupts are configured through software command.

CONNECTORS

Front Panel Field I/O Connector P1

The front panel connector P1 provides the field I/O interface connections. The front panel connector is a SCSI-2 50-pin female connector (AMP 787082-5 or equivalent) employing latch blocks and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the front panel via round shielded cable (Model 5028-187).

Front panel connector P1 pin assignments are shown in Table 2.1.

Table 2.1: PMC408 Field I/O Pin Connections P1

Pin Description	Number	Pin Description	Number
OD00	1	OD25	32
OD01	2	OD26	33
OD02	3	OD27	34
OD03	4	OD28	36
OD04	6	OD29	37
OD05	7	OD30	38
OD06	8	OD31	39
OD07	9	***Not Used***	41
OD08	11	***Not Used***	42
OD09	12	***Not Used***	43
OD10	13	***Not Used***	44
OD11	14	***Not Used***	46
OD12	16	***Not Used***	47
OD13	17	***Not Used***	48
OD14	18	***Not Used***	49
OD15	19	COMMON	5
OD16	21	COMMON	10
OD17	22	COMMON	15
OD18	23	COMMON	20
OD19	24	COMMON	25
OD20	26	COMMON	30
OD21	27	COMMON	35
OD22	28	COMMON	40
OD23	29	COMMON	45
OD24	31	COMMON	50

I/O Noise and Grounding Considerations

The output channels of this model are the open drains of mosfets with a common source connection. The PMC408 is non-isolated between the logic and field I/O grounds since output common is electrically connected to the PMC module ground. Consequently, the field I/O connections are not isolated from the carrier/CPU board and backplane. A copper ground plane foil has been employed in the design of this model to help minimize the effects of ground bounce, impedance drops, and switching transients. However, care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

This device is capable of switching many channels at high currents. Additionally, the nature of the PMC interface is inherently inductive. The outputs of this model are protected to voltages up to 60V. As such, when switching inductive loads, it is important that careful consideration be given to the use of snubber devices to shunt the reverse emf that develops when the current through an inductor is interrupted. Filtering and bypassing at the load may also be necessary. Additionally, proper grounding with thick conductors is essential. Interface cabling and ground wiring should be kept as short as possible. For outputs, the use of an interposing relay may also be desireable for isolating the load, raising the drive capability, or providing additional system protection. Please refer to Drawing Drawing 4501-867 & 4501-868 for examples of these connections and proper output and grounding connections.

Output Off-State Loading Considerations

With respect to output control, the 100KΩ input buffer current-limiting resistors in combination with +4.7V voltage clamps will tend to increase the off-state drain current with increased drain voltage (up to 0.5mA at 60V). This is due to the fact that the input buffer circuitry and output mosfet drain circuitry are connected in tandem to the same I/O pin. If this presents a problem for your application, then you should consider separating the inputs and outputs by using multiple PMC408 modules.

PCI Local Bus Connector

The PMC408 module provides a 32-bit PCI interface to the carrier/CPU via two 64 pin connectors. These connectors are 64-pin female receptacle header (AMP 120527-1 or equivalent) which mates to the male connector of the carrier/CPU board (AMP 120521-1 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric screws and spacers are supplied with the PMC module to provide additional stability for harsh environments (see Drawing 4501-859 for assembly details). The pin assignments of the PCI local bus connector are standard for all PMC modules according to the PCI Mezzanine Card Specification (see Tables 2.2 and 2.3).

Table 2.2: PMC Connector Pin Assignments for J1 (32-bit PCI)

Signal Name	Pin #	Signal Name	Pin #
TCK	1	-12V	2
GND	3	INTA#	4
INTB#	5	***INTC#***	6
BUSMODE1#	7	+5V	8
INTD#	9	***PCI-RSVD****	10
GND	11	***PCI-RSVD****	12
CLK	13	GND	14
GND	15	***GNT#***	16
REQ#	17	+5V	18
V(I/O)	19	AD[31]	20
AD[28]	21	AD[27]	22
AD[25]	23	GND	24
GND	25	C/BE[3]#	26
AD[22]	27	AD[21]	28
AD[19]	29	+5V	30
V(I/O)	31	AD[17]	32
FRAME#	33	GND	34
GND	35	IRDY#	36
DEVSEL#	37	+5V	38
GND	39	***LOCK#***	40
SDONE#	41	***SBO#***	42
PAR	43	GND	44
V(I/O)	45	AD[15]	46
AD[12]	47	AD[11]	48
AD[09]	49	+5V	50
GND	51	C/BE[0]#	52
AD[06]	53	AD[05]	54
AD[04]	55	GND	56
V(I/O)	57	AD[03]	58
AD[02]	59	AD[01]	60
AD[00]	61	+5V	62
GND	63	***REQ64#***	64

# Indicates that the signal is active low.
BOLD ITALIC Signals are NOT USED by this PMC Model.

Table 2.3: PMC Connector Pin Assignments for J2 (32-bit PCI)

Signal Name	Pin #	Signal Name	Pin #
+12V	1	***TRST#***	2
TMS	3	***TDO***	4
TDI	5	GND	6
GND	7	***PCI-RSVD****	8
PCI-RSVD*	9	***PCI-RSVD****	10
BUSMODE2#	11	+3.3V	12
RST#	13	BUSMODE3#	14
+3.3V	15	BUSMODE4#	16
PCI-RSVD*	17	GND	18
AD[30]	19	AD[29]	20
GND	21	AD[26]	22
AD[24]	23	+3.3V	24
IDSEL	25	AD[23]	26
+3.3V	27	AD[20]	28
AD[18]	29	+GND	30
AD[16]	31	C/BE[2]#	32
GND	33	***PCI-RSVD***	34
TRDY#	35	+3.3V	36
GND	37	STOP#	38
PERR#	39	GND	40
+3.3V	41	SERR#	42
C/BE[1]#	43	GND	44
AD[14]	45	AD[13]	46
GND	47	AD[10]	48
AD[08]	49	+3.3V	50
AD[07]	51	***PCI-RSVD***	52
+3.3V	53	***PCI-RSVD***	54
PCI-RSVD	55	GND	56
PCI-RSVD	57	***PCI-RSVD***	58
GND	59	***PCI-RSVD***	60
ACK64#	61	+3.3V	62
GND	63	***PCI-RSVD***	64

# Indicates that the signal is active low.
BOLD ITALIC Signals are NOT USED by this PMC Model.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the PMC408 module.

This Acromag PMC408 is a PCI Local Bus Specification version 2.2 compliant PCI bus target only PMC module. The carrier/CPU connects a PCI host bus to the PMC module.

The PCI bus is defined to address three distinct address spaces: I/O, memory, and configuration space. The PMC module can be accessed via the PCI bus memory space and configuration spaces, only.

The PCI card's configuration registers are initialized by system software at power-up to configure the card. The PMC408 module is a Plug-and-Play PCI card. As a Plug-and-Play card the board's base address and system interrupt request line are not selected via jumpers but are assigned by system software upon power-up via the configuration registers. A PCI bus configuration access is used to access a PCI card's configuration registers.

PCI Configuration Address Space

When the computer is first powered-up, the computer's system configuration software scans the PCI bus to determine what PCI devices are present. The software also determines the configuration requirements of the PCI card.

The system software accesses the configuration registers to determine how many blocks of memory space the carrier requires. It then programs the PMC module's configuration registers with the unique memory address range assigned.

The configuration registers are also used to indicate that the PMC module requires an interrupt request line. The system software then programs the configuration registers with the interrupt request line assigned to the PMC module.

Since this PMC module is relocatable and not fixed in address space, this module's device driver provided by Acromag uses the mapping information stored in the module's Configuration Space registers to determine where the module is mapped in memory space and which interrupt line will be used.

Configuration Registers

The PCI specification requires software driven initialization and configuration via the Configuration Address space. This PMC module provides 256 bytes of configuration registers for this purpose. The PMC408 contains the configuration registers, shown in Table 3.1, to facilitate Plug-and-Play compatibility.

The Configuration Registers are accessed via the Configuration Address and Data Ports. The most important Configuration Registers are the Base Address Registers and the Interrupt Line Register which must be read to determine the base address assigned to the PMC408 and the interrupt request line that goes active on a PMC408 interrupt request.

Table 3.1 Configuration Registers

Reg. Num.	D31 D24	D23 D16	D15 D8	D7 D0
0	Device ID=464D		Vendor ID= 16D5	
1	Status		Command	
2	Class Code=118000			Rev ID=00
3	BIST	Header	Latency	Cache
4	32-bit Memory Base Address for PMC408 4K-Byte Block			
5 : 10	Not Used			
11	Subsystem ID=0000		Subsystem Vendor ID=0000	
12	Not Used			
13,14	Reserved			
15	Max_Lat	Min_Gnt	Inter. Pin	Inter. Line

MEMORY MAP

This board is allocated a 4K byte block of memory that is addressable in the PCI bus memory space to control the ON/OFF states of individual low-side switches and/or the acquisition of digital inputs from the field.

The memory space address map for the PMC408 is shown in Table 3.2. Note that the base address for the PMC408 in memory space must be added to the addresses shown to properly access the PMC408 registers. Register accesses as 32, 16, and 8-bit data in memory space are permitted. All the registers of the PMC408 are accessed via data lines D0 to D15. The most significant word of a 32-bit access is not used by the PMC408. A 32-bit read will return logic "0" for the most significant word

Table 3.2: PMC408 I/O Space Address Memory Map

Hex Base Addr.+	MSB D15 D08	LSB D07 D00	Hex Base Addr.+
001	INTERRUPT REGISTER		000
201	READ- Digital Input Channel Register A CH15 ↔ CH08	READ- Digital Input Channel Register A CH07 ↔ CH00	200
205	READ- Digital Input Channel Register B CH31 ↔ CH24	READ- Digital Input Channel Register B CH23 ↔ CH16	204
209	R/W -Digital Output Channel Register A CH15 ↔ CH08	R/W -Digital Output Channel Register A CH07 ↔ CH00	208
20D	R/W - Digital Output Channel Register B CH31 ↔ CH24	R/W -Digital Output Channel Register B CH23 ↔ CH16	20C
211	NOT DRIVEN[1]	R/W - Interrupt Enable Register[1] CH07 ↔ CH00	210
215	NOT DRIVEN[1]	R/W -Interrupt Type Config. Register[1] CH07 ↔ CH00	214
219	NOT DRIVEN[1]	R/W - Interrupt Polarity Register[1] CH07 ↔ CH00	218
21D	NOT DRIVEN[1]	R/W - Interrupt Status Register[1] CH07 ↔ CH00	21C
221	NOT DRIVEN[1]	NOT USED[2]	220
225 ↓ 2FD	NOT USED[2]		224 ↓ 2FC

Notes (Table 3.2):

1. Bits 15-8 of these registers are not used. Bits 15-8 will be driven high (1's).
2. The PMC408 will respond to addresses that are "Not Used".

Interrupt Register, (Read/Write) - (Base + 000H)

This read/write register is used to: enable board interrupt, determine the pending status of interrupts, and release an interrupt.

The function of each of the interrupt register bits are described in Table 3.3. This register can be read or written with either 8-bit, 16-bit, or 32-bit data transfers. A power-up or system reset sets all interrupt register bits to 0.

Table 3.3: Interupt Register

BIT	FUNCTION
0	Board Interrupt Enable Bit. This bit must be set to logic "1" to enable generation of interrupts from the PMC module. Setting this bit to logic "0" will disable board interrupts. (Read/Write Bit)
1	Interrupt Pending Status Bit. This bit can be read to determine the interrupt pending status of the PMC module. When this bit is logic "1" an interrupt is pending and will cause an interrupt request if bit-0 of the register is set. When this bit is a logic "0" an interrupt is not being requested.
7 to 2	Not Used[1]
8	Software Reset Writing a logic "1" to this bit will cause a reset of PMC module. Bit-0 of this register will not be affected.
15 to 9	Not Used[1]

Notes (Table 3.3):

1. All bits labeled "Not Used" will return logic "0" when read.

Digital Input Registers A & B (Read Only)

When the Digital Input Channel Data Registers are read, the value read corresponds to the actual state of the input channels at the time of the read. If the channel's tandem output mosfet is being controlled and its drain is loaded, then reading the digital input channel data register will return the state of the output (it is directly connected to the drain). This is an efficient method of accomplishing “loopback” control of the output. A “0” bit means that the corresponding input signal is below the threshold value (or the tandem output mosfet is ON), a “1” bit means that the corresponding input signal is at or above the threshold value (or the tandem mosfet is OFF and pulled up).

Thirty-two possible input channels numbered 0 through 31 may be read. Channel read operations use 8-bit (LSB or MSB), or 16-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest (see below). Register A monitors input channels 0 through 15. Register B monitors input channels 16 through 31.

It is recommended that unused inputs not be left floating, but pulled low by turning on the corresponding tandem output (see PMC Digital Output Registers).

REGISTER A (INPUT CHANNELS 0 THROUGH 15):

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 LSB
CH15....................................CH8								CH7...................................CH0							

REGISTER B (INPUT CHANNELS 16 THROUGH 31):

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 LSB
CH31.................................CH24								CH23................................CH16							

Digital Output Registers A & B (Read/Write)

When the Digital Output Channel Data Registers are written to, the value written is represented at the corresponding output channels. A “0” bit means that the corresponding output switch is OPEN (OFF). Writing a “1” bit CLOSES the corresponding output switch (turns it ON). There are two ways to accomplish an output read. Reading the digital output channel register returns the state configuration of this register (which is equivalent to the output mosfet gate signal). Since input channels operate in tandem with the output channels, reading the digital input channel register will return the actual state of the output (it returns the level of the output mosfet drain). That is, writing a ‘1’ to an output turns the switch ON (gate signal high). In turn, this drives the drain low (mosfet is conducting). As such, a read of the input channel register will be the inverse of a read of the output channel register for a loaded output channel.

Read/Write Control for 32 output channels numbered 0 through 31 is provided. Channel state Read/Write operations use 8-bit, 16-bit, or 32-bit data transfers with the lower ordered bits corresponding to the lower-numbered channels for the register of interest (see below). Register A controls output channels 0 through 15. Register B controls output channels 16 through 31.

REGISTER A (OUTPUT SWITCHES 0 THROUGH 15):

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 LSB
CH15..................................CH08								CH7...................................CH0							

REGISTER B (OUTPUT SWITCHES 16 THROUGH 31):

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 LSB
CH31..................................CH24								CH23................................CH16							

Each output channel register can be conveniently read back for verification purposes. However, for critical control applications, it is recommended that outputs be directly fed back to input points and the input points monitored (loopback I/O). By design, input channels are tied to the drains of the tandem output mosfet and a read of the input channel register will return the inverse of a read of the output channel register (a read of the input returns the drain level, a read of the output returns the gate level). This is an efficient method of accomplishing loopback output control without requiring additional channels. However, this only applies for a loaded drain (a pullup or other load connected to the drain).

All outputs are OFF (switch OPEN) following a power-on reset, and are immediately cleared following a system reset. It is recommended that unused outputs be turned on so that the corresponding unused inputs are pulled low, rather than floating.

Interrupt Enable Register (R/W)

The digital input channel Interrupt Enable Registers provide a mask bit for each of the 8 possible interrupt channels (channels 0-7 only). A “0” bit will prevent the corresponding input channel from generating an external interrupt. A “1” bit will allow the corresponding input channel to generate an interrupt. The unused upper 8 bits of these 16-bit registers are “Don’t Care” and will always read high (1’s).

INTERRUPT ENABLE REGISTER:

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 LSB
X	X	X	X	X	X	X	X	CH7...................................CH0							

All input channel interrupts are masked (“0”) following a reset.

Interrupt Type (COS or H/L) Configuration Register (R/W)

The Interrupt Type Configuration Registers determine the type of input channel transition that will generate an interrupt for each of the 8 possible interrupt channels (channels 0-7 only). A “0” bit means that an interrupt will be generated when the input channel level specified by the Interrupt Polarity Register occurs (i.e. Low or High level transition interrupt). A “1” bit means the interrupt will occur when a Change-Of-State (COS) occurs at the corresponding input channel (i.e. any state transition). The unused upper 8 bits of these 16-bit registers are “Don’t Care” and will always read high (1’s). Note that interrupts will not occur unless they are enabled.

INTERRUPT TYPE (COS or H/L) CONFIGURATION REGISTER:

MSB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 LSB
X	X	X	X	X	X	X	X	CH7...................................CH0							

All bits are set to “0” following a reset which means that the inputs will cause interrupts for the levels specified by the digital input channel Interrupt Polarity Register.

Interrupt Polarity Register (R/W)

The Interrupt Polarity Register determines the level that will cause a channel interrupt to occur for each of the 8 possible interrupt channels (channels 0-7 only). A “0” bit specifies that an interrupt will occur when the corresponding input channel is *BELOW* TTL threshold (i.e. a “0” in the digital input channel data register). A “1” bit means that an interrupt will occur when the input channel is *ABOVE* TTL threshold (i.e. a “1” in the digital input channel data register). Note that no interrupts will occur unless they are enabled by the Interrupt Enable Register. Further, the Interrupt Polarity

Register will have no effect if the Change-of-State (COS) interrupt type is configured by the Interrupt Type Configuration Register.

INTERRUPT POLARITY (HIGH/LOW) REGISTER:

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	CH7	...	...	...	...	...	...	CH0

The unused upper 8 bits of these 16-bit registers are "Don't Care" and will always read high (1's). All bits are set to "0" following a reset which means that the inputs will cause interrupts when they are below TTL threshold.

Interrupt Status Register (R/W)

The Interrupt Status Register reflects the status of the 8 possible interrupt channels (channels 0-7 only). A "1" bit indicates that an interrupt is pending for the corresponding channel. A channel that does not have interrupts enabled will never set its interrupt status flag. A channel's interrupt can be cleared by writing a "1" to its bit position in the Interrupt Status Register (writing a "1" acts as a reset signal to clear the set state). However, if the condition which caused the interrupt to occur remains, the interrupt will be generated again (unless disabled via the Interrupt Enable Register).

Note that the input channel bandwidth should be limited to reduce the possibility of missing channel interrupts. For a specific input channel, this could happen if multiple changes occur before the channel's interrupt is serviced.

INTERRUPT STATUS REGISTER:

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	CH7	...	...	...	...	...	...	CH0

All interrupts are cleared following a reset.

PMC408 PROGRAMMING CONSIDERATIONS

To make programming and communicating with the board easier, Acromag provides a software product (sold separately) consisting of PMC module VxWorks® libraries. This software (Model PMCSW-API-VXW, MSDOS format) is composed of VxWorks® (real time operating system) libraries for all Acromag PMC modules. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PMC modules.

Acromag, also provides a software product (sold separately) consisting of PMC module ActiveX (Object Linking and Embedding) controls for Windows 98, 95®, ME, 2000 and Windows NT® compatible application programs (Model PMCSW- ATX, MSDOS format) to program and communicate with the board.

The following sections give some pointers for programming interrupts.

Programming Interrupts

Digital input channels can be programmed to generate interrupts for the following conditions (channels 0-7 only):

- Change-of-State (COS) at selected channels.
- Input level (polarity) match at selected input channels.

Interrupts generated by the PMC408 use interrupt request line INTA#. The interrupt release mechanism employed is the Release On Register Access (RORA) type. This means that the interrupter will release the interrupt request line (INTA#) after the interrupt has been cleared by writing a "1" to the appropriate bit position in the input channel Interrupt Status Register.

When using interrupts, input channel bandwidth should be limited to reduce the possiblity of missing channel interrupts. For a given input channel, this could happen if multiple changes occur before the channel's interrupt is serviced. The response time of the input channels should also be considered when figuring this bandwidth. The total response time is the sum of the input buffer response time, plus the interrupt logic circuit response time, and this time must pass before another interrupt condition will be recognized.

PMC Programming Example for Change-of-State Interrupts:

1. Enable PMC408 board interrupt by writing a "1" to bit 0 of the Interrupt Register at Base Address + 000H.
2. Select channel Change-of-State interrupts by writing a "1" to each channel's respective bit in the Interrupt Type Register at Base Address + 214H. Note that Change-Of-State interrupts (specified with "1") may be mixed with polarity match interrupts (specified with "0").
3. Enable individual input channel interrupts by writing a "1" to each channel's respective bit in the Interrupt Enable Register at Base Address + 210H.
4. Clear pending interrupts by writing a "1" to each channel's respective bit in the Interrupt Status Register at Base Address + 21CH.

   Change-of-State Interrupts may now be generated by the input channels programmed above for any Change-Of-State transition.

PMC Programming Example for Level (Polarity) Match Interrupts:

1. Enable PMC408 board interrupt by writing a "1" to bit 0 of the Interrupt Register at Base Address + 000H.
2. Select channel polarity match interrupts by writing a "0" to each channel's respective bit in the Interrupt Type Register at Base Address + 214H. Note that Change-Of-State interrupts (specified with "1") may be mixed with polarity match interrupts (specified with "0").
3. Select the desired polarity (High/Low) level for interrupts by writing a "0" (Low), or "1" (High) level to each channel's respective bit in the Interrupt Polarity Registers at Base Address + 218H.
4. Enable individual input channel interrupts by writing a "1" to each channel's respective bit in the Interrupt Enable Registers at Base Address + 210H.
5. Clear pending interrupts by writing a "1" to each channel's respective bit in the Interrupt Status Register at Base Address + 21CH.

   Interrupts can now be generated by matching the input level with the selected polarity for programmed interrupt channels.

General Sequence of Events for Processing an Interrupt

1. The PMC408 asserts the Interrupt Request Line (INTA#) in response to an interrupt condition.

2. Determine the IRQ line assigned to the PMC408 during system configuration (read configuration register number 15).
3. Set up the system interrupt vector for the appropriate interrupt.
4. Unmask the IRQ in the system interrupt controller.
5. The interrupt service routine pointed to by the vector set up in step 3 starts.
6. Interrupt service routine determines if the PMC408 has a pending interrupt request by reading the Interrupt pending bit-1 of the Interrupt Register.
7. Example of Generic Interrupt Handler Actions:
   A. Disable the interrupting channel(s) by writing a "0" to the appropriate bits in the PMC408 Interrupt Enable Register.
   B. Clear the interrupting channel(s) by writing a "1" to the appropriate bits in the PMC408 Interrupt Status Register.
   C. Enable the interrupting channel(s) by writing a "1" to the appropriate bits in the PMC408 Interrupt Enable Registers at Base Address + 210H. Also, write a "1" to bit-0 of the Interrupt Register at Base Address + 000H.
8. Write "End-Of-Interrupt" command to systems interrupt controller.
9. If the PMC408's interrupt stimulus has been removed, the interrupt cycle is completed and the board holds the INTA# inactive.

4.0 THEORY OF OPERATION

This section describes the basic functionality of the circuitry used on the board. Refer to the Block Diagram shown in Drawing 4501-866 as you review this material.

INPUT/OUTPUT

The field I/O interface to the carrier board is provided through connector P1 (refer to Table 2.1). Field I/O points are NON-ISOLATED. This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Drawings 4501-867 & 4501-868 for example I/O and grounding connections.

A Field Programmable Gate Array (FPGA) is used to generate all the logic necessary to operate the board. With respect to input acquisition, the interrupt channels drive the FPGA through 8 individual buffers (channels 0-7 only). The input buffers of the other 24 channels are selectively enabled and drive the data bus directly. The field input signals are tied to the inputs of these buffers via a 100KΩ series connected resistor which limits the input current (but raises the tandem output's off-state drain current). Additionally, the buffer inputs are clamped to +4.7V (generated from the +12V supply to minimize +5V loading). The input signal threshold is TTL compatible. The typical threshold is 1.5V DC with 200mV of hysteresis.

For output control, 32 open-drain outputs are connected in tandem with 32 input buffers to each I/O channel. The outputs are the open drains of individual mosfets. The gates of the mosfets are driven by the FPGA. The sources of these mosfets are connected in common. This configuration provides up to 32 low-side switches for digital control. Writing a '1' to the output will turn the switch ON (closed-circuit), a '0' will turn it OFF (open-circuit). Since the input buffers are connected in tandem with the output mosfets, efficient loopback monitoring of the output state can be accomplished by reading the input channel registers.

With respect to output control, the 100KΩ input buffer resistors in combination with +4.7V voltage clamps will tend to increase the off-state drain current with increased drain voltage (up to 0.5mA at 60V). This is due to the fact that the input buffer circuitry and output mosfet drain circuitry are connected in tandem to the same I/O pin. If this presents a problem for your application, then you should consider separating the inputs and outputs by using multiple boards.

Output operation is considered 'Fail-safe'. That is, the outputs are always OFF upon power-up reset, and are automatically cleared following a system software reset. This is done for safety reasons to ensure reliable control of the output state under all conditions. Further, unlike some competitive units, output gate pulldowns are included to ensure that the outputs do not turn on momentarily when output load power is applied with no power to the PMC module.

The output mosfets employed are rated for a much higher current than specified. However, the field connector and cabling used are only rated to 1A per pin (limiting a single channel to 1A). For compatibility with other PMC models, 10 pins have been reserved for ground return (hence; the 10A total current limitation placed on this module). The low R_{dsON} of the output mosfets will ensure TTL-level compatible logic-low output signals even at high (1A) output currents.

The output mosfets include an integrated zener diode between the drain and the source. This provides output voltage clamp protection to 60V. The tandem input channel is also rated to 60V. However, when driving inductive loads such as relay coils, you should always place a shunt diode across the load to shunt the reverse EMF that develops across the coil when the current through it is turned off (refer to Section 2 and see Drawing 4501-867 for an example of this type of protection).

Since the input buffer and output mosfet circuitry share an I/O pin, inputs and outputs may be intermixed in any combination. Further, by providing an input channel for each output, efficient loopback monitoring of the output state can be easily accomplished (see Drawing 4501-868).

Digital input channels of this model can be configured to generate interrupts for Change-Of-State (COS) and input level (polarity) match conditions at selected input channels (channels 0-7 only). The interrupt release mechanism employed is RORA (Release On Register Access).

PCI INTERFACE LOGIC

The PCI bus interface logic is imbedded within the FPGA. This logic includes support for PCI commands, including: configuration read/write, and memory read/write. In addition, the PCI target interface performs parity error detection, uses a single 4K base address register, and implements target abort, retry, and disconnect. The PMC408 logic also implements interrupt requests via interrupt line INTA#. J1 and J2 connectors also provide ±12V and +5V to power the module (-12V is not used).

A PCI bus read of the PMC module will initially terminate with a retry. While the read data is moved to the read register (typically 1000ns), continued retries will result in retry terminations. The retry termination allows the PCI bus to be free for other system operations while the data is moved to the read register.

A PCI bus write to the PMC module will result in 1) immmediately accepting the write data and normal cycle termination or 2) issue of a retry termination. A retry termination will be issued if the previous write cycle has not completed on the PMC module. It will typically take the PMC module 1000ns to write the data to the required internal register. Thus if another write cycle is initiated on the PCI bus before the typical 1000ns has lapsed, the write cycle will be terminated with a retry.

A programmable logic device provides the control signals required to operate the board. It decodes the selected addresses, control signals, and interrupt handling. It also returns the acknowledgement signal required by the carrier/CPU board per the PMC specification. The program for the gate array is stored in separate PROM memory and loaded upon power-up.

PMC Module Software

Acromag also provides a software product (sold separately) consisting of PMC module ActiveX (Object Linking and Embedding) controls for Windows 98, 95®, ME, 2000 and Windows NT® compatible application programs (Model PMCSW- ATX, MSDOS format). This software provides individual controls that allow Acromag PMC modules to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Microsoft® Office® 97 applications and others. The ActiveX controls provide a high-level interface to PMC modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the ActiveX controls. These functions consist of ActiveX control for each Acromag PMC module.

In addition, Acromag provides a software product (sold separately) consisting of PMC module VxWorks® libraries. This software (Model PMCSW-API-VXW, MSDOS format) is composed of VxWorks® (real time operating system) libraries for all Acromag PMC modules. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag PMC modules.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment. Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Applications Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration……... Single PMC Module.
Height.............................. 15.11 mm (0.595 in). (See Drawing 4501-859)
Stacking Height………….. 10.0 mm (0.394 in).
Length.............................. 149.0 mm (5.866 in).
Width................................ 74.0 mm (2.913 in).
Board Thickness............... 1.59 mm (0.062 in).

Connectors:
PCI Local Bus Interface..... Two 64-pin female receptacle header (AMP 120527-1 or equivalent).
Field I/O……..................... 50-pin, SCSI-2, female receptacle header (AMP 787082-5 or equivalent).

Power Requirements		PMC408(E)
5V[1] (±5%)	Typical	65 mA
	Max.	90 mA
+12V (±5%)	Typical	8 mA
	Max.	12 mA
-12V (±5%)	Typical	Not Used
	Max.	

1. Maximum rise time of 100 milliseconds

ENVIRONMENTAL

Operating Temperature........... 0 to +70°C. -40 to +85°C (E Versions)
Relative Humidity…...................5-95% Non-Condensing.
Storage Temperature…............. -55 to 105°C.
Non-Isolated.............................. Logic and field commons have a direct electrical connection.
Radiated Field Immunity (RFI).. Designed to comply with IEC1000-4-3 Level 3 (10V/m, 80 to 1000MHz AM & 900MHz. Keyed) and European Norm EN50082-1 with no data upsets.
Electromagnetic Interference Immunity (EMI)…..……….…..... No data upsets occur under the influence of EMI from switching solenoids, commutator motors, and drill motors.
Surge Immunity…………………. Not required for signal I/O per European Norm EN50082-1.
ESD Protection……..........…..... Complies with IEC1000-2 Level 1 (2KV direct contact discharge at input/output terminals) and European Standard EN50082-1.

Electric Fast Transient Immunity (EFT)………………..... Complies with IEC1000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.

Radiated Emissions ………....... Meets or exceeds European Norm EN50081-1 for class A equipment.

> Warning: This is a class A product. In a domestic environment this product may cause radio interference in which the user may be required to take adequate measures.

Reliability Prediction

Mean Time Between Failure…... MTBF = TBD hours (not available at time of printing) @ 25°C, Using MIL-HDBK-217F, Notice 2.

DIGITAL INPUTS

Input Channel Configuration.........32 non-inverting buffered inputs with a common connection. For DC voltage applications only, observe proper polarity.

Input Signal Voltage Range...........0 to +60V DC, Maximum.

Input Signal Threshold.................TTL compatible. 1.5V DC with 200mV of hysteresis, typical. Thus, Low-to-High threshold is 1.6VDC, High-to-Low is 1.4VDC, typical. Limited to TTL levels of 0.8VDC (Max LOW level) and 2.0VDC (Min HIGH level).

Input Resistance...........................100KΩ, Typical.

Input Hysteresis...........................200mVDC centered at a 1.5VDC threshold, Typical.

Input Current................................560uA, Typical at 60VDC.

Interrupt Input Response Time......250nS minimum to 375nS maximum, depending on when the input transition occurs with respect to the 8MHz clock. Measured from input transition to INTA# line assertion.

DIGITAL OUTPUTS

Output Channel Configuration.......32 open-drain DMOS Mosfets with common source connection. For DC voltage applications only, observe proper polarity.

Output “OFF” Voltage Range.........0 to +60V DC, Maximum.

Output “OFF” Leakage Current......25uA Maximum (Mosfet Only, 55°C, 48V). Does not include tandem input bias current. NOTE: The 100KΩ input buffer resistors in combination with +4.7V voltage clamps will tend to increase the off-state drain current with increased drain voltage (up to 0.5mA at 60V). This is due to the fact that the input buffer circuitry and output mosfet drain circuitry are connected in tandem to the same I/O pin.

Output “ON” Current Range...........0 to +1A DC, continuous (up to 10A total for all channels combined), or 300mA DC, continuous (all channels ON). No deration required at elevated ambients.

Output R_{ds} ON Resistance.............0.2Ω, Maximum (25°C).

Turn-ON Time...............................Varies with load, 620ns Typical, with 330Ω pull-up to +5V and 12-inch ribbon cable. Measured from FRAME# line assertion to output drain state transfer to TTL 0.8V level.

Turn-OFF Time.............................Varies with load, 800ns Typical, with 330Ω pull-up to +5V and 12-inch ribbon cable. Measured from FRAME# line assertion to output drain state transfer to TTL 2.0V level.

OUTPUT MOSFETS
(These specifications are included for reference and apply to the output driver only. See DIGITAL OUTPUTS above for module specifications).

Manufacturer/Part Number............National NDS9945, Siliconix Si9945DY.

Voltage V_{DSS}.................................60V DC, Maximum.

Current I_D......................................3.5A, Continuous (25°C), 2.8A, Continuous (70°C).

ON Resistance R_{DS}.......................0.2Ω (VGS=4.5V, 25°C).

Power Dissipation P_D...................2W (25°C).

Output “OFF” Leakage Current....25uA Maximum (55°C, 48V).

PCI Local Bus Interface

Compatibility.............................. Conforms to PCI Local Bus Specification, Revision 2.2 and PMC Specification, P1386.1/Draft 2.4. (See Note 2)

Electrical/Mechanical Interface... Single-Width PMC Module.

PCI Target ……………………… Implemented by Altera FPGA.

4K Memory Space Required…… One Base Address Register.

PCI commands Supported…….. Configuration Read/Write, Memory Read/Write, 32,16, and 8-bit data transfer types supported.

Signaling………………………… 5V Compliant, 3.3V Tolerant

PCI bus Write Cycle Time[1]…… 150 nS Typical measured from falling edge of FRAME# to the falling edge of TRDY#.

PCI bus Read Cycle Time[1]…… 150 nS Typical.

Notes (PCI Local Bus Interface):

1. Although the typical read or write PCI bus cycle time is only 150nS the actual read or write implemented on the PMC Module will be typically 1000 nS. Thus, the PMC Module will issue a RETRY when a new read or write cycle is implemented before the PMC modules 1000 nS read or write has completed. When the PMC Module issues a RETRY this frees the PCI bus while the previous read or write operation is completed.
2. Due to the unique modular nature of the PMC408 assembly, it is impossible to comply with the solder side component height per the PMC Mechanical Standand. Refer to Mechanical

Assembly Drawing 4501-859 for details. You must determine whether there will be adequate clearance for your application.

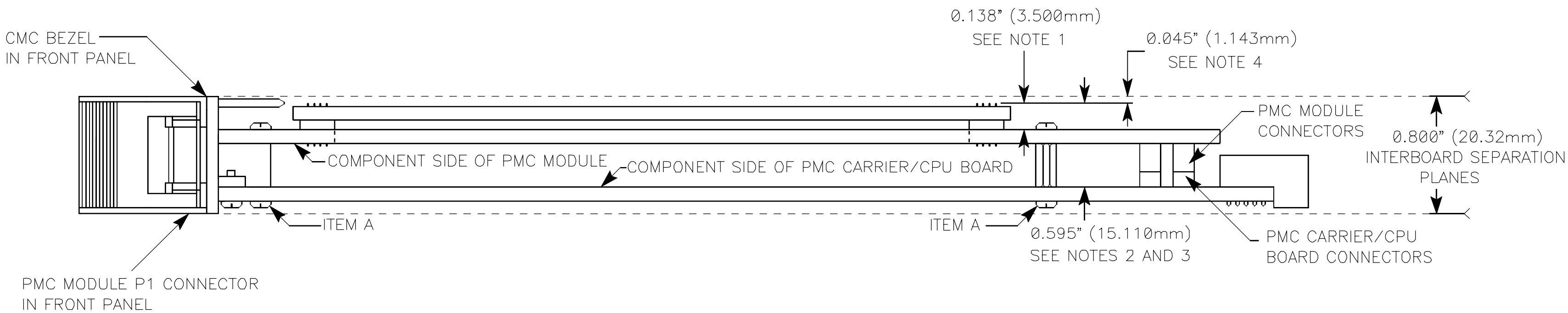
APPENDIX

CABLE: MODEL 5028-187 (SCSI-2 to Flat Ribbon, Shielded)

Type: Round shielded cable, 50-wires (SCSI-2 male connector at one end and a flat female ribbon connector at the other end). The cable length is 2 meters (6.56 feet). This shielded cable is recommended for all I/O applications (both digital I/O and precision analog I/O).
Application: Used to connect Model 5025-552 termination panel to the PMC Module.
Length: Standard lenght is 2 meters (6.56 feet). Consult factory for other lenghts. It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50 conductors, 28 AWG on 0.050 inch centers (permits mass termination for IDC connectors), foil/braided shield inside a PVC jacket.
Connectors: (One End): SCSI-2, 50-pin male connector with backshell and spring latch hardware.
(Other End): IDC, 50-pin female connector with strain relief.
Keying: The SCSI-2 connector has a “D Shell” and the IDC connector has a polarizing key to prevent improper installation.
Schematic and Physical Attributes: See Drawing 4501-758.
Electrical Specifications: 30 VAC per UL and CSA (SCSI-2 connector spec.’s). 1 Amp maximum at 50% energized (SCSI-2 connector spec.’s).
Operating Temperature: -20°C to +80°C.
Storage Temperature: -40°C to +85°C.
Shipping Weight: 1.0 pound (0.5Kg), packed.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For PMC Module Boards
Application: To connect field I/O signals to the PMC Module. *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the PMC Module via a flat ribbon cable (Model 5025-551-x). Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to field I/O (pins 1-50) on the PMC module. Each PMC module has its own unique pin assignments. Refer to the PMC module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight: 1.25 pounds (0.6kg) packaged.



ASSEMBLY PROCEDURE:

1. INSERT PMC MODULE (P1 CONNECTOR SIDE) INTO THE CMC BEZEL IN THE FRONT PANEL OF THE PMC CARRIER/CPU BOARD. THEN, ALIGN THE CONNECTORS ON THE PMC MODULE AND PMC CARRIER/CPU BOARD. ONCE ALIGNED THEN PUSH TOGETHER. STACKING HEIGHT BETWEEN PMC MODULE AND PMC CARRIER/CPU BOARD IS 0.394" (10.000mm).

2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF PMC CARRIER/CPU BOARD AND INTO PMC MODULE AS SHOWN (4 PLACES). THEN TIGHTEN SCREWS.

NOTE:

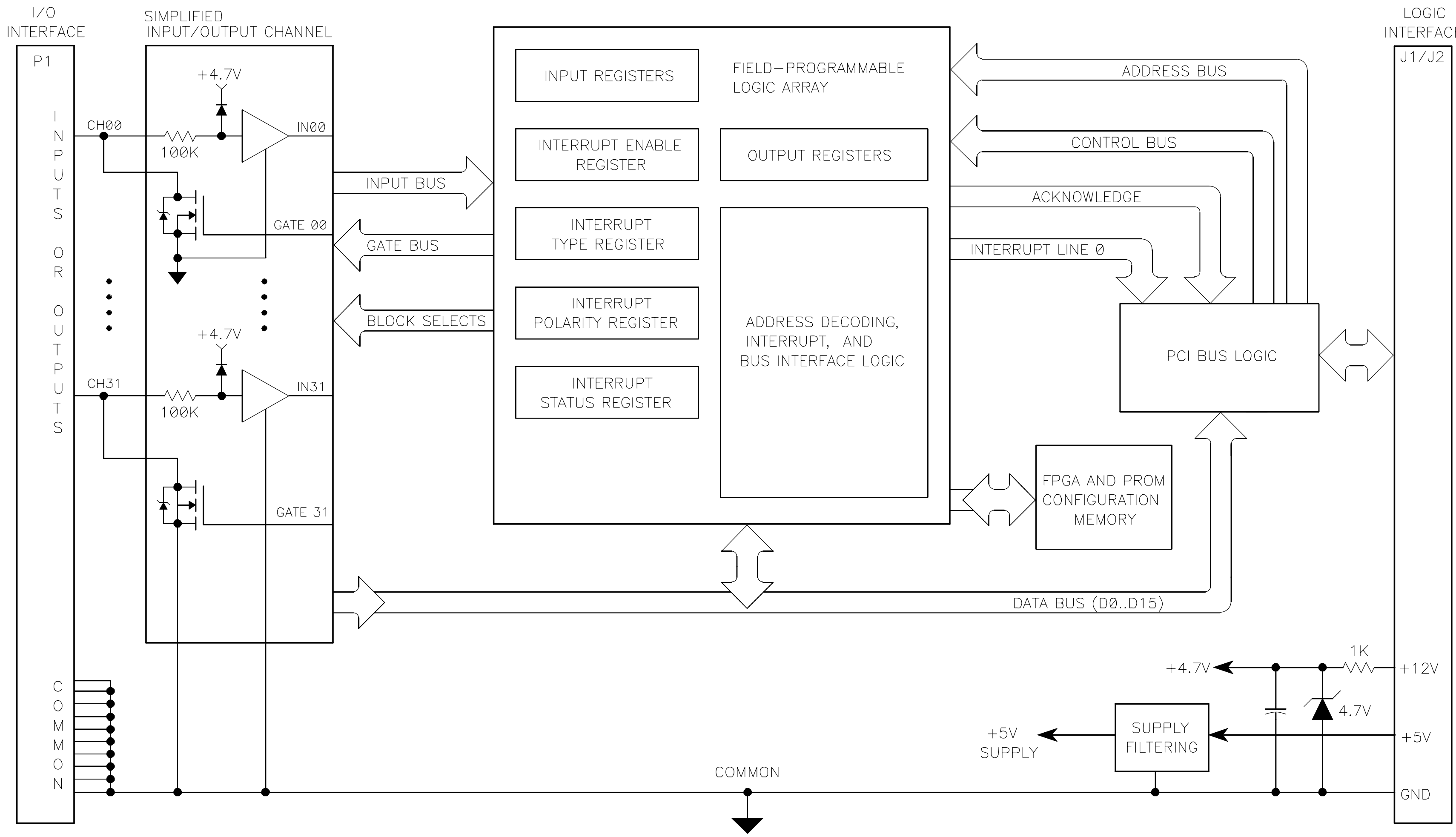
1. THE USEABLE SPACE ON THE SOLDER SIDE OF THE PMC MODULE IS 0.075"(1.900mm) PER PMC MECHANICAL STANDARD P1386.1. THIS PMC MODULE EXCEEDS THIS BY 0.063" (1.600mm).

2. THE TOTAL HEIGHT OFF THE PMC CARRIER/CPU BOARD IS 0.532" (13.500mm) PER PMC MECHANICAL STANDARD P1386.1. THIS PMC MODULE EXCEEDS THIS BY 0.063" (1.600mm).

3. THE MAXIMUM COMPONENT HEIGHT FOR VME AND CompactPCI IS 0.540"(13.720mm). THIS PMC MODULE EXCEEDS THIS BY 0.055" (1.400mm).

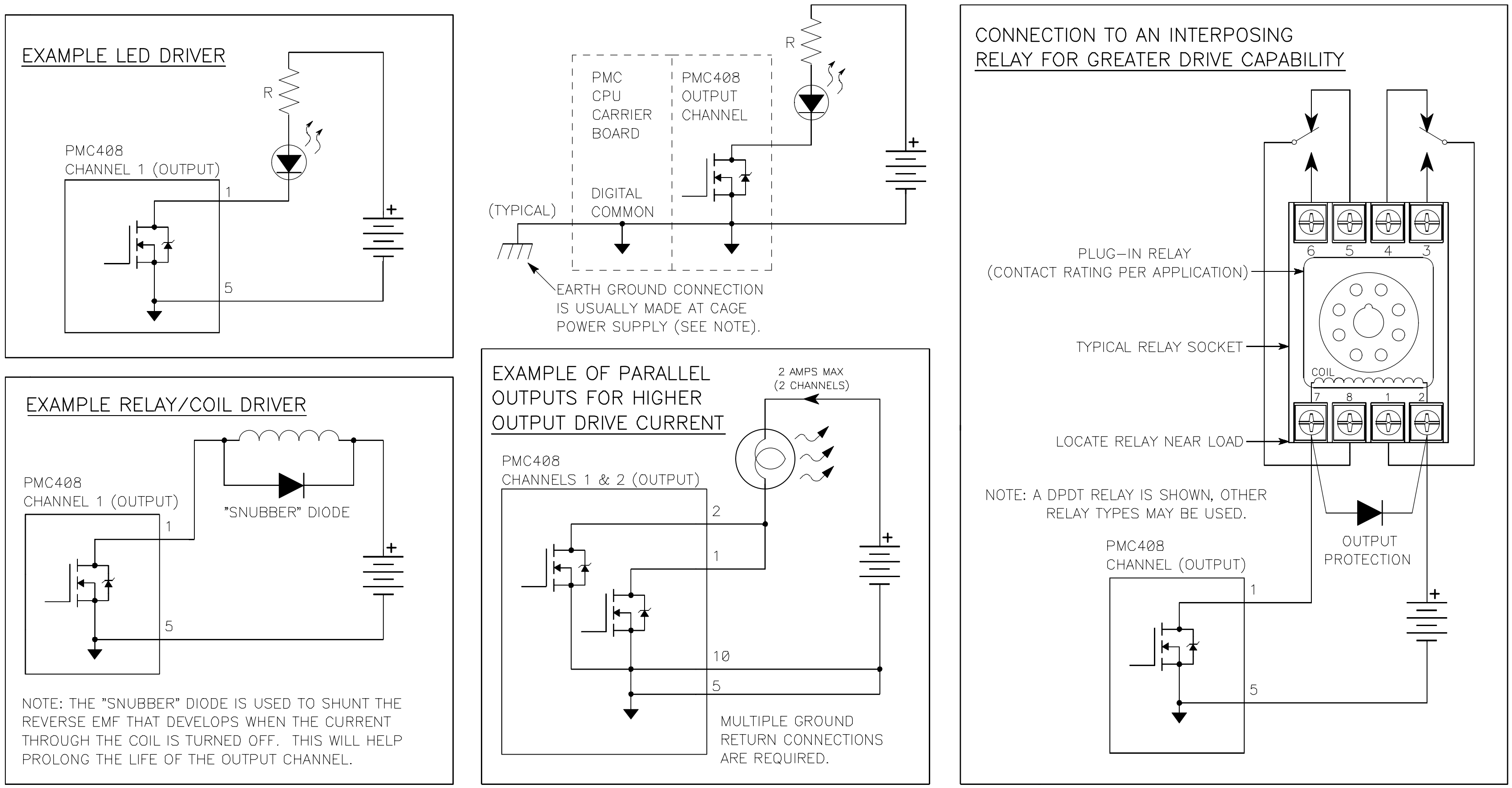
4. DISTANCE TO INTERBOARD SEPARATION PLANE IS 0.045" (1.143mm). THE DESIRED SPACING IS 0.100" (2.540mm) FOR VME AND CompactPCI .

PMC MODULE TO PMC CARRIER/CPU BOARD MECHANICAL ASSEMBLY 4501−859A



PMC408 BLOCK DIAGRAM

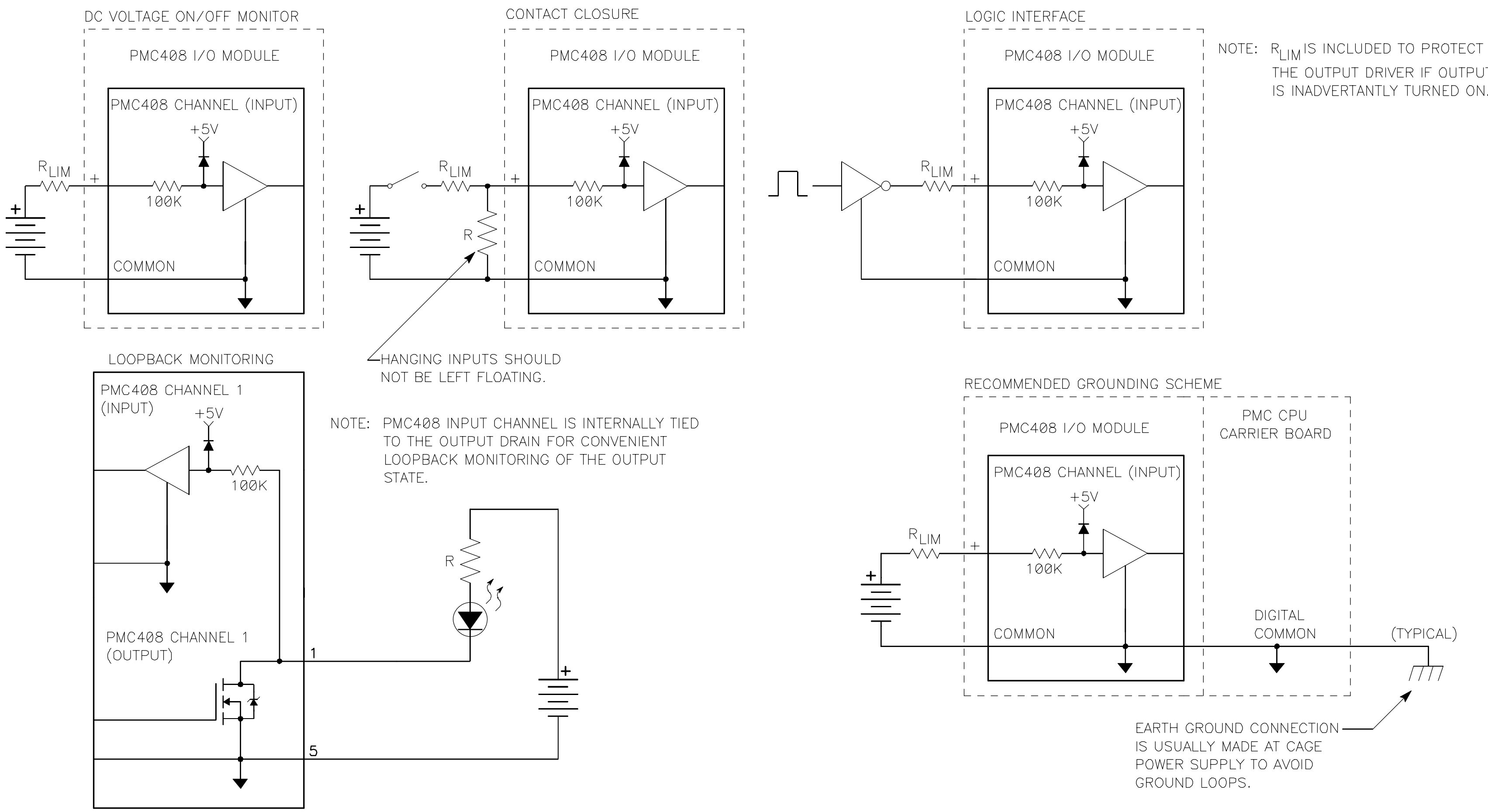
4501−866A



NOTE: MULTIPLE EARTH GROUNDS CAUSE
GROUND LOOPS AND MUST BE AVOIDED.

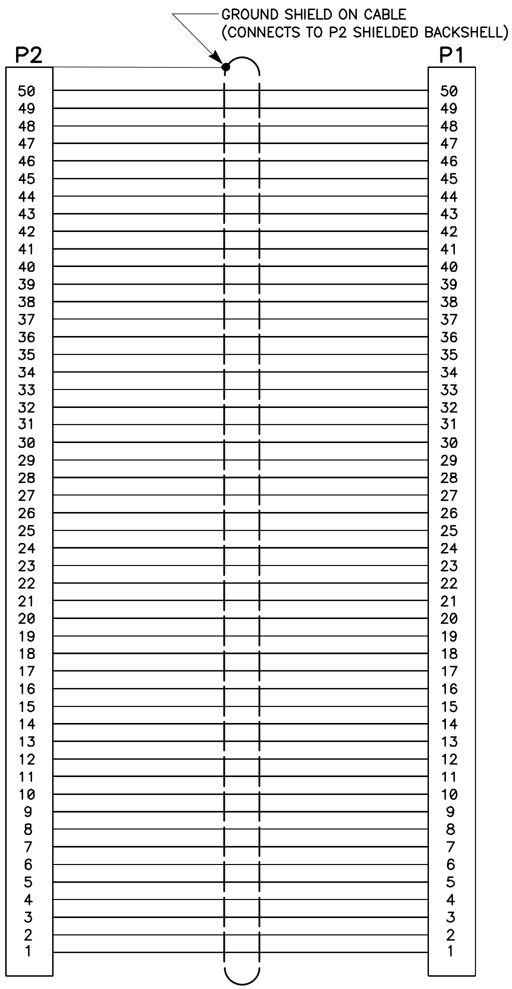
PMC408 EXAMPLE OUTPUT CONNECTIONS

4501-867

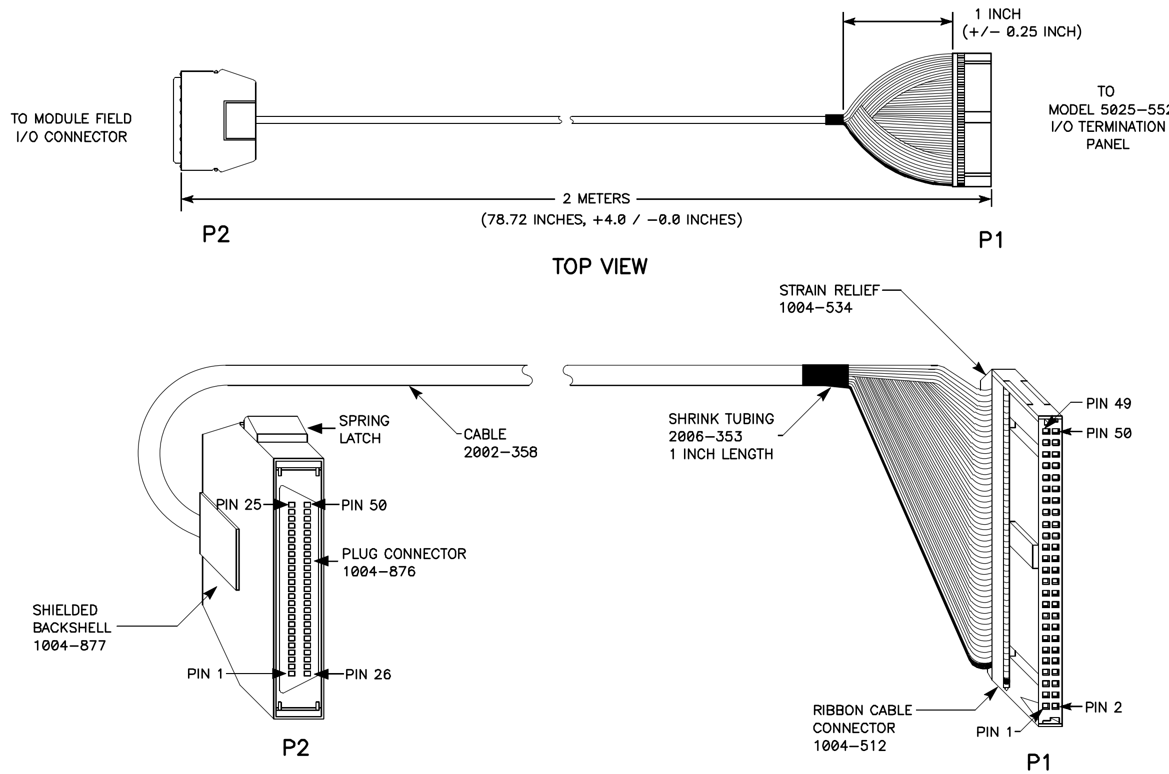


PMC408 EXAMPLE INPUT CONNECTIONS

4501−868A



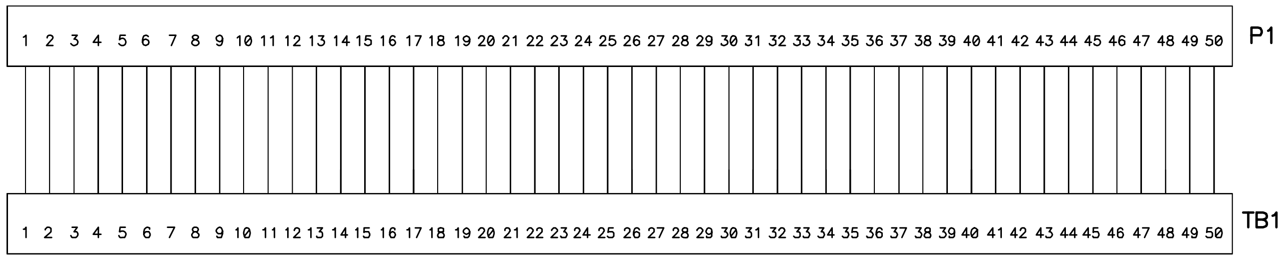
SCHEMATIC



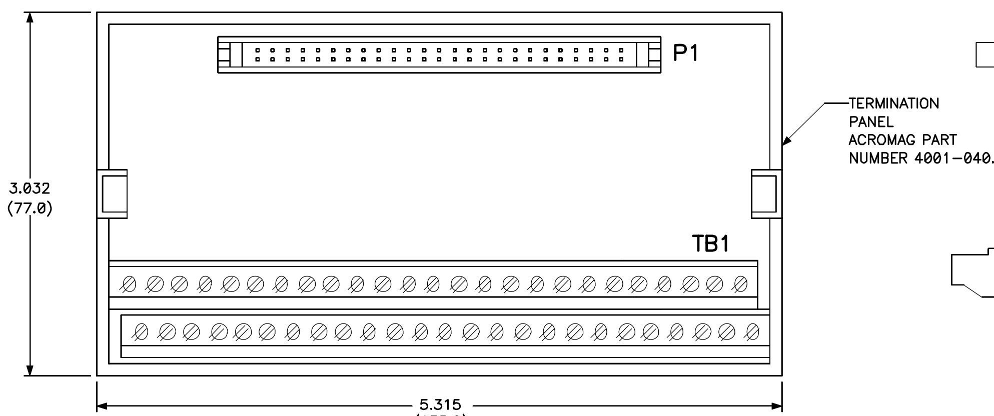
NOTE: SEVEN DIGIT PART NUMBERS ARE ACROMAG PART NUMBERS (XXXX−XXX).

MODEL 5028−187, SCSI−2 TO FLAT RIBBON CABLE, SHIELDED

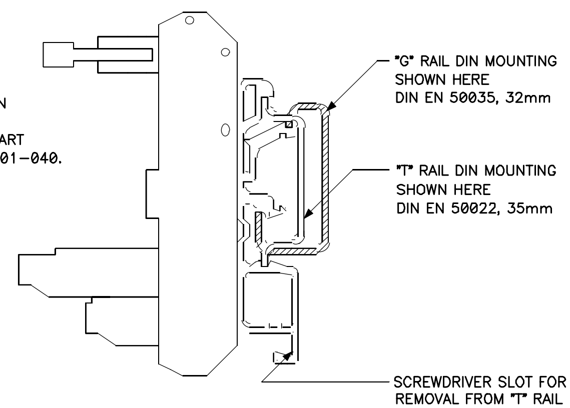
4501−758B



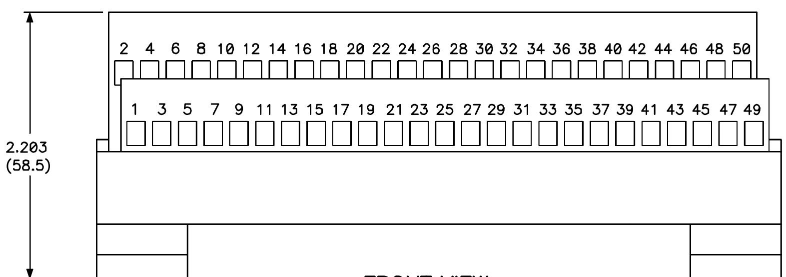
MODEL 5025–552 TERMINATION PANEL SCHEMATIC



TOP VIEW



SIDE VIEW



FRONT VIEW

NOTES:

DIMENSIONS ARE IN INCHES (MILLIMETERS).

TOLERANCE: ±0.020 (±0.5).

MODEL 5025–552 TERMINATION PANEL

4501–464A