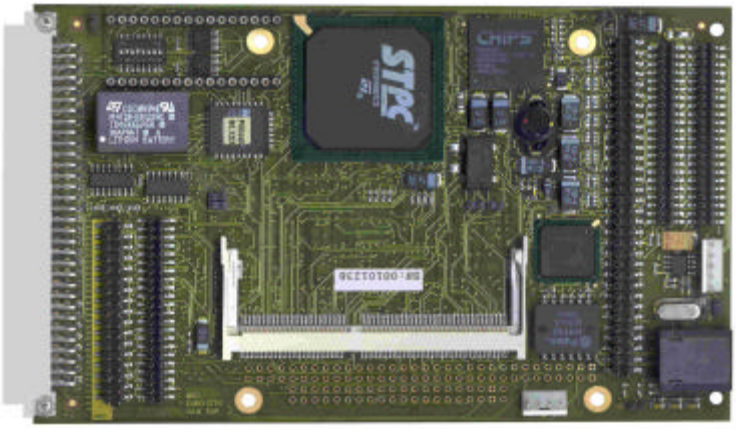
EURO STPC-I

ISA96 (AT96)
All-In-One CPU Card

User's Manual
Version 0.6
Preliminary



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Contents

1. General Information

1.1. Introduction

The EURO STPC-I is an all-in-one single board X86 computer card for the ISA-96 bus (AT-96 option is available).

With an on-chip TFT/CRT XGA controller and an onboard 100BaseT Ethernet controller, the EURO STPC-I packs all the functions of an industrial computer and its display capabilities onto a single, EURO-size (100x160mm) card. This makes the EURO STPC-I an ideal solution for embedded applications.

The EURO STPC-I is based on the STMicroelectronics STPC-Industrial X86 CPU running at 66MHz / 80MHz. The CPU runs at 3.3V consuming very low power .

The board supports 3.3V EDO DRAMs and FPM DRAMs . It provides a 144-pin standard SO-DIMM socket giving you the flexibility to configure your system from 8 MB to 64 MB of DRAM.

The on-chip XGA graphics controller uses up to 4 MB of system memory . Its CRT interface supports graphic windows up to 1280 x 1024 and 16 bpp at 75 Hz. The TFT interface has a maximal programmable resolution of 1024 X 1024 pixels and supports active matrix panels up to 1024 X 768 with 9-, 12- and 18- bit with one and two pixels per clock.

An optional C&T 69000 flat panel / CRT controller with 2 MB internal SDRAM may be used for extended graphic applications. It supports CRT graphic windows up to 1280 x 1024 pixels with 8 bpp color depth at 60 Hz. Its flat panel interface can support a various number of different display types like SS-, DD- STN active TFT-, EL- and plasma panels up to 1280 x 1024 pixels with 8 bpp color depth.

Another onboard device is the PCI 100 MBit Ethernet controller (82559ER). A standard RJ45 100BaseT connector is provided.

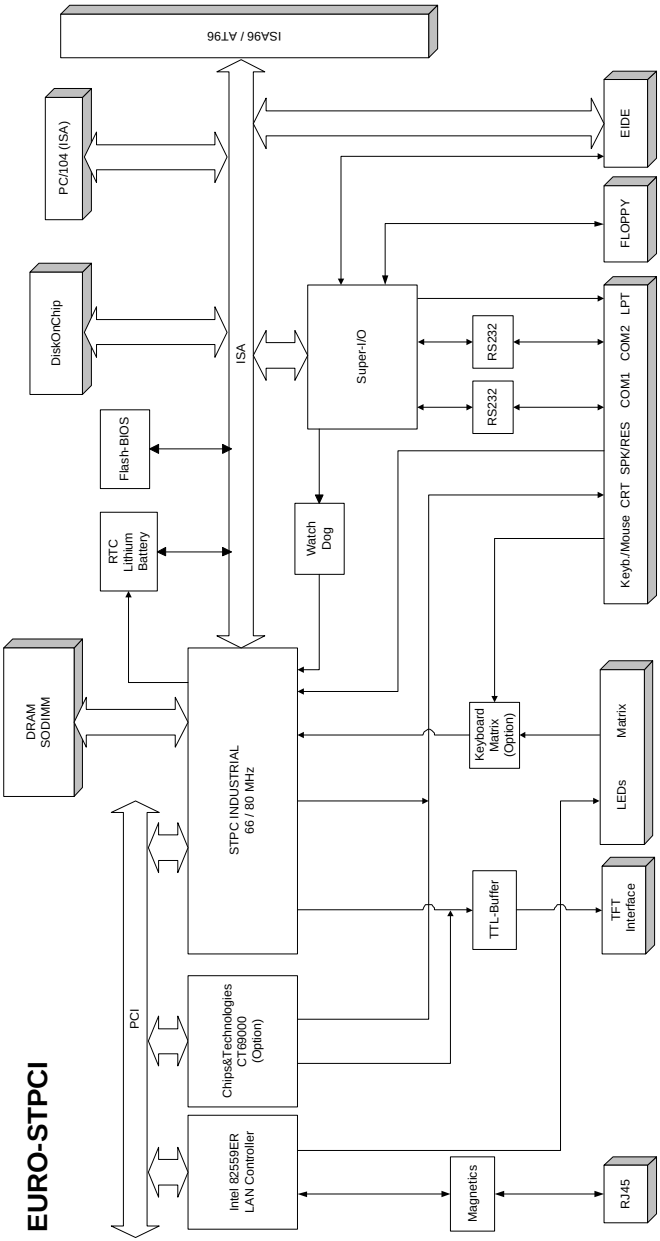
The EURO STPC-I includes a high speed, local bus IDE controller. Up to two IDE devices can be connected, including hard disks up to 8,4 GB, CD-ROM drives, tape backup drives, or other IDE devices.

Onboard features include two high-speed RS-232 serial ports, one bidirectional SPP/EPP/ECP parallel port and one floppy drive controller.

A standard DiskOnChip socket allows to install up to 144MByte flashdisk.

A PC/104 interface (on solder side) and a 8 x 8 matrix keyboard encoder are additional options of the EURO STPC-I card.

1.2. Block Diagram



1.3. Specifications

CPU:

STMicroelectronics STPC Industrial
fully compatible with standard fifth generation x86 processors.
8KB unified instruction and data L1-cache
66/80 MHz, 388-ball PBGA

64-bit DRAM controller supports EDO or FPM memory modules
1 standard 144-pin SO-DIMM socket
4 Mbit, 16 Mbit, 64 Mbit, 3.3 V technology
min. 8 MByte, max. 64 MByte

ISA-Bus Interface:

On-chip ISA Master/Slave controller
ISA96 (optional AT96) - bus
PC/104 (optional, on solder side)

Video:

On-chip 64-bit XGA graphics controller
*Up to 4 MB of system memory (**U**nified **M**emory **A**rchitecture)*
CRT-interface (max. 1280 X 1024, 65536 colors, 75 Hz)
TFT-interface (3.3V or 5 V TTL, max. 1024 X 1024, 18-bit 1pixel/clock or 9-bit 2 pixels/clock)

Optional

Chips & Technology 69000 graphics accelerator
2 MB internal SDRAM for graphics frame buffer
CRT-interface (max. 1280 X 1024, 256 colors, 60 Hz)
Flat panel interface (3,3V or 5V TTL, max. 1280 X 1024, 24-bit 1pixel/clock or 9-bit 2 pixels/clock)
Single-panel, single drive (SS) displays, dual-panel, dual drive (DD) passive STN displays, active TFT/MIN LCD displays, EL panels, plasma panels.

Ethernet (optional):

INTEL 82559ER ethernet controller 10/100 MBit
RJ45-interface

IDE:

Super-I/O controller FDC37C669
Single IDE port (1 master / 1 slave)

Floppy:

Super-I/O controller FDC37C669
Standard floppy disk interface
360kB / 720kB / 1,2MB / 1,44MB

Serial:

Super-I/O controller FDC37C669
2 x RS232 or 1 x RS232 / 1 x IrDA

Parallel:

Super-I/O controller FDC37C669
1 x parallel port (PS/2-compatible / ECP / EPP, configurable via BIOS Setup)

Keyboard, Mouse:

On-chip keyboard / mouse controller
PS2 keyboard interface
PS/2 mouse interface
Optional: 8 x 8 matrix-keyboard controller (KeyWarrior 8 Operator)

BIOS:

256 kByte flash (PLCC32) boot block 29F002
System-BIOS and VGA-BIOS
BIOS recovery support

Flashdisk:

M-Systems DiskOnChip 2000 (32pin socket)

Real Time Clock:

STMicroelectronics MT48T86 RTC
Removable lithium battery (SnapHat)

Power supply:

+5V	*±5%*	
+12V	*±5%*	*only if required externally*
-12V	*±5%*	*only if required for PC/104*

Power supply current:

+5V	*ca. 1,5A*	*board without additional peripherals*
+12V		*depends on PC/104 requirements*
-12V		*depends on PC/104 requirements*

Environment :

Temperature: $T_{ambient}$ *= 0 .. 60°C (non-condensing)*

Mechanical:

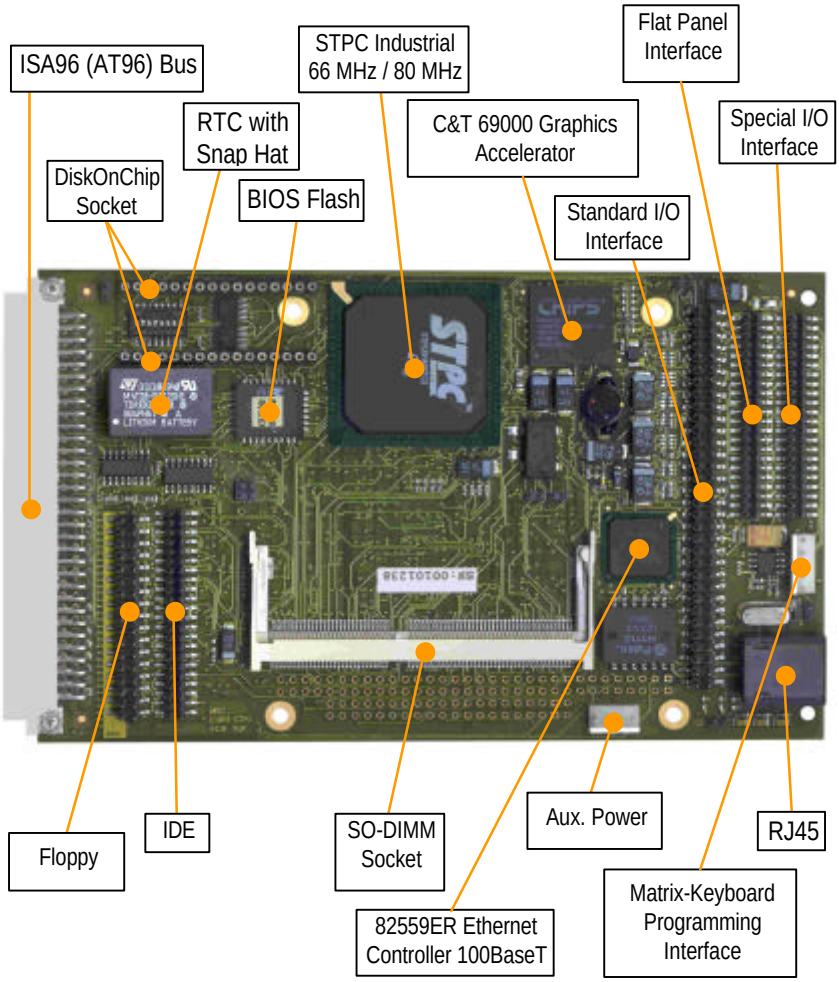
Connectors:

Function	*Type*
ISA96 (AT96) bus	*96 pin VG connector*
Floppy	*34 pin 2,54mm pin header (SMD)*
IDE	*44 pin 2mm pin header (SMD)*
Standard I/O	*64 pin 2,54mm pin header (SMD)*
LCD (digital)	*44 pin 2mm pin header (SMD)*
Special I/O	*44 pin 2mm pin header (SMD)*
Ethernet	*RJ45 100BaseT connector*

Dimensions:

160 x 100 mm
Height: *max. 17 mm (component side)*
max. 3mm (solder side, without PC/104 option)

1.4. Board Layout

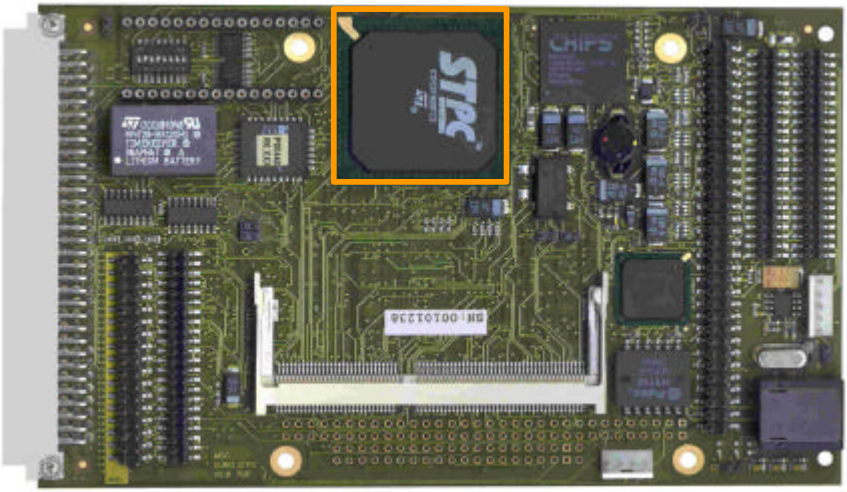


2. Installation

2.1. Jumpers

2.1.1. CPU

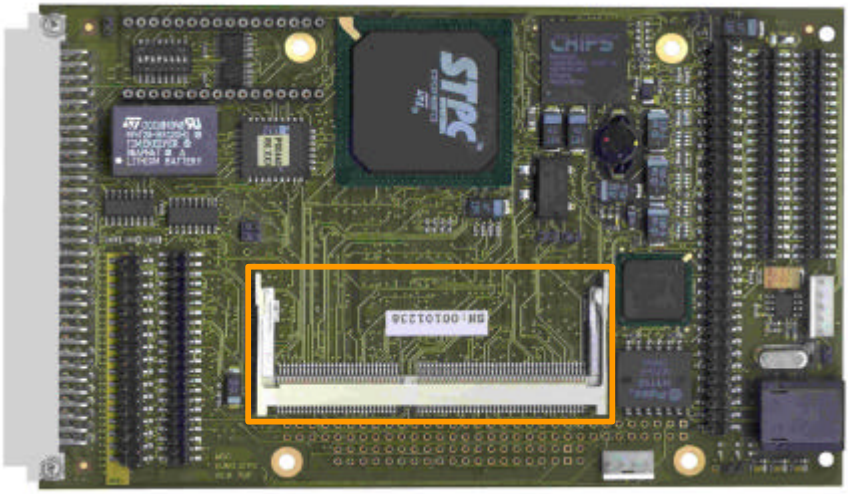
The CPU is a STMicroelectronics STPC Industrial processor in a 388-balls PBGA package. It is soldered so it cannot be removed or exchanged.



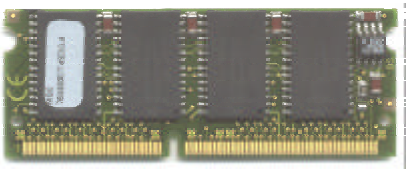
All settings of the CPU are installed by factory, the user does not have to set switches or jumpers.

The PBGA package has excellent thermal parameters, the maximum case temperature is 100°C. The board is shipped with a passive heat sink.

2.1.2. Installing a DRAM SO-DIMM Module



The EURO STPC-I board has a SO-DIMM socket for standard 3,3V SO-DIMM modules (Fast Page Mode or EDO):



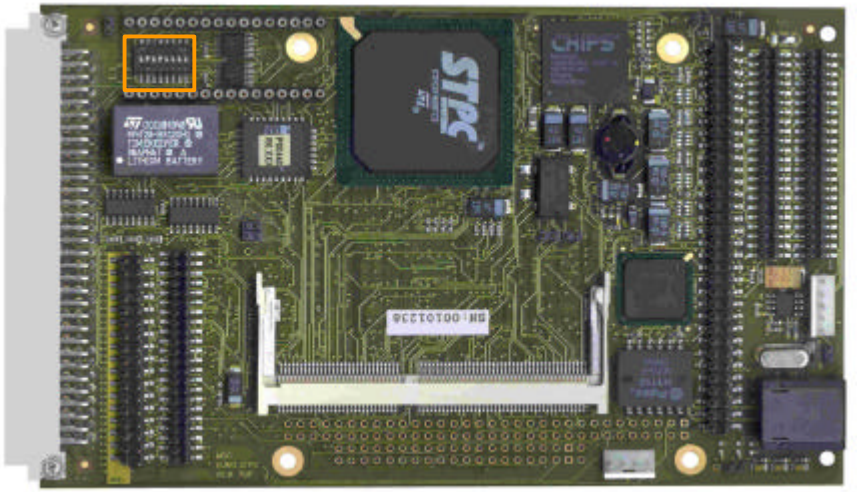
Module organization	Capacity
1M x 64	8 MByte
2M x 64	16 MByte
4M x 64	32 MByte
2 x 4M x 64	64 MByte (*)

(*) Two bank modules only

The following options are available via SETUP:

Fast Page Mode or EDO modules (3.3V).
Access time : 70ns or <=60ns.

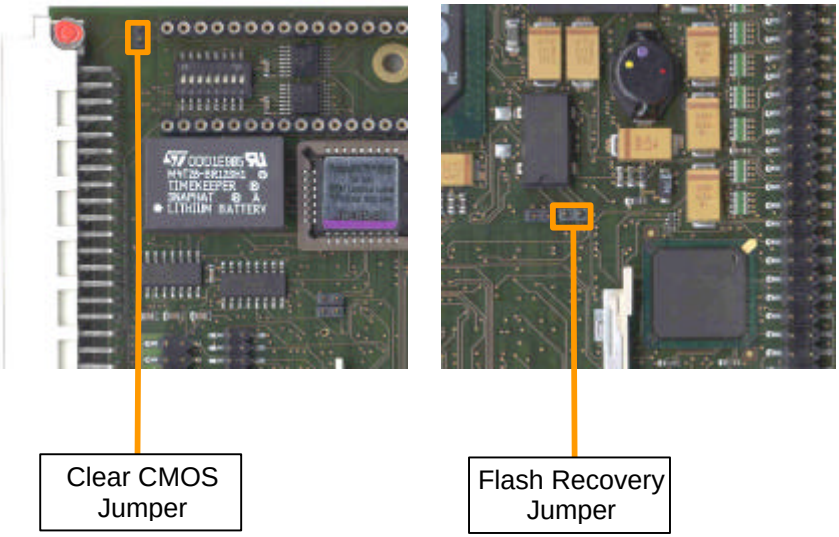
2.1.3. DiskOnChip Address Select



Switch	Address Range 8kB segment	Switch	Address Range 16kB segment
	C8000 .. C9FFF [1]		C8000 .. CBFFF [1]
	CA000 .. CBFFF [1]		not available [2]
	CC000 .. CDFFF [1]		CC000 .. CFFFF [1]
	CE000 .. CFFFF [1]		not available [2]
	D0000 .. D1FFF [3]		D0000 .. D3FFF
	D2000 .. D3FFF		not available [2]
	D4000 .. D5FFF		D4000 .. D7FFF
	D6000 .. D7FFF		not available [2]
	D8000 .. D9FFF		D8000 .. DBFFF
	DA000 .. DBFFF		not available [2]
	DC000 .. DCFFF		DC000 .. DFFFF
	DE000 .. DFFFF		not available [2]

[1] Do not use these settings. Otherwise there will be conflicts with VGA-BIOS.
[2] Device will not be selected, do not use these settings.
[3] Factory default setting.

2.1.4. Clear CMOS Data And Flash Recovery Jumper



Clear CMOS Jumper:

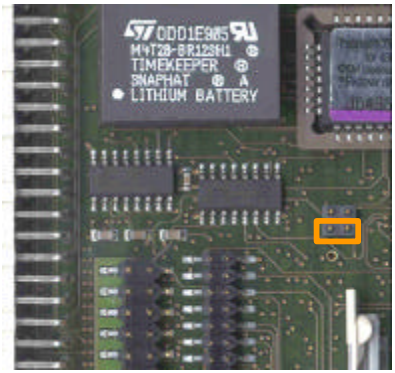
To clear the contents of the CMOS (setup configuration) the following procedure has to be done :

1. *Switch off power.*
2. *Install jumper.*
3. *Switch on power again and wait for a few seconds.*
4. *Switch off power.*
5. *Remove jumper.*

Flash Recovery Jumper:

If removed, the flash recovery jumper forces a BIOS update. A flash crisis recovery disk has to be inserted into floppy drive <A>.

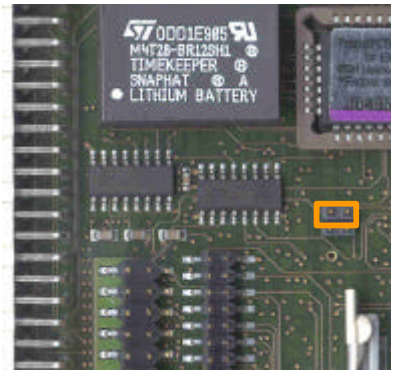
2.1.5. Disable Boot Block Write Protection



open	BIOS boot block write protected (factory default)
closed	BIOS boot block write unprotected

Note : +12V from the ISA96 (AT96) bus is required for boot block programming.

2.1.6. COM2 Disable



open	COM2 enabled (factory default)
closed	COM2 disabled

Note : Close this jumper if the IrDA interface on the special I/O connector should be used.

2.1.7. STPC Industrial Graphics Controller Disable

open	STPC graphics controller enabled
closed	STPC graphics controller disabled

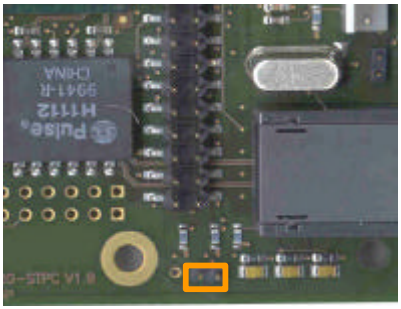
This Jumper must be closed if an external graphics adapter card will be installed.
If the C&T69000 graphics accelerator option is assembled this jumper must remain closed.

2.1.8. C&T69000 Graphics Controller Disable (optional)

open	C&T69000 enabled
closed	C&T69000 disabled

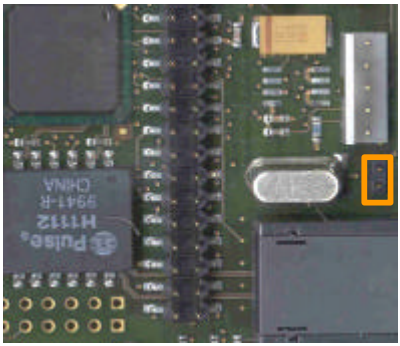
This jumper must be closed if an external graphics adapter card will be installed.

2.1.9. Ethernet Controller Disable (optional)



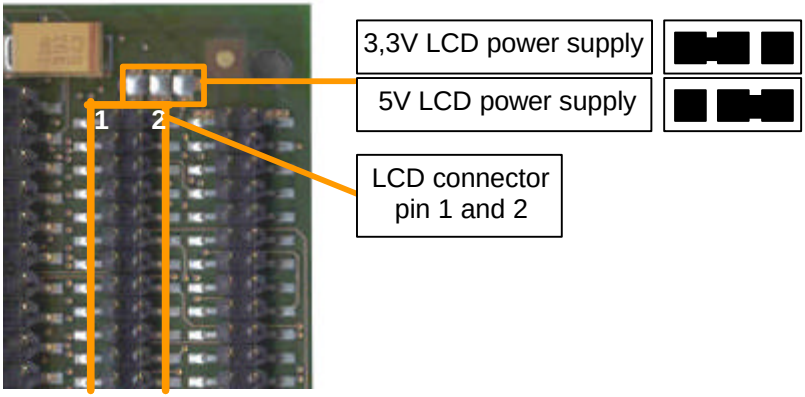
open	ethernet-controller enabled
closed	ethernet-controller disabled

2.1.10. Matrix-Keyboard Controller Disable (optional)

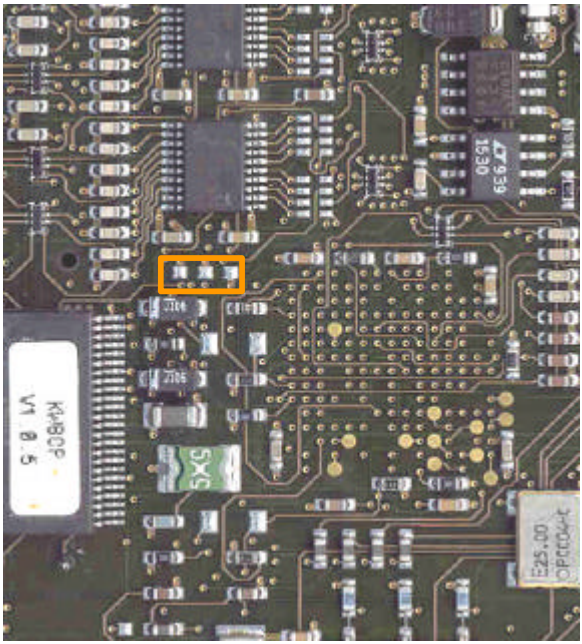


open	matrix-keyboard enabled
closed	matrix-keyboard disabled

2.1.11. LCD Power Supply



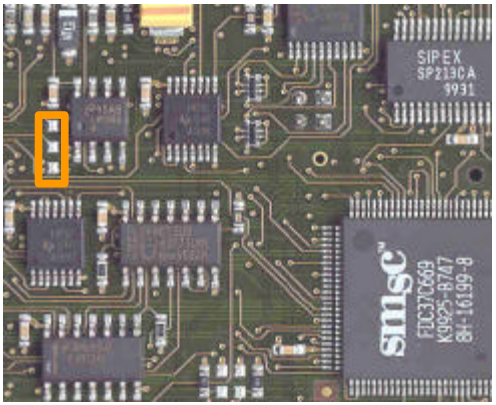
2.1.12. LCD Driver Level



3.3V LCD driver level

5V LCD driver level

2.1.13. LCD Back-Light Enable Polarity



active high (BLIGHT)

active low (BLIGHT#)

The back-light enable signal (BLIGHT or BLIGHT#) is on pin 6 of the LCD connector.

2.2. Watchdog

The EURO STPC-I board has a watchdog function implemented. If the watchdog is enabled a counter is started which creates a reset if it is not re-triggered within a defined time interval (1s).

The watchdog is controlled by the General Purpose I/O-Port of the STPC Industrial processor .

Bit	Description	Low (0)	High (1)
0	watchdog trigger	rising or falling edge triggers	
1	watchdog enable	disabled	enabled
2	not used		
3	not used		
4	back-light control	off	on
5	not used		
6	not used		
7	flash write enable	disabled	enabled

The port is accessed via I/O addresses 22H (write), 23H (read) and index 7BH :

enable_watchdog:

```
Write 7BH to 22H        ; set index to general purpose register
Read from 23H
SetBit 1
Write to 23H            ; enable watchdog
```

retrigger_watchdog: ; has to be done in 1 second

```
Write 7BH to 22H        ; set index to general purpose register
Read from 23H
```

The backlight enable signal (BLIGHT or BLIGHT#) is on pin 6 of the LCD connector.

```
SetBit 6
Write to 23H            ; create rising edge
```

read_register:

```
Write 7BH to 22H        ; set index to general purpose register
Read from 23H           ; read data
```

disable_watchdog:

```
Write 7BH to 22H        ; set index to general purpose register
Read from 23H
ResetBit 1
Write to 23H            ; disable watchdog
```

2.3. Interrupts, DMA Channels, Upper Memory

Interrupts:

IRQ	used for	available	comment
0	timer 0	no	
1	keyboard	no	
2	slave 8259	no	
3	COM2	no	(1)
4	COM1	no	(1)
5	-	yes	
6	floppy disk controller	no	(1)
7	LPT1	no	(1)
8	real time clock	no	
9	(ethernet controller)	(yes)	(2)
10	-	yes	
11	-	yes	
12	PS/2 mouse	no	
13	floating point unit	no	
14	IDE 0	no	(1)
15	-	yes	

(1) If the device is disabled in SETUP, the interrupt is available.
(2) If the PCI-ethernet controller is present, typically IRQ9 is allocated by the BIOS. This can be changed via SETUP.

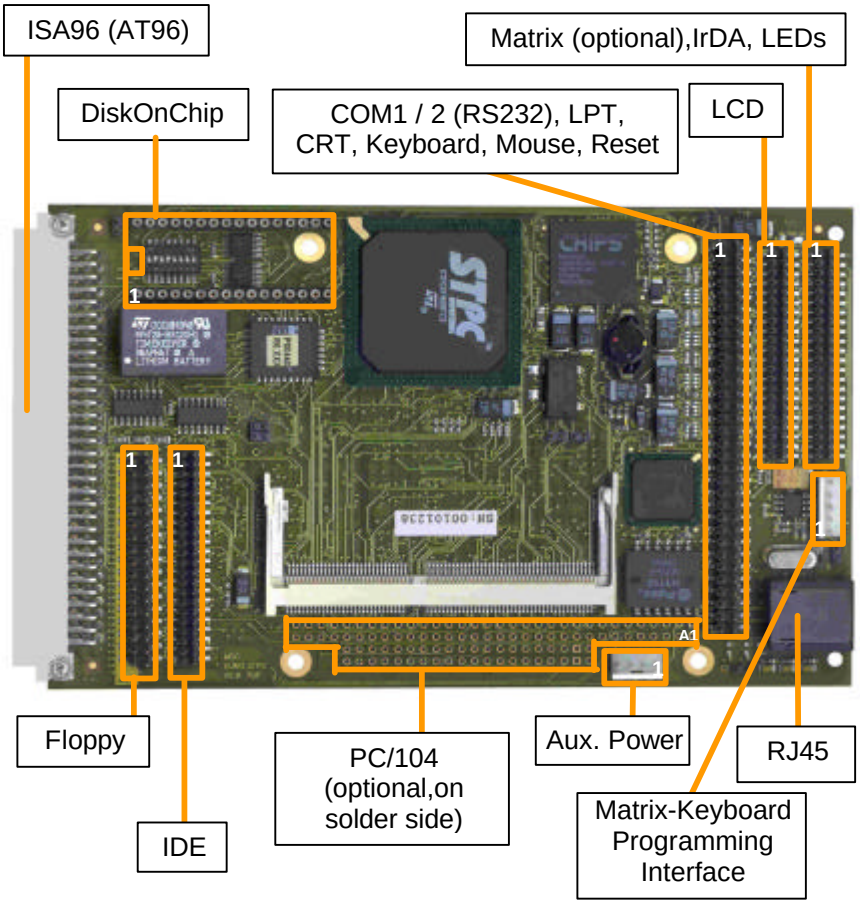
DMA channels :

DMA	used for	available	comment
0	- - -	yes	
1	- - -	yes	
2	floppy disk controller	no	
3	- - -	yes	
4	cascade	no	
5..7	- - -	yes	

Upper Memory Map:

Upper Memory	Used For	Available	Comment
C0000h..CBFFFh	VGA BIOS	no	
CC000h..DFFFFh		yes	ISA bus or shadow RAM (DiskOnChip)
E0000h..EFFFFh		(yes)	used by system BIOS during POST
F0000h..FFFFFh	Sys. BIOS	no	

2.4. Connectors Overview



2.4.1. ISA96 (AT96, optional)

Pin	a	b	c
1	GND	MASTER# (SBHE#)	IOCHCK#
2	RESET	SD15 (MEMCS16#)	SD7
3	+5V	SD14 (SA23)	SD6
4	IRQ9	SD13 (IOCS16#)	SD5
5	MEMR# (LA17/n.c.)	SD12 (SA22)	SD4
6	DRQ2	SD11 (IRQ10)	SD3
7	-12V	SD10 (SA21)	SD2
8	/0WS	SD9 (IRQ11)	SD1
9	+12V	SD8 (SA20)	SD0
10	GND	SBHE# (IRQ12)	IOCHRDY
11	SMEMW#	LA23 (VBAT)	AEN
12	SMEMR#	LA22 (IRQ15)	SA19
13	IOW#	LA21 (LA19/n.c.)	SA18
14	IOR#	LA20 (IRQ14)	SA17
15	DACK3#	LA19 (LA18/n.c.)	SA16
16	DRQ3	LA18 (DACK0#)	SA15
17	DACK1#	LA17 (MEMR#)	SA14
18	DRQ1	/DACK7 (DRQ0)	SA13
19	REFSH#	DRQ7 (MEMW#)	SA12
20	SYSCLK	DACK6# (DACK5#)	SA11
21	IRQ7	DRQ6 (SD8)	SA10
22	IRQ6	DACK5# (DRQ5)	SA9
23	IRQ5	DRQ5 (SD9)	SA8
24	IRQ4	DACK0# (DACK6#)	SA7
25	IRQ3	DRQ0 (D10)	SA6
26	DACK2#	MEMCS16# (DRQ6)	SA5
27	TC	IOCS16# (SD11)	SA4
28	BALE	IRQ15 (SD12)	SA3
29	+5V	IRQ14 (SD13)	SA2
30	OSC	IRQ12 (SD14)	SA1
31	MEMW# (GND)	IRQ11 (SD15)	SA0
32	GND (DRQ7)	IRQ10 (MASTER#)	GND (DACK7#)

2.4.2. PC/104 (optional)

Pin	A	B	C	D
0	—	—	GND	GND
1	IOCHCK#	GND	SBHE#	MEMS16#
2	SD7	RESET	LA23	IOCS16#
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	MEMR#	LA20	IRQ12B
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12V	LA18	IRQ14
8	SD1	0WS#	LA17	DACK0#
9	SD0	+12V	MRDC#	DRQ0
10	IOCHRDY	GND	MWTC#	DACK5#
11	AEN	SMEMW#	SD8	DRQ5
12	SA19	SMEMR#	SD9	DACK6#
13	SA18	IOW#	SD10	DRQ6
14	SA17	IOR#	SD11	DACK7#
15	SA16	DACK3#	SD12	DRQ7
16	SA15	DRQ3	SD13	+5 V
17	SA14	DACK1#	SD14	MASTER#
18	SA13	DRQ1	SD15	GND
19	SA12	REFSH#	KEY	GND
20	SA11	SYSCLK	—	—
21	SA10	IRQ7	—	—
22	SA9	IRQ6	—	—
23	SA8	IRQ5	—	—
24	SA7	IRQ4	—	—
25	SA6	IRQ3	—	—
26	SA5	DACK2#	—	—
27	SA4	TC	—	—
28	SA3	BALE	—	—
29	SA2	+5V	—	—
30	SA1	OSC	—	—
31	SA0	MEMW#	—	—
32	GND	GND	—	—

2.4.3. IDE

Pin	Name	Pin	Name
1	IDE_RESET#	2	GND
3	DATA7	4	DATA
5	DATA6	6	DATA9
7	DATA5	8	DATA10
9	DATA4	10	DATA11
11	DATA3	12	DATA12
13	DATA2	14	DATA13
15	DATA1	16	DATA14
17	DATA0	18	DATA15
19	GND	20	n.c.
21	n.c.	22	GND
23	IDE_IOW#	24	GND
25	IDE_OR#	26	GND
27	IORDY	28	BALE
29	n.c.	30	GND
31	INTRQ	32	n.c.
33	IDE_ADR1	34	/IOCS16
35	IDE_ADR0	36	IDEADR2
37	IDE_CS0#	38	IDE_CS1
39	IDE_ACTIV#	40	GND
41	+5 V	42	+5 V
43	GND	44	reserved

2.4.4. Floppy

Pin	Name	Pin	Name
1	GND	2	DENSEL#
3	GND	4	n.c.
5	GND	6	n.c.
7	GND	8	INDEX#
9	GND	10	MOTOR1#
11	GND	12	DRVSEL2#
13	GND	14	DRVSEL1#
15	GND	16	MOTOR2#
17	GND	18	DIR
19	GND	20	STEP#
21	GND	22	WRDATA#
23	GND	24	WRGATE#
25	GND	26	TRACK 0#
27	GND	28	WRPROTECT#
29	GND	30	RDDATA#
31	GND	32	HEADSEL
33	GND	34	DISKCHANGE#

2.4.5. COM1, COM2, LPT, CRT, Keyboard/Mouse, Reset

Pin	Name	Pin	Name
1	COM1: DCD1	2	COM1: DSR1
3	COM1: RXD1#	4	COM1: RTS1
5	COM1: TXD1#	6	COM1: CTS1
7	COM1: DTR1	8	COM1: RI1
9	GND	10	COM2: DCD2
11	COM2: DSR2	12	COM2: RXD2#
13	COM2: RTS2	14	COM2: TXD2#
15	COM2: CTS2	16	COM2: DTR2
17	COM2: RI2	18	GND
19	LPTSTROBE#	20	LPTAFD#
21	LPTD0	22	LPTERR#
23	LPTD1	24	LPTINIT#
25	LPTD2	26	LPTSLIN#
27	LPTD3	28	GND
29	LPTD4	30	GND
31	LPTD5	32	GND
33	LPTD6	34	GND
35	LPTD7	36	GND
37	LPTACK#	38	GND
39	LPTBUSY	40	GND
41	LPTPE	42	GND
43	LPTSLCT	44	n.c.
45	HDLED#	46	+5 V
47	SPEAKEROUT#	48	n.c.
49	RESETIN#	50	n.c
51	KEYBOARD DATA	52	GND
53	KEYBOARD CLOCK	54	MOUSE DATA
55	CRT RED	56	MOUSE CLOCK
57	CRT BLUE	58	CRT GREEN
59	GND	60	n.c.
61	n.c	62	n.c.
63	CRT HSYNC	64	CRT VSYNC

Note: COM2 port can be disabled by a jumper in order to use the IrDA interface at the special I/O connector. Refer to chapters 2.1.6 and 2.4.6 for further information.

2.4.6. Matrix-Keyboard (optional), IrDA, LEDs (Special I/O Connector)

Pin	Name	Pin	Name
1	(KSI0)	2	(KSI1)
3	(KSI2)	4	(KSI3)
5	(KSI4)	6	(KSI5)
7	(KSI6)	8	(KSI7)
9	(KSO0)	10	(KSO1)
11	(KSO2)	12	(KSO3)
13	(KSO4)	14	(KSO5)
15	(KSO6)	16	(KSO7)
17	(NUM LED) *	18	(CAPS LED) *
19	n.c.	20	(SCROLL LED) *
21	GND	22	+5 V
23	KEYBOARD2 CLOCK	24	KEYBOARD2 DATA
25	MOUSE2 CLOCK	26	MOUSE2 DATA
27	GND	28	+5 V
29	IRTX	30	IRRX
31	n.c.	32	n.c.
33	n.c.	34	n.c.
35	n.c.	36	GND
37	n.c.	38	n.c.
39	n.c.	40	GND
41	ETH_BUSY_LED	42	ETH_LINK_LED
43	ETH_SPEED_LED	44	n.c.

*) Open drain LED driver outputs, each capable of sinking 16 mA maximum.

Note: Do not connect multiple keyboards and mice at the PS/2 interface of the standard I/O Connector (chapter 2.3.5) and at the PS/2 interface of the special I/O connector. One PS/2 keyboard at the standard I/O connector or the Special I/O Connector and one matrix-keyboard may be used in parallel. In that case the PS/2 keyboard must be connected after the system has booted.

Note: In order to use the IrDA interface the COM2 port must be disabled. For more information refer to chapter 2.1.6 and 2.4.5.

2.4.7. Flat Panel Interface

2.4.7.1. STPC Industrial TFT Interface

Pin	Name	Pin	Name
1	+5V /3,3V (*)	2	+5V /3,3V (*)
3	ENVDD#	4	ENVEE#
5	DE	6	BLIGHT / BLIGHT# (*)
7	HSLP	8	FLM
9	GND	10	SHFCLK
11	GND	12	GND
13	n.c.	14	n.c.
15	B0 [LSB]	16	B1
17	B2	18	B3
19	B4	20	B5 [MSB]
21	n.c.	22	n.c.
23	G0 [LSB]	24	G1
25	G2	26	G3
27	G4	28	G5 [MSB]
29	n.c.	30	n.c.
31	R0 [LSB]	32	R1
33	R2	34	R3
35	R4	36	R5 [MSB]
37	GND	38	GND
39	+5V	40	+5V
41	GND	42	GND
43	DDC SDA	44	DDC CLK

(*) +5V / +3,3V jumper selectable
(*) BLIGHT# / BLIGHT polarity jumper selectable

TFT Flat Panel Signal Description:

Name	Pin(s)	Description
+5V / 3,3V	1	TFT Power (jumper)
+5V / 3,3V	2	TFT Power (jumper)
ENVDD#	3	Flat Panel VDD Enable
ENVEE#	4	Flat Panel VEE Enable
DE	5	DE = DE/M/Blank#
BLIGHT / BLIGHT#	6	Back-Light Enable (jumper)
HSLP	7	VHSLP = LP/CL1/DE/Blank# (HSYNC)
FLM	8	VVSFLM = FLM (VSYNC)
SHFCLK	10	Shift Clock
B[0:5]	15 - 20	Blue Output (6-bits, MSB aligned)
G[0:5]	23 - 28	Green Output (6-bits, MSB aligned)
R[0:5]	31 - 36	Red Output (6-bits, MSB aligned)
DDC SDA	43	Direct Data Channel Serial Link Data
DDC CLK	44	Direct Data Channel Serial Link Clock
GND	9,11,12,37,38,41,42	Ground
+ 5V	39,40	5 Volts fix
n.c.	13,14,21,22,29,30	not connected

2.4.7.2. C&T69000 LCD Interface (Option)

Pin	Name	Pin	Name
1	+5V /3,3V (*)	2	+5V /3,3V (*)
3	ENVDD#	4	ENVEE#
5	DE	6	BLIGHT / BLIGHT# (*)
7	HSLP	8	FLM
9	GND	10	SHFCLK
11	GND	12	GND
13	VPNL0	14	VPNL1
15	VPNL2	16	VPNL3
17	VPNL4	18	VPNL5
19	VPNL6	20	VPNL7
21	VPNL8	22	VPNL9
23	VPNL10	24	VPNL11
25	VPNL12	26	VPNL13
27	VPNL14	28	VPNL15
29	VPNL16	30	VPNL17
31	VPNL18	32	VPNL19
33	VPNL20	34	VPNL21
35	VPNL22	36	VPNL23
37	GND	38	GND
39	+5V	40	+5V
41	GND	42	GND
43	DDC SDA	44	DDC CLK

(*) +5V / +3,3V jumper selectable
(*) BLIGHT# / BLIGHT polarity jumper selectable

LCD signal description :

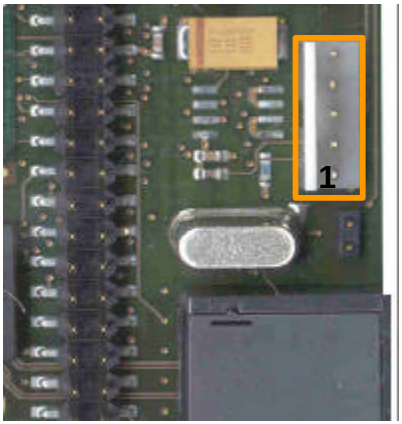
Name	Pin(s)	
+5V / 3,3V	1,2	LCD Power (jumper)
ENVDD#	3	Flat Panel VDD Enable
ENVEE#	4	Flat Panel VEE Enable
DE	5	DE = DE/M/Blank#
BLIGHT / BLIGHT#	6	Back-Light Enable (jumper)
HSLP	7	VHSLP = LP/CL1/DE/Blank# (HSYNC)
FLM	8	VVSFLM = FLM (VSYNC)
SHFCLK	10	Shift Clock
VPNL[0:23]	13 - 36	Panel Data Outputs
DDC SDA	43	Direct Data Channel Serial Link Data
DDC CLK	44	Direct Data Channel Serial Link Clock
GND	9,11,12,37,38,41,42	Ground
+ 5V	39,40	5 Volts fix

Mapping of the LCD-signals for different display types:

	Display-Type	**Mono SS**	**Mono DD**	**Mono DD**	**Color TFT**	**Color TFT**
	Width	**8-bit**	**8-bit**	**16-bit**	**9/12/16-bit**	**18/24 bit**
	Pixelds/Clock	**8**	**8**	**16**	**1**	**1**
Pin	**Name**					
13	VPNL0		UD3	UD7	B0	B0
14	VPNL1		UD2	UD6	B1	B1
15	VPNL2		UD1	UD5	B2	B2
16	VPNL3		UD0	UD4	B3	B3
17	VPNL4		LD3	UD3	B4	B4
18	VPNL5		LD2	UD2	G0	B5
19	VPNL6		LD1	UD1	G1	B6
20	VPNL7		LD0	UD0	G2	B7
21	VPNL8	P0		LD7	G3	G0
22	VPNL9	P1		LD6	G4	G1
23	VPNL10	P2		LD5	G5	G2
24	VPNL11	P3		LD4	R0	G3
25	VPNL12	P4		LD3	R1	G4
26	VPNL13	P5		LD2	R2	G5
27	VPNL14	P6		LD1	R3	G6
28	VPNL15	P7		LD0	R4	G7
29	VPNL16					R0
30	VPNL17					R1
31	VPNL18					R2
32	VPNL19					R3
33	VPNL20					R4
34	VPNL21					R5
35	VPNL22					R6
36	VPNL23					R7

	Display-Type	**Color STN SS**	**Color STN SS**	**Color STN DD**	**Color STN DD**	**Color STN DD**
	Width	**8-bit (X4bP)**	**16-bit (4bP)**	**8-bit (4bP)**	**16-bit (4bP)**	**24 bit**
	Pixels/Clock	**2-2/3**	**5-1/3**	**2-2/3**	**5-1/3**	**8**
Pin	**Name**					
13	VPNL0	R1	R1	UR1	UR0	UR0
14	VPNL1	B1	G1	UG1	UG0	UG0
15	VPNL2	G2	B1	UB1	UB0	UB0
16	VPNL3	R3	R2	UR2	UR1	LR0
17	VPNL4	B3	G2	LR1	LR0	LG0
18	VPNL5	G4	B2	LG1	LG0	LB0
19	VPNL6	R5	R3	LB1	LB0	UR1
20	VPNL7	B5	G3	LR2	LR1	UG1
21	VPNL8	SHFCLKU	B3		UG1	UB1
22	VPNL9		R4		UB1	LR1
23	VPNL10		G4		UR2	LG1
24	VPNL11		B4		UG2	LB1
25	VPNL12		R5		LG1	UR2
26	VPNL13		G5		LB1	UG2
27	VPNL14		B5		LR2	UB2
28	VPNL15		R6		LG2	LR2
29	VPNL16					LG2
30	VPNL17					LB2
31	VPNL18					UR3
32	VPNL19					UG3
33	VPNL20					UB3
34	VPNL21					LR3
35	VPNL22					LG3
36	VPNL23					LB3

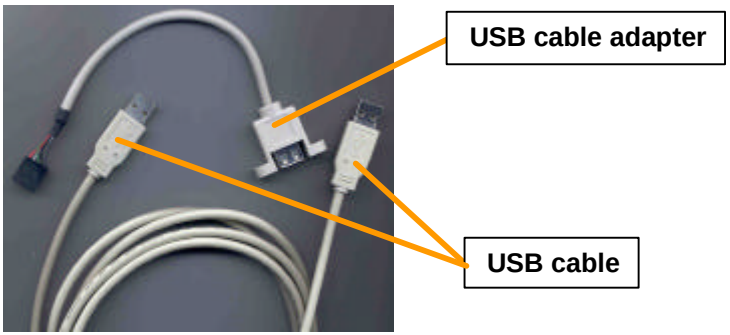
2.4.8. Matrix-Keyboard Programming Connector



Pin	Name
1	n.c.
2	USB-
3	USB+
4	GND
5	n.c.

In order to download a scan code table into the matrix-keyboard controller's E^2PROM the following equipment is required:

- One USB cable adapter.
- One standard USB cable



- A host computer with Win98 operating system and USB support.
- The utility program *KeyWarriorFlex.exe.*
- Your custom scan code table *Key_Table.asm.*

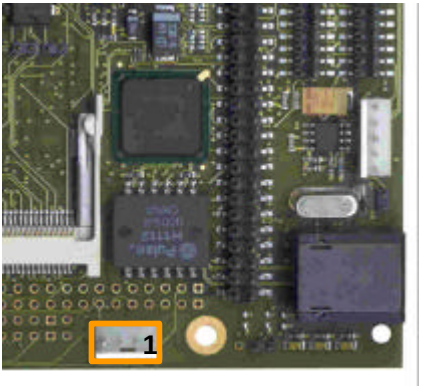
Matrix Keyboard Programming Procedure.

The matrix keyboard controller programming interface has a protection circuit. The board should neither be powered on nor should it be plugged into a backplane during the programming procedure.

1. Boot Windows98 on the host computer.
3. Copy the utility program and the scan code table to the host computer or a floppy disk.
4. Plug the USB adapter to the 5 position single row header on EURO STPC-I board.
   Take care that the red cable of the USB adapter cable is connected to pin 1 of the header.
5. Connect the host computer and the EURO STPC-I board via the standard USB cable.
   KeyWarrior 8 Operator will be recognized by Windows98 as a new device. Follow the setup procedure and install the HID driver for Human Interface Devices if necessary (only during the very first installation).
6. Start the utility program *KeyWarriorFlex.exe*.
7. Disconnect the USB cable at on side.
8. Load your scan code table *Key_Table.asm* from the menu File -> open table...
9. Again reconnect the USB cable. The scan code table will be loaded into the KeyWarrior's E^2PROM. The utility program will show you the progress of the download.
10. Disconnect the USB cable and USB adapter.

For further information how to create a scan code table refer to
http://www.codemercs.com/KeyWarriorResE.html

2.4.9. Auxiliary Power Connector



Pin	Name
1	+ 5V
2	GND
3	GND
4	+ 12V

This connector may be used e.g. to supply a back-light inverter or a floppy disk with +12V or + 5V power.

3. System Software

3.1. System BIOS

PhoenixBIOS 4.0:

- Plug & Play (PCI, ISA)
- PCI Auto Configuration (PCI 2.1)
- DRAM configuration via Setup
- BIOS Update via floppy incl. Crisis Recovery in case of a damaged system BIOS
- Quick Boot
- System and Setup Password

3.2. Utility Programs

3.2.1. Display Configuration Utility

For display configuration the DOS utility *ESTPCCFG.EXE* is used. Depending on the on-board graphics controller type the program options are different.

STPC-I graphics controller:

ESTPCCFG V1.01 - (c) MSC Vertriebs GmbH, 2001

ESTPCCFG [/,-][command] [file]
Command:
h / ? help screen
info displays EEPROM information string
load writes a display configuration file to EEPROM
Example:
write configuration file stpc64.dat to EEPROM
ESTPCCFG -load stpc64.dat

stpc64.dat is for 640 X 480 TFT color displays and stpc80.dat is for 800 X 600 TFT color panels.
Both files will install simultaneous TFT and CRT display mode.

C&T69000 graphics accelerator:

ESTPCCFG V1.01 - (c) MSC Vertriebs GmbH, 2001

Syntax: ESTPCCFG [/,-][command] [[/,-][command] .. [/,-][panel=][#]]
Command:
- h / ? help screen
- info displays C&T-VGA-Controller-Typ and EEPROM data

Boot options with /save or temporarily switches (without /save)
- e[+/-] expansion ON or OFF c[+/-] centering ON or OFF
- lin toggle linear line replication mode
- p[on/off] panel/crt ON or OFF (at boot)

switch to display / boot display:
- [s],[sim] simultaneous [fp] flatpanel [crt] crt display

Boot options use with command /save to store! Active after reboot.
- a[+/-] auto boot on crt, if crt is attached ON or OFF
- fr toggle force fast refresh (dos mode)
- save save to eeprom
- panel= number of panel entry (1 - 16), use /save to store!

Example:
save to eeprom with panel index 6, expansion and centering on
ESTPCCFG -save -e+ -c+ -panel=6

Panel Table (C&T69000 only):

Entry#	Display Type
Type_01	1024x768 Dual Scan STN Color
Type_02	1280x1024 TFT Color
Type_03	640x480 Dual Scan STN Color
Type_04	800x600 Dual Scan STN Color
Type_05	640x480 Sharp 16-Bit TFT Color
Type_06	640x480 18-Bit TFT Color
Type_07	1024x768 TFT Color 2p/clk
Type_08	800x600 TFT Color
Type_09	800x600 TFT Color 18 Bit
Type_10	800x600 TFT Color
Type_11	800x600 Dual Scan STN Color
Type_12	800x600 Dual Scan STN Color
Type_13	1024x768 TFT Color 1p/clk
Type_14	1280x1024 Dual Scan STN Color
Type_15	1024x600 Dual Scan STN Color
Type_16	1024x600 TFT Color

The display parameters are stored in a serial E^2PROM and will be read by the graphics controller during the next system boot.

3.2.2. Matrix Keyboard Programming Utility

The matrix keyboard controller KeyWarrior 8 Operator uses a master translation table to translate the physical scan codes of a key into a logical scan code.
This master translation table can be loaded into the controller by a Win98 programming utility called *KeyWarriorFlex.exe.*
The table must be loaded only once and resides in the chip until it will be overwritten.
For further information how to create a master translation table refer to http://www.codemercs.com/KeyWarriorResE.html.
Also refer to chapter 2.3.8. for detailed information about the programming procedure.