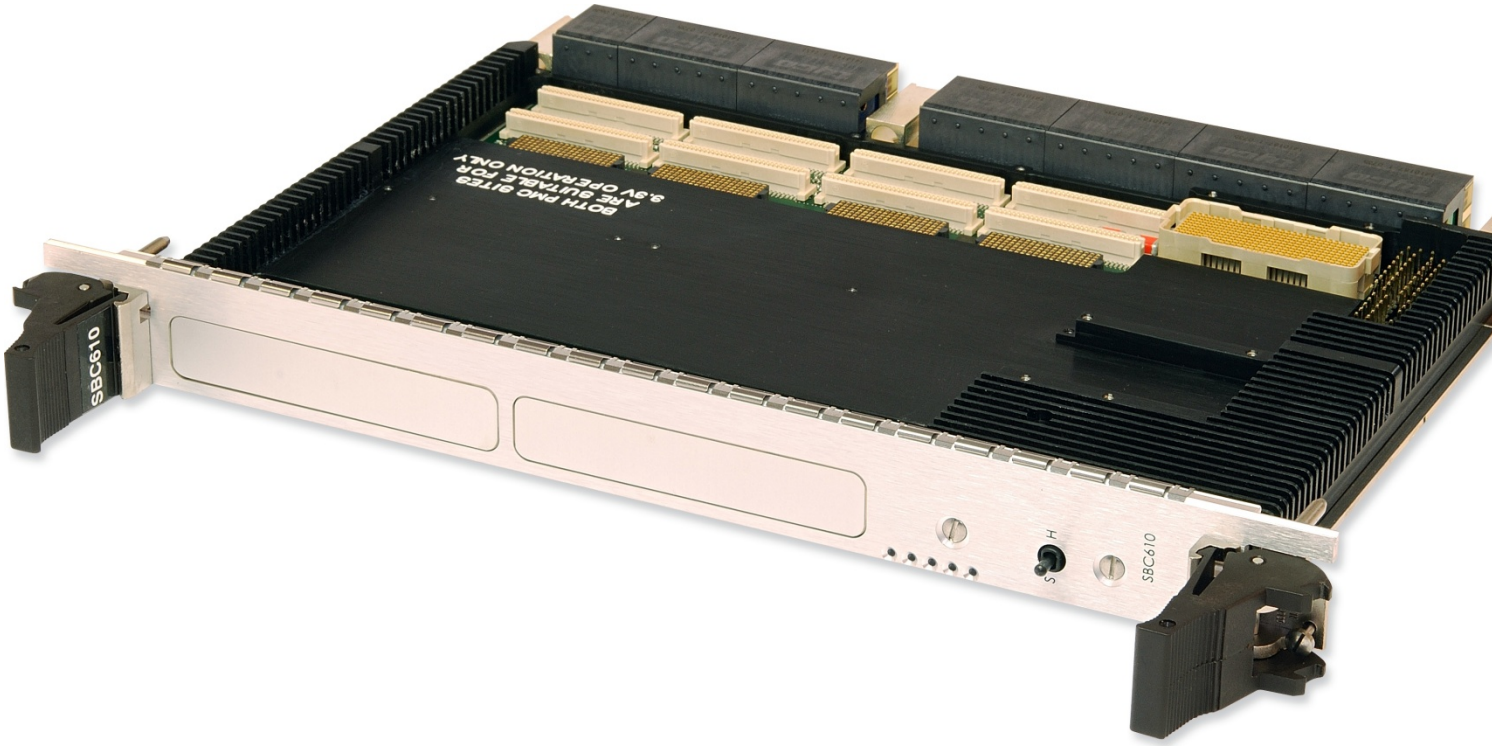
GE
Intelligent Platforms

# Hardware Reference Manual

## SBC610 6U VPX Single Board Computer

## Edition 2

Publication No. SBC610-0HH/2




imagination at work

## Document History

| Edition | Date | Board Artwork Revision |
|---|---|---|
| First | July 2008 | Rev 1 |
| 1DF | March 2010 | Rebranding only, no technical content change |
| 2 | October 2012 | Rev 4 |

## Waste Electrical and Electronic Equipment (WEEE) Returns

GE Intelligent Platforms Limited is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

GE Intelligent Platforms Limited will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

# About This Manual

## Conventions

### Notices

This manual uses the following types of notice:

NOTE
Notes call attention to important features or instructions.

WARNING
Warnings alert you to the risk of severe personal injury.

CAUTION
Cautions alert you to system danger or loss of data.

TIP
Tips give guidance on procedures that may be tackled in several ways.

LINK
Links go to other documents or websites. The purple link color may also be used within a body of text or paragraph to indicate a link (or hyperlink) to a different part of the same document.

### Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a "D" subscript and binary numbers have a "b" subscript. The prefix "0x" shows a hexadecimal number, following the 'C' programming language convention. Thus:

One dozen = $12_D$ = 0x0C = $1100_b$

The multipliers "k", "M" and "G" have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when "K", "M" and "G" mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

NOTE
When describing transfer rates, "k", "M" and "G" mean $*10^3$, $*10^6$ and $*10^9$ *not* $*2^{10}$, $*2^{20}$ and $*2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n the LSB. PCI and VME terminology follows the more familiar convention that bit 0 is the LSB and n the MSB.

### Text

Signal names ending with a tilde (~) denote active low signals; all other signals are active high. "N" and "P" denote the low and high components of a differential signal respectively.

# Further Information

## GE Intelligent Platforms Documents

This document is distributed via the internet. You may register for access to all manuals via the website whose link is given overleaf.

LINKS

PMC Installation Note, publication number HN4/3-99.

AFIX Family Product Manual, publication number AFIX-0HH.

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH.

AXISFlow Programmer's Guide, publication number AXISFLOW-0HU.

Radstone Signal Processing Library Manual, publication number RSPL-0HL.

Vector Signal and Image Processing Library Manual, publication number VSIPL-0HL.

AXISView Applications Software User Guide, publication number AXISVIEW-0HU.

NOTE

Cross-document links are intended for use where the document files are saved under their original file names in the same directory on a server, PC hard drive, or similar. If accessing this document via the GE website, cross-doc links will not work.

## Third Party Documents

Due to the complexity of some of the parts used on the SBC610, it is not possible to include all the detailed data on all such devices in this manual. A list of the specifications and data sheets that provide any additional information follows:

**Specifications**

| | |
|---|---|
| IEEE 1101.1-1998 | IEEE Standard for Mechanical Core Specifications for Microcomputers. |
| IEEE 1101.2-1992 | Conduction cooled VME mechanics. |
| IEEE 1101.10-1996 | Additional Mechanical Specifications. |
| ANSI/VITA 20-2001 | Conduction Cooled PMC. |
| ANSI/VITA 42.0-2008 | XMC. |
| ANSI/VITA 42.3-2006 | XMC PCI Express Protocol Layer Standard. |
| ANSI/VITA 46.0-2007 | VPX Baseline Standard. |
| ANSI/VITA 46.1-2007 | VMEbus Signal Mapping on VPX |
| VITA46.3 (Draft 0.5) | Serial RapidIO on VPX. |
| VITA46.4 (Draft 0.5) | PCI Express on VPX. |
| ANSI/VITA46.9-2010 | XMC and PMC User I/O Mapping for VPX. |

These are the latest version at time of writing; check associated websites for later updates.

NOTE

Registration may be required for access to these specifications.

**Component Information**

MPC8641 and MPC8641D Integrated Host Processor Hardware Specifications, Freescale Semiconductor.

MPC8641D Integrated Host Processor Family Reference Manual, Freescale Semiconductor.

PEX8548 Data Book, PLX Technology.

PEX8518 Data Book, PLX Technology.

Tsi578 Serial RapidIO Switch User Manual, Tundra Semiconductor.

Tsi148 PCI/X-to-VME Bus Bridge User Manual, Tundra Semiconductor.

NOTE

Access to these documents may require a Non-Disclosure Agreement to be in place with the component vendor. Contact the manufacturer for more information.

## GE Website

Information regarding all GEIP Mil-Aero products can be found on the following website:

LINK

http://defense.ge-ip.com/products/family/military-and-aerospace

## Third Party Websites

Manufacturers of many of the devices used on the SBC610 maintain FTP or websites. Some useful sites are:

| | |
|---|---|
| http://www.vita.com | For VPX (VITA 46) standards. |
| http://www.pcisig.org | For PCI Bus standards. |
| http://www.freescale.com/ | For MPC8641D processor information. |
| http://www.plxtech.com/ | For PCI Express Bridge/Switch information. |
| http://www.tundra.com/ | For Serial RapidIO Switch and VME Bridge information. |

NOTE

Registration may be required for access to standards.

## Technical Support

Technical assistance contact details can be found on the website Support Locator page. The appropriate location is headed “DSP, SBCs, Multiprocessors and Graphics (formerly Radstone)”.

LINK
http://defense.ge-ip.com/support/embeddedsupport/locator.

Queries will be logged on the Technical Support database and allocated a unique Service Request (SR) number for use in future correspondence.

Alternatively, you may also contact GEIP’s Technical Support via:

LINK
support.towcester.ip@ge.com

TELEPHONE
+44 (0) 1327 322760

## Returns

If you need to return a product, there is a Return Materials Authorization (RMA) request form available via the web site Support Locator page.

LINK
http://defense.ge-ip.com/support/embeddedsupport/locator.

Do not return products without first contacting the GEIP Repairs facility.

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*(continued overleaf)*

*(continued overleaf)*

## 5 • Functional Description (continued)

## 6 • Control and Status Registers (continued)



*(continued overleaf)*

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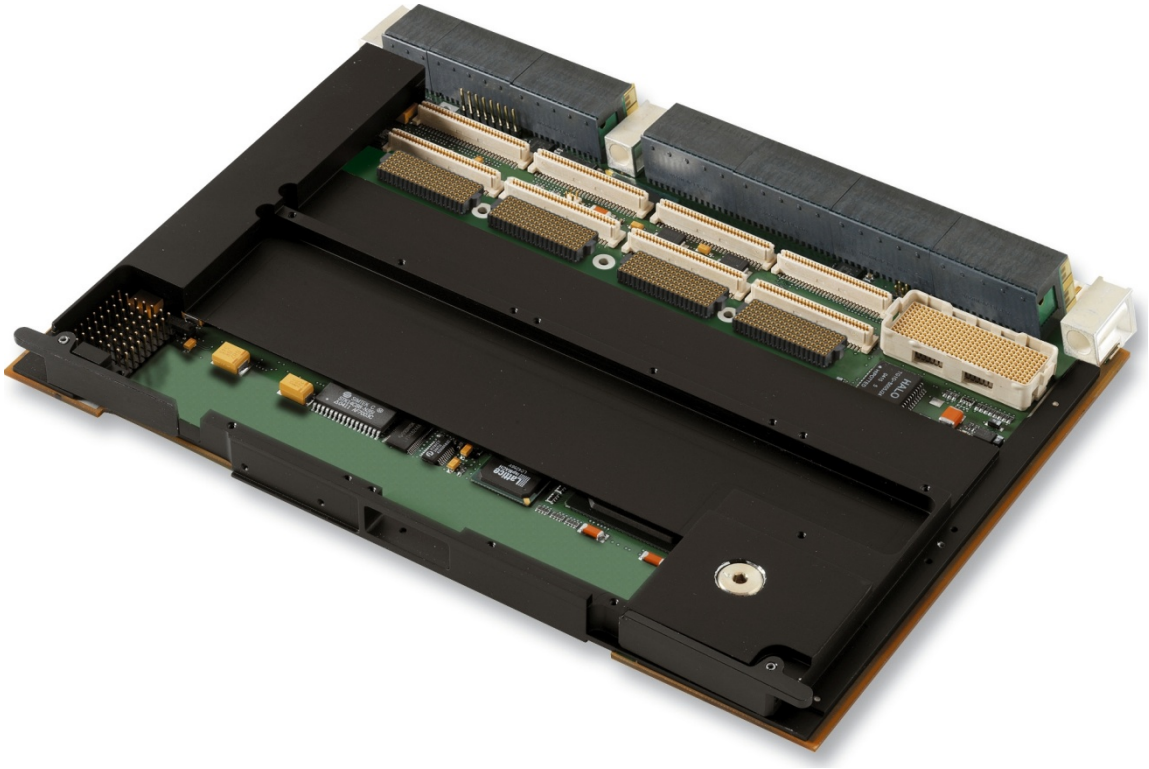
# 1 • Introduction

The GE Intelligent Platforms SBC610 is a member of the VPXtreme6 family of 6U VPX PowerPC-based Single Board Computers. It uses the Freescale MPC8641D dual-core integrated host processor, which contains two e600 PowerPC processing cores running at 1.33 GHz with dual memory controllers, serial fabric and I/O interfaces. The SBC610 offers up to 4 GBytes of DDR2 SDRAM with ECC, up to 1 GByte of Flash memory, two Gigabit Ethernet channels, serial, USB 2.0 and SATA interfaces. Up to four x4 Serial RapidIO ports and up to eight lanes of PCI Express are available on the backplane. A VME interface with 2eSST support is also provided for connection to legacy hardware.

The MPC8641D processor is connected to all on-board PCI devices and mezzanine sites using PCI Express through a non-blocking switch architecture. Two 64-bit PMC sites are provided, each supporting PCI-X operation at up to 133 MHz, allowing for off-the-shelf or custom mezzanines to be fitted to add further functionality to the SBC610. Both sites also support XMC mezzanine cards, supporting a x8 PCI Express link to each site, for higher bandwidth connectivity to the host and high-speed rear I/O. Expansion capabilities are further extended with the addition of an AFIX module connector. This proprietary interface is intended to allow additional functionality (such as MIL-STD-1553 or Graphics) to be added to the host card without taking up a mezzanine site.

The SBC610 couples familiar software interfaces and reliability with high-speed fabric interfaces, offering significant increases in inter-board bandwidth.

Figure 1-1 SBC610 General View



## 1.1 Safety Notices

The following general safety precautions represent warnings of certain dangers of which GE Intelligent Platforms (GEIP) is aware. Failure to comply with these or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of the equipment. GEIP assumes no liability for the user's failure to comply with these requirements.

Also follow all warning instructions contained in associated system equipment manuals.

WARNINGS

Use extreme caution when handling, testing and adjusting this equipment. This device may operate in an environment containing potentially dangerous voltages.

Ensure that all power to the system is removed before installing any device.

To minimize shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet IEC safety standards.

### 1.1.1 Flammability

The SBC610 circuit board is made by a UL-recognized manufacturer and has a flammability rating of UL94V-1.

### 1.1.2 EMI/EMC Regulatory Compliance

CAUTION

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to EMI if not installed and used in a cabinet with adequate EMI protection.

The SBC610 is designed using good EMC practices and, when used in a suitably EMC-compliant chassis, should maintain the compliance of the total system. The SBC610 also complies with EN60950 (product safety), which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

Air-cooled build levels of the SBC610 are designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

Conduction-cooled build levels of the SBC610 are designed for integration into EMC hardened cabinets/boxes.

### 1.1.3 Cooling

CAUTION

The SBC610 requires air-flow of at least 300 lfm for build levels 1 and 2, and at least 600 lfm for build level 3. If a conduction-cooled (level 4 or 5) SBC610 is operating on an extender card, it requires air-flow of at least 300 lfm across it and careful monitoring of board temperatures.

### 1.1.4 Handling

CAUTION

Only handle the board by the edges or front panel

Figure 1-2 ESD Label (Present on Board Packaging)


### 1.1.5 Heatsink

CAUTION

Do not remove the heatsink. There are no user-alterable components underneath the heatsink, so users should have no reason to remove it.

Users should not attempt reattachment of the heatsink, as this requires precise torque on the screws attaching the heatsink to the PCB. Over-tightening the screws may cause the heatsink to damage components beneath it. *Removal and re-attachment of the heatsink should only be carried out by the factory.*

# 2 • Unpacking

On receipt of the shipping container, if there is any evidence of physical damage, the Terms and Conditions of Sale (provided with your delivery) give information on what to do. If you need to return the product, contact your local GEIP sales office or agent.

The SBC610 is sealed into an antistatic bag and housed in a padded cardboard box. Failure to use the correct packaging when storing or shipping the board may invalidate the warranty.

## 2.1 Box Contents Checklist

1. SBC610 in antistatic packaging.
2. Embedded Software License Agreement (GFJ-353).

## 2.2 Identifying Your Board

The SBC610 is identified by labels at strategic positions. These can be cross-checked against the Advice Note provided with your delivery.

Identification labels, similar to the example shown in Figure 2-1, attached to the shipping box and the antistatic bag give identical information: product code, product description, equipment number and board revision.

Figure 2-1 Product Label (Packaging)


On the board within the antistatic bag, there is an identifying label similar to the example shown in Figure 2-2, attached to the PCB.

Figure 2-2 Product Label (Product)

On the conduction-cooled version of the board (build levels 4 and 5), there is also a label similar to the example shown in Figure 2-3, attached to the front panel.

Figure 2-3 Product Label (Conduction-cooled Product)


See the Product Codes section in Appendix A for more details on the product code (SBC610-xxxxxxxxx).

# 3 • Configuration

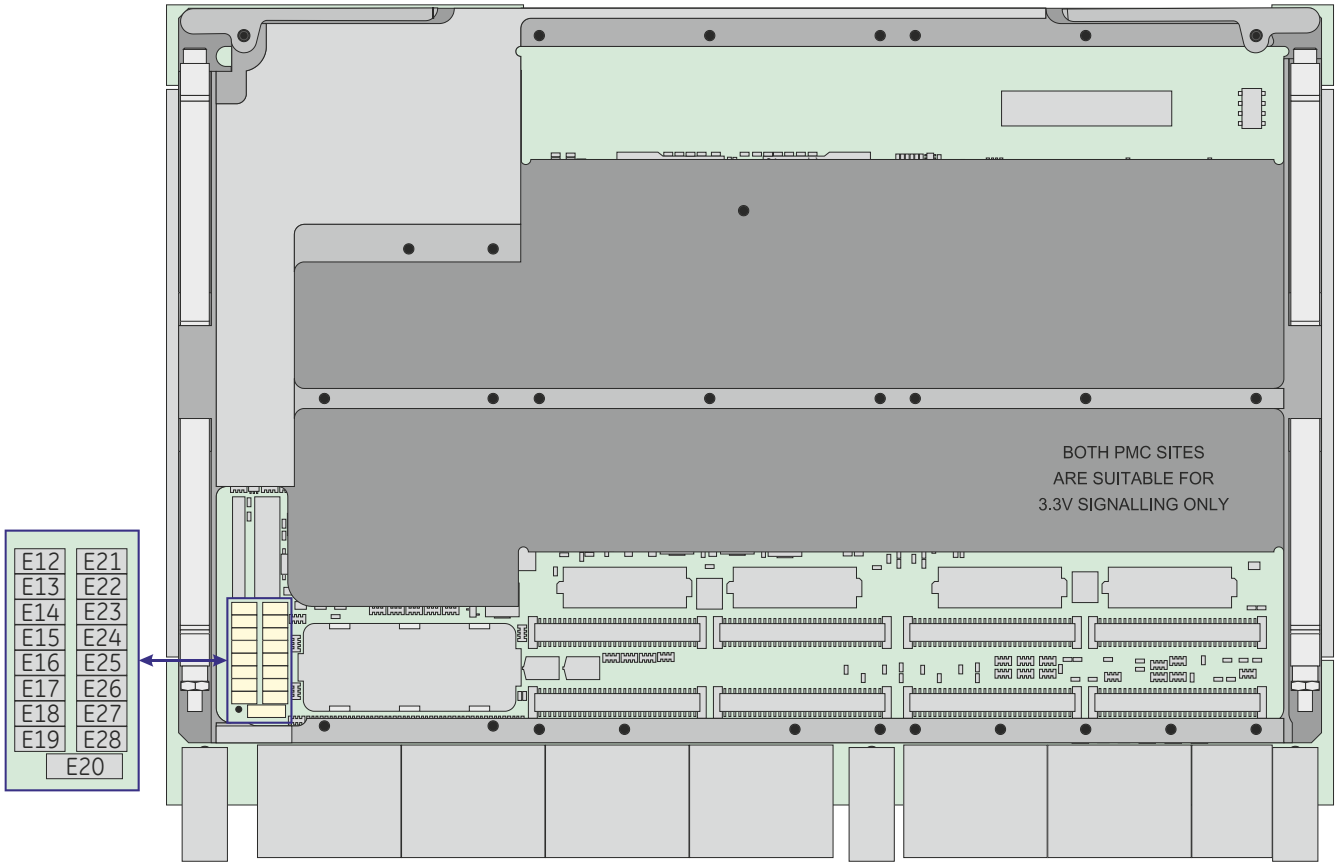
## 3.1 Link Configuration

The SBC610 has push-on jumpers included in the standard kit of parts; additional jumpers may be obtained on request. These are suitable for level 1 to 3 low vibration applications.

TIP

For Level 4 and 5 products, make links by wire-wrapping between the pin posts and then cover these wire wrapped links with the same conformal coating as that used on the board. This will provide a reliable connection under heavy shock and vibration conditions and further prevent oxidation of the connection due to moisture ingress.

Figure 3-1 Link Positions




The diagram above shows standard 2.54 mm pitch headers for general use.

This manual refers to jumper settings as In or Out. Meanings are as follows:

In = jumper fitted -

Out = jumper not fitted -

## 3.2 Inspection

The SBC610 is shipped from the factory with no jumpers fitted.

## 3.3 Link Descriptions

NOTES

Ordinary operation requires no jumpers to be fitted.

The state of most of the links can be read from the Link Status Register.

TIP

If you are about to install your board and power-up for the first time, leaving your board in the default configuration will enable board operation to be proven before tackling any further configuration issues.

### 3.3.1 Core 0 Boot Area Selection Links (E12 and E14)

The Boot Flash for Processing Core 0 is divided into four sections, allowing for three different boot images to be loaded into the Flash. There is also a factory-programmed Recovery boot image. These links are used to select which image is used at boot time.

Table 3-1 E12 and E14 Link Settings

| E12 | E14 | Active Boot Image |
|---|---|---|
| Out | Out | Main |
| In | Out | Alternate |
| Out | In | Recovery |
| In | In | Extended |

In normal operation, these links are not fitted and the SBC610 boots from the Main boot image.

The active boot image may also be affected in a deployed system using the BOOT_SWAP0~ backplane input (see the Boot Flash section).

### 3.3.2 Core 1 Boot Area Selection Links (E13 and E14)

Processing Core 1 may boot either from the same Flash image as Processing Core 0 or from its own Boot Flash, which is divided into four sections, allowing for three different boot images along with the factory-programmed Recovery boot image. These links are used to select which of the Core 1 boot images is used at boot time, if selected.

Table 3-2 E13 and E14 Link Settings

| E13 | E14 | Active Boot Image |
|---|---|---|
| Out | Out | Main |
| In | Out | Alternate |
| Out | In | Recovery |
| In | In | Extended |

In normal operation, these links are not fitted and the SBC610 boots from the Main boot image.

The active boot image may also be affected in a deployed system using the BOOT_SWAP1~ backplane input (see the Boot Flash section).

### 3.3.3 Recovery Boot Link (E14)

In addition to selecting the Recovery boot image, link E14 also prevents the loading of EEPROM configuration data by any of the devices on the board. This is useful in the event that EEPROM data becomes corrupted and needs to be reprogrammed.

Table 3-3 E14 Link Setting

| Setting | Meaning |
|---|---|
| Out | Normal operation |
| In | EEPROM load is disabled |

### 3.3.4 Boot Flash Write Enable Link (E15) and User Flash Write Enable Link (E16)

These links tell the software how it should configure the default non-persistent sector protection of the Boot and User areas of Flash. They are provided for compatibility with previous GEIP hardware, where links enabled write accesses to the 8 MByte Boot Area of Flash and the remaining User Flash. These links now have no effect on the hardware interface to the Flash devices, as all sector protection is controlled by software. See the Flash Sector Protection section for further details.

NOTES

User software may subsequently alter sector protection at any time following the boot sequence.

Regardless of any link settings for the Flash write protection, the Recovery boot area cannot be write-enabled.

Table 3-4 E15 and E16 Link Setting

| Setting | Meaning |
|---|---|
| Out | Boot/User Flash sectors are write-protected by default |
| In | Boot/User Flash sectors are write-enabled by default |

CAUTION

These links provide no write protection in hardware when not fitted.
All Flash write protection is provided by software.

### 3.3.5 Flash Protection Unlock Link (E17)

A jumper must be fitted on this link to allow software to alter the Flash persistent sector protection, which remains unchanged following a reset or a power-cycle. If no jumper is fitted, the software is prevented from altering any previously configured sector protection. See the Flash Sector Protection section for further details.

Table 3-5 E17 Link Setting

| Setting | Meaning |
|---|---|
| Out | Persistent Flash sector protection cannot be altered |
| In | Persistent Flash sector protection can be altered |

NOTE

The VPX backplane Non-Volatile Memory Read Only (NVMRO) signal (on connector P0 pin A4) must also be set inactive low before the Flash sector protection can be altered.

### 3.3.6 NVRAM Write Enable Link (E18)

Fitting a jumper on this link enables writes to the NVRAM device. It also allows writes to the I²C and Serial Configuration EEPROMs to be enabled using Control Register 2.

Not fitting a jumper ensures that software cannot corrupt any of the non-volatile memory (apart from the Flash, which must be protected separately) during operation.

Table 3-6 E18 Link Setting

| Setting | Meaning |
|---|---|
| Out | NVRAM writes disabled |
| In | NVRAM writes enabled |

NOTE

The VPX backplane Non-Volatile Memory Read Only (NVMRO) signal (on connector P0 pin A4) must also be set inactive low before the NVRAM can be altered.

### 3.3.7 SMP Mode Link (E19)

When the two processing cores are running different operating systems, or different instance of the same operating system, the MPC8641D provides the ability to offset Core 1 accesses to the bottom of RAM by 256 MBytes (addresses 0x0000 0000 to 0x1000 0000 are offset to 0x1000 0000 to 0x2000 0000). This allows both processing cores to maintain separate stacks and private memory without any software intervention. This is the default mode selected with this link not fitted.

When the two processors are operating in SMP mode, this feature is not desirable, as both processors need to share the same memory space. Fitting a jumper on this link in this mode disables this feature.

Table 3-7 E19 Link Setting

| Setting | Function |
|---|---|
| Out | AMP Mode – Core 1 has 256 MByte memory offset |
| In | SMP Mode – no offset |

If a single-core MPC8641 processor is fitted, the setting of this link has no effect.

### 3.3.8 Factory Link (E20)

This link is for factory use only. It should not be fitted by the user.

### 3.3.9 Boot Hold-off Link (E21)

Fitting a jumper on this link prevents Processing Core 0 from booting, and configures the board to allow a PMC fitted onto PMC Site 1 to access the MPC8461D and program the Flash. This feature may be used to program a blank board.

Table 3-8 E21 Link Setting

| Setting | Function |
|---|---|
| Out | Normal operation |
| In | Core 0 boot hold-off |

### 3.3.10 Factory Link (E22)

This link is for factory use only. It should not be fitted in normal operation.

### 3.3.11 JTAG Scanbridge Output Enable Link (E23)

The SBC610 uses a JTAG Scanbridge device to connect all of the JTAG-compliant devices on the board. This link is provided to enable the Scanbridge during boundary scan. It should not normally be fitted in deployed systems and must not be fitted when the BDM Header or PLD Programming Header are in use.

Table 3-9 E23 Link Setting

| Setting | Function |
|---|---|
| Out | Scanbridge disabled |
| In | Scanbridge enabled |

### 3.3.12 PCI Express Selection Links (E24 and E25)

These links are used to control the fabric multiplexer for two of the x4 fabric links on the P1 connector. Link E24 controls the selection of Fabric Port 3 and Link E25 controls the selection of Fabric Port 4. If a x8 PCI Express port is required on the backplane, both links should be fitted.

Table 3-10 E24 and E25 Link Settings

| Setting | Function |
|---|---|
| Out | Serial RapidIO routed to the backplane |
| In | PCI Express routed to the backplane |

The state of these links is reflected in Control Register 2, and may be overridden by software if required.

### 3.3.13 AFIX Links (E26 and E27)

These links control features of the AFIX module, and their function is determined by the module in use. See the appropriate AFIX manual for further information.

Link E26 controls the state of the P41 connector pin D2 and link E27 controls the state of the P41 connector pin D3.

On the AFIXSG, these links are used to enable SCSI termination as defined below:

Table 3-11 E26 and E27 Link Settings

| E26 | E27 | AFIXSG SCSI Termination |
|---|---|---|
| Out | Out | No termination |
| In | Out | 8-bit signals terminated |
| Out | In | 16-bit extension signals terminated |
| In | In | 8- and 16-bit signals terminated |

The state of these links is reflected in the Board Configuration Register.

### 3.3.14 Spare Link (E28)

This link is reserved for future use.

## 3.4 Mezzanine Installation

As shown in Figure 3-2, the SBC610 has two mezzanine sites that both support suitably compliant PMCs or XMCs (including support for front-panel I/O). The two sites allow for the fitting of two single-width PMCs/XMCs or one double-width PMC/XMC. One AFIX site is also provided. This is a GEIP proprietary interface allowing additional functionality to be added without taking up a mezzanine site.

The presence of a mezzanine in the various sites can be determined from the Board Configuration Register.

### 3.4.1 PMC Installation

CAUTION

The SBC610 PMC sites are *not* 5V tolerant. VIO pins are connected directly to the +3.3V supply. *Do not* fit PMCs that use 5V signaling.

PMCs supplied by GEIP are delivered with a full kit of parts for mounting them. A PMC ordered with an SBC610 can be supplied factory fitted, if required.

LINK

PMC Installation Note, publication number HN4/3-99.

CAUTION

Observe handling and anti-static precautions when fitting the PMC.

It will usually be necessary to install driver software or implement other firmware configuration to achieve full functionality of a PMC (see the specific PMC manual for the exact procedure).

TIP

Where a PMC is not pre-installed, prove operation of the SBC610 *before* installing the PMC.

### 3.4.2 XMC Installation

XMCs supplied by GEIP are delivered with a full kit of parts for mounting them. Fitting is similar to a PMC. An XMC ordered with an SBC610 can be supplied factory fitted, if required.

CAUTION

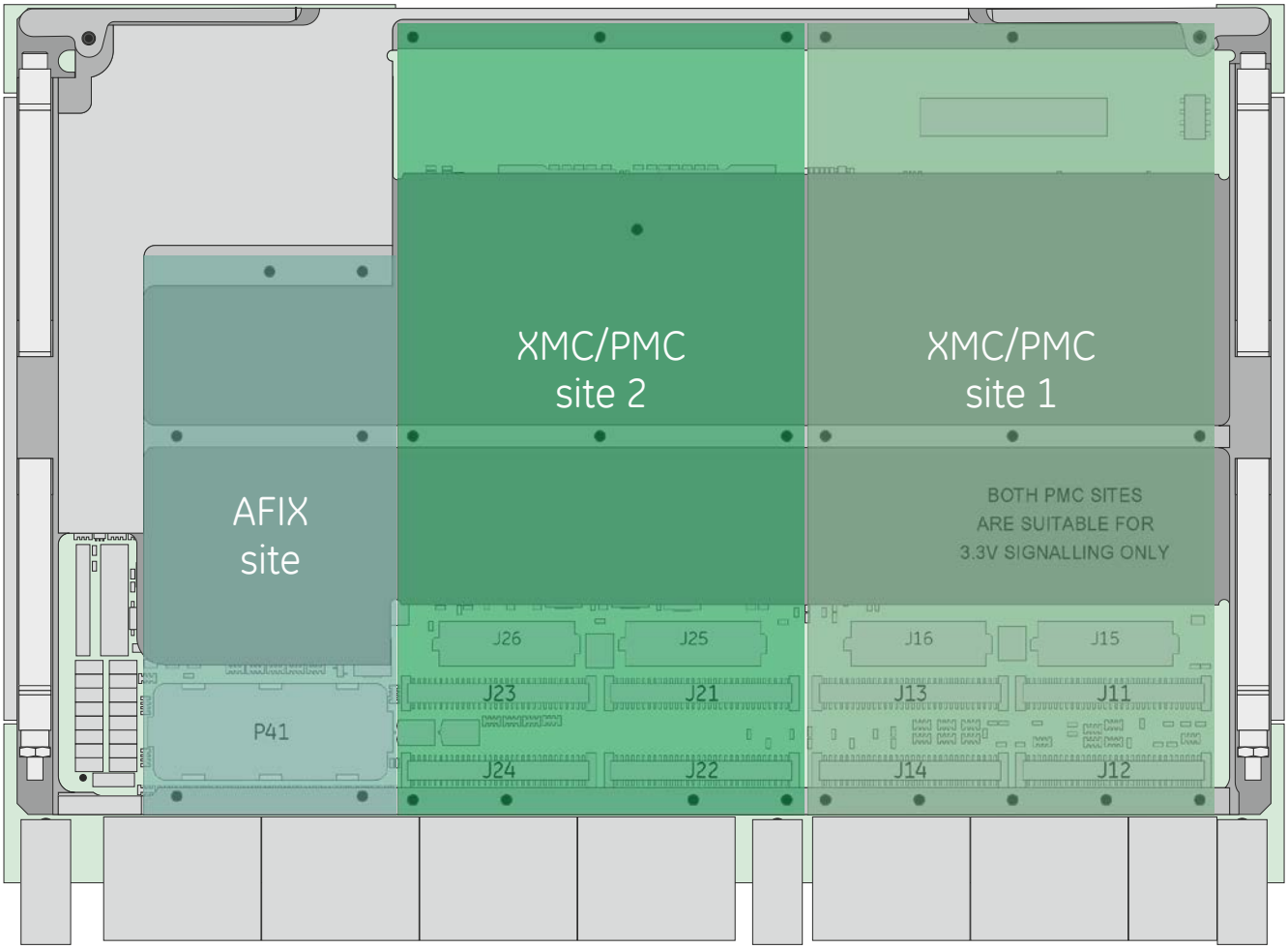
Observe handling and anti-static precautions when fitting the XMC.

It will usually be necessary to install driver software or implement other firmware configuration to achieve full functionality of an XMC (see the specific XMC manual for the exact procedure).

TIP

Where an XMC is not pre-installed, prove operation of the SBC610 *before* installing the XMC.

Figure 3-2 Mezzanine Positions




### 3.4.1 AFIX Installation

AFIX modules are supplied factory fitted, and are a build option (see the Product Codes section).

The current range of AFIX cards includes support for dual MIL-STD-1553 interfaces (AFIX1553), SCSI and graphics (AFIXSG), USB Flash memory (AFIXM) and differential GPIO (AFIXDIO1).

The AFIX site also allows specific customer requirements to be accommodated more quickly and easily than a modification to the main host board. Contact your local GEIP sales representative with any specific requirements.

For more details on AFIX, see the AFIX family manual.

LINKS
AFIX Family Product Manual, publication number AFIX-0HH.

# 4 • Installation and Power Up/Reset

Review the Safety Notices section before installing the SBC610. The following notices also apply:

CAUTION

Consult the enclosure documentation to ensure that the SBC610's power requirements are compatible with those supplied by the backplane.

## 4.1 Power Supply Requirements

The SBC625 requires the backplane to provide 5V (VS3) and 3V3_AUX supplies. Requirements are as follows:

Table 4-1 Power Supply Requirements

| Supply | Current Requirement | VPX Specification Limits |
|---|---|---|
| VS3 | Up to 18 A | +5 V +5% -2.5% |
| P3V3_AUX | Up to 100 mA | +3.3 V ±5 % |

No voltage is required to be supplied on the Vs1 and Vs2 supplies as the SBC610 does not connect to these pins. P12V_AUX and N12V_AUX are not required for board operation, but are used to supply the ±12 V pins of the PMC and AFIX mezzanine sites and the auxiliary supplies of the XMC sites.

The VBAT supply may be used to power the Real-Time Clock in isolation when the board is powered down, to maintain the time/date information. This requires up to 1 µA at 3.3 V ±5%.

See the Electrical Specification section for more details.

## 4.2 Board Keying

The VPX specification defines three keying pins.

The keying pin at Position 1 (adjacent to the P0 connector) is used to define the voltage present on the Vs1 and Vs2 supply pins on the backplane J0 connector. As the SBC610 does not use these supplies, the module keying device in this position is of the unkeyed type to allow the board to be fitted to any type of backplane.

The keying pins at Position 2 (adjacent to the P2 connector) and Position 3 (adjacent to the P6 connector) are used to define slot-specific keying. The SBC610 is delivered with module keying devices of the unkeyed type in these positions to allow the board to be fitted to any backplane slot.

Contact the factory to discuss any specific keying requirements.

## 4.3 Board Installation Notes

1. The VPX specification allows for a variety of different backplane pinouts depending on the mix of differential and single-ended connectors. Take care to ensure that the pinout of the SBC610 matches that of the backplane slot before insertion.

CAUTION

The SBC610 has been specifically designed for use with 6U VPX backplanes designed to accommodate a single-ended pin out on the J2 connector and is *not* compatible with 6U backplanes where the J2 connector is intended for differential signaling. Plugging the SBC610 into such a 6U backplane may cause permanent component damage.

2. Air-cooled versions of the SBC610 have injector/ejector handles to ensure that the backplane connectors mate properly with the backplane. The captive screws at the top and bottom of the front panel allow the board to be tightly secured in position, which provides continuity with the chassis ground of the system.

3. Conduction-cooled versions of the SBC610 have screw-driven wedgelocks at the top and bottom of the board to provide the necessary mechanical/thermal interface. Correct adjustment requires a calibrated torque wrench with a hexagonal head of size $^{3}/_{32}$" (2.38 mm), set to between 0.6 and 0.8 Nm.

4. In an air-cooled development enclosure, when taking I/O connections from the backplane connectors, use of GEIP I/O modules (or some equivalent system) ensures optimum operation of the SBC610 with regard to EMI. See the VPX I/O Modules manual for more details.

LINK

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH.

## 4.4 Connecting to SBC610

To interact with on-board firmware requires the SBC610 to have, as a minimum, a terminal connection present on the serial COM1 port. Ethernet and USB connections may also be required, depending on Operating System requirements. These ports may be accessed through the backplane signals, using a Rear Transition Module (RTM).

COM1 is configured as DTE with default settings of 9600 baud, 8 bits/character, 1 stop bit, parity disabled and no flow control.

### 4.4.1 Rear Transition Module

For development systems, connection to the Serial and Ethernet I/O can be achieved using an RTM. This converts the condensed pin out of the backplane connectors to pinouts suitable for use by industry standard connectors.

The following items are required:

- The SBC610
- The appropriate RTM (VPX6UX600)
- A null-modem 9-way D to 9-way D-type cable for connecting COM1 to a control terminal or PC running terminal emulation software
- For the Ethernet ports, a CAT5 (or better) straight-through patch cable for 10/100/1000BaseTX
- For USB, the required peripheral with a standard type A connector

The VPX I/O Modules manual contains more details on fitting RTMs. Similar antistatic and safety precautions apply when handling and/or installing RTMs as for the SBC610.

LINKS

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH.

VPX6UX600 Hardware Reference Manual, publication number VPX6UX600-0HH.

## 4.5 Reset and Power-up Sequence

An on-board power sequencer monitors the backplane supply voltages and will hold the SBC610 in reset or shut down the on-board power supplies if the backplane supplies are not within specified limits.

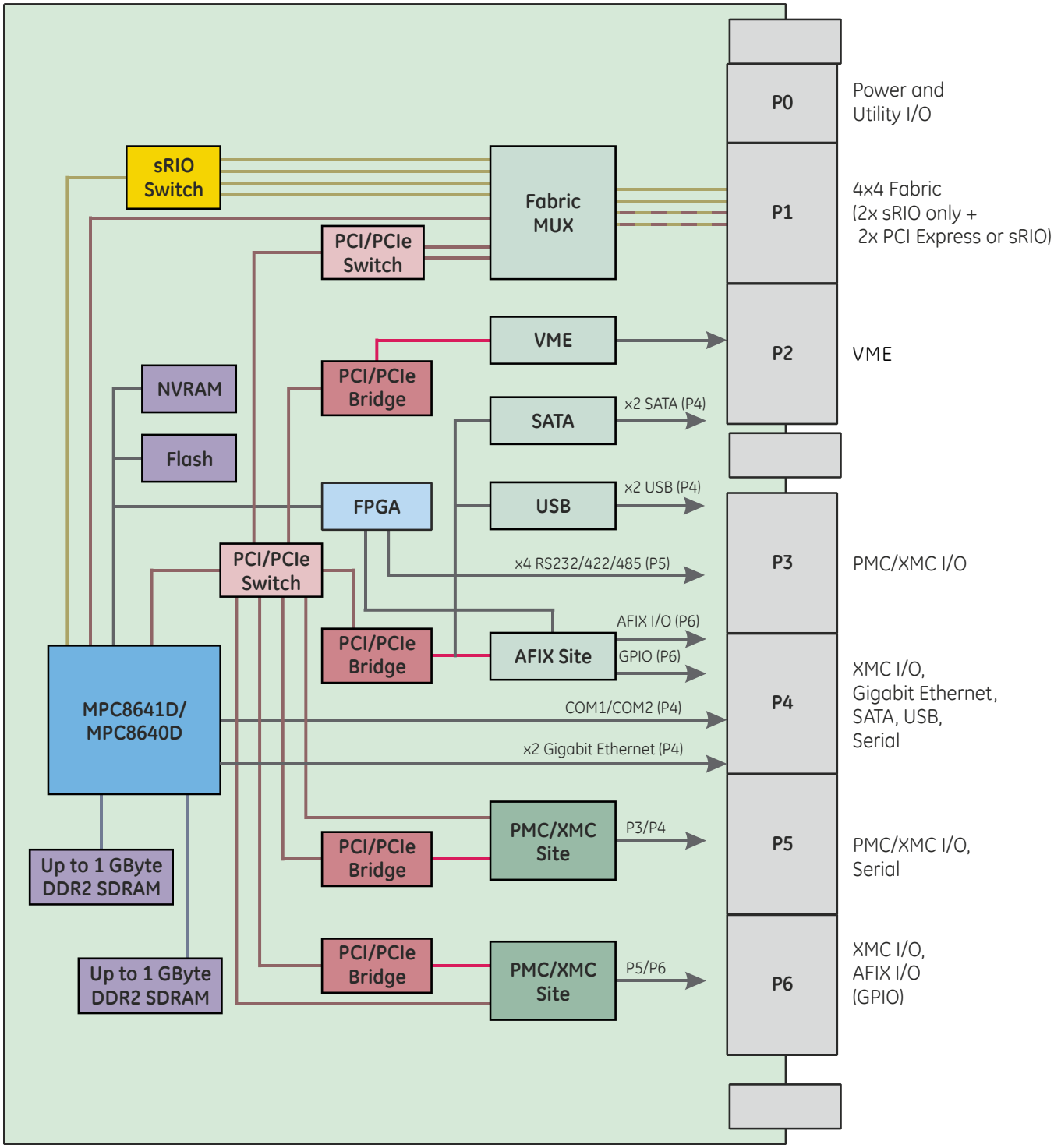
The green, front-panel Power Good LED (DS317) is lit when the backplane and all on-board supplies are within specification.

The +5V supply to the mezzanine cards is switched, under the control of the power manager device, so that the 5V and 3.3V supplies are applied to the mezzanines at approximately the same time.

The SBC610 supports the PSU_SEQ_IN/PSU_SEQ_OUT power sequencing signals (on the P1 connector pins G9 and G11) in line with other GEIP boards. When connected in a power-sequencing daisy chain, the on-board power supplies will only power up when SEQ_IN pin is asserted or floated high. An automatic override function is used which will power-up the board if the SEQ_IN pin has been low for more than 500 ms. See the Inter-board Sequencing section for more details.

# 5 • Functional Description

Figure 5-1 Block Diagram



NOTES

Due to the increasingly short lifetimes of system components, the I/O devices used on the SBC610 are not guaranteed to remain fixed in the future.

Hardware should be accessed only through mechanisms provided by the Operating System's Board Support Package, and not directly by application software.

If a standard operating system is not being used, then it is recommended that applications are written in such a way as to minimize direct access to hardware resources, bearing in mind that changes may be necessary to support future iterations of the hardware.

GEIP-supported Operating Systems guarantee compatibility at the application level through hardware independent mechanisms.

## 5.1 Features

- Freescale MPC8641D Integrated Host Processor with dual processing cores at 1.33 GHz
- Up to 4 GBytes of dual-channel DDR2 SDRAM with ECC
- Up to 1 GByte of Flash memory with enhanced write-protection features
- 128 KBytes of Non-Volatile RAM with power-down AutoStore
- PCI Express board interconnect with non-blocking switch architecture
- Two mezzanine sites supporting PMC and XMC modules. Each PMC interface has a 64-bit PCI/PCI-X interface and can operate at up to 133 MHz. Each XMC interface has a x8 PCI Express link
- AFIX site (accommodating the GEIP range of AFIX expansion modules)
- Up to four x4 Serial RapidIO backplane ports operating at up to 3.125 GHz
- Up to eight lanes of PCI Express backplane ports operating at 2.5 GHz
- VME64x interface with 2eSST support
- Two 10/100/1000Base-T Ethernet ports
- Six serial I/O channels (two RS232, two RS232/422/485 Async/Sync, two RS232/422/485 Async only)
- Up to five USB 2.0 ports
- Two SATA disk interfaces (up to 1.5 Gbits/second)
- 19 bits of General Purpose I/O with interrupt capability
- Real-Time Clock
- Elapsed Time Indicator
- Watchdog timers
- CPU die and ambient temperature sensors
- 6U VPX form factor
- Five environmental build levels

## 5.2 Integrated Host Processor

The SBC610 is based around the Freescale MPC8641D Integrated Host Processor. This provides:

- Dual e600 PowerPC processing cores
- Internal MPX bus
- Dual DDR2 memory controllers
- PCI Express interface
- Serial RapidIO interface
- Gigabit Ethernet interfaces
- Local Bus interface
- $I^2C$ interfaces
- Serial I/O interfaces
- DMA engines
- Interrupt controller

### 5.2.1 PowerPC Processing Cores

The MPC8641D contains two e600 high-performance, 32-bit, superscalar, PowerPC processing cores, as used in the MPC7448 processor, clocked at up to 1.33 GHz. The e600 processing core implements a fully static architecture and offers sophisticated power management capabilities. Each core includes:

- 32 KByte Level 1 instruction and data caches
- 1 MByte Level 2 backside cache with ECC
- 36-bit physical addressing
- AltiVec Vector Unit
- Enhanced branch prediction capabilities
- MMU and integral FPU

Table 5-1 Processor Specifications

| Processor Type | Core Frequency | MPX Bus Frequency |
|---|---|---|
| MPC8641D | 1333 MHz | 533 MHz |
| MPC8640D | 1067 MHz | 533 MHz |

The default build of the SBC610 uses the MPC8641D. Single processing core and reduced-frequency versions of the SBC610 are available for lower power requirements. See the Product Codes section.

### 5.2.2 Core Interaction

The MPC8641D contains two processing cores. Following reset, Processing Core 1 is prevented from accessing the MPX bus until it is enabled by Core 0.

The two processing cores are able to run two different operating systems or two separate instances of the same operating system. This is called Asymmetric Multi-Processing (AMP) Mode. This mode is aided by the Low Memory Offset Mode of the MPC8641D, which is able to apply a 256 MByte address offset to accesses by Core 1 to the bottom of RAM (addresses 0x0000 0000 to 0x1000 0000 are offset to 0x1000 0000 to 0x2000 0000). This allows both processing cores to maintain separate stacks and private memory without any software intervention.

The two processor cores are also able to run a single operating system, with tasks divided between them. This is called Symmetric Multi-Processing (SMP) mode. In this mode, the Low Memory Offset feature is not desirable, as both processors need to share the same memory space. Link E19 can be fitted in this mode to disable the Low Memory Offset feature.

### 5.2.3 Processor Power Management

All power management features of the processing cores, such as the programmable power states (Doze, Nap and Sleep), Dynamic Power Management, Instruction Cache Throttling and Dynamic Frequency switching, are available to the software within the 8641D. No external hardware support is required.

### 5.2.4 MPX Bus

The MPX bus, connecting the processing cores to the host bridge functions, is integrated into the MPC8641D and so is able to run at up to 533 MHz, more than twice as fast as an external implementation. This gives increased memory bandwidth and reduced latency, giving a significant performance increase.

### 5.2.5 Memory Map

The SBC610 supports a fully programmable memory map, defined by the MPC8641D. Memory windows are software-configured and the hardware does not carry out any configuration of the memory map. For this reason, no memory maps are provided in this manual.

Where addresses are provided in this manual, they are stated as a fixed offset from a software-programmable base address.

See the applicable software manuals for more information.

### 5.2.6 Local Bus

The MPC8461D local bus is a 32-bit multiplexed address/data bus, which is used to access the following devices on the SBC610:

- Local Bus Control FPGA
- Register FPGA
- I/O FPGA
- Flash
- NVRAM
- AFIX local bus

To reduce the loading on the local bus, the Flash and NVRAM are connected to separate data and address buses created by the Local Bus Control FPGA.

### 5.2.7 Local Bus Memory Map

The MPC8641D local bus controller provides eight chip selects, which are allocated to devices as defined in the table below. The minimum possible window size is 32 KBytes.

Table 5-2 Flash Memory Allocation

| Chip Select | Target | Device Width | Window Size |
|---|---|---|---|
| CS0 | Boot Flash | 32-bit[a] | 16 MBytes |
| CS1 | User Flash 0 | 32-bit[a] | 128 MBytes in Paged Mode<br>Up to 2 GBytes otherwise |
| CS2 | User Flash 1 | 32-bit[a] | 128 MBytes in Paged Mode<br>Up to 2 GBytes otherwise |
| CS3 | NVRAM | 8-bit | 128 KBytes |
| CS4 | Control/Status Registers<br>Interrupt Controller<br>Watchdogs<br>AXIS Registers | 32-bit | 32 KBytes |
| CS5 | AFIX local Bus | 8-bit | 32 KBytes |
| CS6 | I/O FPGA<br>- ESCC IP Cores<br>- External SRAM | 8-bit | 4 MBytes |
| CS7 | I/O FPGA<br>- DMA Engines<br>- Internal Dual-Port RAM<br>- GPIO Controller | 32-bit | 4 MBytes |

a. 16-bit in Redundant Flash mode.

## 5.3 RAM

The MPC8641D contains dual 64-bit DDR2 memory controllers and has the ability to interleave accesses between the two controllers to further increase the available RAM bandwidth. The controllers have full ECC error-correction support, with the ability to detect multi-bit errors and correct single-bit errors within a nibble.

The SBC610 provides up to a total of 4 GBytes of SDRAM, split between the two memory controllers. The following table shows the possible RAM configurations:

Table 5-3 RAM Configurations

| Total RAM | RAM per Controller | Banks per Controller | Device Size | Bus Speed |
|---|---|---|---|---|
| 2 GBytes | 1 GByte | 2 | 64Mx8 | 266 MHz |
| 4 GBytes | 2 GBytes | 2 | 128Mx8 | 266 MHz |

Configuration information for the RAM attached to each controller is contained within I²C EEPROM devices connected to I²C Bus 2.

## 5.4 Flash

The SBC610 supports up to 1 GByte of Flash memory, with 512 MBytes fitted as standard. The Flash devices are configured as 2 or 4 banks of two 16-bit wide devices, accessed as a 32-bit wide device. The Flash supports page-mode accesses to allow for maximum bus bandwidth and must be written to as 32-bits. The Flash is arranged in 256 KByte sectors, has an erase capacity of 100,000 cycles per sector and typical data retention of 20 years.

CAUTION

Integrity of Flash data cannot be guaranteed if a hard reset occurs during a Flash write cycle.

The following table shows the Flash options available for the SBC610:

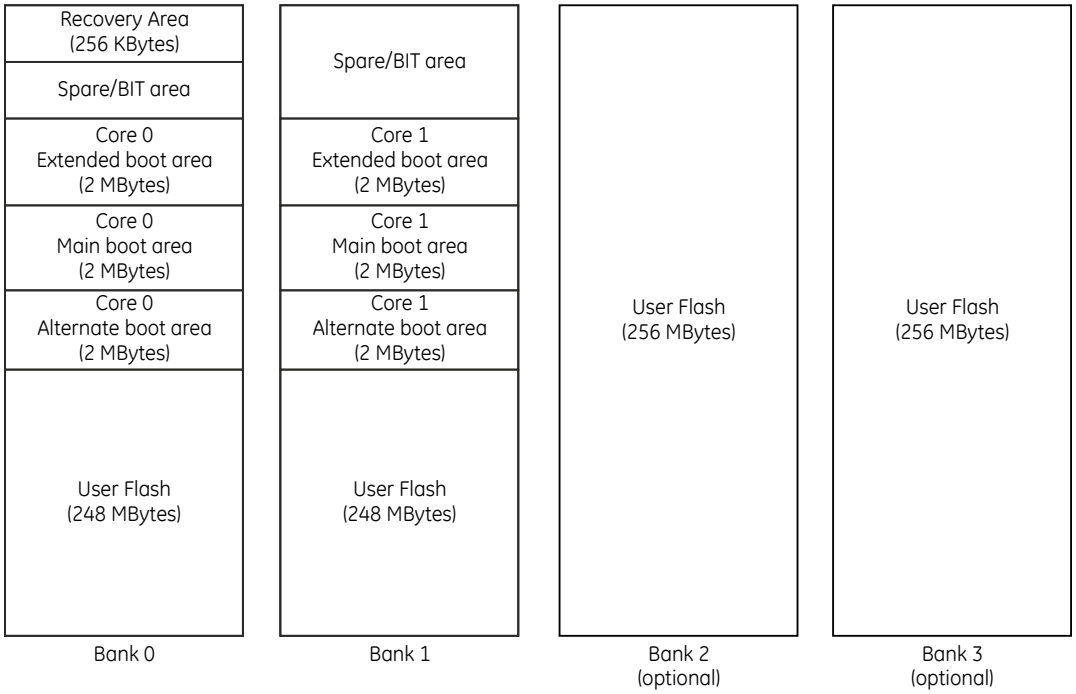
Table 5-4 Flash Options

| Flash Size | Banks | Flash Bank Organization |
|---|---|---|
| 512 MBytes | 2 | 2 x 1024Mbit |
| 1024 MBytes | 4 | 2 x 1024Mbit |

The Flash details can be determined from the Board Configuration Register.

The Flash is divided into two area types: Boot Flash and User Flash. The top 8 MBytes of the first two Flash banks are useable as Boot Flash for each of the two processing cores. These each hold four 2 MByte boot images that may be selected using hardware links. The remainder of the Flash memory is allocated as User Flash.

Figure 5-2 Flash Memory Structure



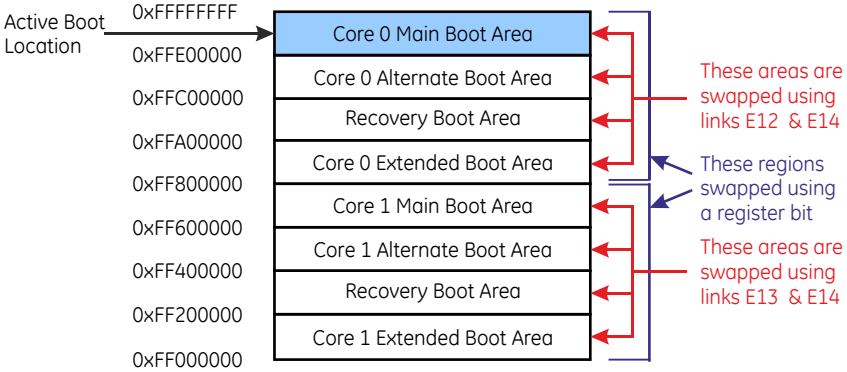

## 5.4.1 Boot Flash

The top 8 MBytes of Flash memory on each of the first two Flash banks is used as Boot Flash, holding initialization and operating system boot routines. Each of the 8 MByte regions are used to hold boot images for one of the processing cores and are divided into four independent 2 MByte boot images. When a single-core device is used or a separate boot image for Core 1 is not required, the second 8 MByte region may be utilized as User Flash.

The Recovery Boot image contains a 256 KByte factory-programmed boot image, shared by both processing cores, allowing the Flash to be reprogrammed if other boot images become corrupted. The Recovery area is protected by hardware and is not writeable by the user. The remainder of this 2 MByte area can be used to store BIT results.

The Boot Flash is accessed using Chip Select 0 on the Local Bus Controller of the MPC8641D, and is configured as the default boot location for the PowerPC reset vector (0xFFF0 0100). The boot areas are mapped into a 16 MByte window as shown below:

Figure 5-3 Local Bus CS0 Mapping



The active boot image for each processing core is selected using the appropriate links (E12 and E14 for Processing Core 0, and E13 and E14 for Processing Core 1). It may also be affected from the backplane using the BOOT_SWAP0~ or BOOT_SWAP1~ inputs. These signals are pulled up on board and may be pulled low externally to select an alternate boot image for each processing core.

Table 5-5 Boot Image Selection

| E12 | E14 | BOOT_SWAP0~ | Core 0 Active Boot Image |
|---|---|---|---|
| Out | Out | 1 | Main |
| In | Out | 1 | Alternate |
| Out | In | 1 | Recovery |
| In | In | 1 | Extended |
| Out | Out | 0 | Alternate |
| In | Out | 0 | Main |
| Out | In | 0 | Extended |
| In | In | 0 | Recovery |

| E13 | E14 | BOOT_SWAP1~ | Core 1 Active Boot Image |
|---|---|---|---|
| Out | Out | 1 | Main |
| In | Out | 1 | Alternate |
| Out | In | 1 | Recovery |
| In | In | 1 | Extended |
| Out | Out | 0 | Alternate |
| In | Out | 0 | Main |
| Out | In | 0 | Extended |
| In | In | 0 | Recovery |

The Core 1 boot region is made active by setting the Core 1 Enable bit in the Flash Control Register. If a separate boot image is required for Core 1, Core 0 should boot normally from its boot region and then set this bit before allowing Core 1 to boot.

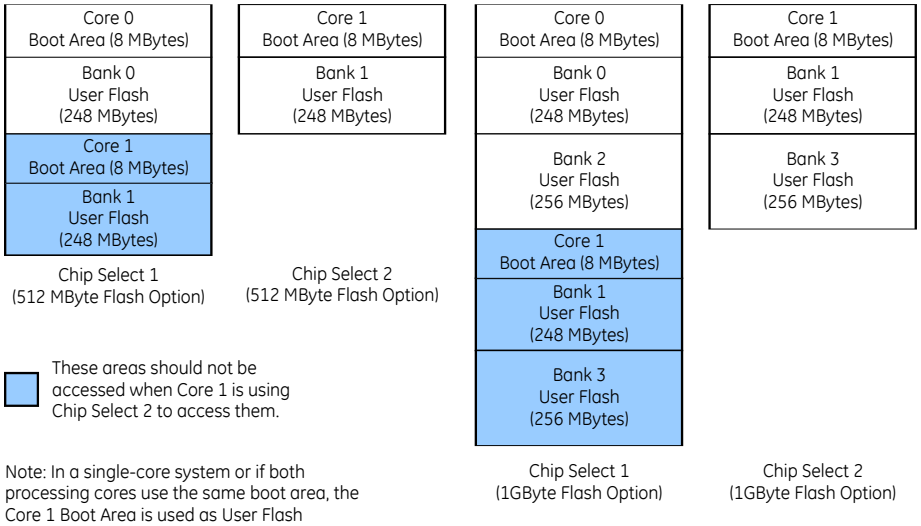
## 5.4.2 User Flash

Any Flash that is not used as Boot Flash is designated as User Flash and is intended to hold user application code or data.

User Flash is accessed using Chip Selects 1 and 2 (CS1 and CS2) on the Local Bus Controller of the MPC8641D. CS1 is intended for use by Processing Core 0 and may be used to access all areas of Flash, as required when using a single-core or SMP system; CS2 is intended for use by Processing Core 1 and may only access the lower area of Flash. When Core 1 is using CS2 to access Flash, Core 0 should not normally use CS1 to access these same areas to ensure private access for Core 1.

The 8 MBytes of Boot Flash appears at the top of the User Flash area, with the four boot images appearing in their physical locations (as shown below) unaffected by the state of the Flash Boot Image Select links.

Figure 5-4 User Flash Chip Select Mapping



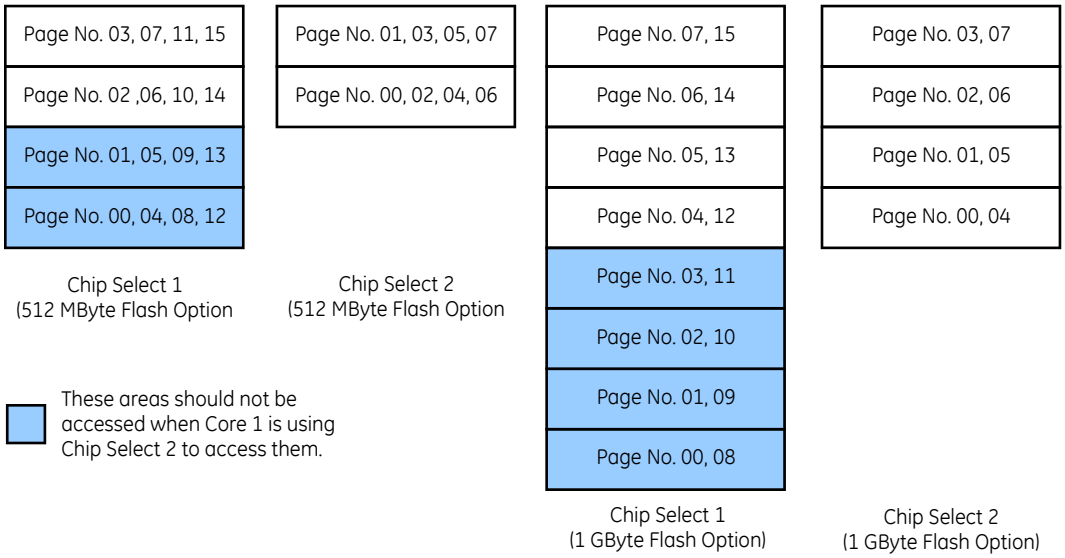
### 5.4.3 MAC Address Mirror Mode

The Recovery Boot Area is present in User Flash, only in the top sector of Flash Bank 0 accessed via CS1. This area also contains the board's serial number and MAC addresses, which may be required by Processing Core 1. There is a function to "mirror" the top sector of Flash Bank 0 to Flash Bank 1 to allow this to be invisible to software. This mode is controlled by the Flash Control Register and is enabled by default, although it may be disabled as this feature is not desirable in a single processor or SMP mode.

### 5.4.4 Paged Flash Mode

Due to limitations on the size of the processor memory map, a paged mode is provided where the User Flash area is divided into 128 MByte pages, with separate pages selectable for CS1 and CS2. This mode is controlled using the Flash Control Register and is enabled by default, with each Chip Select pointing to the top page of Flash.

Figure 5-5 Flash Paged Access Mode



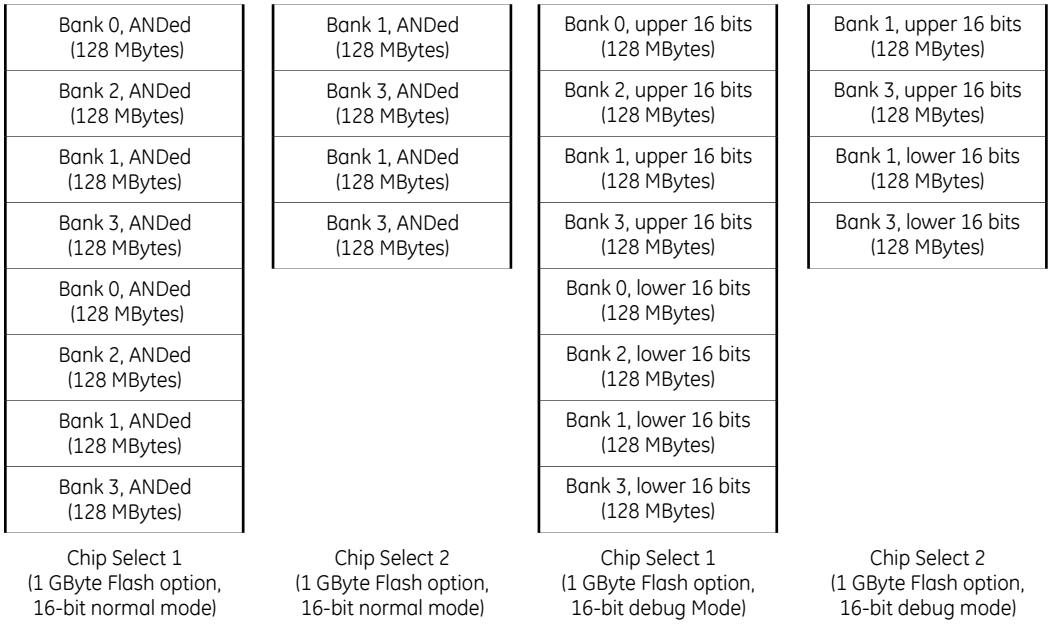

### 5.4.5 Redundant Flash Mode

The SBC610 provides an option where the configuration of the Flash width is changed to 16-bit, and each data word is stored in two Flash devices in parallel. The data read from the Flash is then the logical AND of the data from each device, ensuring that any bits that have become unprogrammed in one of the devices (due to exposure to radiation for example) do not result in a corruption of the data returned. In this mode, the Flash capacity is halved and access times may be increased.

Writes to the Flash are sent to both devices in parallel, and the software should poll the appropriate busy bit within the Flash Control Register to ensure that the write has completed in both devices before further commands are issued.

In this mode, it is possible to read or write the contents of each device independently by enabling a debug mode within the Flash Control Register. This allows BIT or other software to verify each Flash image separately and even correct any errors that are detected.

Figure 5-6 Redundant Flash Mode Mapping




This is feature is part of the Nuclear Event Detection hardware build option.

### 5.4.6 Flash Sector Protection

The SBC610 uses Spansion S29GL01GP Flash devices, which provide advanced methods of sector protection to ensure the integrity of code data contained in the Flash array. Protection is defined on a per-sector basis, where a sector is 256 KBytes in size. Locked sectors cannot be erased or programmed; they may only be read.

No write protection of Flash is provided by hardware. Software must be used to configure the Flash devices to protect against corruption of Flash data. The following types of protection are provided:

1. Persistent sector protection provides non-volatile protection that remains in place when a board is power cycled or reset. Each Flash sector may be set to be locked (write-protected) or unlocked (write-enabled) by writing to configuration registers within the Flash. The configuration of this protection is only possible when the Flash Protection Unlock Link (E17) is fitted and the backplane NVMRO signal (on connector P0 pin A4) is inactive low. If these conditions are not met, the software is unable to change the sector protection and those sectors that are locked may not be erased or reprogrammed under any circumstances.

2. Non-persistent protection may also be used. In this case, sectors locked using Persistent mode may not be erased or reprogrammed, but previously unlocked may now be locked. However, this protection is only present until a power cycle or hardware reset occurs.

NOTE
Do not rely on non-persistent protection, as it may be subsequently altered by software. If further protection is required, use the Persistent protection method.

For further details of these protection mechanisms, see the S29GL01P 1Gbit page-mode Flash data sheet.

## 5.5 Non-Volatile RAM (NVRAM)

The SBC610 has a 128 KByte AutoStore NVRAM for non-volatile set-up and configuration data storage. The NVRAM used is a Simtek STK14CA8, which is configured as an 8-bit wide device and is accessed using Chip Select 3 on the Local Bus Controller of the MPC8641D.

The NVRAM is write-protected when the NVRAM Write Enable Link (E18) is not fitted or if the NVMRO backplane signal (on connector P0 pin A4) is active high. The status of this link and backplane signal may be read back in the Link Status Register.

## 5.6 PCI Express Infrastructure

All on-board PCI devices and mezzanine sites are connected to the MPC8641D using PCI Express. The PCIe and PCI structure of the SBC610 is shown in Figure 5-1.

PCIe is a high-speed serial, point-to-point interconnect running at 2.5 Gbits/second in each direction. PCIe links are scalable, meaning that multiple lanes can be used between devices to increase the aggregate bandwidth. The following table shows a comparison of the bandwidth of PCI Express links with PCI implementations:

Table 5-6 PCI Bus

| Bus Type | Bus Width | Frequency | Bandwidth | Notes |
|---|---|---|---|---|
| PCI | 32-bit | 33 MHz | 133 MBytes/s | |
| PCI | 32-bit | 66 MHz | 266 MBytes/s | |
| PCI | 64-bit | 66 MHz | 533 MBytes/s | |
| PCI-X | 64-bit | 133 MHz | 1066 MBytes/s | |
| PCIe | x1 | 2.5 Gbps | 250 MBytes/s | Per direction |
| PCIe | X4 | 2.5 Gbps | 1000 MBytes/s | Per direction |
| PCIe | X8 | 2.5 Gbps | 2000 MBytes/s | Per direction |
| PCIe Bandwidths shown include 8b/10b encoding overheads | | | | |

PCIe is a packet-based protocol, but uses the same address spaces as standard PCI, meaning that the software interfaces are backwards-compatible. PCIe-to-PCI Bridges convert to PCI-X or standard PCI where connection to these devices is required.

The maximum packet payload size for the PCIe sub-system is 256 bytes.

CRC error-checking is performed on each packet transmitted between devices in the system and any corrupted packets are retransmitted. End-to-end error-checking can also be performed by the target device, to ensure integrity of the received data.

### 5.6.1 PCI Express Power Management

All PCIe links support several power management features, which are under software control and no hardware support is required.

The SBC610 does not support the WAKE~ signal and recovery from a $D3_{COLD}$ state under auxiliary power.

### 5.6.2 MPC8641D

The MPC8641D has two high-speed I/O ports.

The SerDes1 port is configured as a x8 PCIe link and is connected to Port 0 of the PCIe Switch. The port can operate in x1, x2, x4 or x8 modes. This port is normally configured as the system Root Complex but when the Boot Hold-off Link (E21) is fitted, the configuration is changed such that this port becomes a PCIe Endpoint. This allows configuration transactions to be accepted, to allow programming of the Boot Flash from a PMC.

The SerDes2 port is configured as a x4 Serial RapidIO port.

### 5.6.3 PCI Express Switch

The SBC610 uses a PLX PEX8548 PCIe Switch to connect all of the various PCIe devices together. This is a 48-lane, non-blocking switch that can support up to nine PCIe ports. The device also supports cut-thru mode to reduce packet latency.

Each PCIe port of the PEX8548 appears to software as a PCI-to-PCI bridge, with its own PCI- compatible configuration registers. Each port is accessed on the internal virtual PCI bus using a device number equal to its port number.

The port configuration of the switch is initially set up by hardware strapping as follows:

Table 5-7 PCI Express Switch Port Configurations

| Port | Width | Lanes | Link To | Lane Reversal |
|---|---|---|---|---|
| 0 | x8 | 0 to 7 | MPC8641D SerDes Port 1 | No |
| 1 | x4 | 8 to 11 | AFIX PCIe-PCI Bridge | Yes |
| 2 | x4 | 12 to 15 | PMC2 PCIe-PCI Bridge | Yes |
| 8 | x8 | 16 to 23 | PEX8518 PCI Express Switch | Yes |
| 9 | x8 | 24 to 31 | XMC Site 1 | Yes |
| 12 | x8 | 32 to 39 | XMC Site 2 | Yes |
| 13 | x4 | 40 to 43 | PMC1 PCIe-PCI Bridge | No |
| 14 | x4 | 44 to 47 | VME PCIe-PCI Bridge | Yes |

Each port is able to negotiate down to smaller link widths if required (such as if a fault occurs on any particular lane). Port widths of x1, x2, x4 and x8 are supported.

The PEX8548 also supports the optional PCIe lane-reversal feature, and the above table highlights where this has been used to aid PCB tracking. Where used, both the transmit and receive lanes for the link have been reversed.

Port 0 is connected to the MPC8461D and is usually configured as the upstream port. When the Boot Hold-off Link (E21) is fitted, the configuration is changed such that Port 13 is the upstream port. This allows configuration transactions to be forwarded from PMC site 1 to the processor, to allow programming of the Flash from a PMC.

A serial EEPROM can also be used to configure registers within the device if required. This EEPROM is write-protected by default and can be write-enabled by clearing the Serial EEPROM Write Protect bit in Control Register 1. This bit may only be cleared when the NVRAM Write Enable Link (E18) is fitted and the backplane NVMRO signal (on connector P0 pin A4) is inactive low. The Switch can be prevented from accessing the EEPROM, under software control, if the data becomes corrupted and configures the switch such that the EEPROM contents cannot be overwritten. This may be done by setting the PEX8548 Serial EEPROM Disable bit in Control Register 2 or by fitting the Recovery Boot Link (E14).

The PEX8548 is connected to on-board I²C Bus 1 (Address 0x58) to allow configuration by the processor and out-of-band monitoring of link status.

LEDs on the rear of the board show whether each of the on-board PCIe links is active or inactive. Further status information (number of active lanes, etc.) can be ascertained from registers within the switch.

### 5.6.4 PCIe to PCI Bridge

Where connection to PCI or PCI-X devices is required, the SBC610 uses PLX PEX8114 Bridges. The bridges can operate in forward (PCIe-to-PCI) or reverse (PCI-to-PCIe) mode; they are normally used in forward mode on the SBC610.

The bridge has a x4 PCIe interface, but can also operate in x1 or x2 mode, and supports lane reversal.

The PCI/PCI-X interface is 64-bits wide and can operate at frequencies up to 133 MHz. The bridge generates the clock outputs to external PCI/PCI-X devices. It samples the XCAP and M66EN signals to determine the correct operating frequency for the PCI bus and drives the PCI-X initialization pattern during reset. The current operating frequency of each bus may be ascertained by reading registers within the appropriate PEX8114. The bridge also contains the arbiter for the PCI bus. This supports up to four external masters and the priority of each is programmable.

The bridges are initially configured by hardware strapping, but each has a serial EEPROM that can also be used to configure registers within the device if required. The EEPROMs are write-protected by default and can be write-enabled by clearing the Serial EEPROM Write Protect bit in Control Register 1. This bit may only be cleared when the NVRAM Write Enable Link (E18) is fitted and the backplane NVMRO signal (on connector P0 pin A4) is inactive low. Each bridge can be prevented from accessing the EEPROM, under software control, if the data becomes corrupted and configures the device such that the EEPROM contents cannot be overwritten. This may be done by setting the relevant Serial EEPROM Disable bit in Control Register 2 or by fitting the Recovery Boot Link (E14).

The PEX8114 can report any errors detected to the processor via PCIe using legacy interrupt messages or Message Signaled Interrupts.

## 5.7 PCI Buses

There are four parallel PCI buses on the SBC610.

### 5.7.1 PCI Buses to PMC Sites

Each PMC Site is connected to a PEX8114 PCIe-to-PCI bridge via a 64-bit PCI/PCI-X bus, capable of running at up to 133 MHz. The speed of the bus is based on the capability of the PMC and is determined by the bridge. The current operating frequency of each bus may be ascertained by reading registers within the appropriate PEX8114.

The device number mapping for the PMC PCI buses are as follows:

Table 5-8 PMC PCI Device Mapping

| Device | IDSEL | Function |
|---|---|---|
| 0 to 7 | 16 to 23 | Not implemented |
| 8 | 24 | PMC Device A |
| 9 | 25 | PMC Device B |
| 10 | 26 | PEX8114 Bridge[a] |
| 11 to 15 | 27 to 31 | Not implemented |

a. The PEX8114 is connected to an IDSEL only on the PCI bus to PMC site 1.

Fitting a jumper to the Boot Hold-off Link (E21) changes the bridge to PMC site 1 into reverse mode. This allows configuration transactions to be forwarded from PMC site 1 to the processor, to allow programming of the Flash from a PMC.

### 5.7.2 PCI Bus to VME Bridge

The Tsi148 PCI-X-to-VME Bridge is connected to a PEX8114 PCIe-to-PCI Bridge via a 64-bit PCI-X bus running at 133 MHz.

The device number mapping for the VME PCI bus is as follows:

Table 5-9 VME PCI Mapping

| Device | IDSEL | Function |
|---|---|---|
| 0 | 16 | Tsi148 VME Bridge |
| 1 to 7 | 17 to 23 | Not implemented |
| 8 | 24 | PEX8114 Bridge |
| 9 to 15 | 25 to 31 | Not implemented |

### 5.7.3 PCI Bus to AFIX, USB and SATA

The AFIX site, USB and SATA devices are connected to a PEX8114 PCIe-to-PCI bridge via a 32-bit PCI bus running at 33 MHz.

The device number mapping for the PCI bus is as follows:

Table 5-10 PCI Bus Device Number Mapping

| Device | IDSEL | Function |
|---|---|---|
| 0 | 16 | Not implemented |
| 1 | 17 | USB Controller |
| 2 | 18 | SATA Controller |
| 3 | 19 | AFIX Device 0 |
| 4 | 20 | AFIX Device 1 |
| 5 | 21 | AFIX Device 2 |
| 6 | 22 | AFIX Device 3 |
| 7 to 15 | 23 to 31 | Not implemented |

## 5.8 Input/Output

The SBC610 has a variety of possible I/O connectivity, including the following:

- Ethernet
- Serial Ports
- USB
- Serial ATA
- General Purpose I/O

## 5.9 Ethernet

The MPC8641D has four on-chip enhanced Three-Speed Ethernet Controllers (eTSECs). These incorporate a Media Access Controller (MAC) that supports 10/100/1000BaseT and half- or full-duplex operation.

The eTSECs support several TCP offload features (including checksum generation and verification) that reduce the amount of software interaction required. Jumbo frames are also supported.

The SBC610 uses two of these controllers to provide external Ethernet interfaces. eTSEC1 and eTSEC3 are used, as these have independent connections to the platform bus. The controllers are connected via a GMII interface to Marvell 88E1111 PHYs. The PHYs are isolated from the backplane using transformer-coupled magnetics.

The network (MAC) addresses of the Ethernet ports are factory configured and may be displayed by software.

Six status LEDs are provided on the rear of the board to allow the status of each Ethernet interface to be monitored.

The SBC610 routes the two 10/100/1000BaseT Ethernet ports to the P4 Connector in accordance with VITA46.9, as follows:

Table 5-11 ETH0/ETH1 Pin Mapping

| Signal | P4 Pin | Signal | P4 Pin |
|---|---|---|---|
| ETH0_0P | A13 | ETH1_0P | A15 |
| ETH0_0N | B13 | ETH1_0N | B15 |
| ETH0_1P | D13 | ETH1_1P | D15 |
| ETH0_1N | E13 | ETH1_1N | E15 |
| ETH0_2P | B14 | ETH1_2P | B16 |
| ETH0_2N | C14 | ETH1_2N | C16 |
| ETH0_3P | E14 | ETH1_3P | E16 |
| ETH0_3N | F14 | ETH1_3N | F16 |

## 5.10 Serial Communication Ports

The SBC610 has six serial ports, which are sourced from different devices and so have different capabilities.

### 5.10.1 COM1 and COM2

COM1 and COM2 are provided by the DUART module within the MPC8641D, and are intended to operate as debug ports for the two processing cores.

Each of the two UARTs provides 16-byte FIFOs and is software-compatible with the PC16450 and PC16550D UART devices. Hardware flow control signals (RTS/CTS) are supported.

The baud rate is software programmable between and is derived from the MPX bus frequency using the following equation:

Baud Rate = (1/16) * (MPX Bus Frequency / Divisor Value)

The table below shows the divisors used for some commonly used baud rates and the percentage error associated with the use of an integer divider. Note that the percentage error will increase significantly at higher baud rates. Different divisors will be required if a different MPX Bus Frequency is used.

Table 5-12 COM1/2 Baud Rate, Frequency and Divisor Values

| Target Baud Rate | MPX Bus Frequency (MHz) | Divisor (Decimal) | Divisor (Hexadecimal) | Actual Baud Rate | Error (%) |
|---|---|---|---|---|---|
| 9600 | 533.333 | 3472 | 0D90 | 9600.61 | 0.0063 |
| 19200 | 533.333 | 1736 | 06C8 | 19201.22 | 0.0063 |
| 38400 | 533.333 | 868 | 0364 | 38402.43 | 0.0063 |
| 57600 | 533.333 | 579 | 0243 | 57570.52 | 0.0512 |
| 115200 | 533.333 | 289 | 0121 | 115340.25 | 0.1217 |

The actual performance of these ports will be limited by the throughput capability of the software driver.

The serial ports are driven by ISL41334 bus transceivers and can be individually software configured through Control Register 1 to operate in RS232 or RS422 mode, though the flow control signals are not available in RS422 mode.

The following COM1 and COM2 signals are available through the P4 connector.

Table 5-13 COM1/COM2 Signal Availability

| RS232 Signal | RS422 Signal | Input/Output | P4 Pin |
|---|---|---|---|
| COM1_TXD | COM1_TXD_A | Output | A11 |
| COM1_RXD | COM1_RXD_A | Input | D11 |
| COM1_RTS | COM1_TXD_B | Output | B11 |
| COM1_CTS | COM1_RXD_B | Input | E11 |

| RS232 Signal | RS422 Signal | Input/Output | P4 Pin |
|---|---|---|---|
| COM2_TXD | COM2_TXD_A | Output | B12 |
| COM2_RXD | COM2_RXD_A | Input | E12 |
| COM2_RTS | COM2_TXD_B | Output | C12 |
| COM2_CTS | COM2_RXD_B | Input | F12 |

### 5.10.2 COM3 and COM4

COM3 and COM4 are provided by the I/O FPGA. This is a Virtex 4 device, connected to the MPC8641D local bus, which contains an IP core based on the Zilog 85230 Enhanced Serial Communications Controller (ESCC). Each channel supports asynchronous and synchronous communication, with features providing support for SDLC and HDLC protocols.

Data is transferred between the IP core and dual-port RAM within the FPGA by dedicated DMA engines, allowing for increased throughput and reduced processor loading.

The FPGA provides additional Baud Rate Generation capabilities over the original Zilog Z85230 device, meaning that a greatly improved range and resolution of baud rates is available.

The serial ports are driven by ISL41334 bus transceivers and can be configured by software to operate in RS232, RS422 or RS485 modes. In RS485 mode, the serial controller is able to automatically disable the transmit buffer after transmission is completed.

The serial ports are intended only to be used by GEIP software drivers. See the relevant software manual for details.

The following COM3 and COM4 signals are available through the P5 connector, under certain I/O configuration options.

Table 5-14 COM3/4 Serial Port Signal Set

| RS232 Mode | RS422 Mode | Input/Output | P5 Pin |
|---|---|---|---|
| COM3_TXD | COM3_TX_A | Output | A5 |
| Not Used | COM3_TX_B | Output | B5 |
| COM3_RTS~ | COM3_RTS_A | Output | B6 |
| COM3_DTR | COM3_RTS_B | Output | C6 |
| COM3_RXD | COM3_RX_A | Input | D5 |
| COM3_DSR | COM3_RX_B | Input | E5 |
| COM3_CTS | COM3_CTS_A | Input | E6 |
| COM3_DCD | COM3_CTS_B | Input | F6 |
| Not Used | COM3_TT_A | Output | A7 |
| Not Used | COM3_TT_B | Output | B7 |
| Not Used | COM3_RT_A | Input | D7 |
| Not Used | COM3_RT_B | Input | E7 |
| Not Used | COM3_ST_A | Input | E8 |
| Not Used | COM3_ST_B | Input | F8 |

| RS232 Mode | RS422 Mode | Input/Output | P5 Pin |
|---|---|---|---|
| COM4_TXD | COM4_TX_A | Output | A9 |
| Not Used | COM4_TX_B | Output | B9 |
| COM4_RTS~ | COM4_RTS_A | Output | B10 |
| COM4_DTR | COM4_RTS_B | Output | C10 |
| COM4_RXD | COM4_RX_A | Input | D9 |
| COM4_DSR | COM4_RX_B | Input | E9 |
| COM4_CTS | COM4_CTS_A | Input | E10 |
| COM4_DCD | COM4_CTS_B | Input | F10 |
| Not Used | COM4_TT_A | Output | A11 |
| Not Used | COM4_TT_B | Output | B11 |
| Not Used | COM4_RT_A | Input | D11 |
| Not Used | COM4_RT_B | Input | E11 |
| Not Used | COM4_ST_A | Input | E12 |
| Not Used | COM4_ST_B | Input | F12 |

### 5.10.3 COM5 and COM6

COM5 and COM6 are provided by a second ESCC IP Core within the I/O FPGA. Each channel is able to support synchronous and asynchronous communication protocols, though it is intended for use in asynchronous modes only.

There is no local DMA support within the FPGA for these interfaces so their throughput is dependent on the capability of the software driver and the processor loading.

The FPGA provides additional Baud Rate Generation capabilities over the original Zilog Z85230 device, meaning that a greatly improved range and resolution of baud rates is available.

The serial ports are driven by ISL41334 bus transceivers and can be configured by software to operate in RS232, RS422 or RS485 modes. In RS485 mode, the serial controller automatically disables the transmit buffer after transmission is completed.

The serial ports are intended only to be used by GEIP software drivers. See the relevant software manual for details.

The following COM5 and COM6 signals are available through the P5 connector, under certain I/O configuration options.

Table 5-15 COM5/6 Serial Port Signal Set

| RS232 Mode | RS422 Async Mode | RS422 Sync Mode | Input/Output | P5 Pin |
|---|---|---|---|---|
| COM3_TXD | COM3_TX_A | COM3_TX_A | Output | A13 |
| Not Used | COM3_TX_B | COM3_TX_B | Output | B13 |
| COM3_RTS~ | COM3_RTS_A | COM3_TT_A | Output | B14 |
| COM3_DTR | COM3_RTS_B | COM3_TT_B | Output | C14 |
| COM3_RXD | COM3_RX_A | COM3_RX_A | Input | D13 |
| COM3_DSR | COM3_RX_B | COM3_RX_B | Input | E13 |
| COM3_CTS | COM3_CTS_A | COM3_RT_A | Input | E14 |
| COM3_DCD | COM3_CTS_B | COM3_RT_B | Input | F14 |

| RS232 Mode | RS422 Async Mode | RS422 Sync Mode | Input/Output | P5 Pin |
|---|---|---|---|---|
| COM4_TXD | COM4_TX_A | COM4_TX_A | Output | A15 |
| Not Used | COM4_TX_B | COM4_TX_B | Output | B15 |
| COM4_RTS~ | COM4_RTS_A | COM4_TT_A | Output | B16 |
| COM4_DTR | COM4_RTS_B | COM4_TT_B | Output | C16 |
| COM4_RXD | COM4_RX_A | COM4_RX_A | Input | D15 |
| COM4_DSR | COM4_RX_B | COM4_RX_B | Input | E15 |
| COM4_CTS | COM4_CTS_A | COM4_RT_A | Input | E16 |
| COM4_DCD | COM4_CTS_B | COM4_RT_B | Input | F16 |

## 5.11 USB

An NEC µPD720101 device provides five USB ports on the SBC610 and is connected to a 32-bit, 33 MHz PCI bus. The device is capable of operation at low-, full- or high-speed. The device contains two OHCI controllers (for USB1.1 operation) and one EHCI controller (for USB2.0 operation). Alternate ports use a different OCHI controller for USB1.1 operation and all ports share the EHCI controller for USB2.0 operation. The internal functions are configured as follows:

Table 5-16 EHCI Internal Functions

| Controller | PCI Function No | Interrupt | SBC610 Connection |
|---|---|---|---|
| OHCI0 | 0 | INTA~ | USB ports 1, 3 and 5 |
| OHCI1 | 1 | INTB~ | USB ports 2 and 4 |
| EHCI | 2 | INTC~ | USB ports 1 to 5 |

Two USB ports (ports 1 and 2 from the USB device) are available on the P4 connector as follows:

Table 5-17 USB1/USB2 Signal Availability

| Signal | P4 Pin | Signal | P4 Pin |
|---|---|---|---|
| USB1_P | A9 | USB2_P | D9 |
| USB1_N | B9 | USB2_N | E9 |
| USB1_PWR | B10 | USB2_PWR | C10 |

Ports 3 to 5 are routed to the AFIX P41 connector to accommodate USB AFIX modules such as the AFIXM or may be routed to the P6 connector if a module with appropriate I/O routing (such as the AFIXDIO1) is fitted to the site.

Table 5-18 USB3 to USB5 Signal Routing

| Signal | P41 Pin | Signal | P41 Pin | Signal | P41 Pin |
|---|---|---|---|---|---|
| USB3_P | G7 | USB4_P | G10 | USB5_P | G19 |
| USB3_N | G8 | USB4_N | G11 | USB5_N | G20 |

## 5.12 SATA

A Silicon Image Sil3512 device is used to provide two SATA ports from the SBC610, supporting Generation 1 transfer speeds of 1.5Gbits/s. The device is connected to a 32-bit, 33 MHz PCI bus.

The SATA ports are available on the P4 connector, as follows:

Table 5-19 SATA Signal Availability

| Signal | P4 Pin | Signal | P4 Pin |
|---|---|---|---|
| SATA0_TXP | A7 | SATA1_TXP | B8 |
| SATA0_TXN | B7 | SATA1_TXN | C8 |
| SATA0_RXP | D7 | SATA1_RXP | E8 |
| SATA0_RXN | E7 | SATA1_RXN | F8 |

Two activity LEDs are provided on the rear of the board, each indicating activity on one of the two Serial ATA channels.

## 5.13 GPIO

The SBC610 supports up to 19 GPIO lines, each with interrupt generation capabilities. These are 3.3 V single-ended signals with 5V tolerance. These signals are controlled by the I/O FPGA and can be configured as inputs, with the ability to generate level- or edge-triggered interrupts, or outputs, with totem-pole or open-drain drivers.

The GPIO signals are intended only to be used by GEIP software drivers. See the relevant software manual for details.

The GPIO signals are routed to the P6 connector via the AFIX connector (P41) and share I/O pins with the AFIX site. If no AFIX module is fitted, then the signals bypass the AFIX site and all 19 GPIO signals are available. If an AFIX module is fitted, then only the GPIO lines not used for AFIX I/O are available. To determine the number of GPIO present with a given AFIX, see the appropriate AFIX manual.

Table 5-20 and 5-21 show the GPIO line routing, via the AFIX connector (which remaps the signals) to the P6 connector.

GPIO lines 17 and 18 can also be used to control the behavior of BIT following reset. These signals are readable by software as BIT_MODE[1:0] in the Link Status Register and, if used for this purpose, should not be driven by the GPIO controller.

Table 5-20 GPIO Line Routing

| GPIO Line | P41 Input Pin | P41 Output Pin | P6 Pin |
|---|---|---|---|
| 0 | H2 | B5 | F8 |
| 1 | H3 | A6 | B9 |
| 2 | H5 | A8 | B10 |
| 3 | H6 | A9 | F10 |
| 4 | H8 | B12 | B11 |
| 5 | H9 | A13 | D11 |
| 6 | H11 | B13 | E11 |
| 7 | H12 | A14 | C12 |
| 8 | H14 | A16 | A13 |
| 9 | H15 | B16 | B13 |

| GPIO Line | P41 Input Pin | P41 Output Pin | P6 Pin |
|---|---|---|---|
| 10 | H20 | A17 | E13 |
| 11 | H21 | A21 | E14 |
| 12 | H23 | B21 | F14 |
| 13 | H24 | A22 | A15 |
| 14 | H26 | A24 | B15 |
| 15 | H27 | B24 | D15 |
| 16 | H29 | A25 | E15 |
| 17 | H30 | B25 | B16 |
| 18 | J29 | A28 | C16 |

When no AFIX is fitted, the P6 pinout on rows 7 to 16 is as follows:

Table 5-21 P6 Pin Assignments (No AFIX Fitted)

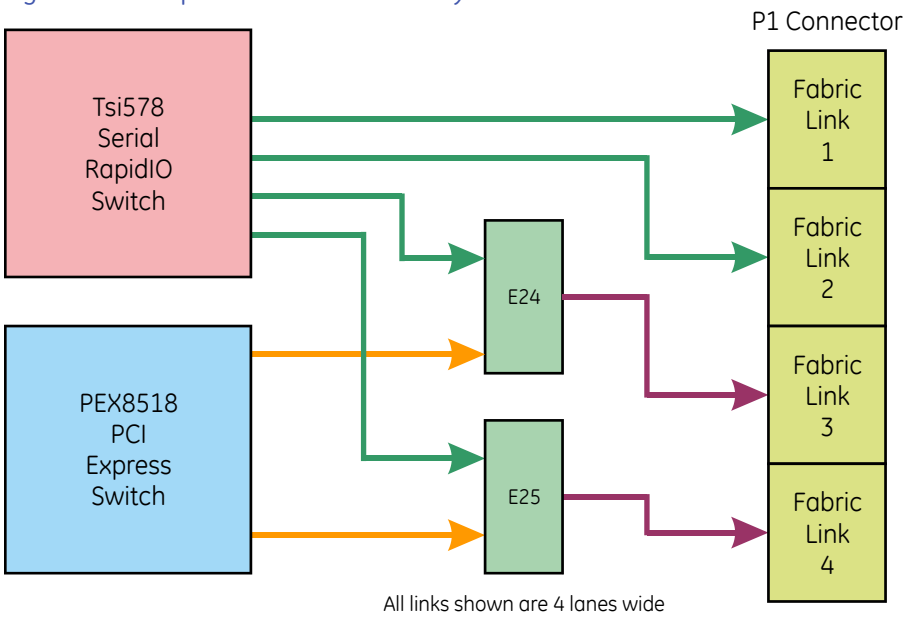
| Pin | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|
| 7 | No connection | No connection | GND | No connection | No connection | GND | No connection |
| 8 | GND | No connection | No connection | GND | No connection | GPIO0 | GND |
| 9 | No connection | GPIO1 | GND | No connection | No connection | GND | No connection |
| 10 | GND | GPIO2 | No connection | GND | No connection | GPIO3 | GND |
| 11 | No connection | GPIO4 | GND | GPIO5 | GPIO6 | GND | No connection |
| 12 | GND | No connection | GPIO7 | GND | No connection | No connection | GND |
| 13 | GPIO8 | GPIO9 | GND | No connection | GPIO10 | GND | No connection |
| 14 | GND | No connection | No connection | GND | GPIO11 | GPIO12 | GND |
| 15 | GPIO13 | GPIO14 | GND | GPIO15 | GPIO16 | GND | No connection |
| 16 | GND | GPIO17 | GPIO18 | GND | No connection | BITFAIL~ | GND |

## 5.14 Off-Board Serial Fabrics

VITA46 makes provision for four x4 off-board serial fabric links from the P1 connector.

The SBC610 provides two fixed SRIO ports and the option to allow the remaining two links to be configured as either SRIO or PCIe.

Figure 5-7 Backplane Fabric Connectivity




The fabric to be routed to Backplane Fabric Ports 3 and 4 on the P1 connector is selected by fitting Links E24 and E25. If the links are fitted, then PCIe is routed to the connector. If they are not fitted, then SRIO is routed to the connector. The state of these links is reflected in Control Register 2, and may be overridden by software if required.

### 5.14.1 PCI Express

The SBC610 uses a PLX PEX8518 PCIe switch to connect between the PEX8548 PCIe switch and the backplane PCIe ports. This device allows flexible port configurations and non-transparent ports to be used to meet a variety of customer requirements. Up to four backplane ports are available, sharing a maximum of 8 lanes.

Each PCIe port of the PEX8518 appears to software as a PCI-to-PCI bridge, with its own PCI- compatible configuration registers. Each port is accessed on the internal virtual PCI bus using a device number equal to its port number.

The port configuration of the switch is initially set up by hardware strapping to use two x4 transparent ports to the backplane, as shown below:

Table 5-22 PCIe Port Configuration

| Port | Width | Lanes | Link To | Upstream | Non-Transparent |
|---|---|---|---|---|---|
| 0 | x8 | 0 to 7 | PEX8548 Port 8 | Yes | No |
| 1 | x4 | 8 to 11 | Backplane Fabric Port 3 | No | No |
| 2 | x4 | 12 to 15 | Backplane Fabric Port 4 | No | No |

Port 0 is always configured as the upstream switch port with a width of x8. The configuration of the downstream ports of the switch, which are connected to the backplane, may be altered to meet specific system requirements. The following port configurations are supported:

Table 5-23 Supported PCIe Configurations

| Port 0 Width (Upstream) | Port 1 Width | Port 2 Width | Port 3 Width | Port 4 Width |
|---|---|---|---|---|
| x8 (Lanes 0-7) | x8 (Lanes 8-15) | | | |
| x8 (Lanes 0-7) | x4 (Lanes 8-11) | x4 (Lanes 12-15) | | |
| x8 (Lanes 0-7) | x4 (Lanes 8-11) | x2 (Lanes 12-13) | x2 (Lanes 14-15) | |
| x8 (Lanes 0-7) | x2 (Lanes 8-9) | x2 (Lanes 10-11) | x4 (Lanes 12-15) | |
| x8 (Lanes 0-7) | x2 (Lanes 8-9) | x4 (Lanes 10-13) | x2 (Lanes 14-15) | |
| x8 (Lanes 0-7) | x2 (Lanes 8-9) | x2 (Lanes 10-11) | x2 (Lanes 12-13) | x2 (Lanes 14-15) |

Each port is able to negotiate down to smaller link widths if required (such as if a fault occurs on any particular lane). Port widths of x1, x2, x4 and x8 are supported.

The PEX8518 also supports a non-transparent port which can be set to any one of the downstream ports. This feature allows the SBC610 to be connected to another host card, with the port providing windows and address translation between the address domains.

Any changes to the configuration of the PEX8518 (number and width of ports and selection of the non-transparent port) must be set up by software in the serial EEPROM. No alternative hardware strapping is provided for these features. This EEPROM is write-protected by default and can be write-enabled by clearing the Serial EEPROM Write Protect bit in Control Register 1. This bit may only be cleared when the NVRAM Write Enable Link (E18) is fitted and the backplane NVMRO signal (on connector P0 pin A4) is inactive low. The switch can be prevented from accessing the EEPROM, under software control, if the data becomes corrupted and configures the switch such that the EEPROM contents cannot be overwritten. This may be done by setting the PEX8518 Serial EEPROM Disable bit in Control Register 2 or by fitting the Recovery Boot Link (E14).

The PEX8518 is connected to I²C Bus 1 (Address 0x70) to allow configuration by the processor and out-of-band monitoring of link status.

The link status of each of the backplane PCI Express lanes is reflected by LEDs the rear of the PCB.

The PCI Express register block is intended to be made accessible from the PCI Express backplane, allowing external boards to interrupt the local processors and lock shared resources.

### 5.14.2 Serial RapidIO

The SBC610 can support up to four off-board x4 SRIO links on the P1 connector.

SRIO on the SBC610 is provided by a Tundra Tsi578 Serial RapidIO switch, which has eight x4 SRIO ports, capable of operating at 1.25, 2.5 and 3.125 GHz. The initial configuration of the ports is set by hardware strapping options as follows:

Table 5-24 SRIO Hardware Strapping Options

| Port | Width | Link To | Lane Reversal | Speed | Power-Down |
|---|---|---|---|---|---|
| 0 | x4 | MPC8641D SERDES2 Port | No | 3.125 GHz | No |
| 2 | x4 | Backplane Fabric Link 4 (via multiplexer) | No | 3.125 GHz | Yes |
| 4 | x4 | Backplane Fabric Link 1 | No | 3.125 GHz | Yes |
| 6 | x4 | Unused | No | 3.125 GHz | Yes |
| 8 | x4 | Unused | No | 3.125 GHz | Yes |
| 10 | x4 | Backplane Fabric Link 3 (via multiplexer) | No | 3.125 GHz | Yes |
| 12 | x4 | Backplane Fabric Link 2 | No | 3.125 GHz | Yes |
| 14 | x4 | Unused | No | 3.125 GHz | Yes |

All SRIO ports are powered-down by default by resistor strapping options. Any ports that are required to be used must be enabled either by configuration EEPROM or software via I²C.

The default port speed is configured (by resistor strapping options) to be 3.125 GHz.

An I²C configuration EEPROM for the switch is provided on I²C Bus 2 to allow initial power-up configuration to be performed if required. The EEPROM is write-protected by default to ensure its contents are not corrupted. It may be write-enabled by software only when the NVRAM Write Enable Link (E18) is fitted and the backplane NVMRO signal (on connector P0 pin A4) is inactive low. The switch can be prevented from accessing the EEPROM, under software control, if the data becomes corrupted and configures the switch such that it cannot be overwritten. This may be done by setting the Tsi578 I²C EEPROM Disable bit in Control Register 2 or by fitting a jumper on the Recovery Boot Link (E14).

The Tsi578 is connected to I²C Bus 2 (address 0x02) to allow it to access its configuration EEPROM, be configured by software or provide out-of-band monitoring of the link status.

The Tsi578 is able to generate a reset on the SBC610 or an interrupt to a local processor core in response to an internal event or if requested by an external host.

## 5.15 Mezzanines

### 5.15.1 PMC/XMC Sites

The SBC610 has two mezzanine sites that both support PMCs or XMCs (including support for front-panel I/O). The two mezzanine sites are spaced to allow fitting of a double-width PMC/XMC if required.

The presence of a PMC or XMC in a site can be read from the Board Configuration Register.

### 5.15.2 PCI Mezzanine Cards (PMCs)

Each site has Jn1, Jn2, Jn3 and Jn4 connectors to provide a 64-bit PCI bus capable of PCI-X operation at frequencies of up to 133 MHz.

Each PCI bus is connected to a PEX8114 PCIe-to-PCI Bridge, which provides frequency negotiation, clocks and arbitration for the bus. The PEX8114 device is not 5V-tolerant and so the SBC610 does not support PMCs which use 5V signaling.

CAUTION

The SBC610 PMC site is *not* 5V tolerant. *Do not* fit PMCs that use 5V signaling

Each PMC site has a dedicated PCI bus, so fitting a PMC that runs at a lower frequency does not limit the other PMC or the performance of other functions of the SBC610.

### 5.15.3 PCI Express Mezzanine Cards (XMCs)

Each site also provides Jn5 and Jn6 connectors. Jn5 provides a x8 PCIe link to the PEX8548 switch and Jn6 is used to route XMC I/O to the backplane.

### 5.15.4 I/O Routing

Rear I/O tracking is provided from the Jn4 and Jn6 connectors of both PMC/XMC sites to the rear connectors in accordance with VITA 46.9. This can be in one of the following configurations:

For Site 1:

- P64sX12d (full 64 PMC signals from J14 and 12 differential XMC signals from J16)
- X20d38s (10 PMC signals from J14, full 20 differential and 38 single ended XMC signals from J16)

For Site 2:

- P64sX12d (full 64 PMC signals from J24 and 12 differential XMC signals from J26)
- X20d38s (10 PMC signals from J24, full 20 differential and 38 single ended XMC signals from J26)
- 16 PMC signals from J24, 12 differential XMC signals from J26, COM3/4/5/6
- 48 PMC signals from J24, 12 differential XMC signals from J26, COM5/6

The configuration selected can be read from the Board Configuration Register. Further custom splits are possible if required to suit a particular mezzanine card.

The I/O from PMC connector Jn4 pins 1 to 48 is tracked as 50Ω single ended signals, and that from pins 49 to 64 is tracked as 100Ω differential pairs (49 and 51, 50 and 52, etc.)

The I/O from XMC connectors Jn6 pins C1 to C19 and F1 to F19 is tracked as 50Ω Single Ended signals and that from columns A, B, D and E is tracked as 100Ω differential pairs (A01 and B01, D01 and E01, etc.)

## Table 5-25 PMC/XMC Site 1 Signal Availability

### P64s+X12d Option

| PMC I/O | P3 Pin | PMC I/O | P3 Pin | XMC I/O | P4 Pin |
|---|---|---|---|---|---|
| P14_IO_1 | E1 | P14_IO_33 | E9 | P16_IO_A05 | E1 |
| P14_IO_2 | B1 | P14_IO_34 | B9 | P16_IO_B05 | D1 |
| P14_IO_3 | D1 | P14_IO_35 | D9 | P16_IO_D05 | B1 |
| P14_IO_4 | A1 | P14_IO_36 | A9 | P16_IO_E05 | A1 |
| P14_IO_5 | F2 | P14_IO_37 | F10 | P16_IO_A07 | F2 |
| P14_IO_6 | C2 | P14_IO_38 | C10 | P16_IO_B07 | E2 |
| P14_IO_7 | E2 | P14_IO_39 | E10 | P16_IO_D07 | C2 |
| P14_IO_8 | B2 | P14_IO_40 | B10 | P16_IO_E07 | B2 |
| P14_IO_9 | E3 | P14_IO_41 | E11 | P16_IO_A09 | E3 |
| P14_IO_10 | B3 | P14_IO_42 | B11 | P16_IO_B09 | D3 |
| P14_IO_11 | D3 | P14_IO_43 | D11 | P16_IO_D09 | B3 |
| P14_IO_12 | A3 | P14_IO_44 | A11 | P16_IO_E09 | A3 |
| P14_IO_13 | F4 | P14_IO_45 | F12 | P16_IO_A15 | F4 |
| P14_IO_14 | C4 | P14_IO_46 | C12 | P16_IO_B15 | E4 |
| P14_IO_15 | E4 | P14_IO_47 | E12 | P16_IO_D15 | C4 |
| P14_IO_16 | B4 | P14_IO_48 | B12 | P16_IO_E15 | B4 |
| P14_IO_17 | E5 | P14_IO_49 | E13 | P16_IO_A17 | E5 |
| P14_IO_18 | B5 | P14_IO_50 | B13 | P16_IO_B17 | D5 |
| P14_IO_19 | D5 | P14_IO_51 | D13 | P16_IO_D17 | B5 |
| P14_IO_20 | A5 | P14_IO_52 | A13 | P16_IO_E17 | A5 |
| P14_IO_21 | F6 | P14_IO_53 | F14 | P16_IO_A19 | F6 |
| P14_IO_22 | C6 | P14_IO_54 | C14 | P16_IO_B19 | E6 |
| P14_IO_23 | E6 | P14_IO_55 | E14 | P16_IO_D19 | C6 |
| P14_IO_24 | B6 | P14_IO_56 | B14 | P16_IO_E19 | B6 |
| P14_IO_25 | E7 | P14_IO_57 | E15 | | |
| P14_IO_26 | B7 | P14_IO_58 | B15 | | |
| P14_IO_27 | D7 | P14_IO_59 | D15 | | |
| P14_IO_28 | A7 | P14_IO_60 | A15 | | |
| P14_IO_29 | F8 | P14_IO_61 | F16 | | |
| P14_IO_30 | C8 | P14_IO_62 | C16 | | |
| P14_IO_31 | E8 | P14_IO_63 | E16 | | |
| P14_IO_32 | B8 | P14_IO_64 | B16 | | |

### P10s+X20d38s Option

| PMC I/O | P3 Pin | XMC I/O | P3 Pin | XMC I/O | P3 Pin | XMC I/O | P4 Pin |
|---|---|---|---|---|---|---|---|
| P14_IO_1 | E1 | P16_IO_C01 | B3 | P16_IO_A01 | E13 | P16_IO_A05 | E1 |
| P14_IO_2 | B1 | P16_IO_F01 | A3 | P16_IO_B01 | D13 | P16_IO_B05 | D1 |
| P14_IO_3 | D1 | P16_IO_C02 | F4 | P16_IO_D01 | B13 | P16_IO_D05 | B1 |
| P14_IO_4 | A1 | P16_IO_C03 | E4 | P16_IO_E01 | A13 | P16_IO_E05 | A1 |
| P14_IO_5 | F2 | P16_IO_F02 | C4 | P16_IO_A03 | F14 | P16_IO_A07 | F2 |
| P14_IO_6 | C2 | P16_IO_F03 | B4 | P16_IO_B03 | E14 | P16_IO_B07 | E2 |
| P14_IO_7 | E2 | P16_IO_C04 | E5 | P16_IO_D03 | C14 | P16_IO_D07 | C2 |
| P14_IO_8 | B2 | P16_IO_C05 | D5 | P16_IO_E03 | B14 | P16_IO_E07 | B2 |
| P14_IO_9 | E3 | P16_IO_F04 | B5 | P16_IO_A11 | E15 | P16_IO_A09 | E3 |
| | | P16_IO_F05 | A5 | P16_IO_B11 | D15 | P16_IO_B09 | D3 |
| P14_IO_11 | D3 | P16_IO_C06 | F6 | P16_IO_D11 | B15 | P16_IO_D09 | B3 |
| | | P16_IO_C07 | E6 | P16_IO_E11 | A15 | P16_IO_E09 | A3 |
| | | P16_IO_F06 | C6 | P16_IO_A13 | F16 | P16_IO_A15 | F4 |
| | | P16_IO_C07 | B6 | P16_IO_B13 | E16 | P16_IO_B15 | E4 |
| | | P16_IO_C08 | E7 | P16_IO_D13 | C16 | P16_IO_D15 | C4 |
| | | P16_IO_C09 | D7 | P16_IO_E13 | B16 | P16_IO_E15 | B4 |
| | | P16_IO_F08 | B7 | | | P16_IO_A17 | E5 |
| | | P16_IO_F09 | A7 | | | P16_IO_B17 | D5 |
| | | P16_IO_C10 | F8 | | | P16_IO_D17 | B5 |
| | | P16_IO_C11 | E8 | | | P16_IO_E17 | A5 |
| | | P16_IO_F10 | C8 | | | P16_IO_A19 | F6 |
| | | P16_IO_F11 | B8 | | | P16_IO_B19 | E6 |
| | | P16_IO_C12 | E9 | | | P16_IO_D19 | C6 |
| | | P16_IO_C13 | D9 | | | P16_IO_E19 | B6 |
| | | P16_IO_F12 | B9 | | | | |
| | | P16_IO_F13 | A9 | | | | |
| | | P16_IO_C14 | F10 | | | | |
| | | P16_IO_C15 | E10 | | | | |
| | | P16_IO_F14 | C10 | | | | |
| | | P16_IO_F15 | B10 | | | | |
| | | P16_IO_C16 | E11 | | | | |
| | | P16_IO_C17 | D11 | | | | |
| | | P16_IO_F16 | B11 | | | | |
| | | P16_IO_F17 | A11 | | | | |
| | | P16_IO_C18 | F12 | | | | |
| | | P16_IO_C19 | E12 | | | | |
| | | P16_IO_F18 | C12 | | | | |
| | | P16_IO_F19 | B12 | | | | |

= Differential pairs

## Table 5-26 PMC/XMC Site 2 Signal Availability 1

### P64s+X12d Option

| PMC I/O | P5 Pin | PMC I/O | P5 Pin | XMC I/O | P6 Pin |
|---|---|---|---|---|---|
| P24_IO_1 | E1 | P24_IO_33 | E9 | P26_IO_A05 | E1 |
| P24_IO_2 | B1 | P24_IO_34 | B9 | P26_IO_B05 | D1 |
| P24_IO_3 | D1 | P24_IO_35 | D9 | P26_IO_D05 | B1 |
| P24_IO_4 | A1 | P24_IO_36 | A9 | P26_IO_E05 | A1 |
| P24_IO_5 | F2 | P24_IO_37 | F10 | P26_IO_A07 | F2 |
| P24_IO_6 | C2 | P24_IO_38 | C10 | P26_IO_B07 | E2 |
| P24_IO_7 | E2 | P24_IO_39 | E10 | P26_IO_D07 | C2 |
| P24_IO_8 | B2 | P24_IO_40 | B10 | P26_IO_E07 | B2 |
| P24_IO_9 | E3 | P24_IO_41 | E11 | P26_IO_A09 | E3 |
| P24_IO_10 | B3 | P24_IO_42 | B11 | P26_IO_B09 | D3 |
| P24_IO_11 | D3 | P24_IO_43 | D11 | P26_IO_D09 | B3 |
| P24_IO_12 | A3 | P24_IO_44 | A11 | P26_IO_E09 | A3 |
| P24_IO_13 | F4 | P24_IO_45 | F12 | P26_IO_A15 | F4 |
| P24_IO_14 | C4 | P24_IO_46 | C12 | P26_IO_B15 | E4 |
| P24_IO_15 | E4 | P24_IO_47 | E12 | P26_IO_D15 | C4 |
| P24_IO_16 | B4 | P24_IO_48 | B12 | P26_IO_E15 | B4 |
| P24_IO_17 | E5 | P24_IO_49 | E13 | P26_IO_A17 | E5 |
| P24_IO_18 | B5 | P24_IO_50 | B13 | P26_IO_B17 | D5 |
| P24_IO_19 | D5 | P24_IO_51 | D13 | P26_IO_D17 | B5 |
| P24_IO_20 | A5 | P24_IO_52 | A13 | P26_IO_E17 | A5 |
| P24_IO_21 | F6 | P24_IO_53 | F14 | P26_IO_A19 | F6 |
| P24_IO_22 | C6 | P24_IO_54 | C14 | P26_IO_B19 | E6 |
| P24_IO_23 | E6 | P24_IO_55 | E14 | P26_IO_D19 | C6 |
| P24_IO_24 | B6 | P24_IO_56 | B14 | P26_IO_E19 | B6 |
| P24_IO_25 | E7 | P24_IO_57 | E15 | | |
| P24_IO_26 | B7 | P24_IO_58 | B15 | | |
| P24_IO_27 | D7 | P24_IO_59 | D15 | | |
| P24_IO_28 | A7 | P24_IO_60 | A15 | | |
| P24_IO_29 | F8 | P24_IO_61 | F16 | | |
| P24_IO_30 | C8 | P24_IO_62 | C16 | | |
| P24_IO_31 | E8 | P24_IO_63 | E16 | | |
| P24_IO_32 | B8 | P24_IO_64 | B16 | | |

### P10s+X20d38s Option

| PMC I/O | P5 Pin | XMC I/O | P6 Pin | XMC I/O | P6 Pin | XMC I/O | P6 Pin |
|---|---|---|---|---|---|---|---|
| P24_IO_1 | E1 | P26_IO_C01 | B3 | P26_IO_A01 | E13 | P26_IO_A05 | E1 |
| P24_IO_2 | B1 | P26_IO_F01 | A3 | P26_IO_B01 | D13 | P26_IO_B05 | D1 |
| P24_IO_3 | D1 | P26_IO_C02 | F4 | P26_IO_D01 | B13 | P26_IO_D05 | B1 |
| P24_IO_4 | A1 | P26_IO_C03 | E4 | P26_IO_E01 | A13 | P26_IO_E05 | A1 |
| P24_IO_5 | F2 | P26_IO_F02 | C4 | P26_IO_A03 | F14 | P26_IO_A07 | F2 |
| P24_IO_6 | C2 | P26_IO_F03 | B4 | P26_IO_B03 | E14 | P26_IO_B07 | E2 |
| P24_IO_7 | E2 | P26_IO_C04 | E5 | P26_IO_D03 | C14 | P26_IO_D07 | C2 |
| P24_IO_8 | B2 | P26_IO_C05 | D5 | P26_IO_E03 | B14 | P26_IO_E07 | B2 |
| P24_IO_9 | E3 | P26_IO_F04 | B5 | P26_IO_A11 | E15 | P26_IO_A09 | E3 |
| | | P26_IO_F05 | A5 | P26_IO_B11 | D15 | P26_IO_B09 | D3 |
| P24_IO_11 | D3 | P26_IO_C06 | F6 | P26_IO_D11 | B15 | P26_IO_D09 | B3 |
| | | P26_IO_C07 | E6 | P26_IO_E11 | A15 | P26_IO_E09 | A3 |
| | | P26_IO_F06 | C6 | P26_IO_A13 | F16 | P26_IO_A15 | F4 |
| | | P26_IO_C07 | B6 | P26_IO_B13 | E16 | P26_IO_B15 | E4 |
| | | P26_IO_C08 | E7 | P26_IO_D13 | C16 | P26_IO_D15 | C4 |
| | | P26_IO_C09 | D7 | P26_IO_E13 | B16 | P26_IO_E15 | B4 |
| | | P26_IO_F08 | B7 | | | P26_IO_A17 | E5 |
| | | P26_IO_F09 | A7 | | | P26_IO_B17 | D5 |
| | | P26_IO_C10 | F8 | | | P26_IO_D17 | B5 |
| | | P26_IO_C11 | E8 | | | P26_IO_E17 | A5 |
| | | P26_IO_F10 | C8 | | | P26_IO_A19 | F6 |
| | | P26_IO_F11 | B8 | | | P26_IO_B19 | E6 |
| | | P26_IO_C12 | E9 | | | P26_IO_D19 | C6 |
| | | P26_IO_C13 | D9 | | | P26_IO_E19 | B6 |
| | | P26_IO_F12 | B9 | | | | |
| | | P26_IO_F13 | A9 | | | | |
| | | P26_IO_C14 | F10 | | | | |
| | | P26_IO_C15 | E10 | | | | |
| | | P26_IO_F14 | C10 | | | | |
| | | P26_IO_F15 | B10 | | | | |
| | | P26_IO_C16 | E11 | | | | |
| | | P26_IO_C17 | D11 | | | | |
| | | P26_IO_F16 | B11 | | | | |
| | | P26_IO_F17 | A11 | | | | |
| | | P26_IO_C18 | F12 | | | | |
| | | P26_IO_C19 | E12 | | | | |
| | | P26_IO_F18 | C12 | | | | |
| | | P26_IO_F19 | B12 | | | | |

## Table 5-27 PMC/XMC Site 2 Signal Availability 2

### P16s+X12d+COM3-6 Option

| PMC I/O | P5 Pin | COMs | P5 Pin | XMC I/O | P6 Pin |
|---|---|---|---|---|---|
| P24_IO_1 | E1 | COM3_RX_B | E5 | P26_IO_A05 | E1 |
| P24_IO_2 | B1 | COM3_RX_A | D5 | P26_IO_B05 | D1 |
| P24_IO_3 | D1 | COM3_TX_B | B5 | P26_IO_D05 | B1 |
| P24_IO_4 | A1 | COM3_TX_A | A5 | P26_IO_E05 | A1 |
| P24_IO_5 | F2 | COM3_CTS_B | F6 | P26_IO_A07 | F2 |
| P24_IO_6 | C2 | COM3_CTS_A | E6 | P26_IO_B07 | E2 |
| P24_IO_7 | E2 | COM3_RTS_B | C6 | P26_IO_D07 | C2 |
| P24_IO_8 | B2 | COM3_RTS_A | B6 | P26_IO_E07 | B2 |
| P24_IO_9 | E3 | COM3_RT_B | E7 | P26_IO_A09 | E3 |
| P24_IO_10 | B3 | COM3_RT_A | D7 | P26_IO_B09 | D3 |
| P24_IO_11 | D3 | COM3_TT_B | B7 | P26_IO_D09 | B3 |
| P24_IO_12 | A3 | COM3_TT_A | A7 | P26_IO_E09 | A3 |
| P24_IO_13 | F4 | COM3_ST_B | F8 | P26_IO_A15 | F4 |
| P24_IO_14 | C4 | COM3_ST_A | E8 | P26_IO_B15 | E4 |
| P24_IO_15 | E4 | COM4_RX_B | E9 | P26_IO_D15 | C4 |
| P24_IO_16 | B4 | COM4_RX_A | D9 | P26_IO_E15 | B4 |
| | | COM4_TX_B | B9 | P26_IO_A17 | E5 |
| | | COM4_TX_A | A9 | P26_IO_B17 | D5 |
| | | COM4_CTS_B | F10 | P26_IO_D17 | B5 |
| | | COM4_CTS_A | E10 | P26_IO_E17 | A5 |
| | | COM4_RTS_B | C10 | P26_IO_A19 | F6 |
| | | COM4_RTS_A | B10 | P26_IO_B19 | E6 |
| | | COM4_RT_B | E11 | P26_IO_D19 | C6 |
| | | COM4_RT_A | D11 | P26_IO_E19 | B6 |
| | | COM4_TT_B | B11 | | |
| | | COM4_TT_A | A11 | | |
| | | COM4_ST_B | F12 | | |
| | | COM4_ST_A | E12 | | |
| | | COM5_RX_B | E13 | | |
| | | COM5_RX_A | D13 | | |
| | | COM5_TX_B | B13 | | |
| | | COM5_TX_A | A13 | | |
| | | COM5_CTS_B | F14 | | |
| | | COM5_CTS_A | E14 | | |
| | | COM5_RTS_B | C14 | | |
| | | COM5_RTS_A | B14 | | |
| | | COM6_RX_B | E15 | | |
| | | COM6_RX_A | D15 | | |
| | | COM6_TX_B | B15 | | |
| | | COM6_TX_A | A15 | | |
| | | COM6_CTS_B | F16 | | |
| | | COM6_CTS_A | E16 | | |
| | | COM6_RTS_B | C16 | | |
| | | COM6_RTS_A | B16 | | |

### P48s+X12d+COM5-6 Option

| PMC I/O | P5 Pin | PMC I/O | P5 Pin | COMs | P5 Pin | XMC I/O | P6 Pin |
|---|---|---|---|---|---|---|---|
| P24_IO_1 | E1 | P24_IO_33 | E9 | COM5_RX_B | E13 | P26_IO_A05 | E1 |
| P24_IO_2 | B1 | P24_IO_34 | B9 | COM5_RX_A | D13 | P26_IO_B05 | D1 |
| P24_IO_3 | D1 | P24_IO_35 | D9 | COM5_TX_B | B13 | P26_IO_D05 | B1 |
| P24_IO_4 | A1 | P24_IO_36 | A9 | COM5_TX_A | A13 | P26_IO_E05 | A1 |
| P24_IO_5 | F2 | P24_IO_37 | F10 | COM5_CTS_B | F14 | P26_IO_A07 | F2 |
| P24_IO_6 | C2 | P24_IO_38 | C10 | COM5_CTS_A | E14 | P26_IO_B07 | E2 |
| P24_IO_7 | E2 | P24_IO_39 | E10 | COM5_RTS_B | C14 | P26_IO_D07 | C2 |
| P24_IO_8 | B2 | P24_IO_40 | B10 | COM5_RTS_A | B14 | P26_IO_E07 | B2 |
| P24_IO_9 | E3 | P24_IO_41 | E11 | COM6_RX_B | E15 | P26_IO_A09 | E3 |
| P24_IO_10 | B3 | P24_IO_42 | B11 | COM6_RX_A | D15 | P26_IO_B09 | D3 |
| P24_IO_11 | D3 | P24_IO_43 | D11 | COM6_TX_B | B15 | P26_IO_D09 | B3 |
| P24_IO_12 | A3 | P24_IO_44 | A11 | COM6_TX_A | A15 | P26_IO_E09 | A3 |
| P24_IO_13 | F4 | P24_IO_45 | F12 | COM6_CTS_B | F16 | P26_IO_A15 | F4 |
| P24_IO_14 | C4 | P24_IO_46 | C12 | COM6_CTS_A | E16 | P26_IO_B15 | E4 |
| P24_IO_15 | E4 | P24_IO_47 | E12 | COM6_RTS_B | C16 | P26_IO_D15 | C4 |
| P24_IO_16 | B4 | P24_IO_48 | B12 | COM6_RTS_A | B16 | P26_IO_E15 | B4 |
| P24_IO_17 | E5 | | | | | P26_IO_A17 | E5 |
| P24_IO_18 | B5 | | | | | P26_IO_B17 | D5 |
| P24_IO_19 | D5 | | | | | P26_IO_D17 | B5 |
| P24_IO_20 | A5 | | | | | P26_IO_E17 | A5 |
| P24_IO_21 | F6 | | | | | P26_IO_A19 | F6 |
| P24_IO_22 | C6 | | | | | P26_IO_B19 | E6 |
| P24_IO_23 | E6 | | | | | P26_IO_D19 | C6 |
| P24_IO_24 | B6 | | | | | P26_IO_E19 | B6 |
| P24_IO_25 | E7 | | | | | | |
| P24_IO_26 | B7 | | | | | | |
| P24_IO_27 | D7 | | | | | | |
| P24_IO_28 | A7 | | | | | | |
| P24_IO_29 | F8 | | | | | | |
| P24_IO_30 | C8 | | | | | | |
| P24_IO_31 | E8 | | | | | | |
| P24_IO_32 | B8 | | | | | | |

### 5.15.5 AFIX Site

An AFIX site is provided. This is a proprietary interface allowing additional functionality to be added without taking up a PMC site.

GEIP's current range of AFIX cards includes support for dual MIL-STD-1553 interfaces (AFIX1553), SCSI and graphics (AFIXSG), USB Flash memory (AFIXM) and differential GPIO (AFIXDIO1).

This site also allows specific customer requirements to be accommodated more quickly and easily than a modification to the main host board. Contact your local sales representative with any specific requirements.

The AFIX site is connected to a 32-bit 33MHz PCI bus, shared with the SATA and USB functions.

An 8-bit, multiplexed address/data, parallel I/O bus is also provided for communication with devices on the AFIX that do not support a PCI interface and to determine the type of AFIX fitted to the board. This interface is accessed using Chip Select 5 on the MPC8461D Local Bus interface.

The AFIX I/O is routed to the P6 connector.

The presence of an AFIX card in the site can be determined from the Board Configuration Register.

## 5.16 VME

The SBC610 uses a Tundra Semiconductors Tsi148 (“Tempe”) PCI-to-VME bridge to provide a full master/slave VME interface.

The Tsi148 is compliant with the following standards:

- American National Standard for VME64 (ANSI/VITA 1.0 - 1994 (R2002))
- American National Standard for VME64 Extensions (ANSI/VITA 1.1 - 1997)
- Source Synchronous Transfer (2eSST) Standard (ANSI/VITA 1.5 – 2003)

The Tsi148 features:

- Support for 2eVME and 2eSST protocols
- Full VMEbus system controller functionality
- Interrupt and Interrupt handling capability
- Two independent DMA controllers

VME System Controller status can be read from the Address Register.

### 5.16.1 VMEbus Compliance

Table 5-28 VMEbus Compliance

| | |
|---|---|
| Master: | A16, A24, A32 and A64<br>D08(EO), D16 and D32 Single Cycle Transaction (SCT)<br>D08(EO), D16 and D32 Read Modify Write Transaction (RMW)<br>D16 and D32 Block Transaction (BLT)<br>D64 Multiple Block Transaction (MBLT)<br>D64 2eVME<br>D64 2eSST |
| Slave: | A16, A24, A32 and A64<br>D08(EO), D16 and D32 Single Cycle Transaction (SCT)<br>D08(EO), D16 and D32 Block Transaction (BLT)<br>D64 Multiple Block Transaction (MBLT)<br>D64 2eVME<br>D64 2eSST |
| Interrupt Handler: | IH(1-7)<br>D08(O), D16, D32 |
| Interrupter: | I(1-7)<br>D08(O) |
| VMEbus Arbiter: | SGL, RRS, PRI |
| VMEbus Requester: | ROR, RWD, FAIR |
| Bus Time-out Module: | Disable, 8, 16, 32, 64, 128, 256, 512, 1024, 2048µs |
| Other Slot 1 Functions | IACK~ Daisy Chain driver<br>SYSCLK Driver<br>First Slot Detector |
| Auto Slot ID: | VME64 specified mode or Geographical Addressing via five-row P1 connector |

### 5.16.2 VMEbus Master Access

Eight software programmable PCI target images are available for master accesses to the VMEbus. An offset may be applied to translate the local address to a different address on the VMEbus, allowing access to any VMEbus address.

VMEbus master read cycles use delayed transactions. Delayed transactions are used to free the PCI bus from waiting for the potentially long VMEbus arbitration and transfer. The Tsi148 manages the completion of the read transfer on the VMEbus, issuing retries on the PCI bus until the transfer is completed. This allows other PCI bus masters to use the PCI bus while the VMEbus transfer is in progress.

VMEbus master write cycles use posted writes. Posted writes are acknowledged immediately on the PCI bus, allowing the PCI bus to be used by other masters while the VMEbus transfer is in progress. The transaction is queued in a write buffer until the VMEbus is available for the data to be transferred. If the posted write buffer is full, the PCI transaction is retried until there is space available.

The Tsi148 is able to accept its own transaction on the VMEbus, if the address driven by the VME master falls within a VME slave address window.

### 5.16.3 VMEbus Slave Access

Eight software programmable VMEbus slave images are available. An offset may be applied to translate the VMEbus address to a different address on the PCI bus, allowing any VMEbus address to access any on-board address.

The Tsi148 internal registers can be accessed as part of the 512 KByte CR/CSR area at an address dependent on its Geographic Address as defined in the VME64 standard.

Single Cycle Transaction VMEbus slave read accesses cause the VMEbus acknowledgement to be held until the data is received from the PCI bus. In the case of block read transfers, the VME slave requests a block of data from the PCI bus, which is stored in a read buffer until it is needed to complete a VMEbus transaction.

All VMEbus slave write transactions are posted. Write data is queued in the write buffer until the PCI bus is available for the data to be transferred. The transaction is immediately acknowledged on the VMEbus.

VMEbus slave Read-Modify-Write transactions are accepted but cannot be completed as indivisible cycles on the PCI bus as the PCI LOCK signal is not support.

### 5.16.4 VMEbus Master Block Transfers (DMA)

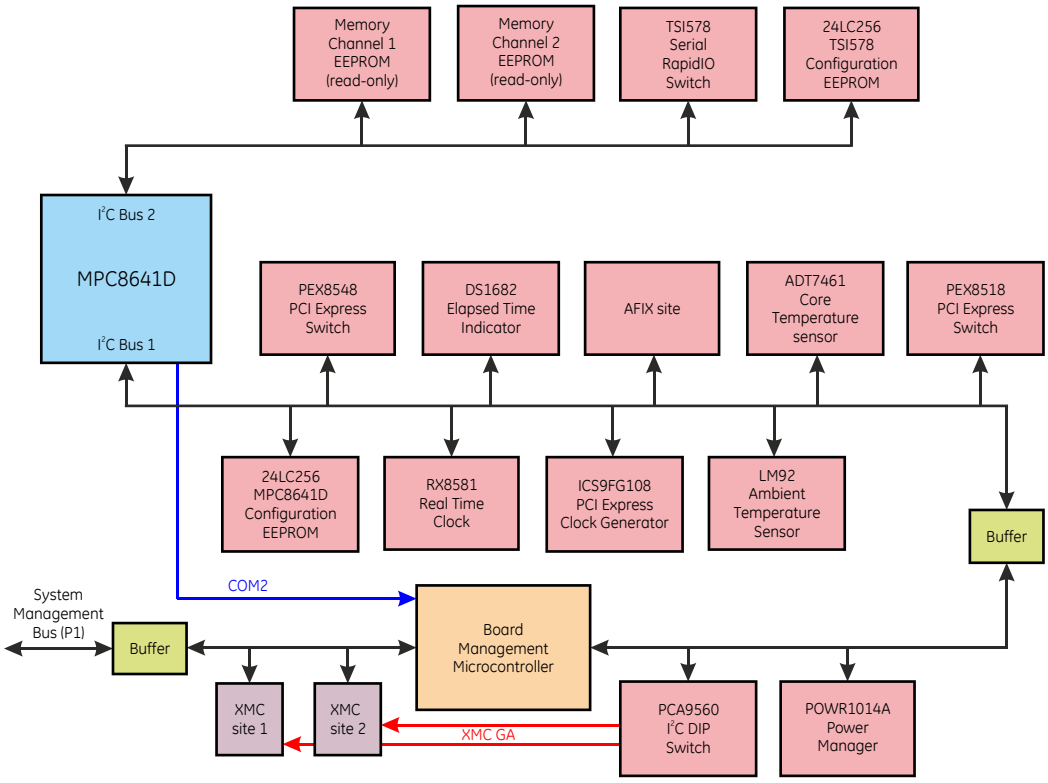
The Tsi148 has two independent DMA controllers, which may be used to transfer data between the PCI and the VMEbus. The controllers support 32 or 64-bit burst transfers on the PCI bus and 16, 32 or 64-bit transfers on the VMEbus. The DMA controllers support both direct and linked-list operation modes.

All DMA operations are passed through buffers in the DMA controller.

## 5.17 I²C Buses

The MPC8641D provides two I²C buses.

Figure 5-8 I²C Architecture




I²C Bus 2 connects to two read-only EEPROMs, which contain the configuration data for the two DDR2 memory interfaces. It also connects to the Tsi578 Serial Rapid IO Switch and its EEPROM.

All other devices with an I²C interface are connected to I²C Bus 1 to allow monitoring, either by the processor or by an external device via the Board Management Microcontroller.

Where I²C addresses are quoted in the following sections, the 8-bit address is the value that would be used to write to the device on the bus (i.e. the 7-bit device address and the LSB set to '0').

### 5.17.1 I²C Reset

An I²C bus may potentially lock-up if the reset is applied (stopping the I²C clock) when a slave device (without a reset pin) is driving out data.

The Local Bus Control FPGA provides logic to recover both I²C buses from this locked-up state by clocking the bus during reset until the data line is released.

### 5.17.2 Addressing

Table 5-29 $I^2C$ Bus Addresses

| Device | 7-Bit Address (Hex) | 8-Bit Address (Hex) |
|---|---|---|
| MPC8641D | Software Programmable (00 by default) | Software Programmable (00 by default) |
| Bus 1 | | |
| PSU Manager | 40 | 80 |
| Board Temp Sensor | 48 | 90 |
| Core Temp Sensor | 4C | 98 |
| PCA9650 I2C DIP Switch | 4E | 9C |
| MPC8641D Config EEPROM | 50 | A0 |
| Real-Time Clock | 51 | A2 |
| PEX8548 PCIe Switch | 58 | B0 |
| PEX8518 PCI Express Switch | 70 | E0 |
| Elapsed-Time Indicator | 6B | D6 |
| PCIe Clock Generator | 6E | DC |
| Bus 2 | | |
| Tsi578 Serial RapidIO Switch | 02 | 04 |
| RAM Channel 1 Config EEPROM | 50 | A0 |
| RAM Channel 2 Config EEPROM | 51 | A2 |
| Tsi578 Config EEPROM | 52 | A4 |

### 5.17.3 Real-Time Clock

The SBC610 provides an Epson RX8581 RTC, which has a minimum of 1 second resolution. This device can be powered from the P3V3_AUX supply or the VBAT signal (P1 pin G3) when the main power supply is removed.

The interrupt output of this device can generate an interrupt to either processor core, via the Register FPGA.

### 5.17.4 Elapsed Time Indicator

A Dallas DS1682 ETI logs the amount of time the SBC610 has been powered and the number of power cycles.

### 5.17.5 Temperature Sensors

The SBC610 has two temperate sensors: an ADT7461 remotely monitors the MPC8641D core temperature and the ambient temperature, and an LM92 monitors the ambient temperature on the PCB.

The interrupt outputs of these devices can generate interrupts to either processor core, via the Register FPGA, at two software-defined thresholds. One of these thresholds can optionally be configured to generate a Machine-Check exception.

### 5.17.6 Power Manager

The SBC610 uses a Lattice ispPAC-POWR1014A to monitor and sequence the on-board voltages. The device provides an I²C interface that can be used to access an internal A-to-D converter to measure the value of each of the on-board voltage rails, as shown below. Discrete inputs to and outputs from the device can also be monitored.

Table 5-30 Power Manager Monitor Points

| POWR1014A Input | Rail Monitored | Nominal Voltage |
|---|---|---|
| VMON1 | VCC | 5.00V |
| VMON2 | P3V3_AUX | 3.30V |
| VMON3 | P3V3 | 3.30V |
| VMON4 | P2V5 | 2.50V |
| VMON5 | P1V8 | 1.80V |
| VMON6 | P1V5 | 1.50V |
| VMON7 | P1V2 | 1.20V |
| VMON8 | Rev 1 – VBAT | 3.00V (Optional) |
| | Rev 2+ – PVDD_PLAT | 1.05V |
| VMON9 | VCORE | 1.05 (8641/D) |
| | | 0.95 (8640/D) |
| VMON10 | P1V | 1.00 |

### 5.17.7 I²C DIP Switch

The XMC sites each have a 3-bit Geographic Address, which is used to access the board information on the System Management bus. Due to the number of potential XMC sites in the system, this address cannot be derived from the board Geographic Address and must be configured by the user on the sites that are occupied.

The SBC610 uses a PCA9650 I²C DIP Switch device to provide six discrete outputs (three to each XMC Site GA) from non-volatile EEPROM registers within the device. These can be configured by the user to suit the system requirements. The value of the GA pins is determined by the value of EEPROM Register 0 as shown in the table below:

Table 5-31 EEPROM Register 0

| Register | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| EEPROM Register 0 | N/A | N/A | XMC Site 2 GA2 | XMC Site 2 GA1 | XMC Site 2 GA0 | XMC Site 1 GA2 | XMC Site 1 GA1 | XMC Site 1 GA0 |

The factory default value of all bits in this register is '0'.

The EEPROM is write-protected by default and can be write-enabled by clearing the I²C EEPROM Write Protect bit in Control Register 1. This bit may only be cleared when the NVRAM Write Enable Link (E18) is fitted and the backplane NVMRO signal (on connector P0 pin A4) is inactive low.

### 5.17.8 MPC8641D Configuration EEPROM

Initial configuration of the processor is performed by driving strapping signals to the correct state during reset.

An I²C EEPROM is provided, should further configuration information need to be loaded into the device before software boots. The processor's boot sequencer, which uses the EEPROM, is always enabled and the device must therefore be loaded with valid data (including preamble and CRC) at all times for the processor to boot correctly. If valid data is not read, then the device will request a hard reset.

The EEPROM is write-protected by default and can be write-enabled by clearing the I²C EEPROM Write Protect bit in Control Register 1. This bit may only be cleared when the NVRAM Write Enable Link (E18) is fitted and the backplane NVMRO signal (on connector P0 pin A4) is inactive low.

The processor can be prevented from accessing the EEPROM, in the event that the data becomes corrupted and configures the device such that the EEPROM contents cannot be overwritten, by fitting the Recovery Boot Link (E14). The EEPROM should then be reprogrammed with a valid image.

### 5.17.9 Board Management Microcontroller

The SBC610 contains a Board Management Microcontroller (BMM), which provides a proprietary mechanism to share of BIT results between boards in a system and remote monitoring of board status.

The BMM is connected to a backplane I²C Serial Management bus (using the SM_CLK and SM_DATA connections on the P0 connector) which is bused between all slots in the system. The BMM on each board is addressed based on its Geographic Address as shown in the table below. These are the 7-bit device addresses:

Table 5-32 BMM Address Allocation

| Slot | GA[4:0] | I2C Address | Slot | GA[4:0] | I2C Address | Slot | GA[4:0] | I2C Address |
|---|---|---|---|---|---|---|---|---|
| 1 | 11110 | 0x68 | 8 | 10111 | 0x6F | 15 | 10000 | 0x77 |
| 2 | 11101 | 0x69 | 9 | 10110 | 0x70 | 16 | 01111 | 0x78 |
| 3 | 11100 | 0x6A | 10 | 10101 | 0x72 | 17 | 01110 | 0x79 |
| 4 | 11011 | 0x6B | 11 | 10100 | 0x73 | 18 | 01101 | 0x7A |
| 5 | 11010 | 0x6C | 12 | 10011 | 0x74 | 19 | 01100 | 0x7B |
| 6 | 11001 | 0x6D | 13 | 10010 | 0x75 | 20 | 01011 | 0x7C |
| 7 | 11000 | 0x6E | 14 | 10001 | 0x76 | 21 | 01010 | 0x7D |

The system management pins of both XMC sites are also connected to the backplane Serial Management Bus. Their addresses are determined by the three Geographic Address pins generated by the I²C DIP Switch device as shown in the table below. These are the 7-bit device addresses:

Table 5-33 XMC Geographic Address

| XMC_GA[2:0] | I2C Address |
|---|---|
| 000 | 0x50 |
| 001 | 0x51 |
| 010 | 0x52 |
| 011 | 0x53 |
| 100 | 0x54 |
| 101 | 0x55 |
| 110 | 0x56 |
| 111 | N/A |

The local processor communicates with the BMM via the COM2 port from the MPC8641D. The BMM serial interface is enabled when the COM2 transceiver is disabled (using the COM2 Transceiver Enable Bit in Control Register 1).

The BMM is connected to on-board I²C Bus 1, providing access for out-of-band monitoring of board status information such as on-board voltage rail status or board temperatures by any other board in the system.

The BMM is programmed using bits in Control Register 1, though programming may only be performed when the NVRAM Write Enable Link (E18) is fitted.

The BMM is powered from the P3V3_AUX supply, meaning that board configuration information or BIT status can be read out of the device without enabling the main +5V power rail. An I²C buffer is sited on the on-board I²C Bus 1 to allow the BMM to access the Power Manager device and XMC Geographic Address I²C DIP Switch when the on-board supplies are not powered up.

## 5.18 FPGAs

### 5.18.1 Local Bus Control FPGA

This is a Lattice MachXO1200C that provides the following functions:

- Local bus address latching and chip select generation for Flash/NVRAM
- Data bus buffering to Flash/NVRAM
- AXIS Message Passing Interface

### 5.18.2 Register FPGA

This is a Lattice MachXO1200C device that provides the following functions:

- Control/Status Registers
- Reset Logic
- Interface to AFIX Parallel Bus
- Secondary interrupt controller

### 5.18.3 I/O FPGA

This is a Xilinx Virtex 4 LX25 device that provides the following functions:

- Two ESCC IP cores, used to generate COM3, COM4, COM5 and COM6 serial ports
- DMA engines for transfer of data between serial ports and internal block RAM used for data buffering (COM3/4 only)
- Enhanced Baud Rate Generation capabilities
- General Purpose I/O Controller

An external SRAM device is connected to the I/O FPGA for local buffering of data as required by the application. The device fitted is 16-bits wide and has a capacity of 2 MBytes.

The I/O FPGA is configured using a Xilinx parallel configuration PROM (XCF08P). The DONE and INIT configuration signals are made available in Control Register 2. This allows software to see when the FPGA is configured or to cause the device to reconfigure if required. The SBC610 also has the ability to fit a larger configuration PROM supporting revision control, with the active revision selected by the value in Control Register 2.

NOTE

There is the potential to tailor the functionality of this device to accommodate specific customer requirements. Contact your local sales representative for further details.

## 5.19 Timers

The 8641D provides eight 31-bit general-purpose timers. Each timer is capable of generating interrupts to either or both processing cores and can be programmed to generate periodic interrupts.

Each group of 4 timers can be set to operate from a divider of the MPX bus clock (divided by 8, 16, 32 or 64) or from an external 14.318 MHz clock. The minimum resolution of each timer is 15ns.

Each group of timers can be cascaded to form two 63-bit timers, one 95-bit timer or one 127-bit timer, if required.

### 5.19.1 Watchdog Timers

The SBC610 provides two independent, programmable 32-bit Watchdog timers. These are count-down timers and are capable of generating interrupts to the either or both of the two processing cores at a programmable threshold and resetting the board if expired.

The timers are disabled following reset but, once enabled, the Watchdog must be serviced periodically to prevent a reset.

Further details on the operation of the Watchdog can be found in the Watchdog register definitions.

## 5.20 AXIS Support

The SBC610 provides hardware features required to support GE's AXIS software suite.

Four 32-bit wide FIFOs, capable of holding 64 messages each, are provided to support message passing between the two on-board processing nodes or from other nodes in the system to the on-board processing nodes. An interrupt can be generated to the receiving processing node when a message is received and remains asserted until the message queue is empty.

The SBC610 supports a 48-bit timer, clocked by the external AXIS_TIMER_CLK signal and reset by the AXIS_TIMER_RST signal. This allows several boards to be connected to these signals and generates a common timestamp for data passed between them. The SBC610 can also act as a master on these signals, generating a clock (with programmable frequency) and asserting the reset under software control.

Eight hardware semaphores are also provided for use in locking common resources.

See the AXIS and FIFO register definitions for more details.

## 5.21 Resets, Interrupts and Error Reporting

The following table shows the various external interrupt sources to the processor and their relative priorities. It also shows whether the previous state of the processor is recoverable.

Table 5-34 Processor Interrupts

| Priority | Interrupt | Cause | Recoverability |
|---|---|---|---|
| 0 | System Reset | Power on, Hard Reset Input | Non-recoverable |
| 1 | Machine Check | MCP~ Input | Non-recoverable in most cases |
| 2 | System Reset | Soft Reset Input | Recoverable unless Machine Check occurs |
| 3 | System Management Interrupt | SMI~ input | Recoverable unless Machine Check or System Reset occurs |
| 4 | External Interrupt | INT~ input | Recoverable unless Machine Check or System Reset occurs |

### 5.21.1 Hard Reset

A hard reset is used to reset the MPC8641D (including the processing cores) and all other devices on the SBC610 that require resetting. When released from reset, Processing Core 0 will begin executing from the Boot Flash at address 0xFFF0 0100.

A hard reset is asserted when any of the following events occur:

- Any of the power supplies fall outside specification
- The VME SYSRESET~ signal is asserted
- The processor HRESET_REQ~ output is asserted
- Hard reset is selected via the front panel Reset switch (when enabled in software)
- The HRESET~ signal on the BDM Header is asserted
- The reset output of the BMM is asserted
- The EXT_RESET~ backplane pin is asserted
- The RESET_OUT~ signal from any PMC/XMC site is asserted
- Either of the two watchdog timers expire
- Reset generated by Tsi578 from Serial RapidIO source
- Reset generated by PEX8518 from PCI Express Non-Transparent backplane port

The duration of the internal hard reset signal is at least 10 ms.

A hard reset may also be initiated by software setting the LRESET, LRST or LRSTS bits within the Tsi148 VME Bridge and may be used by other boards with a VME interface to reset the SBC610.

The cause of a hard reset event may be determined from the Link Status Register.

The processing cores may be individually reset by software using the Processor Core Reset Register within the MPC8641D interrupt controller.

### 5.21.2 SYSRESET~ Signal

The SYSRESET~ signal is asserted by hardware under the following conditions:

- Any of the power supplies fall outside specification
- A hard reset event occurs and the board is the VPX System Controller

A SYSRESET~ may also be initiated by software setting the SRESET bit within the Tsi148 VME Bridge, even if the board is not System Controller.

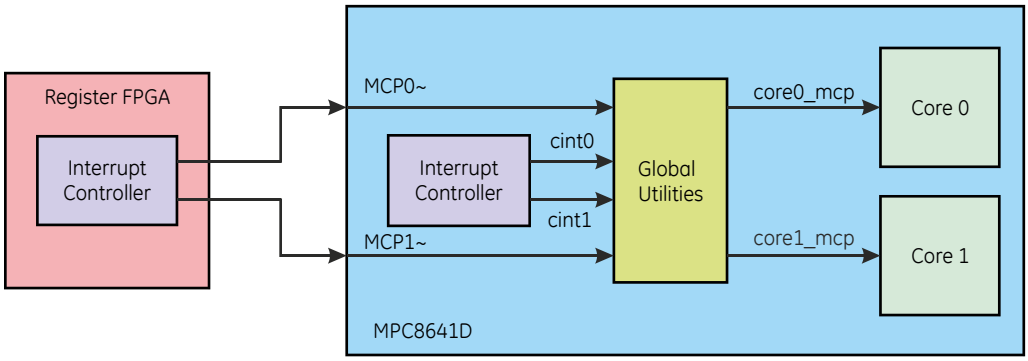
The duration of the SYSRESET~ backplane signal is at least 200ms and will be stretched to 200ms if a SYSRESET~ assertion of < 200ms is observed (in accordance with VITA46.1).

### 5.21.3 Machine Check Exception

When the MCP~ input to the processing core is asserted, it may be configured to take a machine check exception or enter the checkstop state.

The MCP~ input to each of the two processing cores can be driven either by interrupts within the interrupt controller within the Register FPGA being enabled by software to drive the MCP0~ or MCP1~ inputs to the MCP8641D or by software enabling interrupt sources from within the MPC8641D interrupt controller to drive the MCP~ input to one of the two processing cores.

Figure 5-9 SBC610 Machine Check Exceptions




### 5.21.4 Soft Reset

A soft reset causes the processing core to reach a recoverable state and then branch to either 0x0000 0100 or 0xFFF0 0100, depending on the state of the IP bit in the core's Machine State Register. No other on-board resources are reset.

A soft reset is initiated on both processing cores when one of the following hardware events occurs:

- Soft reset is selected via the front panel Reset switch (when enabled in software)
- The SRESET~ signal on the BDM header is asserted
- The EXT_ABORT~ backplane signal is asserted

The processing cores may be individually soft reset by software using the Processor Core Initialization Register within the MPC8641D interrupt controller.

### 5.21.5 System Management Interrupt (SMI~)

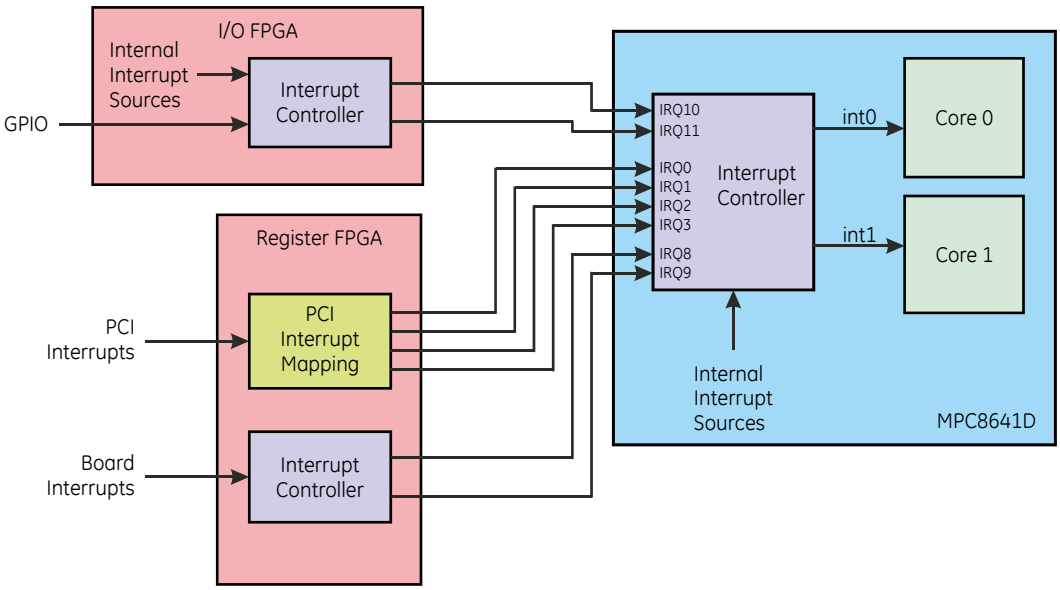
An SMI~ interrupt to the processing cores can only be generated by asserting the external SMI0~ or SMI1~ pins on the MPC8641D. These pins are unused on the SBC610.

### 5.21.6 External Interrupt (INT~)

The processing core external interrupt pin (INT~) is asserted for a pending interrupt from the interrupt controller in the MPC8641D.

The MCP8641D interrupt controller supports routing of internal and external interrupt sources to one of the two processing cores, including programmable priority levels. All interrupt routing between source and the processing cores is established by software.

Figure 5-10 SBC610 Interrupts




### 5.21.7 PCI Interrupts

PCIe provides a mechanism for passing interrupts from legacy PCI devices through the PCIe fabric to the interrupt controller at the Root Complex, using Assert_INTx and Deassert_INTx messages. These messages are, however, subject to the same latency and non-determinism as any other PCIe packet.

To reduce this latency, the SBC610 takes the interrupts from all PCI devices and mezzanines and routes them directly to the interrupt controller, via the Register FPGA, bypassing the fabric altogether.

The MPC8641D PCI Express Root Complex generates internal interrupt signals (equivalent to INTA to INTD) to the Interrupt Controller, which are shared with external interrupt signals (INTA with IRQ0, INTB with IRQ1, etc.) Mapping the individual device interrupts to the correct external signals allows this mechanism to appear transparent to software. This mapping must account for rotation due to the device number of both the switch port and the device on the PCI bus. The mapping used is shown in the table below:

Table 5-35 PCI Interrupt Rotation

| Interrupt Source | PEX8518 Port | Device Number | Device Interrupt to MPC8641D IRQ Pin Mapping | | | |
|---|---|---|---|---|---|---|
| | | | IRQ A | IRQ B | IRQ C | IRQ 3 |
| PMC1 | 13 | 8 | IRQ 1 | IRQ 2 | IRQ 3 | IRQ 0 |
| PMC2 | 2 | 8 | IRQ 2 | IRQ 3 | IRQ 0 | IRQ 1 |
| VME | 14 | 0 | IRQ 2 | IRQ 3 | IRQ 0 | IRQ 1 |
| USB | 1 | 1 | IRQ 2 | IRQ 3 | IRQ 0 | |
| SATA | 1 | 2 | IRQ 3 | | | |
| AFIX | 1 | 3 | IRQ 0 | IRQ 1 | IRQ 2 | IRQ 3 |

### 5.21.8 Board Interrupts

See the Board Interrupt Status Register and the Board Interrupt Core INT Mask Register for more details.

## 5.22 Power Sequencing

### 5.22.1 On-board Sequencing

The SBC610 uses a Lattice ispPAC Power Manager device to sequence the power supplies in the required order for on-board devices. The Power Manager also monitors the backplane supply voltages and shuts down the on-board supplies if these fall below their specified levels. The Power Manager is connected to I²C Bus 1, allowing software read-out of the voltages of all on and off-board supplies.

The Power Manager will shut down all on-board supplies (except P3V3_AUX) when the BMM asserts the BMM_OFF signal.

The 5V supply to the mezzanine cards is switched, under the control of the Power Manager, so that the 5V and 3.3V supplies are applied to the mezzanines at approximately the same time.

### 5.22.2 Inter-board sequencing

The SBC610 supports a proprietary inter-board power sequencing mechanism. This allows for the sequencing of power between several boards in a system to be controlled (limiting overall inrush current). This is achieved by the PSU_SEQ_OUT and PSU_SEQ_IN signals on the P1 connector, which can be daisy-chained between boards.

The SBC610 drives the PSU_SEQ_OUT signal low when the backplane supplies are out of specification and holds it low until all on-boards supplies are within specification. The PSU_SEQ_OUT signal is not driven low when the power is removed as a result of the BMM_OFF signal being asserted.

The SBC610 holds off all on-board supplies (except P3V3_AUX) when the PSU_SEQ_IN signal is held low. The power-on sequence is initiated if the PSU_SEQ_IN signal remains low 500ms after the off-board supplies are within specification, which may occur if the previous board in the chain fails.

### 5.22.3 Nuclear Event Detection

The SBC610 provides the capability to safely crowbar all on-board supplies, without damage to any on-board components, to less than 20% of their initial value within 300µs of the application of a positive pulse of 12V to the P6 Connector pin G1. This feature is used to prevent the SBC610 from damage during a nuclear event.

## 5.23 JTAG

The SBC610 provides JTAG boundary scan facilities for all IEEE1149.1 and IEEE1149.6-compliant devices.

The JTAG interface is provided by a Firecron JTS06Bu Scanbridge. This allows the boundary scan path to be partitioned into smaller chains, providing easier fault diagnosis and faster Flash programming. The device supports six Test Access Ports (TAPs), which are allocated as follows:

Table 5-36 JTAG Access Ports

| TAP | Devices |
|---|---|
| 1 | BDM Header<br>MPC8641D processor |
| 2 | PEX8548 PCIe Switch, VME PEX8114 PCIe-PCI Bridge<br>Tsi148 PCI-VME Bridge |
| 3 | PMC1 PEX8114 PCIe-PCI Bridge, PMC2 PEX8114 PCIe-PCI Bridge<br>AFIX PEX8114 PCIe-PCI Bridge, 88E1111 PHY 1, 88E1111 PHY 3 |
| 4 | XMC Site 1, PMC Site 1<br>XMC Site 2, PMC Site 2<br>AFIX Site |
| 5 | PEX8518 PCIe Switch, Tsi578 Serial RapidIO Switch |
| 6 | PLD Header, Local Bus Control FPGA<br>Register FPGA, I/O FPGA<br>I/O FPGA Configuration PROM |

The input to the Scanbridge is driven from the VPX P0 connector.

The JTAG architecture supports the use of the JTAG Technologies AutoWrite signal to accelerate flash programming via JTAG. This signal is connected to the VPX reserved P1 connector pin G7 and could be disconnected if required.

The address of the backplane JTAG Scanbridge is derived from the VPX geographic address. This is used when operating a bused JTAG system with multiple boards.

The SBC610 provides a standard BDM header for JTAG access to the 8641D processor. The BDM header uses its own isolated JTAG chain.

A separate FPGA programming header is provided for factory updates to the FPGA code.

CAUTION

When using the BDM or FPGA programming headers, ensure that the JTAG Scanbridge is disabled (link E23 is not fitted).

Mezzanine cards (such as PMCs or the AFIX) are automatically bypassed (using on-board buffers) when the mezzanine card is not fitted.

NOTES

The PCI specification requires that if a PMC cannot support JTAG, then it must have TDI connected to TDO ensuring that the JTAG chain remains intact.

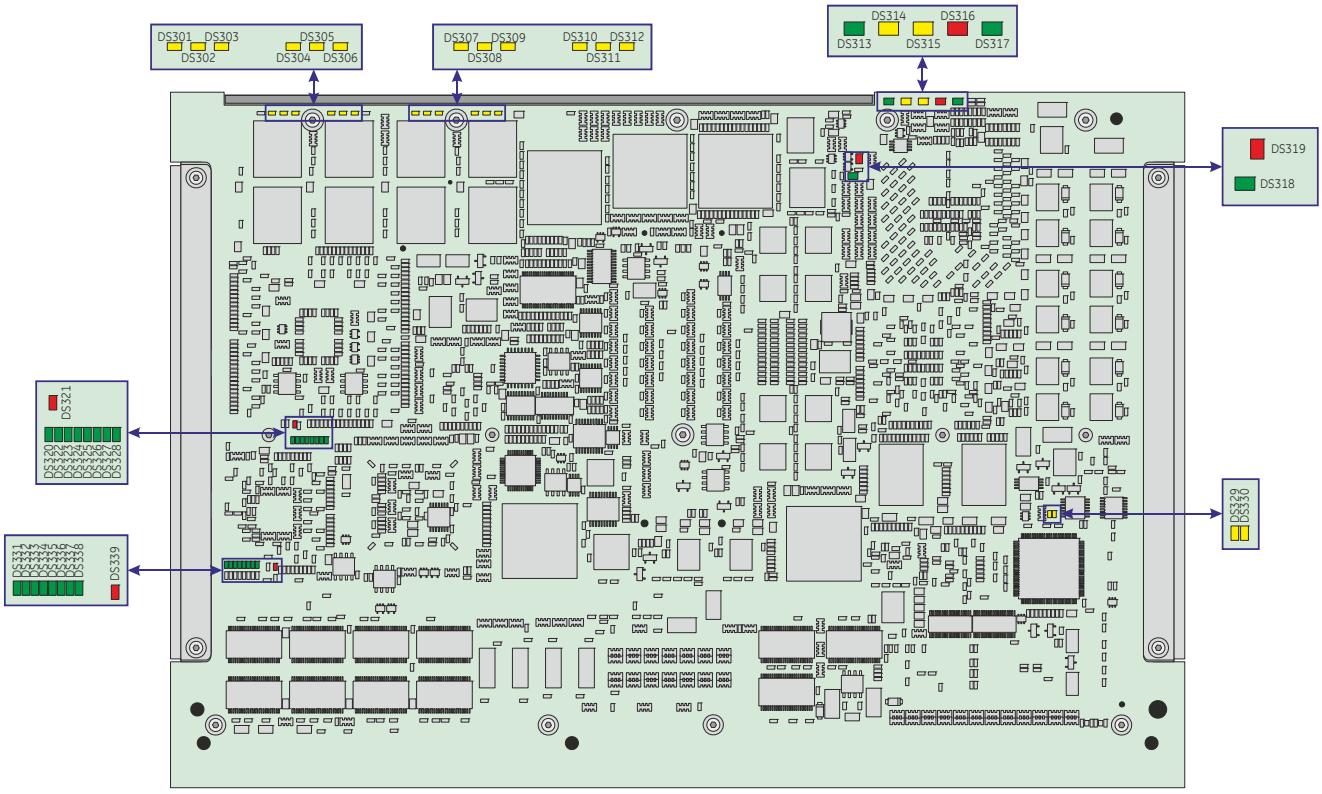
The XMC specification (VITA 42.0) requires that if an XMC cannot support JTAG, then it must have TDI connected to TDO on the XMC and PMC connectors (if fitted) ensuring that the JTAG chain remains intact. It also requires that if both connector sets are present, then the XMC connector is used for the JTAG interface and the PMC connector connects TDI to TDO.

## 5.24 LEDs

LEDs are mounted on the back of the SBC610 to reflect the status of the following functions:

- Power Supplies
- BIT
- PCI Express links (on and off-board)
- Ethernet links
- SATA activity
- Reset Status

Figure 5-11 LED Positions



### 5.24.1 Ethernet Link Status LEDs (DS301 to DS312)

Table 5-37 Ethernet Link Status LEDs

| LED | Color | Function | Meaning When Lit |
|---|---|---|---|
| DS301 | Yellow | Ethernet Port 3 Transmit | Ethernet traffic being transmitted |
| DS302 | Yellow | Ethernet Port 3 Receive | Ethernet traffic being received |
| DS303 | Yellow | Ethernet Port 3 Duplex | Ethernet port operating in Duplex mode |
| DS304 | Yellow | Ethernet Port 3 1000BaseT | Ethernet port operating in 1000BaseT mode |
| DS305 | Yellow | Ethernet Port 3 100BaseT | Ethernet port operating in 100BaseT mode |
| DS306 | Yellow | Ethernet Port 3 10BaseT | Ethernet port operating in 10BaseT mode |
| DS307 | Yellow | Ethernet Port 1 Transmit | Ethernet traffic being transmitted |
| DS308 | Yellow | Ethernet Port 1 Receive | Ethernet traffic being received |
| DS309 | Yellow | Ethernet Port 1 Duplex | Ethernet port operating in Duplex mode |
| DS310 | Yellow | Ethernet Port 1 1000BaseT | Ethernet port operating in 1000BaseT mode |
| DS311 | Yellow | Ethernet Port 1 100BaseT | Ethernet port operating in 100BaseT mode |
| DS312 | Yellow | Ethernet Port 1 10BaseT | Ethernet port operating in 10BaseT mode |

These LEDs are under the control of the 88E1111 PHYs and the descriptions define the default functions of the LED outputs. These are under software control, however, and may be subsequently reassigned.

### 5.24.2 BIT LEDs (DS313 to DS316)

Table 5-38 BIT LEDs

| LED | Color | Function | Description |
|---|---|---|---|
| DS316 | Red | BIT Fail | Software-controlled LEDs used to show the status of BIT or other boot software |
| DS315 | Yellow | BIT LED 1 | |
| DS314 | Yellow | BIT LED 2 | |
| DS313 | Green | BIT Pass | |

DS313 to DS316 are used by the software running on the SBC610 (e.g. BIT) to indicate its status. The BIT Fail LED (DS316) is illuminated following reset and must be turned off by software. The BIT Pass LED (DS313) is used to indicate that the software has completed any power-up tests and is running correctly.

Table 5-39 BIT Status LED Meanings

| BIT Fail LED (DS316) | BIT Passed LED (DS313) | Status |
|---|---|---|
| On | Off | BIT not yet run (Reset state) or BIT failed |
| Off | On | BIT complete and passed |

The yellow BIT LEDs (DS314 and DS315) are used to indicate progress through BIT and so may provide information for debugging purposes in the event of failure.

These LEDs are software-programmable via Control Register 1, and may be reassigned for another purpose after BIT has completed.

The status of the software can also be monitored using the BITFAIL~ signal on the P6 connector pin F16.

### 5.24.3 Power Good LED (DS317)

When on, this green LED indicates on-board and off-board power supplies are within their specified limits.

### 5.24.4 Reset Status LEDs

Table 5-40 Reset Status LEDs

| LED | Color | Function | Meaning When Lit |
|---|---|---|---|
| DS318 | Green | CPU Ready | MPC8641D processor has completed initialization and is not in a sleep mode |
| DS319 | Red | Reset | SBC610 is in hard reset |

NOTE

DS318 is illuminated when the MPC8641D internal initialization is complete but may be extinguished when either of the processing cores is in a low power mode (such as nap mode). These modes are under software control so the LED may toggle during operation if these modes are in use.

### 5.24.5 PCI Express Link Status LEDs (DS320 to DS328)

Table 5-41 PCI Express Link Status LEDs

| LED | Color | Function | Meaning When Lit |
|---|---|---|---|
| DS320 | Green | PEX8548 Port 0 Good | The PCIe link to the MPC8641D is active |
| DS321 | Red | PEX8548 Fatal Error | A fatal error has occurred has been detected by the PEX8548 switch |
| DS322 | Green | PEX8548 Port 1 Good | The PCIe link to the AFIX PCIe-PCI Bridge is active |
| DS323 | Green | PEX8548 Port 2 Good | The PCIe link to the PMC2 PCIe-PCI Bridge is active |
| DS324 | Green | PEX8548 Port 8 Good | The PCIe link to the PEX8518 PCIe Switch is active |
| DS325 | Green | PEX8548 Port 9 Good | The PCIe link to XMC1 is active |
| DS326 | Green | PEX8548 Port 12 Good | The PCIe link to XMC2 is active |
| DS327 | Green | PEX8548 Port 13 Good | The PCIe link to the PMC1 PCIe-PCI Bridge is active |
| DS328 | Green | PEX8548 Port 14 Good | The PCIe link to the VME PCIe-PCI Bridge is active |

The Port Good LEDs will light if *any* link has been made between the two devices, even if it is of reduced width (a x1 link on a x8 connection for example). The exact state of each link can only be determined by software interrogation of the device registers.

### 5.24.6 SATA Activity LEDs (DS329 and DS330)

Table 5-42 SATA Activity LEDs

| LED | Color | Function | Meaning When Lit |
|---|---|---|---|
| DS329 | Yellow | SATA Ch0 Activity | SATA activity on Channel 0 |
| DS330 | Yellow | SATA Ch1 Activity | SATA activity on Channel 1 |

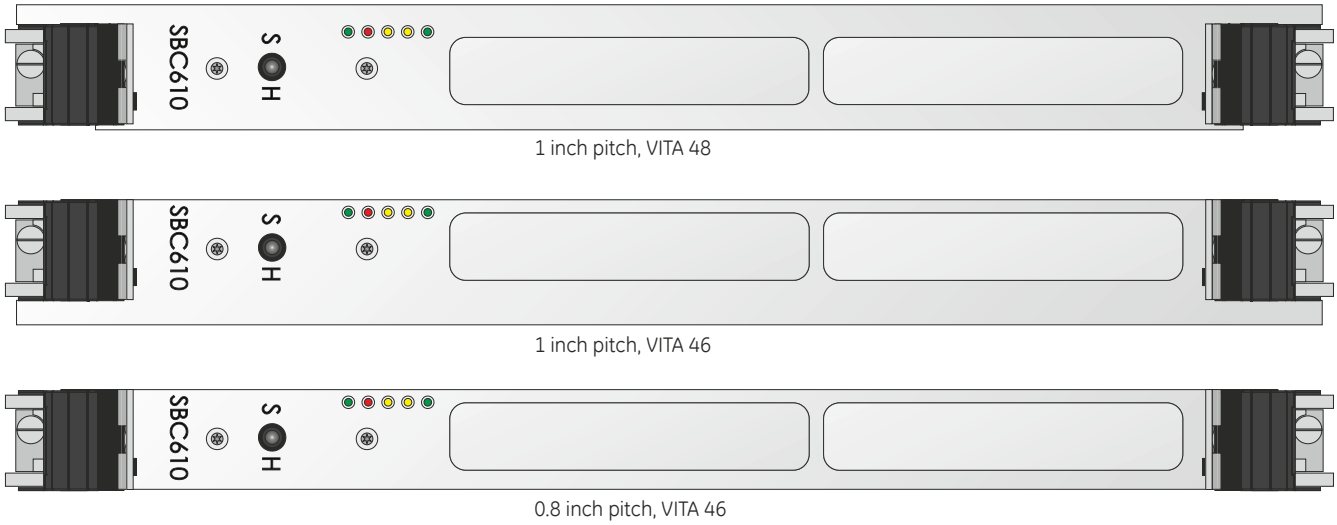
### 5.24.7 Backplane PCI Express Lane Status LEDs (DS331 to DS339)

Table 5-43 Backplane PCI Express Lane Status LEDs

| LED | Color | Function | Meaning When Lit |
|---|---|---|---|
| DS331 | Green | PEX8518 Lane 8 Good | This PCI Express lane connected to backplane port 3, lane 1 is active |
| DS332 | Green | PEX8518 Lane 9 Good | This PCI Express lane connected to backplane port 3, lane 2 is active |
| DS333 | Green | PEX8518 Lane 10 Good | This PCI Express lane connected to backplane port 3, lane 3 is active |
| DS334 | Green | PEX8518 Lane 11 Good | This PCI Express lane connected to backplane port 3, lane 4 is active |
| DS335 | Green | PEX8518 Lane 12 Good | This PCI Express lane connected to backplane port 4, lane 1 is active |
| DS336 | Green | PEX8518 Lane 13 Good | This PCI Express lane connected to backplane port 4, lane 2 is active |
| DS337 | Green | PEX8518 Lane 14 Good | This PCI Express lane connected to backplane port 4, lane 3 is active |
| DS338 | Green | PEX8518 Lane 15 Good | This PCI Express lane connected to backplane port 4, lane 4 is active |
| DS339 | Red | PEX8518 Fatal Error | A fatal error has occurred has been detected by the PEX8518 switch |

## 5.25 Air-cooled Front Panels (Build Levels 1 to 3)

Figure 5-12 Air-cooled Front Panels




### 5.25.1 PMC Slots

The SBC610 front panel has provision for front I/O from both PMC/XMC sites. If PMCs have not been ordered as part of an assembly with the SBC610, then GE will fit a blanking plate in the slot(s) for EMC protection.

If you are fitting a non-GEIP PMC, it must comply with the standard for air-cooled mezzanines to ensure that it mates correctly with the SBC610 mechanics. GEIP PMCs comply with this standard.

If you are fitting a PMC yourself, before fitting the module, remove the corresponding blanking plate from the desired PMC slot. The PMC's bezel should fill the slot and may provide front panel connection to the module. GEIP PMCs are delivered with a full kit of parts for mounting, plus fitting instructions.

### 5.25.2 LEDs

Five LEDs are visible through the front panel. One indicates that all off- and on-board power supplies are within specification and the other four are software-programmable and are used to reflect the status of BIT or other software. See the LEDs section for more details.

### 5.25.3 Switches

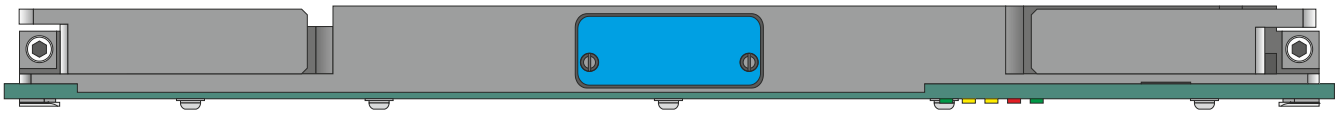
A momentary action toggle switch is fitted through the front panel. The switch allows generation of a hard or soft reset.

With the board inserted vertically into a rack, moving the switch to the "S" position causes a soft reset to the processing cores, and moving the switch to the "H" position causes a hard reset to the board.

The switch may be disabled under software control, via Control Register 1. The switch is enabled following power-up.

## 5.26 Conduction-cooled Front Panel (Build Levels 4 and 5)

Figure 5-13 Conduction-cooled Front Panel



### 5.26.1 PMC Slots

There is no access to front I/O from PMCs in a conduction-cooled environment.

If you are fitting a non-GEIP PMC, it must comply with the standard for rugged, conduction-cooled PMCs (VITA20-2001) to ensure that it mates correctly with the SBC610 mechanics. GEIP PMCs comply with this standard.

### 5.26.2 LEDs

Five LEDs are visible from the front. One indicates that all off- and on-board power supplies are within specification and the other four are software-programmable and are used to reflect the status of BIT or other software. See the LEDs section for more details.

### 5.26.3 Switches

There are no switches on the conduction-cooled front panel, although external reset inputs are available on the backplane connectors.

# 6 • Control and Status Registers

The SBC610 provides numerous registers for software to control or read the status of the board. All registers are accessed using Local Bus Chip Select 4, are configured as 32-bit wide and must be written as a 32-bit word.

The following table gives the locations of the registers, offset from the Chip Select 4 base address (which is configured by software), and access to the register:

Table 6-1 Control and Status Registers

| Register | Offset | R/W | Register | Offset | R/W | Register | Offset | R/W |
|---|---|---|---|---|---|---|---|---|
| Board ID | 0x0000 | RO | Board Semaphore 9 | 0x0060 | R/W | PCIe Scratch 2 | 0x5024 | R/W |
| Address | 0x0004 | RO | Board Semaphore 10 | 0x0064 | R/W | PCIe Doorbell Assert | 0x5030 | WO |
| Board Frequency | 0x0008 | RO | Board Semaphore 11 | 0x0068 | R/W | PCIe Doorbell Clear | 0x5034 | WO |
| Board Configuration | 0x000C | RO | Board Semaphore 12 | 0x006C | R/W | PCIe Doorbell Status | 0x5038 | RO |
| Link Status | 0x0010 | RO | Board Semaphore 13 | 0x0070 | R/W | AXIS Timestamp Low Value | 0x6000 | RO |
| Control 1 | 0x0014 | R/W | Board Semaphore 14 | 0x0074 | R/W | AXIS Timestamp High Value | 0x6004 | RO |
| Control 2 | 0x0018 | R/W | Board Semaphore 15 | 0x0078 | R/W | AXIS Timer Control | 0x6008 | R/W |
| Flash Control | 0x001C | R/W | Board Semaphore 16 | 0x007C | R/W | AXIS Semaphore 1 | 0x6020 | R/W |
| Test Pattern 1 | 0x0020 | RO | Watchdog 0 Control | 0x2000 | R/W | AXIS Semaphore 2 | 0x6024 | R/W |
| Test Pattern 2 | 0x0024 | RO | Watchdog 0 Interrupt Value | 0x2004 | R/W | AXIS Semaphore 3 | 0x6028 | R/W |
| Test Pattern 3 | 0x0028 | RO | Watchdog 1 Control | 0x2010 | R/W | AXIS Semaphore 4 | 0x602C | R/W |
| Scratch 1 | 0x0030 | R/W | Watchdog 1 Interrupt Value | 0x2014 | R/W | AXIS Semaphore 5 | 0x6030 | R/W |
| Scratch 2 | 0x0034 | R/W | Board Interrupt Status | 0x4000 | RO | AXIS Semaphore 6 | 0x6034 | R/W |
| Scratch 3 | 0x0038 | R/W | Board Interrupt Core 0 INT Mask | 0x4010 | R/W | AXIS Semaphore 7 | 0x6038 | R/W |
| Scratch 4 | 0x003C | R/W | Board Interrupt Core 1 INT Mask | 0x4014 | R/W | AXIS Semaphore 8 | 0x603C | R/W |
| Board Semaphore 1 | 0x0040 | R/W | Board Interrupt Core 0 MCP Mask | 0x4018 | R/W | FIFO Data A | 0x6040 | R/W |
| Board Semaphore 2 | 0x0044 | R/W | Board Interrupt Core 1 MCP Mask | 0x401C | R/W | FIFO Data B | 0x6044 | R/W |
| Board Semaphore 3 | 0x0048 | R/W | PCIe Block Configuration | 0x5000 | RO | FIFO Data C | 0x6048 | R/W |
| Board Semaphore 4 | 0x004C | R/W | PCIe Semaphore 1 | 0x5010 | R/W | FIFO Data D | 0x604C | R/W |
| Board Semaphore 5 | 0x0050 | R/W | PCIe Semaphore 2 | 0x5014 | R/W | FIFO Status A | 0x6050 | R/W |
| Board Semaphore 6 | 0x0054 | R/W | PCIe Semaphore 3 | 0x5018 | R/W | FIFO Status B | 0x6054 | R/W |
| Board Semaphore 7 | 0x0058 | R/W | PCIe Semaphore 4 | 0x501C | R/W | FIFO Status C | 0x6058 | R/W |
| Board Semaphore 8 | 0x005C | R/W | PCIe Scratch 1 | 0x5020 | R/W | FIFO Status D | 0x605C | R/W |

Where: R/W = Read/Write RO = Read Only WO = Write Only

The following sections provide the definitions for the function of each bit within a register. All registers are configured such that bit 0 is the most-significant bit and bit 31 is the least-significant bit.

## 6.1 Board ID Register (Offset 0x0000)

Table 6-2 Board ID Register

| Bits | Description | Notes |
|---|---|---|
| 0 to 7 | Board ID | SBC610 = 0x2D |
| 8 to 15 | PCB revision | 1, 2, 3 etc. |
| 16 to 23 | Software board revision | A, B, C etc. |
| 24 to 27 | Reserved | 0x0 |
| 28 to 31 | Register FPGA revision | 1, 2, 3 etc. |

## 6.2 Address Register (Offset 0x0004)

Table 6-3 Address Register

| Bits | Description | Notes |
|---|---|---|
| 0 to 21 | Reserved | 0x000000 |
| 22 | VME System Controller | 0 = SBC610 is not VME System Controller<br>1 = SBC610 is VME System Controller |
| 23 | VPX System Controller | 0 = SBC610 is not VPX System Controller<br>1 = SBC610 is VPX System Controller |
| 24 and 25 | Reserved | $00_b$ |
| 26 | Geographic Address parity[a] | 0 = Odd number of bits set<br>1 = Even number of bits set |
| 27 to 31 | Geographic Address | Contains the VME Geographic Address.<br>All bits are inverted to present the actual address |

a. Inverted from backplane signal.

## 6.3 Board Frequency Register (Offset 0x0008)

Table 6-4 Board Frequency Register

| Bits | Description | Notes |
|---|---|---|
| 0 to 29 | Reserved | 0x00000000 |
| 30 and 31 | SYSCLK frequency | 00 = 66.666 MHz<br>01 = 100 MHz<br>10 = Reserved<br>11 = Reserved |

## 6.4 Board Configuration Register (Offset 0x000C)

Table 6-5 Board Configuration Register

| Bits | Description | Notes |
|---|---|---|
| 0 | Reserved | $0_b$ |
| 1 to 3 | PMC/XMC 2 I/O configuration | 000 = PMC2 1-64 + XMC2 12d (P56-P64sX12d)<br>001 = PMC2 1-9, 11 + XMC2 Full (P56-X20d38s)<br>010 = Reserved<br>011 = Reserved<br>100 = PMC2 1-16 + COM 3/4/5/6 + XMC2 12d<br>101 = PMC2 1-48 + COM 5/6 + XMC2 12d<br>110 = Reserved<br>111 = Reserved |
| 4 | Reserved | $0_b$ |
| 5 and 6 | PMC/XMC 1 I/O configuration | 00 = PMC1 1-64 + XMC1 12d (P34-P64sX12d)<br>01 = Reserved<br>10 = Reserved<br>11 = PMC1 1-9, 11 + XMC1 Full (P34-X20d38s) |
| 7 | Dual Gigabit Ethernet fitted | 0 = Reserved<br>1 = Dual Gigabit Ethernet |
| 8 | Alternate GPIO configuration | 0 = Normal GPIO - GPIO(18:0) routed to I/O FPGA<br>1 = Alternate GPIO – GPIO(7:0) routed to Bus Control FPGA |
| 9 | AFIX link 1 (E27) | 0 = AFIX link 1 not fitted<br>1 = AFIX link 1 fitted |
| 10 | AFIX link 0 (E26) | 0 = AFIX link 0 not fitted<br>1 = AFIX link 0 fitted |
| 11 | AFIX | 0 = No AFIX fitted<br>1 = AFIX fitted |
| 12 | XMC fitted in site 2 | 0 = No XMC fitted<br>1 = XMC fitted |
| 13 | XMC fitted in site 1 | 0 = No XMC fitted<br>1 = XMC fitted |
| 14 | PMC fitted in site 2 | 0 = No PMC fitted<br>1 = PMC fitted |
| 15 | PMC fitted in site 1 | 0 = No PMC fitted<br>1 = PMC fitted |
| 16 | Flash type | 0 = Intel Flash fitted<br>1 = Spansion Flash fitted |
| 17 and 18 | Reserved | $00_b$ |
| 19 | Flash width | 0 = 32-bit Flash<br>1 = 16-bit Flash |
| 20 and 21 | Flash banks | 00 = 1 bank Flash<br>01 = 2 banks Flash<br>10 = 4 banks Flash<br>11 = 8 banks Flash |
| 22 and 23 | Flash device size | 00 = Reserved<br>01 = 512 Mbit Flash devices<br>10 = 1 Gbit Flash devices<br>11 = 2 Gbit Flash devices |
| 24 to 31 | Reserved | 0x00 |

## 6.5 Link Status Register (Offset 0x0010)

For bits 0 to 11, a set bit shows that the last reset was caused by the corresponding device/source. For bits 21 to 27 and 29 to 31, a set bit shows that a jumper is fitted on the corresponding link. The NVMRO signal is on the P0 connector pin A4.

Table 6-6 Link Status Register

| Bits | Description | Notes |
|---|---|---|
| 0 | Backplane SYSRESET~ reset | |
| 1 | 8641D Hard Reset Request reset | |
| 2 | Watchdog 1 reset | |
| 3 | Watchdog 0 reset | |
| 4 | Backplane EXT_RESET~ reset | |
| 5 | Front panel switch reset | |
| 6 | BMM reset | |
| 7 | BDM header reset | |
| 8 | PMC2/XMC2 reset | |
| 9 | PMC1/XMC1 reset | |
| 10 | Serial RapidIO (Tsi578 Switch) reset | |
| 11 | PCI Express (PEX8518) Non-Transparent Port reset | |
| 12 | Reserved | $0_b$ |
| 13 | XMC2 Built-In Self-Test (BIST) | 0 = XMC2 BIST complete<br>1 = XMC2 BIST in progress |
| 14 | XMC1 BIST | 0 = XMC2 BIST complete<br>1 = XMC2 BIST in progress |
| 15 | EREADY | 0 = PMCs/AFIX ready for enumeration<br>1 = PMCs/AFIX not ready for enumeration |
| 16 | Boot Swap 1 | 0 = BOOT_SWAP1~ signal not asserted<br>1 = BOOT_SWAP1~ signal asserted |
| 17 | Boot Swap 0 | 0 = BOOT_SWAP0~ signal not asserted<br>1 = BOOT_SWAP0~ signal asserted |
| 18 | BIT Mode 1 | 0 = BIT_MODE1 signal high<br>1 = BIT_MODE1 signal low |
| 19 | BIT Mode 0 | 0 = BIT_MODE0 signal high<br>1 = BIT_MODE0 signal low |
| 20 | Non-Volatile Memory Read Only | 0 = NVMRO signal high – protected<br>1 = NVMRO signal low – writeable |
| 21 | Spare link (E28) | |
| 22 | SMP Mode link (E19) | |
| 23 | NVRAM Write Enable link (E18) | |
| 24 | Factory link (E20) | |
| 25 | Flash Protection Unlock link (E17) | Set to '0' if the NVMRO signal is active high |
| 26 | User Flash Write Enable link (E16) | Set to '0' if the NVMRO signal is active high |
| 27 | Boot Flash Write Enable link (E15) | Set to '0' if the NVMRO signal is active high |
| 28 | Reserved | $0_b$ |
| 29 | Recovery Boot link (E14) | |
| 30 | Core 1 Boot Area Selection link (E14) | |
| 31 | Core 0 Boot Area Selection link (E12) | |

## 6.6 Control Register 1 (Offset 0x0014)

Table 6-7 Control Register 1

| Bits | Description | Notes |
|---|---|---|
| 0 | BMM programming enable[a] | 0 = BMM_PROGRAM_EN signal inactive (default)<br>1 = BMM_PROGRAM_EN signal active |
| 1 | BMM programming voltage | 0 = Voltage inactive (default)<br>1 = Voltage active |
| 2 | BMM programming data line direction | 0 = Data line is input (default)<br>1 = Data line is output |
| 3 | BMM programming data line input value | 0 = Data line input low<br>1 = Data line input high |
| 4 | BMM programming data line output value | 0 = Data line output low (default)<br>1 = Data line output high |
| 5 | BMM programming clock line value | 0 = Clock line low (default)<br>1 = Clock line high |
| 6 | Reserved | 0[b] |
| 7 | BIT flag[b] | 0 = BIT not run (default)<br>1 = BIT run |
| 8 | Front panel Reset switch enable | 0 = Switch disabled<br>1 = Switch enabled (default) |
| 9 | NVMRO override[c] | 0 = NVMRO backplane signal not driven<br>1 = NVMRO backplane signal driven low (inactive) |
| 10 | Serial EEPROM write protect[a] | 0 = Serial EEPROMs write-enabled<br>1 = Serial EEPROMs write-protected (default) |
| 11 | I2C EEPROM write protect[a] | 0 = I2C EEPROM write-enabled<br>1 = I2C EEPROM write-protected (default) |
| 12 | BIT Pass LED status | 0 = LED off (default)<br>1 = LED lit |
| 13 | BIT LED 2 status | 0 = LED off (default)<br>1 = LED lit |
| 14 | BIT LED 1 status | 0 = LED off (default)<br>1 = LED lit |
| 15 | BIT Fail LED status | 0 = LED off<br>1 = LED lit (default) |
| 16 to 24 | Reserved | 0x00 |
| 25 | COM2 loopback enable | 0 = COM2 loopback disabled (default)<br>1 = COM2 loopback enabled |
| 26 | COM2 RS232 mode | 0 = COM2 RS422 mode<br>1 = COM2 RS232 mode (default) |
| 27 | COM2 transceiver enable[d] | 0 = COM2 transceiver disabled (default)<br>1 = COM2 transceiver enabled |
| 28 | Reserved | 0[b] |
| 29 | COM1 loopback enable | 0 = COM1 loopback disabled (default)<br>1 = COM1 loopback enabled |
| 30 | COM1 RS232 mode | 0 = COM1 RS422 mode<br>1 = COM1 RS232 mode (default) |
| 31 | COM1 transceiver enable | 0 = COM1 transceiver disabled (default)<br>1 = COM1 transceiver enabled |

a. This bit is only writeable if the NVRAM Write Enable Link (E18) is fitted and the backplane NVMRO signal (on connector P0 pin A4) is inactive low.
b. This bit is sticky and is only reset at power-up. It can be used by BIT to indicate its status at last reset.
c. This bit is only writeable when the SBC610 is VPX System Controller.
d. When the COM2 transceiver is disabled, COM2 is used to communicate with the BMM

## 6.7 Control Register 2 (Offset 0x0018)

Table 6-8 Control Register 2

| Bits | Description | Notes |
|---|---|---|
| 0 and 1 | I/O FPGA revision select | Default = 0x0 |
| 2 | Initiate I/O FPGA configuration initialization | 0 = I/O FPGA released to configure (default)<br>1 = Restart I/O FPGA configuration |
| 3 | I/O FPGA configuration done (read only) | 0 = I/O FPGA configuration in progress<br>1 = I/O FPGA configuration complete |
| 4 to 8 | Reserved | 0x00 |
| 9 | Tsi578 $I^2C$ EEPROM disable[a] | 0 = Tsi578 allowed to configure from $I^2C$ EEPROM<br>1 = Tsi578 prevented from configuring from $I^2C$ EEPROM |
| 10 | PEX8518 Serial EEPROM disable[a] | 0 = PEX8518 allowed to configure from Serial EEPROM<br>1 = PEX8518 prevented from configuring from Serial EEPROM |
| 11 | PEX8548 Serial EEPROM disable[a] | 0 = PEX8518 allowed to configure from Serial EEPROM<br>1 = PEX8518 prevented from configuring from Serial EEPROM |
| 12 | AFIX Bridge Serial EEPROM disable[a] | 0 = AFIX Bridge allowed to configure from Serial EEPROM<br>1 = AFIX Bridge prevented from configuring from Serial EEPROM |
| 13 | VME Bridge Serial EEPROM disable[a] | 0 = VME Bridge allowed to configure from Serial EEPROM<br>1 = VME Bridge prevented from configuring from Serial EEPROM |
| 14 | PMC2 Bridge Serial EEPROM disable[a] | 0 = PMC2 Bridge allowed to configure from Serial EEPROM<br>1 = PMC2 Bridge prevented from configuring from Serial EEPROM |
| 15 | PMC1 Bridge Serial EEPROM disable[a] | 0 = PMC1 Bridge allowed to configure from Serial EEPROM<br>1 = PMC1 Bridge prevented from configuring from Serial EEPROM |
| 16 to 29 | Reserved | 0x0000 |
| 30 | Backplane fabric port 4 type | 0 = Serial RapidIO<br>1 = PCI Express<br>The default value of this register is defined by the state of link E25 at reset |
| 31 | Backplane fabric port 3 type | 0 = Serial RapidIO<br>1 = PCI Express<br>The default value of this register is defined by the state of link E24 at reset |

a. These bits are always set to '1' and are not writeable if the Recovery Boot Link (E14) is fitted (BOOT_RECOVERY~ signal is active) to prevent EEPROM contents being used. If the link is not fitted, these registers are 'sticky'. They are only cleared at power-up and not following reset. If a device needs to be reconfigured without its EEPROM, these bits can be set by software and a board reset applied.

## 6.8 Flash Control Register (Offset 0x001C)

Table 6-9 Flash Control Register

| Bits | Mode | Description | Notes |
|---|---|---|---|
| 0 to 15 | RO | Reserved | 0x0000 |
| 16 | RO | Flash bank 3 busy | 0 = Flash bank ready<br>1 = Flash bank busy |
| 17 | RO | Flash bank 2 busy | 0 = Flash bank ready<br>1 = Flash bank busy |
| 18 | RO | Flash bank 1 busy | 0 = Flash bank ready<br>1 = Flash bank busy |
| 19 | RO | Flash bank 0 busy | 0 = Flash bank ready<br>1 = Flash bank busy |
| 20 | R/W | MAC Address Mirror mode enable | 0 = CS2 top sector accesses Flash bank 1<br>1 = CS2 top sector accesses Flash bank 0 (BANC area) (default) |
| 21 | R/W | AND mode enable | 0 = 16-bit User Flash read in non-ANDed mode<br>1 = 16-bit User Flash read in ANDed mode (default) |
| 22 | R/W | Core 1 Boot Select | 0 = Core 0 boot areas reside in Primary boot area (0xFF80 0000) (default)<br>1 = Core 1 boot areas reside in Primary boot area (0xFF80 0000) |
| 23 | R/W | Paged Mode enable | 0 = Flash address derived from local bus<br>1 = Flash address bits 1:4 derived from registers (default) |
| 24 | RO | Reserved | 0 |
| 25 to 27 | R/W | Flash CS2 address bits 2:4 | When the Paged Mode Enable bit is set, these bits provide the MSBs of the Flash address to select a 128 MByte page (default = 0x7) |
| 28 to 31 | R/W | Flash CS1 address bits 1:4 | When the Page Mode Enable bit is set, these bits provide the MSBs of the Flash address to select a 128 MByte page.<br>If bit 28 is set high, the page selected resides in the CS1 area.<br>If bit 28 is set low, the page selected resides in the CS2 area (default = 0xF) |

## 6.9 Test Pattern Registers 1 to 3 (Offsets 0x0020 to 0x0028)

Registers 1 and 2 normally contain alternating set bit test patterns to verify bit ordering and check for stuck bits. When the Flash Protection Unlock Link (E17) is fitted and the backplane NVMRO signal (on connector P0 pin A4) is inactive low, the values of these registers change to allow software to alter the Flash sector protection.

Register 3 contains a test pattern to check for byte ordering from the FPGA.

Table 6-10 Test Pattern Registers

| Register | Offset | Test Pattern |
|---|---|---|
| 1 | 0x0020 | 0xAAAAAAAA |
| 2 | 0x0024 | 0x55555555 |
| 3 | 0x0028 | "SBC6" (0x53424336) |

## 6.10 Scratchpad Registers (Offsets 0x0030 to 0x003C)

These four registers have no effect on the system and are provided for software to store status information or data. Their value on reset is 0x0000 0000

## 6.11 Board Semaphore Registers (Offsets 0x0040 to 0x007C)

Each register controls one of sixteen semaphores.

Table 6-11 Board Semaphore Register Offsets

| Offset | Semaphore | Offset | Semaphore |
|---|---|---|---|
| 0x0040 | 1 | 0x0060 | 9 |
| 0x0044 | 2 | 0x0064 | 10 |
| 0x0048 | 3 | 0x0068 | 11 |
| 0x004C | 4 | 0x006C | 12 |
| 0x0050 | 5 | 0x0070 | 13 |
| 0x0054 | 6 | 0x0074 | 14 |
| 0x0058 | 7 | 0x0078 | 15 |
| 0x005C | 8 | 0x007C | 16 |

A semaphore is taken by reading the corresponding register:

- If the value returned is zero, then semaphore is currently in use
- If the value returned is non-zero, then the semaphore take is successful

The semaphore is released by writing to the corresponding register (the value written is not significant).

The reset value for all semaphore registers is 0x0000 0001.

## 6.12 Watchdog 0 Control Register (Offsets 0x2000) and Watchdog 1 Control Register (Offsets 0x2010)

These registers control the operation of Watchdogs Timers 0 and 1 respectively.

Table 6-12 Watchdog Control Registers

| Bits | Description | Notes |
|---|---|---|
| 0 | Watchdog status[a] | 0 = Watchdog enabled<br>1 = Watchdog disabled |
| 1 | Watchdog expired[a] | 0 = Watchdog not expired<br>1 = Watchdog counter expired (reset) |
| 2 | Watchdog interrupt[a] | 0 = Watchdog interrupt inactive<br>1 = Watchdog interrupt active |
| 3 | Reserved[a] | $0_b$ |
| 4 and 5 | Service Watchdog | Write '01' followed by '10' to these bits to service the Watchdog |
| 6 and 7 | Enable Watchdog | Write '01' followed by '10' to these bits to enable/disable (toggle) the Watchdog |
| 8 to 31 | Counter preset value | Bits 8 to 31 of the value loaded by the Watchdog counter whenever it is enabled or serviced.<br>Bits 0 to 7 are always 0xFF |

a. Read only.

## 6.13 Watchdog 0 Interrupt Value Register (Offsets 0x2004) and Watchdog 0 Interrupt Value Register (Offsets 0x2014)

These registers set the count value when an interrupt is generated for Watchdog 0 and Watchdog 1 respectively.

Table 6-13 Watchdog Interrupt Value Registers

| Bits | Description | Notes |
|---|---|---|
| 0 to 7 | Reserved | 0x00 |
| 8 to 31 | Interrupt Threshold | Bits 0 to 23 of the count threshold at which an interrupt is generated to the interrupt controller.<br>Bits 24 to 31 are always 0x00 |

## 6.14 Board Interrupt Status Register (Offset 0x4000)

This reflects the status of all on-board non-PCI interrupt inputs to the Register FPGA. A set bit indicates an active interrupt from the corresponding device.

Table 6-14 Board Interrupt Status Register

| Bits | Description |
|---|---|
| 0 to 14 | Reserved |
| 15 | PCI Express Doorbell 3 status |
| 16 | PCI Express Doorbell 2 status |
| 17 | PCI Express Doorbell 1 status |
| 18 | PCI Express Doorbell 0 status |
| 19 | RTC interrupt status |
| 20 | Temperature interrupt status |
| 21 | Temperature Critical interrupt status |
| 22 | Ethernet PHY1 interrupt status |
| 23 | Ethernet PHY3 interrupt status |
| 24 | PEX8548 interrupt status |
| 25 | TSI578 interrupt status |
| 26 | Watchdog 0 interrupt status |
| 27 | Watchdog 1 interrupt status |
| 28 | AXIS Message FIFO A interrupt status |
| 29 | AXIS Message FIFO B interrupt status |
| 30 | AXIS Message FIFO C interrupt status |
| 31 | AXIS Message FIFO D interrupt status |

## 6.15 Board Interrupt Core 0 INT Mask Register (Offset 0x4010)

A set bit enables an active interrupt from the corresponding device to drive out the 8641D IRQ8 interrupt.

Table 6-15 Board Interrupt Core 0 INT Mask Register

| Bits | Description |
|---|---|
| 0 to 14 | Reserved |
| 15 | PCI Express Doorbell 3 mask |
| 16 | PCI Express Doorbell 2 mask |
| 17 | PCI Express Doorbell 1 mask |
| 18 | PCI Express Doorbell 0 mask |
| 19 | RTC interrupt mask |
| 20 | Temperature interrupt mask |
| 21 | Temperature Critical interrupt mask |
| 22 | Ethernet PHY1 interrupt mask |
| 23 | Ethernet PHY3 interrupt mask |
| 24 | PEX8548 interrupt mask |
| 25 | TSI578 interrupt mask |
| 26 | Watchdog 0 interrupt mask |
| 27 | Watchdog 1 interrupt mask |
| 28 | AXIS Message Queue 0 interrupt mask |
| 29 | AXIS Message Queue 1 interrupt mask |
| 30 | AXIS Message Queue 2 interrupt mask |
| 31 | AXIS Message Queue 3 interrupt mask |

## 6.16 Board Interrupt Core 1 INT Mask Register (Offset 0x4014)

A set bit enables an active interrupt from the corresponding device to drive out the 8641D IRQ9 interrupt.

The bit allocation is as for the Board Interrupt Core 0 INT Mask Register.

## 6.17 Board Interrupt Core 0 MCP Mask Register (Offset 0x4018)

A set bit enables an active interrupt from the corresponding device to drive out the 8641D machine check interrupt to Processing Core 0.

The bit allocation is as for the Board Interrupt Core 0 INT Mask Register.

## 6.18 Board Interrupt Core 1 MCP Mask Register (Offset 0x401C)

A set bit enables an active interrupt from the corresponding device to drive out the 8641D Machine Check Interrupt to Processing Core 1.

The bit allocation is as for the Board Interrupt Core 0 INT Mask Register.

## 6.19 PCI Express Block Configuration Register (Offset 0x5000)

This register contains details of the configuration of the PCI Express block. This region is intended to be accessible from the PCI Express backplane, allowing external boards to interrupt the local processors and lock shared resources.

Table 6-16 PCI Express Block Configuration Register

| Bits | Description | Notes |
|---|---|---|
| 0 to 7 | Board ID | SBC610 = 0x2D |
| 8 to 15 | Number of Semaphores | 0x4 |
| 16 to 23 | Number of Doorbells | 0x4 |
| 24 to 31 | Number of Scratchpads | 0x2 |

## 6.20 PCI Express Block Semaphore Registers (Offset 0x5010 to 0x501C)

Each register controls one of four semaphores.

Table 6-17 PCI Express Block Semaphore Register Offsets

| Offset | Semaphore |
|---|---|
| 0x5010 | 1 |
| 0x5014 | 2 |
| 0x5018 | 3 |
| 0x501C | 4 |

A semaphore is taken by reading the corresponding register:

- If the value returned is zero, then semaphore is currently in use
- If the value returned is non-zero, then the semaphore take is successful

The semaphore is released by writing to the corresponding register (the value written is not significant).

The reset value for all semaphore registers is 0x0000 0001.

## 6.21 PCI Express Scratchpad Registers (Offsets 0x5020 and 0x5024)

These two registers have no effect on the system and are provided for software to store status information or data. Their value on reset is 0x0000 0000.

## 6.22 PCI Express Doorbell Assert Register (Offset 0x5030)

Writing a '1' to a bit in this register asserts the corresponding doorbell interrupt. This register is write-only, but the doorbell status can be read from the PCI Express Doorbell Status Register.

Table 6-18 PCI Express Doorbell Assert Register

| Bits | Description | Notes |
|---|---|---|
| 0 to 27 | Reserved | 0x0000000 |
| 28 | Assert Doorbell 3 | Write '1' to assert |
| 29 | Assert Doorbell 2 | Write '1' to assert |
| 30 | Assert Doorbell 1 | Write '1' to assert |
| 31 | Assert Doorbell 0 | Write '1' to assert |

## 6.23 PCI Express Doorbell Clear Register (Offset 0x5034)

Writing a '1' to a bit in this register clears the corresponding doorbell interrupt. This register is write-only but the doorbell status can be read from the PCI Express Doorbell Status Register.

Table 6-19 PCI Express Doorbell Clear Register

| Bits | Description | Notes |
|---|---|---|
| 0 to 27 | Reserved | 0x0000000 |
| 28 | Clear Doorbell 3 | Write '1' to clear |
| 29 | Clear Doorbell 2 | Write '1' to clear |
| 30 | Clear Doorbell 1 | Write '1' to clear |
| 31 | Clear Doorbell 0 | Write '1' to clear |

## 6.24 PCI Express Doorbell Status Register (Offset 0x5038)

This register reflects the status of the doorbell interrupts. The register is read-only. The interrupts must be asserted or cleared using the PCI Express Doorbell Assert/Clear register. Active doorbell interrupts can be routed to processing cores using the Board Interrupt Core x INT Mask Registers.

Table 6-20 PCI Express Doorbell Status Register

| Bits | Description | Notes |
|---|---|---|
| 0 to 27 | Reserved | 0x0000000 |
| 28 | Doorbell 3 Status | 0 = Doorbell interrupt not active<br>1 = Doorbell interrupt active |
| 29 | Doorbell 2 Status | 0 = Doorbell interrupt not active<br>1 = Doorbell interrupt active |
| 30 | Doorbell 1 Status | 0 = Doorbell interrupt not active<br>1 = Doorbell interrupt active |
| 31 | Doorbell 0 Status | 0 = Doorbell interrupt not active<br>1 = Doorbell interrupt active |

## 6.25 AXIS Timestamp Low and High Value Registers (Offsets 0x6000 and 0x6004)

These registers hold bits 0 to 31 and 32 to 47 respectively of the 48-bit AXIS Timestamp value.

NOTE

Reading the AXIS Timestamp Low Value Register causes the value of the whole timestamp (including the high 16 bits) to be latched. The AXIS Timestamp Low Value Register should therefore always be read *before* the AXIS Timestamp High Value Register to prevent the reading of stale data.

## 6.26 AXIS Timer Control Register (Offset 0x6008)

This register contains the control bits for the 48-bit AXIS timer when operating in Master mode.

Table 6-21 AXIS Timer Control Register

| Bits | Description | Notes |
|---|---|---|
| 0 to 23 | Reserved | 0x000000 |
| 24 to 29 | Timer Clock Prescaler | This value determines the frequency of the output clock when in Master mode. The clock period is calculated as follows:<br>Period = (Prescaler + 1) * Local Bus Clock Period (normally 15ns)<br>The default is 0x07 (nominally a 120ns period) |
| 30 | Timer Reset | This determines the state of the Timer Reset output when in Master mode<br>0 = Timer reset output inactive<br>1 = Timer reset output active |
| 31 | Timer Master | 0 = Timer Slave (accepts clock and reset)<br>1 = Timer Master (generates clock and reset) |

## 6.27 AXIS Semaphore Registers (Offsets 0x6020 to 0x603C)

Each register controls one of eight semaphores.

Table 6-22 AXIS Semaphore Register Offsets

| Offset | Semaphore | Offset | Semaphore |
|---|---|---|---|
| 0x6020 | 1 | 0x6030 | 5 |
| 0x6024 | 2 | 0x6034 | 6 |
| 0x6028 | 3 | 0x6038 | 7 |
| 0x602C | 4 | 0x603C | 8 |

A semaphore is taken by reading the corresponding register:

- If the value returned is zero, then semaphore is currently in use
- If the value returned is non-zero, then the semaphore take is successful

The semaphore is released by writing to the corresponding register (the value written is not significant).

The reset value for all semaphore registers is 0x0001.

## 6.28 FIFO Data Registers (Offsets 0x6040 to 0x604C)

These registers form the data path to each FIFO. A write access adds the 32-bit message onto the back of the queue and a read access removes the first message from the queue.

Table 6-23 FIFO Data Register

| Offset | FIFO |
|---|---|
| 0x6040 | A |
| 0x6044 | B |
| 0x6048 | C |
| 0x604C | D |

The default value of these registers is 0x0000 0000.

## 6.29 FIFO Status Registers (Offsets 0x6050 to 0x605C)

These registers contain status information on each FIFO. A bit is set if the FIFO is full or empty or has only one message or message space remaining.

Table 6-24 FIFO Status Register Offsets

| Offset | FIFO |
|---|---|
| 0x6050 | A |
| 0x6054 | B |
| 0x6058 | C |
| 0x605C | D |

Table 6-25 FIFO Status Register

| Bits | Description | Notes |
|---|---|---|
| 0 to 26 | Reserved | 0x0000000 |
| 27 | FIFO reset | 0 = FIFO normal operation (default)<br>1 = FIFO reset |
| 28 | FIFO full[a] | 0 = FIFO not full<br>1 = FIFO full |
| 29 | FIFO almost full[a] | 0 = FIFO has more than 1 space<br>1 = FIFO has only 1 space |
| 30 | FIFO almost empty[a] | 0 = FIFO has zero or more than 1 entry<br>1 = FIFO has only 1 entry |
| 31 | FIFO empty[a] | 0 = FIFO not empty<br>1 = FIFO empty (default on reset) |

a. Read-only.

## 6.30 I/O FPGA Registers

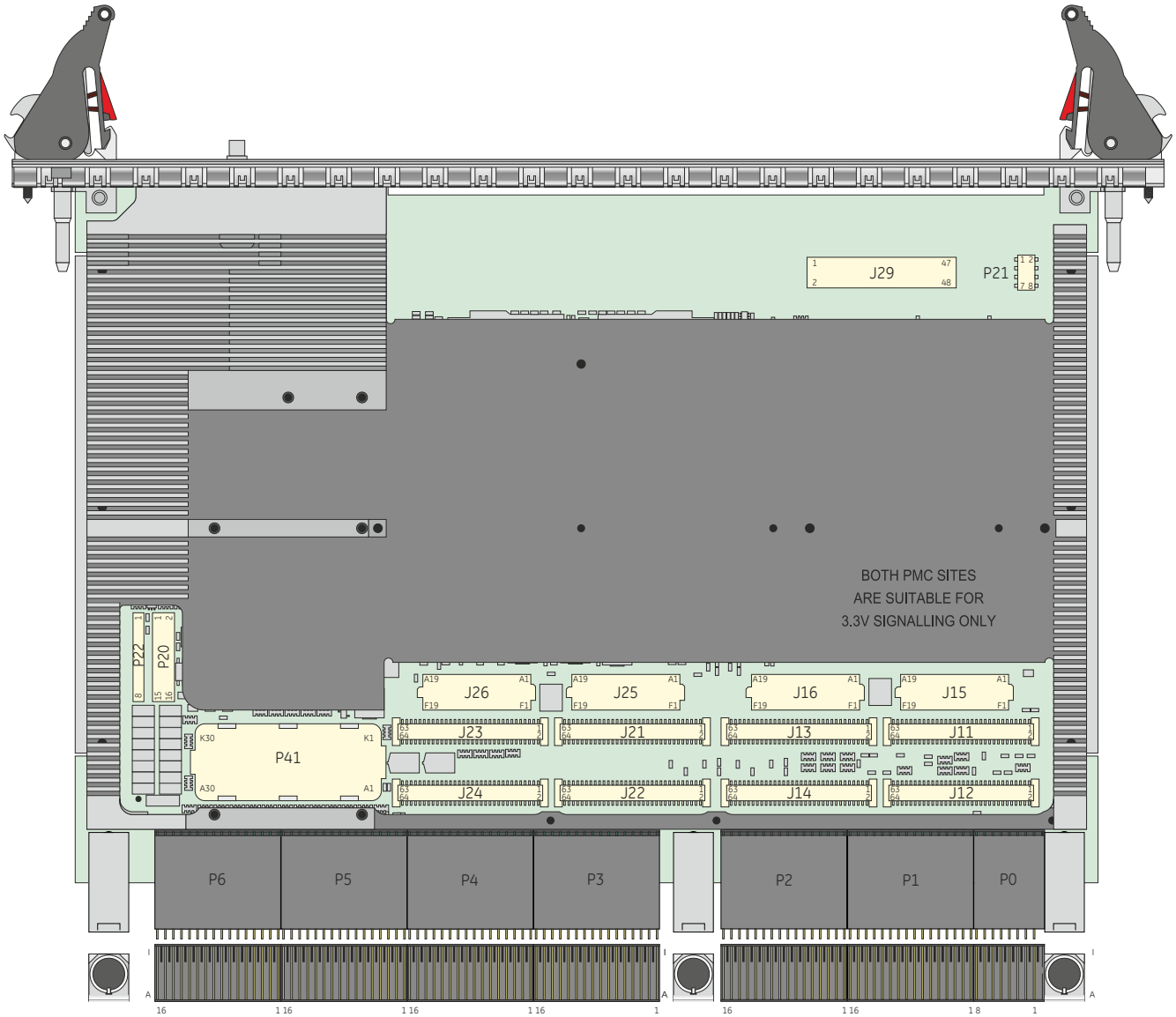
All of the registers concerned with General Purpose I/O and control of COM3 to COM6 on the SBC610 are contained in the I/O FPGA. The register definitions are not documented in this manual as they are intended only to be accessed by GEIP software drivers.

# 7 • Connectors

Table 7-1 Connector Functions

| Connector | Function | Connector | Function |
|---|---|---|---|
| P0 | VPX utility | P21 | JTAG (factory use only) |
| P1 | VPX P1 | P22 | FPGA header |
| P2 | VPX P2 | P41 | AFIX |
| P3 | VPX P3 | J15, J16 | XMC site 1 |
| P4 | VPX P4 | J25, J26 | XMC site 2 |
| P5 | VPX P5 | J11, J12, J13, J14 | PMC site 1 |
| P6 | VPX P6 | J21, J22, J23, J24 | PMC site 2 |
| P20 | BDM header | J29 | PCIe mid-bus probe header (factory use only) |

Figure 7-1 Connector Positions



## 7.1 Backplane Connectors

The following sections show the pin assignments of the SBC610 VPX backplane connectors (P0 to P6). These are shown in the 7-row format as used in the VPX specifications.

Also provided are the corresponding pinouts for the J0 to J6 backplane connectors. These are shown in the 9-row format.

NOTE

Direction of fabrics is shown such that TX is an output from the SBC610 and RX is an input to the SBC610.

### 7.1.1 P0

Table 7-2 P0 Pin Assignments

| Pin | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|
| 1 | N/C (Vs2) | N/C (Vs2) | N/C (Vs2) | N/C | N/C (Vs1) | N/C (Vs1) | N/C (Vs1) |
| 2 | N/C (Vs2) | N/C (Vs2) | N/C (Vs2) | N/C | N/C (Vs1) | N/C (Vs1) | N/C (Vs1) |
| 3 | +5V (Vs3) | +5V (Vs3) | +5V (Vs3) | N/C | +5V (Vs3) | +5V (Vs3) | +5V (Vs3) |
| 4 | NVMRO | SYSRESET~ | GND | N12V_AUX | GND | N/C (SM3) | N/C (SM2) |
| 5 | SM_DATA | SM_CLK | GND | P3V3_AUX | GND | GA4~ | GAP~ |
| 6 | GA0~ | GA1~ | GND | P12V_AUX | GND | GA2~ | GA3~ |
| 7 | JTAG_TRST~ | JTAG_TMS | GND | JTAG_TDI | JTAG_TDO | GND | JTAG_TCK |
| 8 | GND | N/C (RES_BUS+) | N/C (RES_BUS-) | GND | N/C (REF_CLK+) | N/C (REF_CLK-) | GND |

### 7.1.2 Backplane J0

Table 7-3 J0 Pin Assignments

| Fin | A | B | C | D | E | F | G | H | I |
|---|---|---|---|---|---|---|---|---|---|
| 1 | N/C (Vs2) | N/C (Vs2) | N/C (Vs2) | N/C (Vs2) | None | N/C (Vs1) | N/C (Vs1) | N/C (Vs1) | N/C (Vs1) |
| 2 | N/C (Vs2) | N/C (Vs2) | N/C (Vs2) | N/C (Vs2) | None | N/C (Vs1) | N/C (Vs1) | N/C (Vs1) | N/C (Vs1) |
| 3 | +5V (Vs3) | +5V (Vs3) | +5V (Vs3) | +5V (Vs3) | None | +5V (Vs3) | +5V (Vs3) | +5V (Vs3) | +5V (Vs3) |
| 4 | GND | NVMRO | SYSRESET~ | GND | N12V_AUX | GND | N/C (SM3) | N/C (SM2) | GND |
| 5 | GND | SM_DATA | SM_CLK | GND | P3V3_AUX | GND | GA4~ | GAP~ | GND |
| 6 | GND | GA0~ | GA1~ | GND | P12V_AUX | GND | GA2~ | GA3~ | GND |
| 7 | JTAG_TRST~ | JTAG_TMS | GND | GND | JTAG_TDI | JTAG_TDO | GND | GND | JTAG_TCK |
| 8 | GND | GND | N/C (RES_BUS+) | N/C (RES_BUS-) | GND | GND | N/C (REF_CLK+) | N/C (REF_CLK-) | GND |

### 7.1.3 P1

Table 7-4 P1 Pin Assignments

| Pin | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|
| 1 | LINK_A_L0_RXP | LINK_A_L0_RXN | GND | LINK_A_L0_TXP | LINK_A_L0_TXN | GND | N/C (RSVD) |
| 2 | GND | LINK_A_L1_RXP | LINK_A_L1_RXN | GND | LINK_A_L1_TXP | LINK_A_L1_TXN | GND |
| 3 | LINK_A_L2_RXP | LINK_A_L2_RXN | GND | LINK_A_L2_TXP | LINK_A_L2_TXN | GND | VBAT |
| 4 | GND | LINK_A_L3_RXP | LINK_A_L3_RXN | GND | LINK_A_L3_TXP | LINK_A_L3_TXN | GND |
| 5 | LINK_B_L0_RXP | LINK_B_L0_RXN | GND | LINK_B_L0_TXP | LINK_B_L0_TXN | GND | SYS_CON~ |
| 6 | GND | LINK_B_L1_RXP | LINK_B_L1_RXN | GND | LINK_B_L1_TXP | LINK_B_L1_TXN | GND |
| 7 | LINK_B_L2_RXP | LINK_B_L2_RXN | GND | LINK_B_L2_TXP | LINK_B_L2_TXN | GND | JTAG_AUTOWR~[a] |
| 8 | GND | LINK_B_L3_RXP | LINK_B_L3_RXN | GND | LINK_B_L3_TXP | LINK_B_L3_TXN | GND |
| 9 | LINK_C_L0_RXP | LINK_C_L0_RXN | GND | LINK_C_L0_TXP | LINK_C_L0_TXN | GND | PSU_SEQ_IN |
| 10 | GND | LINK_C_L1_RXP | LINK_C_L1_RXN | GND | LINK_C_L1_TXP | LINK_C_L1_TXN | GND |
| 11 | LINK_C_L2_RXP | LINK_C_L2_RXN | GND | LINK_C_L2_TXP | LINK_C_L2_TXN | GND | PSU_SEQ_OUT |
| 12 | GND | LINK_C_L3_RXP | LINK_C_L3_RXN | GND | LINK_C_L3_TXP | LINK_C_L3_TXN | GND |
| 13 | LINK_D_L0_RXP | LINK_D_L0_RXN | GND | LINK_D_L0_TXP | LINK_D_L0_TXN | GND | AXIS_TIMER_CLK |
| 14 | GND | LINK_D_L1_RXP | LINK_D_L1_RXN | GND | LINK_D_L1_TXP | LINK_D_L1_TXN | GND |
| 15 | LINK_D_L2_RXP | LINK_D_L2_RXN | GND | LINK_D_L2_TXP | LINK_D_L2_TXN | GND | AXIS_TIMER_RST |
| 16 | GND | LINK_D_L3_RXP | LINK_D_L3_RXN | GND | LINK_D_L3_TXP | LINK_D_L3_TXN | GND |

a. This pin is reserved in VITA4 6.0. An option is provided to disconnect it from the backplane.

### 7.1.4 Backplane J1

Table 7-5 J1 Pin Assignments

| Fin | A | B | C | D | E | F | G | H | I |
|---|---|---|---|---|---|---|---|---|---|
| 1 | LINK_A_L0_RXP | LINK_A_L0_RXN | GND | GND | LINK_A_L0_TXP | LINK_A_L0_TXN | GND | GND | N/C (RSVD) |
| 2 | GND | GND | LINK_A_L1_RXP | LINK_A_L1_RXN | GND | GND | LINK_A_L1_TXP | LINK_A_L1_TXN | GND |
| 3 | LINK_A_L2_RXP | LINK_A_L2_RXN | GND | GND | LINK_A_L2_TXP | LINK_A_L2_TXN | GND | GND | VBAT |
| 4 | GND | GND | LINK_A_L3_RXP | LINK_A_L3_RXN | GND | GND | LINK_A_L3_TXP | LINK_A_L3_TXN | GND |
| 5 | LINK_B_L0_RXP | LINK_B_L0_RXN | GND | GND | LINK_B_L0_TXP | LINK_B_L0_TXN | GND | GND | SYS_CON~ |
| 6 | GND | GND | LINK_B_L1_RXP | LINK_B_L1_RXN | GND | GND | LINK_B_L1_TXP | LINK_B_L1_TXN | GND |
| 7 | LINK_B_L2_RXP | LINK_B_L2_RXN | GND | GND | LINK_B_L2_TXP | LINK_B_L2_TXN | GND | GND | JTAG_AUTOWR~a |
| 8 | GND | GND | LINK_B_L3_RXP | LINK_B_L3_RXN | GND | GND | LINK_B_L3_TXP | LINK_B_L3_TXN | GND |
| 9 | LINK_C_L0_RXP | LINK_C_L0_RXN | GND | GND | LINK_C_L0_TXP | LINK_C_L0_TXN | GND | GND | PSU_SEQ_IN |
| 10 | GND | GND | LINK_C_L1_RXP | LINK_C_L1_RXN | GND | GND | LINK_C_L1_TXP | LINK_C_L1_TXN | GND |
| 11 | LINK_C_L2_RXP | LINK_C_L2_RXN | GND | GND | LINK_C_L2_TXP | LINK_C_L2_TXN | GND | GND | PSU_SEQ_OUT |
| 12 | GND | GND | LINK_C_L3_RXP | LINK_C_L3_RXN | GND | GND | LINK_C_L3_TXP | LINK_C_L3_TXN | GND |
| 13 | LINK_D_L0_RXP | LINK_D_L0_RXN | GND | GND | LINK_D_L0_TXP | LINK_D_L0_TXN | GND | GND | AXIS_TIMER_CLK |
| 14 | GND | GND | LINK_D_L1_RXP | LINK_D_L1_RXN | GND | GND | LINK_D_L1_TXP | LINK_D_L1_TXN | GND |
| 15 | LINK_D_L2_RXP | LINK_D_L2_RXN | GND | GND | LINK_D_L2_TXP | LINK_D_L2_TXN | GND | GND | AXIS_TIMER_RST |
| 16 | GND | GND | LINK_D_L3_RXP | LINK_D_L3_RXN | GND | GND | LINK_D_L3_TXP | LINK_D_L3_TXN | GND |

### 7.1.5 P2

Table 7-6 P2 Pin Assignments

| Pin | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|
| 1 | VME_D00 | VME_SYSFAIL~ | GND | VME_BBSY~ | GND | VME_ACFAIL~ | VME_D08 |
| 2 | VME_D01 | VME_BR0~ | GND | VME_BCLR~ | GND | VME_BG2IN~ | VME_D09 |
| 3 | VME_D02 | VME_BR1~ | GND | VME_BG0IN~ | GND | VME_BG2OUT~ | VME_D10 |
| 4 | VME_D03 | VME_BR2~ | GND | VME_BG0OUT~ | GND | VME_BG3IN~ | VME_D11 |
| 5 | VME_D04 | VME_BR3~ | GND | VME_BG1IN~ | GND | VME_BG3OUT~ | VME_D12 |
| 6 | VME_D05 | VME_AM0 | GND | VME_BG1OUT~ | GND | VME_BERR~ | VME_D13 |
| 7 | VME_D06 | VME_AM1 | GND | VME_SYSCLK | GND | VME_LWORD~ | VME_D14 |
| 8 | VME_D07 | VME_AM2 | GND | VME_DS1~ | GND | VME_AM5 | VME_D15 |
| 9 | VME_AM4 | VME_AM3 | GND | VME_DS0~ | GND | VME_A23 | VME_A22 |
| 10 | VME_A07 | VME_IRQ7~ | GND | VME_WRITE~ | GND | VME_A21 | VME_A20 |
| 11 | VME_A06 | VME_IRQ6~ | GND | VME_DTACK~ | GND | VME_A19 | VME_A18 |
| 12 | VME_A05 | VME_IRQ5~ | GND | VME_AS~ | GND | VME_A17 | VME_A16 |
| 13 | VME_A04 | VME_IRQ4~ | GND | VME_IACK~ | GND | VME_A15 | VME_A14 |
| 14 | VME_A03 | VME_IRQ3~ | GND | VME_IACKIN~ | GND | VME_A13 | VME_A12 |
| 15 | VME_A02 | VME_IRQ2~ | GND | VME_IACKOUT~ | GND | VME_A11 | VME_A10 |
| 16 | VME_A01 | VME_IRQ1~ | GND | VME_RETRY~ | GND | VME_A09 | VME_A08 |

### 7.1.6 J2 Backplane Connector

CAUTION

The SBC610 has been specifically designed for use with 6U VPX backplanes designed to accommodate a single ended pin out on the J2 connector and is *not* compatible with 6U backplanes where the J2 connector is intended for differential signaling. Plugging the SBC610 into such a 6U backplane may cause permanent component damage.

Table 7-7 J2 Pin Assignments

| Fin | A | B | C | D | E | F | G | H | I |
|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | VME_D00 | VME_SYSFAIL~ | GND | VME_BBSY~ | GND | VME_ACFAIL~ | VME_D08 | GND |
| 2 | GND | VME_D01 | VME_BR0~ | GND | VME_BCLR~ | GND | VME_BG2IN~ | VME_D09 | GND |
| 3 | GND | VME_D02 | VME_BR1~ | GND | VME_BG0IN~ | GND | VME_BG2OUT~ | VME_D10 | GND |
| 4 | GND | VME_D03 | VME_BR2~ | GND | VME_BG0OUT~ | GND | VME_BG3IN~ | VME_D11 | GND |
| 5 | GND | VME_D04 | VME_BR3~ | GND | VME_BG1IN~ | GND | VME_BG3OUT~ | VME_D12 | GND |
| 6 | GND | VME_D05 | VME_AM0 | GND | VME_BG1OUT~ | GND | VME_BERR~ | VME_D13 | GND |
| 7 | GND | VME_D06 | VME_AM1 | GND | VME_SYSCLK | GND | VME_LWORD~ | VME_D14 | GND |
| 8 | GND | VME_D07 | VME_AM2 | GND | VME_DS1~ | GND | VME_AM5 | VME_D15 | GND |
| 9 | GND | VME_AM4 | VME_AM3 | GND | VME_DS0~ | GND | VME_A23 | VME_A22 | GND |
| 10 | GND | VME_A07 | VME_IRQ7~ | GND | VME_WRITE~ | GND | VME_A21 | VME_A20 | GND |
| 11 | GND | VME_A06 | VME_IRQ6~ | GND | VME_DTACK~ | GND | VME_A19 | VME_A18 | GND |
| 12 | GND | VME_A05 | VME_IRQ5~ | GND | VME_AS~ | GND | VME_A17 | VME_A16 | GND |
| 13 | GND | VME_A04 | VME_IRQ4~ | GND | VME_IACK~ | GND | VME_A15 | VME_A14 | GND |
| 14 | GND | VME_A03 | VME_IRQ3~ | GND | VME_IACKIN~ | GND | VME_A13 | VME_A12 | GND |
| 15 | GND | VME_A02 | VME_IRQ2~ | GND | VME_IACKOUT~ | GND | VME_A11 | VME_A10 | GND |
| 16 | GND | VME_A01 | VME_IRQ1~ | GND | VME_RETRY~ | GND | VME_A09 | VME_A08 | GND |

### 7.1.7 P3

Table 7-8 P3 Pin Assignments

| Pin | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|
| 1 | PMC1_IO_04 | PMC1_IO_02 | GND | PMC1_IO_03 | PMC1_IO_01 | GND | VME_A24 |
| 2 | GND | PMC1_IO_08 | PMC1_IO_06 | GND | PMC1_IO_07 | PMC1_IO_05 | GND |
| 3 | PMC1_IO_12/ XMC1_IO_F01 | PMC1_IO_10/ XMC1_IO_C01 | GND | PMC1_IO_11 | PMC1_IO_09 | GND | VME_A25 |
| 4 | GND | PMC1_IO_16/ XMC1_IO_F03 | PMC1_IO_14/ XMC1_IO_F02 | GND | PMC1_IO_15/ XMC1_IO_C03 | PMC1_IO_13/ XMC1_IO_C02 | GND |
| 5 | PMC1_IO_20/ XMC1_IO_F05 | PMC1_IO_18/ XMC1_IO_F04 | GND | PMC1_IO_19/ XMC1_IO_C05 | PMC1_IO_17/ XMC1_IO_C04 | GND | VME_A26 |
| 6 | GND | PMC1_IO_24/ XMC1_IO_F07 | PMC1_IO_22/ XMC1_IO_F06 | GND | PMC1_IO_23/ XMC1_IO_C07 | PMC1_IO_21/ XMC1_IO_C06 | GND |
| 7 | PMC1_IO_28/ XMC1_IO_F09 | PMC1_IO_26/ XMC1_IO_F08 | GND | PMC1_IO_27/ XMC1_IO_C09 | PMC1_IO_25/ XMC1_IO_C08 | GND | VME_A27 |
| 8 | GND | PMC1_IO_32/ XMC1_IO_F11 | PMC1_IO_30/ XMC1_IO_F10 | GND | PMC1_IO_31/ XMC1_IO_C11 | PMC1_IO_29/ XMC1_IO_C10 | GND |
| 9 | PMC1_IO_36/ XMC1_IO_F13 | PMC1_IO_34/ XMC1_IO_F12 | GND | PMC1_IO_35/ XMC1_IO_C13 | PMC1_IO_33/ XMC1_IO_C12 | GND | VME_A28 |
| 10 | GND | PMC1_IO_40/ XMC1_IO_F15 | PMC1_IO_38/ XMC1_IO_F14 | GND | PMC1_IO_39/ XMC1_IO_C15 | PMC1_IO_37/ XMC1_IO_C14 | GND |
| 11 | PMC1_IO_44/ XMC1_IO_F17 | PMC1_IO_42/ XMC1_IO_F16 | GND | PMC1_IO_43/ XMC1_IO_C17 | PMC1_IO_41/ XMC1_IO_C16 | GND | VME_A29 |
| 12 | GND | PMC1_IO_48/ XMC1_IO_F19 | PMC1_IO_46/ XMC1_IO_F18 | GND | PMC1_IO_47/ XMC1_IO_C19 | PMC1_IO_45/ XMC1_IO_C18 | GND |
| 13 | PMC1_IO_52/ XMC1_IO_E01 | PMC1_IO_50/ XMC1_IO_D01 | GND | PMC1_IO_51/ XMC1_IO_B01 | PMC1_IO_49/ XMC1_IO_A01 | GND | VME_A30 |
| 14 | GND | PMC1_IO_56/ XMC1_IO_E03 | PMC1_IO_54/ XMC1_IO_D03 | GND | PMC1_IO_55/ XMC1_IO_B03 | PMC1_IO_53/ XMC1_IO_A03 | GND |
| 15 | PMC1_IO_60/ XMC1_IO_E11 | PMC1_IO_58/ XMC1_IO_D11 | GND | PMC1_IO_59/ XMC1_IO_B11 | PMC1_IO_57/ XMC1_IO_A11 | GND | VME_A31 |
| 16 | GND | PMC1_IO_64/ XMC1_IO_E13 | PMC1_IO_62/ XMC1_IO_D13 | GND | PMC1_IO_63/ XMC1_IO_B13 | PMC1_IO_61/ XMC1_IO_A13 | GND |

### 7.1.8 Backplane J3

Table 7-9 J3 Pin Assignments

| Fin | A | B | C | D | E | F | G | H | I |
|---|---|---|---|---|---|---|---|---|---|
| 1 | PMC1_IO_04 | PMC1_IO_02 | GND | GND | PMC1_IO_03 | PMC1_IO_01 | GND | GND | VME_A24 |
| 2 | GND | GND | PMC1_IO_08 | PMC1_IO_06 | GND | GND | PMC1_IO_07 | PMC1_IO_05 | GND |
| 3 | PMC1_IO_12/ XMC1_IO_F01 | PMC1_IO_10/ XMC1_IO_C01 | GND | GND | PMC1_IO_11 | PMC1_IO_09 | GND | GND | VME_A25 |
| 4 | GND | GND | PMC1_IO_16/ XMC1_IO_F03 | PMC1_IO_14/ XMC1_IO_F02 | GND | GND | PMC1_IO_15/ XMC1_IO_C03 | PMC1_IO_13/ XMC1_IO_C02 | GND |
| 5 | PMC1_IO_20/ XMC1_IO_F05 | PMC1_IO_18/ XMC1_IO_F04 | GND | GND | PMC1_IO_19/ XMC1_IO_C05 | PMC1_IO_17/ XMC1_IO_C04 | GND | GND | VME_A26 |
| 6 | GND | GND | PMC1_IO_24/ XMC1_IO_F07 | PMC1_IO_22/ XMC1_IO_F06 | GND | GND | PMC1_IO_23/ XMC1_IO_C07 | PMC1_IO_21/ XMC1_IO_C06 | GND |
| 7 | PMC1_IO_28/ XMC1_IO_F09 | PMC1_IO_26/ XMC1_IO_F08 | GND | GND | PMC1_IO_27/ XMC1_IO_C09 | PMC1_IO_25/ XMC1_IO_C08 | GND | GND | VME_A27 |
| 8 | GND | GND | PMC1_IO_32/ XMC1_IO_F11 | PMC1_IO_30/ XMC1_IO_F10 | GND | GND | PMC1_IO_31/ XMC1_IO_C11 | PMC1_IO_29/ XMC1_IO_C10 | GND |
| 9 | PMC1_IO_36/ XMC1_IO_F13 | PMC1_IO_34/ XMC1_IO_F12 | GND | GND | PMC1_IO_35/ XMC1_IO_C13 | PMC1_IO_33/ XMC1_IO_C12 | GND | GND | VME_A28 |
| 10 | GND | GND | PMC1_IO_40/ XMC1_IO_F15 | PMC1_IO_38/ XMC1_IO_F14 | GND | GND | PMC1_IO_39/ XMC1_IO_C15 | PMC1_IO_37/ XMC1_IO_C14 | GND |
| 11 | PMC1_IO_44/ XMC1_IO_F17 | PMC1_IO_42/ XMC1_IO_F16 | GND | GND | PMC1_IO_43/ XMC1_IO_C17 | PMC1_IO_41/ XMC1_IO_C16 | GND | GND | VME_A29 |
| 12 | GND | GND | PMC1_IO_48/ XMC1_IO_F19 | PMC1_IO_46/ XMC1_IO_F18 | GND | GND | PMC1_IO_47/ XMC1_IO_C19 | PMC1_IO_45/ XMC1_IO_C18 | GND |
| 13 | PMC1_IO_52/ XMC1_IO_E01 | PMC1_IO_50/ XMC1_IO_D01 | GND | GND | PMC1_IO_51/ XMC1_IO_B01 | PMC1_IO_49/ XMC1_IO_A01 | GND | GND | VME_A30 |
| 14 | GND | GND | PMC1_IO_56/ XMC1_IO_E03 | PMC1_IO_54/ XMC1_IO_D03 | GND | GND | PMC1_IO_55/ XMC1_IO_B03 | PMC1_IO_53/ XMC1_IO_A03 | GND |
| 15 | PMC1_IO_60/ XMC1_IO_E11 | PMC1_IO_58/ XMC1_IO_D11 | GND | GND | PMC1_IO_59/ XMC1_IO_B11 | PMC1_IO_57/ XMC1_IO_A11 | GND | GND | VME_A31 |
| 16 | GND | GND | PMC1_IO_64/ XMC1_IO_E13 | PMC1_IO_62/ XMC1_IO_D13 | GND | GND | PMC1_IO_63/ XMC1_IO_B13 | PMC1_IO_61/ XMC1_IO_A13 | GND |

### 7.1.9 P4

Table 7-10 P4 Pin Assignments

| Pin | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|
| 1 | XMC1_IO_E05 | XMC1_IO_D05 | GND | XMC1_IO_B05 | XMC1_IO_A05 | GND | VME_D16 |
| 2 | GND | XMC1_IO_E07 | XMC1_IO_D07 | GND | XMC1_IO_B07 | XMC1_IO_A07 | GND |
| 3 | XMC1_IO_E09 | XMC1_IO_D09 | GND | XMC1_IO_B09 | XMC1_IO_A09 | GND | VME_D17 |
| 4 | GND | XMC1_IO_E15 | XMC1_IO_D15 | GND | XMC1_IO_B15 | XMC1_IO_A15 | GND |
| 5 | XMC1_IO_E17 | XMC1_IO_D17 | GND | XMC1_IO_B17 | XMC1_IO_A17 | GND | VME_D18 |
| 6 | GND | XMC1_IO_E19 | XMC1_IO_D19 | GND | XMC1_IO_B19 | XMC1_IO_A19 | GND |
| 7 | SATA0_TXP | SATA0_TXN | GND | SATA0_RXP | SATA0_RXN | GND | VME_D19 |
| 8 | GND | SATA1_TXP | SATA1_TXN | GND | SATA1_RXP | SATA1_RXN | GND |
| 9 | USB1_P | USB1_N | GND | USB2_P | USB2_N | GND | VME_D20 |
| 10 | GND | USB1_PWR | USB2_PWR | GND | BOOT_SWAP1~ | BOOT_SWAP0~ | GND |
| 11 | COM1_TXD | COM1_RTS | GND | COM1_RXD | COM1_CTS | GND | VME_D21 |
| 12 | GND | COM2_TXD | COM2_RTS | GND | COM2_RXD | COM2_CTS | GND |
| 13 | ETH0_0P | ETH0_0N | GND | ETH0_1P | ETH0_1N | GND | VME_D22 |
| 14 | GND | ETH0_2P | ETH0_2N | GND | ETH0_3P | ETH0_3N | GND |
| 15 | ETH1_0P | ETH1_0N | GND | ETH1_1P | ETH1_1N | GND | VME_D23 |
| 16 | GND | ETH2_2P | ETH1_2N | GND | ETH1_3P | ETH1_3N | GND |

### 7.1.10 Backplane J4

Table 7-11 J4 Pin Assignments

| Fin | A | B | C | D | E | F | G | H | I |
|---|---|---|---|---|---|---|---|---|---|
| 1 | XMC1_IO_E05 | XMC1_IO_D05 | GND | GND | XMC1_IO_B05 | XMC1_IO_A05 | GND | GND | VME_D16 |
| 2 | GND | GND | XMC1_IO_E07 | XMC1_IO_D07 | GND | GND | XMC1_IO_B07 | XMC1_IO_A07 | GND |
| 3 | XMC1_IO_E09 | XMC1_IO_D09 | GND | GND | XMC1_IO_B09 | XMC1_IO_A09 | GND | GND | VME_D17 |
| 4 | GND | GND | XMC1_IO_E15 | XMC1_IO_D15 | GND | GND | XMC1_IO_B15 | XMC1_IO_A15 | GND |
| 5 | XMC1_IO_E17 | XMC1_IO_D17 | GND | GND | XMC1_IO_B17 | XMC1_IO_A17 | GND | GND | VME_D18 |
| 6 | GND | GND | XMC1_IO_E19 | XMC1_IO_D19 | GND | GND | XMC1_IO_B19 | XMC1_IO_A19 | GND |
| 7 | SATA0_TXP | SATA0_TXN | GND | GND | SATA0_RXP | SATA0_RXN | GND | GND | VME_D19 |
| 8 | GND | GND | SATA1_TXP | SATA1_TXN | GND | GND | SATA1_RXP | SATA1_RXN | GND |
| 9 | USB1_P | USB1_N | GND | GND | USB2_P | USB2_N | GND | GND | VME_D20 |
| 10 | GND | GND | USB1_PWR | USB2_PWR | GND | GND | BOOT_SWAP1~ | BOOT_SWAP0~ | GND |
| 11 | COM1_TXD | COM1_RTS | GND | GND | COM1_RXD | COM1_CTS | GND | GND | VME_D21 |
| 12 | GND | GND | COM2_TXD | COM2_RTS | GND | GND | COM2_RXD | COM2_CTS | GND |
| 13 | ETH0_0P | ETH0_0N | GND | GND | ETH0_1P | ETH0_1N | GND | GND | VME_D22 |
| 14 | GND | GND | ETH0_2P | ETH0_2N | GND | GND | ETH0_3P | ETH0_3N | GND |
| 15 | ETH1_0P | ETH1_0N | GND | GND | ETH1_1P | ETH1_1N | GND | GND | VME_D23 |
| 16 | GND | GND | ETH1_2P | ETH1_2N | GND | GND | ETH1_3P | ETH1_3N | GND |

### 7.1.11 P5

Table 7-12 P5 Pin Assignments

| Pin | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|
| 1 | PMC2_IO_04 | PMC2_IO_02 | GND | PMC2_IO_03 | PMC2_IO_01 | GND | VME_D24 |
| 2 | GND | PMC2_IO_08 | PMC2_IO_06 | GND | PMC2_IO_07 | PMC2_IO_05 | GND |
| 3 | PMC2_IO_12/ XMC2_IO_F01 | PMC2_IO_10/ XMC2_IO_C01 | GND | PMC2_IO_11 | PMC2_IO_09 | GND | VME_D25 |
| 4 | GND | PMC2_IO_16/ XMC2_IO_F03 | PMC2_IO_14/ XMC2_IO_F02 | GND | PMC2_IO_15/ XMC2_IO_C03 | PMC2_IO_13/ XMC2_IO_C02 | GND |
| 5 | PMC2_IO_20/ XMC2_IO_F05/ COM3_TX_A | PMC2_IO_18/ XMC2_IO_F04/ COM3_TX_B | GND | PMC2_IO_19/ XMC2_IO_C05/ COM3_RX_A | PMC2_IO_17/ XMC2_IO_C04/ COM3_RX_B | GND | VME_D26 |
| 6 | GND | PMC2_IO_24/ XMC2_IO_F07/ COM3_RTS_A | PMC2_IO_22/ XMC2_IO_F06/ COM3_RTS_B | GND | PMC2_IO_23/ XMC2_IO_C07/ COM3_CTS_A | PMC2_IO_21/ XMC2_IO_C06/ COM3_CTS_B | GND |
| 7 | PMC2_IO_28/ XMC2_IO_F09/ COM3_TT_A | PMC2_IO_26/ XMC2_IO_F08/ COM3_TT_B | GND | PMC2_IO_27/ XMC2_IO_C09/ COM3_RT_A | PMC2_IO_25/ XMC2_IO_C08/ COM3_RT_B | GND | VME_D27 |
| 8 | GND | PMC2_IO_32/ XMC2_IO_F11/ N/C | PMC2_IO_30/ XMC2_IO_F10/ N/C | GND | PMC2_IO_31/ XMC2_IO_C11/ COM3_ST_A | PMC2_IO_29/ XMC2_IO_C10/ COM3_STB | GND |
| 9 | PMC2_IO_36/ XMC2_IO_F13/ COM4_TX_A | PMC2_IO_34/ XMC2_IO_F12/ COM4_TX_B | GND | PMC2_IO_35/ XMC2_IO_C13/ COM4_RX_A | PMC2_IO_33/ XMC2_IO_C12/ COM4_RX_B | GND | VME_D28 |
| 10 | GND | PMC2_IO_40/ XMC2_IO_F15/ COM4_RTS_A | PMC2_IO_38/ XMC2_IO_F14/ COM4_RTS_B | GND | PMC2_IO_39/ XMC2_IO_C15/ COM4_CTS_A | PMC2_IO_37/ XMC2_IO_C14/ COM4_CTS_B | GND |
| 11 | PMC2_IO_44/ XMC2_IO_F17/ COM4_TT_A | PMC2_IO_42/ XMC2_IO_F16/ COM4_TT_B | GND | PMC2_IO_43/ XMC2_IO_C17/ COM4_RT_A | PMC2_IO_41/ XMC2_IO_C16/ COM4_RT_B | GND | VME_D29 |
| 12 | GND | PMC2_IO_48/ XMC2_IO_F19/ N/C | PMC2_IO_46/ XMC2_IO_F18/ N/C | GND | PMC2_IO_47/ XMC2_IO_C19/ COM4_ST_A | PMC2_IO_45/ XMC2_IO_C18/ COM4_STB | GND |
| 13 | PMC2_IO_52/ XMC2_IO_E01/ COM5_TX_A | PMC2_IO_50/ XMC2_IO_D01/ COM5_TX_B | GND | PMC2_IO_51/ XMC2_IO_B01/ COM5_RX_A | PMC2_IO_49/ XMC2_IO_A01/ COM5_RX_B | GND | VME_D30 |
| 14 | GND | PMC2_IO_56/ XMC2_IO_E03/ COM5_RTS_A | PMC2_IO_54/ XMC2_IO_D03/ COM5_RTS_B | GND | PMC2_IO_55/ XMC2_IO_B03/ COM5_CTS_A | PMC2_IO_53/ XMC2_IO_A03/ COM5_CTS_B | GND |
| 15 | PMC2_IO_60/ XMC2_IO_E11/ COM6_TX_A | PMC2_IO_58/ XMC2_IO_D11/ COM6_TX_B | GND | PMC2_IO_59/ XMC2_IO_B11/ COM6_RX_A | PMC2_IO_57/ XMC2_IO_A11/ COM6_RX_B | GND | VME_D31 |
| 16 | GND | PMC2_IO_64/ XMC2_IO_E13/ COM6_RTS_A | PMC2_IO_62/ XMC2_IO_D13/ COM6_RTS_B | GND | PMC2_IO_63/ XMC2_IO_B13/ COM6_CTS_A | PMC2_IO_61/ XMC2_IO_A13/ COM6_CTS_B | GND |

## 7.1.12 Backplane J5

Table 7-13 J5 Pin Assignments

| Fin | A | B | C | D | E | F | G | H | I |
|---|---|---|---|---|---|---|---|---|---|
| 1 | PMC2_IO_04 | PMC2_IO_02 | GND | GND | PMC2_IO_03 | PMC2_IO_01 | GND | GND | VME_D24 |
| 2 | GND | GND | PMC2_IO_08 | PMC2_IO_06 | GND | GND | PMC2_IO_07 | PMC2_IO_05 | GND |
| 3 | PMC2_IO_12/ XMC2_IO_F01 | PMC2_IO_10/ XMC2_IO_C01 | GND | GND | PMC2_IO_11 | PMC2_IO_09 | GND | GND | VME_D25 |
| 4 | GND | GND | PMC2_IO_16/ XMC2_IO_F03 | PMC2_IO_14/ XMC2_IO_F02 | GND | GND | PMC2_IO_15/ XMC2_IO_C03 | PMC2_IO_13/ XMC2_IO_C02 | GND |
| 5 | PMC2_IO_20/ XMC2_IO_F05/ COM3_TX_A | PMC2_IO_18/ XMC2_IO_F04/ COM3_TX_B | GND | GND | PMC2_IO_19/ XMC2_IO_C05/ COM3_RX_A | PMC2_IO_17/ XMC2_IO_C04/ COM3_RX_B | GND | GND | VME_D26 |
| 6 | GND | GND | PMC2_IO_24/ XMC2_IO_F07/ COM3_RTS_A | PMC2_IO_22/ XMC2_IO_F06/ COM3_RTS_B | GND | GND | PMC2_IO_23/ XMC2_IO_C07/ COM3_CTS_A | PMC2_IO_21/ XMC2_IO_C06/ COM3_CTS_B | GND |
| 7 | PMC2_IO_28/ XMC2_IO_F09/ COM3_TT_A | PMC2_IO_26/ XMC2_IO_F08/ COM3_TT_B | GND | GND | PMC2_IO_27/ XMC2_IO_C09/ COM3_RT_A | PMC2_IO_25/ XMC2_IO_C08/ COM3_RT_B | GND | GND | VME_D27 |
| 8 | GND | GND | PMC2_IO_32/ XMC2_IO_F11/ N/C | PMC2_IO_30/ XMC2_IO_F10/ N/C | GND | GND | PMC2_IO_31/ XMC2_IO_C11/ COM3_ST_A | PMC2_IO_29/ XMC2_IO_C10/ COM3_STB | GND |
| 9 | PMC2_IO_36/ XMC2_IO_F13/ COM4_TX_A | PMC2_IO_34/ XMC2_IO_F12/ COM4_TX_B | GND | GND | PMC2_IO_35/ XMC2_IO_C13/ COM4_RX_A | PMC2_IO_33/ XMC2_IO_C12/ COM4_RX_B | GND | GND | VME_D28 |
| 10 | GND | GND | PMC2_IO_40/ XMC2_IO_F15/ COM4_RTS_A | PMC2_IO_38/ XMC2_IO_F14/ COM4_RTS_B | GND | GND | PMC2_IO_39/ XMC2_IO_C15/ COM4_CTS_A | PMC2_IO_37/ XMC2_IO_C14/ COM4_CTS_B | GND |
| 11 | PMC2_IO_44/ XMC2_IO_F17/ COM4_TT_A | PMC2_IO_42/ XMC2_IO_F16/ COM4_TT_B | GND | GND | PMC2_IO_43/ XMC2_IO_C17/ COM4_RT_A | PMC2_IO_41/ XMC2_IO_C16/ COM4_RT_B | GND | GND | VME_D29 |
| 12 | GND | GND | PMC2_IO_48/ XMC2_IO_F19/ N/C | PMC2_IO_46/ XMC2_IO_F18/ N/C | GND | GND | PMC2_IO_47/ XMC2_IO_C19/ COM4_ST_A | PMC2_IO_45/ XMC2_IO_C18/ COM4_STB | GND |
| 13 | PMC2_IO_52/ XMC2_IO_E01/ COM5_TX_A | PMC2_IO_50/ XMC2_IO_D01/ COM5_TX_B | GND | GND | PMC2_IO_51/ XMC2_IO_B01/ COM5_RX_A | PMC2_IO_49/ XMC2_IO_A01/ COM5_RX_B | GND | GND | VME_D30 |
| 14 | GND | GND | PMC2_IO_56/ XMC2_IO_E03/ COM5_RTS_A | PMC2_IO_54/ XMC2_IO_D03/ COM5_RTS_B | GND | GND | PMC2_IO_55/ XMC2_IO_B03/ COM5_CTS_A | PMC2_IO_53/ XMC2_IO_A03/ COM5_CTS_B | GND |
| 15 | PMC2_IO_60/ XMC2_IO_E11/ COM6_TX_A | PMC2_IO_58/ XMC2_IO_D11/ COM6_TX_B | GND | GND | PMC2_IO_59/ XMC2_IO_B11/ COM6_RX_A | PMC2_IO_57/ XMC2_IO_A11/ COM6_RX_B | GND | GND | VME_D31 |
| 16 | GND | GND | PMC2_IO_64/ XMC2_IO_E13/ COM6_RTS_A | PMC2_IO_62/ XMC2_IO_D13/ COM6_RTS_B | GND | GND | PMC2_IO_63/ XMC2_IO_B13/ COM6_CTS_A | PMC2_IO_61/ XMC2_IO_A13/ COM6_CTS_B | GND |

### 7.1.13 P6

Table 7-14 P6 Pin Assignments

| Pin | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|
| 1 | XMC2_IO_E05 | XMC2_IO_D05 | GND | XMC2_IO_B05 | XMC2_IO_A05 | GND | NED |
| 2 | GND | XMC2_IO_E07 | XMC2_IO_D07 | GND | XMC2_IO_B07 | XMC2_IO_A07 | GND |
| 3 | XMC2_IO_E09 | XMC2_IO_D09 | GND | XMC2_IO_B09 | XMC2_IO_A09 | GND | EXT_RESET~ |
| 4 | GND | XMC2_IO_E15 | XMC2_IO_D15 | GND | XMC2_IO_B15 | XMC2_IO_A15 | GND |
| 5 | XMC2_IO_E17 | XMC2_IO_D17 | GND | XMC2_IO_B17 | XMC2_IO_A17 | GND | EXT_ABORT~ |
| 6 | GND | XMC2_IO_E19 | XMC2_IO_D19 | GND | XMC2_IO_B19 | XMC2_IO_A19 | GND |
| 7 | P41-B1 | P41-A2 | GND | P41-B2 | P41-C2 | GND | P41-A5 |
| 8 | GND | P41-A3 | P41-C3 | GND | P41-B4 | P41-B5 (GPIO0) | GND |
| 9 | P41-C5 | P41-A6 (GPIO1) | GND | P41-C6 | P41-B7 | GND | P41-C27 |
| 10 | GND | P41-A8 (GPIO2) | P41-B8 | GND | P41-C8 | P41-A9 (GPIO3) | GND |
| 11 | P41-C9 | P41-B12 (GPIO4) | GND | P41-A13 (GPIO5) | P41-B13 (GPIO6) | GND | P41-B29 |
| 12 | GND | P41-C13 | P41-A14 (GPIO7) | GND | P41-C14 | P41-B15 | GND |
| 13 | P41-A16 (GPIO8) | P41-B16 (GPIO9) | GND | P41-C16 | P41-A17 (GPIO10) | GND | P41-A30 |
| 14 | GND | P41-C17 | P41-B18 | GND | P41-A21 (GPIO11) | P41-B21 (GPIO12) | GND |
| 15 | P41-A22 (GPIO13) | P41-A24 (GPIO14) | GND | P41-B24 (GPIO15) | P41-A25 (GPIO16) | GND | P41-C30 |
| 16 | GND | P41-B25 (GPIO17) | P41-A28 (GPIO18) | GND | P41-C28 | BITFAIL~ | GND |

### 7.1.14 Backplane J6

Table 7-15 J6 Pin Assignments

| Fin | A | B | C | D | E | F | G | H | I |
|---|---|---|---|---|---|---|---|---|---|
| 1 | XMC2_IO_E05 | XMC2_IO_D05 | GND | GND | XMC2_IO_B05 | XMC2_IO_A05 | GND | GND | NED |
| 2 | GND | GND | XMC2_IO_E07 | XMC2_IO_D07 | GND | GND | XMC2_IO_B07 | XMC2_IO_A07 | GND |
| 3 | XMC2_IO_E09 | XMC2_IO_D09 | GND | GND | XMC2_IO_B09 | XMC2_IO_A09 | GND | GND | EXT_RESET~ |
| 4 | GND | GND | XMC2_IO_E15 | XMC2_IO_D15 | GND | GND | XMC2_IO_B15 | XMC2_IO_A15 | GND |
| 5 | XMC2_IO_E17 | XMC2_IO_D17 | GND | GND | XMC2_IO_B17 | XMC2_IO_A17 | GND | GND | EXT_ABORT~ |
| 6 | GND | GND | XMC2_IO_E19 | XMC2_IO_D19 | GND | GND | XMC2_IO_B19 | XMC2_IO_A19 | GND |
| 7 | P41-B1 | P41-A2 | GND | GND | P41-B2 | P41-C2 | GND | GND | P41-A5 |
| 8 | GND | GND | P41-A3 | P41-C3 | GND | GND | P41-B4 | P41-B5 (GPIO0) | GND |
| 9 | P41-C5 | P41-A6 (GPIO1) | GND | GND | P41-C6 | P41-B7 | GND | GND | P41-C27 |
| 10 | GND | GND | P41-A8 (GPIO2) | P41-B8 | GND | GND | P41-C8 | P41-A9 (GPIO3) | GND |
| 11 | P41-C9 | P41-B12 (GPIO4) | GND | GND | P41-A13 (GPIO5) | P41-B13 (GPIO6) | GND | GND | P41-B29 |
| 12 | GND | GND | P41-C13 | P41-A14 (GPIO7) | GND | GND | P41-C14 | P41-B15 | GND |
| 13 | P41-A16 (GPIO8) | P41-B16 (GPIO9) | GND | GND | P41-C16 | P41-A17 (GPIO10) | GND | GND | P41-A30 |
| 14 | GND | GND | P41-C17 | P41-B18 | GND | GND | P41-A21 (GPIO11) | P41-B21 (GPIO12) | GND |
| 15 | P41-A22 (GPIO13) | P41-A24 (GPIO14) | GND | GND | P41-B24 (GPIO15) | P41-A25 (GPIO16) | GND | GND | P41-C30 |
| 16 | GND | GND | P41-B25 (GPIO17) | P41-A28 (GPIO18) | GND | GND | P41-C28 | BITFAIL~ | GND |

### 7.1.15 Signal Definitions

Table 7-16 Backplane Connector Signal Definitions

| Signal | Description |
|---|---|
| Vs1, Vs2 | VPX Vs1 and Vs2 power inputs. Not connected on the SBC610 |
| Vs3 | VPX Vs3 (+5V) Power input. See the Electrical Specifications section for more details |
| N12V_AUX, P12V_AUX | VPX -12V and +12V DC auxiliary power inputs. Connected to the PMC/XMC site, otherwise unused by the SBC610 |
| P3V3_AUX | VPX +3.3 V DC auxiliary power input. See the Electrical Specifications section for more details |
| N/C | No Connection |
| GND | The DC voltage reference for the system |
| NVMRO | Non-Volatile Memory Read Only. When this signal is high, all on-board non-volatile memory is write-protected. This signal can be externally pulled low (using a link on the backplane or RTM) or driven low under software control by the SBC610 if configured as System Controller |
| SYSRESET~ | System Reset. When this is low, it causes the system to be reset. The SBC610 generates SYSRESET~ when it is configured as System Controller |
| SM_CLK, SM_DATA | System Management bus 0 clock and data. Connects to the BMM via an I2C buffer. Allows access to certain on-board resources from an external I2C master |
| SM2, SM3 | System Management bus 1 clock and data. Not connected on the SBC610 |
| GAP~ | Geographical addressing parity bit input. The sum of all GA bits, including the parity bit, should be an odd number |
| GA[4:0]~ | Geographical Addressing bits |
| JTAG_TCK | JTAG TCK input. AC terminated and connects directly to the JTS06 Scan bridge device |
| JTAG_TDI | JTAG TDI input. Connects to the JTS06 Scanbridge device |
| JTAG_TDO | JTAG TDO output. Driven by the JTS06 Scanbridge device when selected by the JTAG master |
| JTAG_TMS | JTAG TMS input. Connects to the JTS06 Scanbridge device |
| JTAG_TRST~ | JTAG TCK input. Connects to the JTS06 Scanbridge device |
| REF_CLK+, REF_CLK- | VPX REF_CLK+ and REF_CLK-. Not connected on the SBC610 |
| RES_BUS+, RES_BUS- | VPX RES_BUS+ and RES_BUS-. Defined by VITA 46.0 as a reserved bus. Not connected on the SBC610 |
| AXIS_TIMER_CLK | Operates as a clock output in AXIS master mode and a clock input in AXIS slave mode. This signal can be bused between multiple boards to provide a common timestamp |
| AXIS_TIMER_RST | Active high reset signal driven out in AXIS master mode and used to reset the AXIS timer in AXIS slave mode. This signal can be bused between multiple boards to provide a common timestamp |
| JTAG_AUTOWR~ | AutoWrite signal used by JTAG technologies equipment to accelerate programming of Flash via JTAG. Routed to the JTS06 Scanbridge device |
| LINK_x_Ln_RXN | Backplane fabric receive inputs. These should be connected to the transmit outputs of another board to create a link.<br>LINK A and B – Serial RapidIO<br>LINK C and D – Serial RapidIO or PCI Express depending on the state of links E24 and E25, and Control Register 2 |
| LINK_x_Ln_RXP | |
| LINK_x_Ln_TXN | Backplane fabric transmit outputs. These should be connected to the receive inputs of another board to create a link.<br>LINK A and B – Serial RapidIO<br>LINK C and D – Serial RapidIO or PCI Express depending on state of links E24 and E25, and Control Register 2 |
| LINK_x_Ln_TXP | |
| PSU_SEQ_IN | Inter-board PSU Sequencing input. The SBC610 will not start its on-board supplies whilst this signal is driven low. This can be connected to the PSU_SEQ_OUT signal of another board to allow the boards to power up in sequence. A 500 ms timeout applies, in case the preceding board has a fault. This pin may be left unconnected if inter-board power sequencing is not required |
| PSU_SEQ_OUT | Inter-board PSU Sequencing output. Driven low when the backplane supplies are out of specification and held low until all on-board supplies are in specification |
| SYS_CON~ | Pulled low by the backplane to indicate that the module is the VPX System Controller |
| VBAT | Battery supply. Can be used to power the RTC on the SBC610 (max current approximately 1 µA) |

| Signal | Description |
|---|---|
| VME_A[31:01] | VME Address bus |
| VME_ACFAIL~ | AC Failure. Can be used by the system to indicate that the required input voltage levels are not being met |
| VME_AM[5:0] | Address Modifier. Used to broadcast information such as cycle type |
| VME_AS~ | Address Strobe. Driven active when a valid address is placed on the address bus |
| VME_BBSY~ | Bus Busy. Driven low by the current bus master to show that the VME bus is in use |
| VME_BCLR~ | Bus Clear. Driven low by the arbiter to show that there is a higher priority request for the bus. Causes the current master to release the bus |
| VME_BERR~ | Bus Error. Driven low by the slave or bus timer to indicate that the current transfer did not complete |
| VME_BGnIN~ | Bus Grant In. The BGxIN~/BGxOUT~ signals form the bus grant daisy chain, i.e. the BGxOUT~ of one board forms the BGxIN~ of the next board in the daisy chain. The arbiter drives these signals low to tell the board receiving them that if it is requesting the bus on the corresponding level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain |
| VME_BGnOUT~ | Bus Grant Out. Requesters drive these signals to tell the next board in the daisy chain that if it is requesting the bus on that level, then it can use the bus. Otherwise the board should pass the signal down the daisy chain |
| VME_BR[3:0]~ | Bus Request. A requester drives a low level on one of these lines shows to request use of the VMEbus |
| VME_D[31:00] | Data Bus. Used to transfer data between masters and slaves |
| VME_DS[1:0]~ | Data Strobes. These are used with LWORD~ and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows data has been accepted from the data bus |
| VME_DTACK~ | Data Transfer Acknowledge. A slave generates this signal. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle |
| VME_IACK~ | Interrupt Acknowledge. The interrupt handler uses this to acknowledge an interrupt request. It is routed to the IACKIN~ pin of slot 1, where it is monitored by the IACK daisy chain driver |
| VME_IACKIN~ | Interrupt Acknowledge In. IACKIN~/IACKOUT~ form the interrupt acknowledge daisy chain. This tells the board receiving it that that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain |
| VME_IACKOUT~ | Interrupt Acknowledge Out. A board sends this to tell the next board in the daisy chain that it can respond to the Interrupt Acknowledge cycle in progress |
| VME_IRQ[7:1]~ | Interrupt Request (1 to 7). Interrupters drive these low to request an interrupt on the corresponding level |
| VME_LWORD~ | Longword. This is used with DS0~, DS1~ and A01 to select which byte location(s) within the 4-byte group are accessed during the data transfer |
| VME_RETRY~ | Retry. A slave can assert RETRY~, together with BERR~, to postpone a data transfer. The master must then attempt the cycle again at a later time. The retry cycle prevents deadlock |
| VME_SYSCLK | System Clock. This provides a constant 16 MHz clock signal that is independent of any other bus timing |
| VME_SYSFAIL~ | System Fail. Shows a failure has occurred in the system. Any board in the system can generate this signal |
| VME_WRITE~ | Write. A master generates this to show whether the data transfer cycle is a read or a write |
| PMC1_IO_[64:01] | Rear I/O Signals from PMC site 1 (J14 connector). Signal names reflect the pin numbers of this connector |
| PMC2_IO_[64:01] | Rear I/O Signals from PMC site 2 (J24 connector). Signal names reflect the pin numbers of this connector |
| XMC1_IO_x[19:01] | Rear I/O signals from XMC site 1 (J16 connector). Signal names reflect the pin numbers of this connector |
| XMC2_IO_x[19:01] | Rear I/O Signals from XMC site 1 (J26 connector). Signal names reflect the pin numbers of this connector |
| BOOT_SWAPn~ | Used to swap the active boot site of Processing Core 0 and Processing Core 1. See the Boot Flash section for more information |
| COMn_CTS | COM1/2 Clear To Send input for RS232 mode. This signal becomes COMn_RX_B when either port is used in RS422 mode |
| COMn_RTS | COM1/2 Ready To Send output for RS232 mode. This signal becomes COMn_TX_B when either port is used in RS422 mode |
| COMn_RXD | COM1/2 Receive Data input for RS232 mode. This signal becomes COMn_TX_A when either port is used in RS422 mode |
| COMn_TXD | COM1/2 Transmit Data output for RS232 mode. This signal becomes COMn_TX_A when either port is used in RS422 mode |
| ETH0_nN/P | Gigabit Ethernet channel 0 differential pairs |
| ETH1_nN/P | Gigabit Ethernet channel 1 differential pairs |

| Signal | Description |
|---|---|
| SATAn_RXN/P | SATA channel n (n = 0 or 1) Receive input differential pair |
| SATAn_TXN/P | SATA channel n (n = 0 or 1) Transmit output differential pair |
| USBn_N/P | Universal Serial Bus n (n = 1 or 2) differential pairs |
| USBn_PWR | Universal Serial Bus n (n = 1 or 2) switched power outputs (5V) |
| COMn_CTS_A | Serial port Clear To Send input A. COM5/6_CTS_A can alternatively be used as a receive clock input in RS422 mode (selected by I/O FPGA) |
| COMn_CTS_B | Serial port Clear To Send input B. COMn_CTS_B becomes DCD in RS232 mode.<br>COM5/6_CTS_B can alternatively be used as a receive clock input in RS422 mode (selected by I/O FPGA) |
| COMn_RT_A | Serial port Receive Timing (Clock In) input A |
| COMn_RT_B | Serial port Receive Timing (Clock In) input B |
| COMn_RTS_A | Serial port Ready To Send output A. COM5/6_CTS_A can alternatively be used as a transmit clock output in RS422 mode (selected by I/O FPGA) |
| COMn_RTS_B | Serial port Ready To Send output B. COMn_RTS_B becomes DTR in RS232 mode.<br>COM5/6_RTS_B can alternatively be used as a transmit clock output in RS422 mode (selected by I/O FPGA) |
| COMn_RX_A | Serial port Receive Data input A |
| COMn_RX_B | Serial port Receive Data input B. COMn_RX_B becomes DSR in RS232 mode |
| COMn_ST_A | Serial port Send Timing (Transmit Clock In) input A |
| COMn_ST_B | Serial port Send Timing (Transmit Clock In) input B |
| COMn_TT_A | Serial port Transmit Timing (Clock Out) input A |
| COMn_TT_B | Serial port Transmit Timing (Clock Out) input B |
| COMn_TX_A | Serial port Transmit Data output A |
| COMn_TX_B | Serial port Transmit Data output B. COMn_TXD_B is unused in RS232 mode |
| P41-xn | Rear I/O signals from AFIX (P41 connector). Signal names reflect the pin numbers of this connector |
| NED | Nuclear Event Detect input. A 12V level applied to this pin will cause all on-board supplies to reduce to less than 20% of their initial value within 300 µs |
| EXT_RESET~ | External Hard Reset input. Pulling this input low will cause a hard reset to the SBC610. Any switch logic should be debounced externally |
| EXT_ABORT~ | External Soft Reset input. Pulling this input low will cause a soft reset to both processing cores. Any switch logic should be debounced externally |
| BITFAIL~ | BIT Fail output. Reflects the status of the BIT Fail LED. This output is open-drain and so may be used to wire-OR signals from several cards. The output also has a series current limiting resistor and so may be used to drive an LED directly |

## 7.2 PMC Connectors

### 7.2.1 J11/J21 and J12/J22

Table 7-17 J11/J21 Pin Assignments

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | TCK | 2 | N12V_AUX |
| 3 | GND | 4 | INTA~ |
| 5 | INTB~ | 6 | INTC~ |
| 7 | BUSMODE1~ | 8 | P5V |
| 9 | INTD~ | 10 | N/C |
| 11 | GND | 12 | N/C |
| 13 | CLK | 14 | GND |
| 15 | GND | 16 | GNT_A~ |
| 17 | REQ_A~ | 18 | P5V |
| 19 | VIO | 20 | AD31 |
| 21 | AD28 | 22 | AD27 |
| 23 | AD25 | 24 | GND |
| 25 | GND | 26 | C/BE3~ |
| 27 | AD22 | 28 | AD21 |
| 29 | AD19 | 30 | P5V |
| 31 | VIO | 32 | AD17 |
| 33 | FRAME~ | 34 | GND |
| 35 | GND | 36 | IRDY~ |
| 37 | DEVSEL~ | 38 | P5V |
| 39 | XCAP (GND) | 40 | LOCK~ |
| 41 | N/C | 42 | N/C |
| 43 | PAR | 44 | GND |
| 45 | VIO | 46 | AD15 |
| 47 | AD12 | 48 | AD11 |
| 49 | AD09 | 50 | P5V |
| 51 | GND | 52 | C/BE0~ |
| 53 | AD06 | 54 | AD05 |
| 55 | AD04 | 56 | GND |
| 57 | VIO | 58 | AD03 |
| 59 | AD02 | 60 | AD01 |
| 61 | AD00 | 62 | P5V |
| 63 | GND | 64 | REQ64~ |

Table 7-18 J12/J22 Pin Assignments

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | P12V_AUX | 2 | TRST~ |
| 3 | TMS | 4 | TDO |
| 5 | TDI | 6 | GND |
| 7 | GND | 8 | N/C |
| 9 | N/C | 10 | N/C |
| 11 | BUSMODE2~ | 12 | P3V3 |
| 13 | RESET_IN~ | 14 | BUSMODE3~ |
| 15 | P3V3 | 16 | BUSMODE4~ |
| 17 | N/C | 18 | GND |
| 19 | AD30 | 20 | AD29 |
| 21 | GND | 22 | AD26 |
| 23 | AD24 | 24 | P3V3 |
| 25 | IDSELA | 26 | AD23 |
| 27 | P3V3 | 28 | AD20 |
| 29 | AD18 | 30 | GND |
| 31 | AD16 | 32 | C/BE2~ |
| 33 | GND | 34 | IDSELB |
| 35 | TRDY~ | 36 | P3V3 |
| 37 | GND | 38 | STOP~ |
| 39 | PERR~ | 40 | GND |
| 41 | P3V3 | 42 | SERR~ |
| 43 | C/BE1~ | 44 | GND |
| 45 | AD14 | 46 | AD13 |
| 47 | M66EN | 48 | AD10 |
| 49 | AD08 | 50 | P3V3 |
| 51 | AD07 | 52 | REQ_B~ |
| 53 | P3V3 | 54 | GNT_B~ |
| 55 | N/C | 56 | GND |
| 57 | N/C | 58 | EREADY |
| 59 | GND | 60 | RESET_OUT~ |
| 61 | ACK64~ | 62 | P3V3 |
| 63 | GND | 64 | MONARCH~ |

CAUTION

The SBC610 PMC sites are *not* 5V tolerant. VIO pins are connected directly to the +3.3V supply. ***Do not*** fit PMCs that use 5V signaling

### 7.2.2 J13/J23 and J14/J24

Table 7-19 J13/J23 Pin Assignments

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | N/C | 2 | GND |
| 3 | GND | 4 | C/BE7~ |
| 5 | C/BE6~ | 6 | C/BE5~ |
| 7 | C/BE4~ | 8 | GND |
| 9 | VIO | 10 | PAR64 |
| 11 | AD63 | 12 | AD62 |
| 13 | AD61 | 14 | GND |
| 15 | GND | 16 | AD60 |
| 17 | AD59 | 18 | AD58 |
| 19 | AD57 | 20 | GND |
| 21 | VIO | 22 | AD56 |
| 23 | AD55 | 24 | AD54 |
| 25 | AD53 | 26 | GND |
| 27 | GND | 28 | AD52 |
| 29 | AD51 | 30 | AD50 |
| 31 | AD49 | 32 | GND |
| 33 | GND | 34 | AD48 |
| 35 | AD47 | 36 | AD46 |
| 37 | AD45 | 38 | GND |
| 39 | VIO | 40 | AD44 |
| 41 | AD43 | 42 | AD42 |
| 43 | AD41 | 44 | GND |
| 45 | GND | 46 | AD40 |
| 47 | AD39 | 48 | AD38 |
| 49 | AD37 | 50 | GND |
| 51 | GND | 52 | AD36 |
| 53 | AD35 | 54 | AD34 |
| 55 | AD33 | 56 | GND |
| 57 | VIO | 58 | AD32 |
| 59 | N/C | 60 | N/C |
| 61 | N/C | 62 | GND |
| 63 | GND | 64 | N/C |

Table 7-20 J14/J24 Pin Assignments

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | PMCn_IO_01 | 2 | PMCn_IO_02 |
| 3 | PMCn_IO_03 | 4 | PMCn_IO_04 |
| 5 | PMCn_IO_05 | 6 | PMCn_IO_06 |
| 7 | PMCn_IO_07 | 8 | PMCn_IO_08 |
| 9 | PMCn_IO_09 | 10 | PMCn_IO_10 |
| 11 | PMCn_IO_11 | 12 | PMCn_IO_12 |
| 13 | PMCn_IO_13 | 14 | PMCn_IO_14 |
| 15 | PMCn_IO_15 | 16 | PMCn_IO_16 |
| 17 | PMCn_IO_17 | 18 | PMCn_IO_18 |
| 19 | PMCn_IO_19 | 20 | PMCn_IO_20 |
| 21 | PMCn_IO_21 | 22 | PMCn_IO_22 |
| 23 | PMCn_IO_23 | 24 | PMCn_IO_24 |
| 25 | PMCn_IO_25 | 26 | PMCn_IO_26 |
| 27 | PMCn_IO_27 | 28 | PMCn_IO_28 |
| 29 | PMCn_IO_29 | 30 | PMCn_IO_30 |
| 31 | PMCn_IO_31 | 32 | PMCn_IO_32 |
| 33 | PMCn_IO_33 | 34 | PMCn_IO_34 |
| 35 | PMCn_IO_35 | 36 | PMCn_IO_36 |
| 37 | PMCn_IO_37 | 38 | PMCn_IO_38 |
| 39 | PMCn_IO_39 | 40 | PMCn_IO_40 |
| 41 | PMCn_IO_41 | 42 | PMCn_IO_42 |
| 43 | PMCn_IO_43 | 44 | PMCn_IO_44 |
| 45 | PMCn_IO_45 | 46 | PMCn_IO_46 |
| 47 | PMCn_IO_47 | 48 | PMCn_IO_48 |
| 49 | PMCn_IO_49 | 50 | PMCn_IO_50 |
| 51 | PMCn_IO_51 | 52 | PMCn_IO_52 |
| 53 | PMCn_IO_53 | 54 | PMCn_IO_54 |
| 55 | PMCn_IO_55 | 56 | PMCn_IO_56 |
| 57 | PMCn_IO_57 | 58 | PMCn_IO_58 |
| 59 | PMCn_IO_59 | 60 | PMCn_IO_60 |
| 61 | PMCn_IO_61 | 62 | PMCn_IO_62 |
| 63 | PMCn_IO_63 | 64 | PMCn_IO_64 |

Where n = 1 for J14 and n = 2 for J24.

### 7.2.3 Signal Descriptions

Table 7-21 PMC Signal Descriptions

| Signal | Description |
|---|---|
| AD[63:0] | Address/Data bits. Multiplexed address and data bus |
| CBE[7:0]~ | Command/Byte Enables. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus |
| FRAME~ | Frame. Driven low by the current master to signal the start and duration of an access |
| DEVSEL~ | Device Select. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access |
| PAR | Parity. Parity protection bit for AD31 to AD0 and BE3 to BE0 |
| PAR64 | Parity. Parity protection bit for AD63 to AD32 |
| IRDY~ | Initiator Ready. Driven low by the initiator to signal its ability to complete the current data phase |
| LOCK~ | Lock. Driven low to indicate an atomic operation that may require multiple transactions to complete |
| BUSMODE1~ | Bus Mode 1. Driven low by a PMC if it supports the current bus mode. Used to detect the presence of a PMC on the site |
| BUSMODE[4:2]~ | Bus mode. Driven by the host to indicate the bus mode. On the SBC610 this is always PCI. BUSMODE2~ is pulled-up. BUSMODE3~ and BUSMODE4~ are pulled down to GND |
| RESET_IN~ | Reset to the PMC. Driven low to reset the PCI bus |
| TRDY~ | Target Ready. Driven low by the current target to signal its ability to complete the current data phase |
| PERR~ | Parity Error. Driven low by a PCI agent to signal a parity error |
| SERR~ | System Error. Driven low by a PCI agent to signal a system error |
| STOP~ | Stop. Driven low by a PCI target to signal a disconnect or target-abort |
| INT[D:A]~ | Interrupt lines. Level-sensitive, active-low interrupt requests (rotated between PMC sites) |
| CLK | Clock. All PCI bus signals except RST~ are synchronous to this clock |
| REQ[B:A]~ | Request. Driven low by a PCI agent to request ownership of the PCI bus |
| GNT[B:A]~ | Grant. Driven low by the arbiter to grant PCI bus ownership to a PCI agent |
| IDSEL[B:A] | Initialization Device Select. Device chip select during configuration cycles |
| REQ64~ | Request 64 Bit. Driven low by PCI master to request 64-bit transfer |
| ACK64~ | Acknowledge 64 Bit. Driven low by PCI agent in response to REQ64 |
| EREADY | The PMC uses this signal to indicate when it is ready to be enumerated by the PCI software |
| RESET_OUT~ | Reset output. This signal can be driven by a Monarch PMC to reset the SBC610 |
| MONARCH~ | Monarch mode is not supported on the SBC610. This signal is pulled high |
| TCK | Test Clock. Clock for the PMC JTAG |
| TMS | Test Mode Select. Select Test Mode for PMC JTAG |
| TRST~ | Test Reset. Reset any PMC JTAG devices |
| TDI | Test Data In. Input data for PMC JTAG chain |
| TDO | Test Data Out. Data from a PMC JTAG chain |
| P5V | +5V supply pins |
| P3V3 | +3.3V supply pins |
| VIO | PCI V(I/O) pins. Fixed at +3.3V on the SBC610 as +5V signaling is not supported |
| N/C | No connection |
| XCAP | PCI-X Capability detect. Used to determine whether a PMC is PCI-X capable |
| N12V_AUX | -12 V auxiliary supply pins |
| P12V_AUX | +12 V auxiliary supply pins |
| GND | Signal Ground |
| M66EN | Used to determine whether a PMC is 66 MHz PCI capable |
| PMCn_IO_* | Rear I/O connection from PMC site n (n = 1 or 2) |

## 7.3 XMC Connectors

### 7.3.1 J15/J25

J15 and J25 supply the PCI Express interface signals to the XMC1 and XMC2 connectors.

Table 7-22 J15/J25 Pin Assignments

| Pin | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| 1 | PCIE_TX0P | PCIE_TX0N | P3V3 | PCIE_TX1P | PCIE_TX1N | VPWR |
| 2 | GND | GND | JTAG_TRST~ | GND | GND | RESET_IN~ |
| 3 | PCIE_TX2P | PCIE_TX2N | P3V3 | PCIE_TX3P | PCIE_TX3N | VPWR |
| 4 | GND | GND | JTAG_TCK | GND | GND | RESET_OUT~ |
| 5 | PCIE_TX4P | PCIE_TX4N | P3V3 | PCIE_TX5P | PCIE_TX5N | VPWR |
| 6 | GND | GND | JTAG_TMS | GND | GND | P12V_AUX |
| 7 | PCIE_TX6P | PCIE_TX6N | P3V3 | PCIE_TX7P | PCIE_TX7N | VPWR |
| 8 | GND | GND | JTAG_TDI | GND | GND | N12V_AUX |
| 9 | Reserved | Reserved | Reserved | Reserved | Reserved | VPWR |
| 10 | GND | GND | JTAG_TDO | GND | GND | GA0~ |
| 11 | PCIE_RX0P | PCIE_RX0N | MBIST~ | PCIE_RX1P | PCIE_RX1N | VPWR |
| 12 | GND | GND | GA1~ | GND | GND | PRESENT~ |
| 13 | PCIE_RX2P | PCIE_RX2N | P3V3_AUX | PCIE_RX3P | PCIE_RX3N | VPWR |
| 14 | GND | GND | GA2~ | GND | GND | SM_DATA |
| 15 | PCIE_RX4P | PCIE_RX4N | Reserved | PCIE_RX5P | PCIE_RX5N | VPWR |
| 16 | GND | GND | NVMRO | GND | GND | SM_CLK |
| 17 | PCIE_RX6P | PCIE_RX6N | Reserved | PCIE_RX7P | PCIE_RX7N | Reserved |
| 18 | GND | GND | Reserved | GND | GND | Reserved |
| 19 | REFCLK_P | REFCLK_N | Reserved | WAKE~ | ROOT~ | Reserved |

### 7.3.2 J16/J26

J16 and J26 are rear I/O connectivity for the XMC1 and XMC2 connectors.

Table 7-23 J16/J26 Pin Assignments

| Pin | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| 1 | XMCn_IO_A01 | XMCn_IO_B01 | XMCn_IO_C01 | XMCn_IO_D01 | XMCn_IO_E01 | XMCn_IO_F01 |
| 2 | GND | GND | XMCn_IO_C02 | GND | GND | XMCn_IO_F02 |
| 3 | XMCn_IO_A03 | XMCn_IO_B03 | XMCn_IO_C03 | XMCn_IO_D03 | XMCn_IO_E03 | XMCn_IO_F03 |
| 4 | GND | GND | XMCn_IO_C04 | GND | GND | XMCn_IO_F04 |
| 5 | XMCn_IO_A05 | XMCn_IO_B05 | XMCn_IO_C05 | XMCn_IO_D05 | XMCn_IO_E05 | XMCn_IO_F05 |
| 6 | GND | GND | XMCn_IO_C06 | GND | GND | XMCn_IO_F06 |
| 7 | XMCn_IO_A07 | XMCn_IO_B07 | XMCn_IO_C07 | XMCn_IO_D07 | XMCn_IO_E07 | XMCn_IO_F07 |
| 8 | GND | GND | XMCn_IO_C08 | GND | GND | XMCn_IO_F08 |
| 9 | XMCn_IO_A09 | XMCn_IO_B09 | XMCn_IO_C09 | XMCn_IO_D09 | XMCn_IO_E09 | XMCn_IO_F09 |
| 10 | GND | GND | XMCn_IO_C10 | GND | GND | XMCn_IO_F10 |
| 11 | XMCn_IO_A11 | XMCn_IO_B11 | XMCn_IO_C11 | XMCn_IO_D11 | XMCn_IO_E11 | XMCn_IO_F11 |
| 12 | GND | GND | XMCn_IO_C12 | GND | GND | XMCn_IO_F12 |
| 13 | XMCn_IO_A13 | XMCn_IO_B13 | XMCn_IO_C13 | XMCn_IO_D13 | XMCn_IO_E13 | XMCn_IO_F13 |
| 14 | GND | GND | XMCn_IO_C14 | GND | GND | XMCn_IO_F14 |
| 15 | XMCn_IO_A15 | XMCn_IO_B15 | XMCn_IO_C15 | XMCn_IO_D15 | XMCn_IO_E15 | XMCn_IO_F15 |
| 16 | GND | GND | XMCn_IO_C16 | GND | GND | XMCn_IO_F16 |
| 17 | XMCn_IO_A17 | XMCn_IO_B17 | XMCn_IO_C17 | XMCn_IO_D17 | XMCn_IO_E17 | XMCn_IO_F17 |
| 18 | GND | GND | XMCn_IO_C18 | GND | GND | XMCn_IO_F18 |
| 19 | XMCn_IO_A19 | XMCn_IO_B19 | XMCn_IO_C19 | XMCn_IO_D19 | XMCn_IO_E19 | XMCn_IO_F19 |

Where n = 1 for J16 and n = 2 for J26.

### 7.3.3 Signal Descriptions

Table 7-24 XMC Signal Descriptions

| Signal | Description |
|---|---|
| PCIE_TX[7:0]P/N | PCI Express Transmit differential pairs (from XMC to switch) |
| PCIE_RX[7:0]P/N | PCI Express Receive differential pairs (from switch to XMC) |
| REFCLK_P/N | PCI Express Reference Clock. 100 MHz differential clock to XMC |
| PRESENT~ | XMC Present. Pulled low by the XMC to allow the SBC610 to detect if an XMC is fitted |
| RESET_IN~ | XMC Reset In. Reset driven from the SBC610 to the XMC |
| RESET_OUT~ | XMC Reset Out. Reset signal driven by the XMC to the SBC610 (from a front-panel switch for example) |
| SM_DATA | System Management Bus Data. Data line for a two-wire $I^2C$ system management bus |
| SM_CLK | System Management Bus Clock. Clock line for a two-wire $I^2C$ system management bus |
| MBIST~ | XMC Built-in Self-Test. This signal can be held low by the XMC to indicate that it is not yet ready to be enumerated by the root complex |
| GA[2:0]~ | Geographic Address. Used to identify the address of the XMC on a shared I2C bus |
| NVMRO | Non-Volatile Memory Read Only. Used to write protect any non-volatile memory on the XMC. This signal is driven inactive when the NVRAM Write Enable Link (E18) is fitted and the VPX backplane NVMRO signal (on connector P0 pin A4) is low |
| JTAG_TCK | JTAG Test Clock. Clock for the XMC JTAG |
| JTAG_TMS | JTAG Test Mode Select. Select Test Mode for XMC JTAG |
| JTAG_TRST~ | JTAG Test Reset. Reset any XMC JTAG devices |
| JTAG_TDI | JTAG Test Data In. Input data for XMC JTAG chain |
| JTAG_TDO | JTAG Test Data Out. Output data from an XMC JTAG chain |
| XMCn_IO_* | Rear I/O Connection from XMC site n (n = 1 or 2) |
| P12V_AUX | +12V auxiliary supply pins |
| N12V_AUX | -12V auxiliary supply pins |
| VPWR | +5V supply pins |
| P3V3 | +3.3V supply pins |
| P3V3_AUX | +3.3V auxiliary supply pins |
| GND | Signal Ground |
| WAKE~ | PCIe control |
| ROOT~ | PCIe control |
| Reserved | Reserved by VITA 42.0 or 42.3 specification (not connected on the SBC610) |

## 7.4 AFIX Connector (P41)

Table 7-25 P41 Pin Assignments

| Pin | A | B | C | D | E | F | G | H | J | K |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | P41_B1 | GND | GND | JTAG_TCK | GND | N/C | GND | PCI_AD(18) | GND |
| 2 | P41_A2 | P41_B2 | P41_C2 | AFIX_LINK0~ | JTAG_TRST~ | CLK0 | N/C | GPIO(0) | PCI_AD(19) | PCI_AD(0) |
| 3 | P41_A3 | GND | P41_C3 | AFIX_LINK0~ | P5V | CLK1 | P5V | GPIO(1) | P5V | PCI_AD(1) |
| 4 | GND | P41_B4 | GND | P5V | JTAG_TDI | P3V3 | N/C | P3V3 | PCI_AD(20) | P3V3 |
| 5 | P41_A5 | P41_B5 | P41_C5 | INTER_FPGA2 | JTAG_TMS | CLK2 | N/C | GPIO(2) | PCI_AD(21) | PCI_AD(2) |
| 6 | P41_A6 | GND | P41_C6 | INTER_FPGA3 | GND | CLK3 | GND | GPIO(3) | GND | PCI_AD(3) |
| 7 | GND | P41_B7 | GND | GND | JTAG_TDO | GND | USB3_P | GND | PCI_AD(22) | GND |
| 8 | P41_A8 | P41_B8 | P41_C8 | EREADY | PCI_M66EN | POWER_GOOD | USB3_N | GPIO(4) | PCI_AD(23) | PCI_AD(4) |
| 9 | P41_A9 | GND | P41_C9 | N/C | P3V3 | RESET~ | P3V3 | GPIO(5) | P3V3 | PCI_AD(5) |
| 10 | GND | P5V | GND | P3V3 | I2C_CLK | P3V3 | USB4_P | P3V3 | PCI_AD(24) | P3V3 |
| 11 | N12V_AUX | GND | P12V_AUX | N/C | I2C_DATA | IDSEL0 | USB4_N | GPIO(6) | PCI_AD(25) | PCI_AD(6) |
| 12 | GND | P41_B12 | GND | N/C | GND | IDSEL1 | GND | GPIO(7) | GND | PCI_AD(7) |
| 13 | P41_A13 | P41_B13 | P41_C13 | GND | PCI_ACK64~ | GND | PCI_CBE0 | GND | PCI_AD(26) | GND |
| 14 | P41_A14 | GND | P41_C14 | AFIX_FITTED~ | PCI_REQ64~ | IDSEL2 | PCI_CBE1 | GPIO(8) | PCI_AD(27) | PCI_AD(8) |
| 15 | GND | P41_B15 | GND | LOCAL_ALEN | P2V5 | IDSEL3 | P2V5 | GPIO(9) | P2V5 | PCI_AD(9) |
| 16 | P41_A16 | P41_B16 | P41_C16 | P2V5 | PCI_PAR | P2V5 | PCI_CBE2 | P2V5 | PCI_AD(28) | P2V5 |
| 17 | P41_A17 | GND | P41_C17 | LOCAL_RD~ | PCI_PAR64 | P3V3 | PCI_CBE3 | P3V3 | PCI_AD(29) | P3V3 |
| 18 | GND | P41_B18 | GND | LOCAL_WR~ | GND | P3V3 | GND | P3V3 | GND | P3V3 |
| 19 | N12V_AUX | P41_B19 | P12V_AUX | GND | IRQA~ | GND | USB5_P | GND | PCI_AD(30) | GND |
| 20 | GND | GND | GND | LOCAL_AD0 | IRQB~ | PCI_FRAME~ | USB5_N | GPIO(10) | PCI_AD(31) | PCI_AD(10) |
| 21 | P41_A21 | P41_B21 | P41_C21 | LOCAL_AD1 | P5V | PCI_TRDY~ | P5V | GPIO(11) | P5V | PCI_AD(11) |
| 22 | P41_A22 | P41_B22 | P41_C22 | P3V3 | IRQC~ | P3V3 | N/C | P3V3 | N/C | P3V3 |
| 23 | GND | GND | GND | LOCAL_AD2 | IRQD~ | PCI_IRDY~ | N/C | GPIO(12) | N/C | PCI_AD(12) |
| 24 | P41_A24 | P41_B24 | P41_C24 | LOCAL_AD3 | GND | PCI_STOP~ | GND | GPIO(13) | GND | PCI_AD(13) |
| 25 | P41_A25 | P41_B25 | P41_C25 | GND | GNT0~ | GND | PCI_PERR~ | GND | N/C | GND |
| 26 | GND | GND | GND | LOCAL_AD4 | GNT1~ | REQ0~ | PCI_SERR~ | GPIO(14) | N/C | PCI_AD(14) |
| 27 | P41_A27 | P41_B27 | P41_C27 | LOCAL_AD5 | P3V3 | REQ1~ | P3V3 | GPIO(15) | P2V5 | PCI_AD(15) |
| 28 | P41_A28 | GND | P41_C28 | P2V5 | GNT2~ | P3V3 | PCI_DEVSEL~ | P2V5 | N/C | P2V5 |
| 29 | GND | P41_B29 | GND | LOCAL_AD6 | GNT3~ | REQ2~ | PCI_LOCK~ | GPIO(16) | GPIO(18) | PCI_AD(16) |
| 30 | P41_A30 | GND | P41_C30 | LOCAL_AD7 | GND | REQ3~ | GND | GPIO(17) | GND | PCI_AD(17) |

### 7.4.1 Signal Descriptions

Table 7-26 AFIX Signal Descriptions

| Signal | Description |
|---|---|
| P41_* | I/O routed from the AFIX module connector to the P6 connector. For signal descriptions see the AFIX manual |
| PCI_AD[31:0] | AFIX PCI Address/Data bus |
| PCI_* | AFIX PCI Bus Control signals (see the PMC signal descriptions for more details) |
| CLK[3:0] | PCI Clock inputs |
| REQ[3:0]~ | PCI Requests from AFIX |
| GNT[3:0]~ | PCI Grants to AFIX |
| IDSEL[3:0] | IDSELs to AFIX PCI devices |
| RESET~ | PCI Reset to AFIX |
| EREADY | The AFIX uses this signal to indicate when it is ready to be enumerated by the PCI software |
| AFIX_FITTED~ | Grounded by the AFIX to indicate to the SBC610 that it is fitted |
| POWER_GOOD | SBC610 Power Good Signal (for any reset logic on AFIX) |
| LOCAL_ALEN | AFIX Local Bus Address Latch Enable |
| LOCAL_RD~ | AFIX Local Bus Read Strobe |
| LOCAL_WR~ | AFIX Local Bus Write Strobe |
| LOCAL_AD[7:0] | AFIX Local Bus Multiplexed Address/Data Signals. Where this bus is not used, the logic levels are set to allow reading of the AFIX board ID |
| AFIX_LINK[1:0]~ | SBC610 links to control AFIX operation (connected to E26 and E27) |
| INTER_FPGA[3:2] | Inter FPGA lines on SBC610 |
| JTAG_* | JTAG interface to AFIX |
| I2C_CLK/DATA | I2C interface to AFIX |
| USB[3:5]_P/N | USB Port 3, 4 and 5 signal pairs to AFIX |
| IRQ[D:A]~ | PCI interrupts |
| GPIO(18:0) | GPIO input to AFIX. These signals are routed through the AFIX and out on unused I/O (P41_x) pins depending on the AFIX type |
| P5V | +5 Volt supply pins |
| P3V3 | +3.3 Volt supply pins |
| P2V5 | +2.5 Volt supply pins |
| P12V_AUX | +12 Volt auxiliary supply pins |
| N12V_AUX | -12 Volt auxiliary supply pins |
| GND | Signal Ground |
| N/C | No Connection |

## 7.5 BDM Connector (P20)

P20 is the BDM connector allowing the connection of software debugging tools (such as Wind River's VisionProbe or VisionICE) using the processor's JTAG port to control the operation of the processor.

Table 7-27 P20 Pin Assignments

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | JTAG_CPU_TDO | 2 | N/C (QACK~) |
| 3 | JTAG_CPU_TDI | 4 | JTAG_CPU_TRST~ |
| 5 | NC (QREQ~) | 6 | +3.3V pull-up |
| 7 | JTAG_CPU_TCK | 8 | CPU_CHKSTP_IN~ |
| 9 | JTAG_CPU_TMS | 10 | N/C |
| 11 | BDM_SRESET~ | 12 | N/C |
| 13 | BDM_HRESET ~ | 14 | N/C (KEYWAY) |
| 15 | CPU_CHKSTP_OUT~ | 16 | GND |

Table 7-28 P20 Signal Descriptions

| Signal | Description |
|---|---|
| JTAG_CPU_TCK | Processor JTAG Test Clock |
| JTAG_CPU_TMS | Processor JTAG Test Mode Select |
| JTAG_CPU_TDI | Processor JTAG Test Data In |
| JTAG_CPU_TDO | Processor JTAG Test Data Out |
| JTAG_CPU_TRST~ | Processor JTAG Test Reset |
| BDM_SRESET~ | Soft Reset Input |
| BDM_HRESET_CPU~ | Hard Reset Input |
| CPU_CHKSTP_IN~ | Checkstop In. Forces processor to the Checkstop state |
| CPU_CHKSTP_OUT~ | Checkstop Out. Indicates that processor is in the Checkstop state |
| +3.3V PULL-UP | Power-on status signal to RISCWatch hardware |
| GND | Signal ground |
| N/C | No Connection |

CAUTION

When using this connector, ensure that the JTAG Scanbridge is disabled (link E23 is not fitted).

## 7.6 FPGA Programming Header (P22)

P22 is used to access the FPGA JTAG chain for device programming. This is for factory use only.

Table 7-29 P22 Pin Assignments

| Pin | Description |
|---|---|
| 1 | +3V3_AUX |
| 2 | JTAG_TAP6_TDO |
| 3 | JTAG_TAP6_TDI |
| 4 | N/C |
| 5 | (KEYWAY) |
| 6 | JTAG_TAP6_TMS |
| 7 | GND |
| 8 | JTAG_TAP6_TCK |

Table 7-30 P22 Signal Descriptions

| Signal | Description |
|---|---|
| JTAG_TAP6_TDO | FPGA JTAG Test Data Out |
| JTAG_TAP6_TDI | FPGA JTAG Test Data In |
| JTAG_TAP6_TMS | FPGA JTAG Test Mode Select |
| JTAG_TAP6_TCK | FPGA JTAG Test Clock |
| +3.3V_AUX | Power indicator to programming hardware |
| GND | Signal ground |

CAUTION

When using this header, ensure that the JTAG Scanbridge is disabled (link E23 is not fitted).

## 7.7 PCI Express Mid-Bus Probe Header (J29)

This footprint may be used to connect a PCI Express analyzer to monitor traffic between the processor and the PEX8548 switch.

The analyzer site is in the mezzanine keep-out area and is intended for factory use only. A retention module is required to be soldered to the board before a mid-bus probe may be used.

Table 7-31 J29 Pin Assignments

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| G1 | GND | | |
| 1 | PCIE_TX7N | 2 | GND |
| 3 | PCIE_TX7P | 4 | PCIE_RX7N |
| 5 | GND | 6 | PCIE_RX7P |
| 7 | PCIE_TX6N | 8 | GND |
| 9 | PCIE_TX6P | 10 | PCIE_RX6N |
| 11 | GND | 12 | PCIE_RX6P |
| 13 | PCIE_TX5N | 14 | GND |
| 15 | PCIE_TX5P | 16 | PCIE_RX5N |
| 17 | GND | 18 | PCIE_RX5P |
| 19 | PCIE_TX4N | 20 | GND |
| 21 | PCIE_TX4P | 22 | PCIE_RX4N |
| 23 | GND | 24 | PCIE_RX4P |
| 25 | PCIE_TX3N | 26 | GND |
| 27 | PCIE_TX3P | 28 | PCIE_RX3N |
| 29 | GND | 30 | PCIE_RX3P |
| 31 | PCIE_TX2N | 32 | GND |
| 33 | PCIE_TX2P | 34 | PCIE_RX2N |
| 35 | GND | 36 | PCIE_RX2P |
| 37 | PCIE_TX1N | 38 | GND |
| 39 | PCIE_TX1P | 40 | PCIE_RX1N |
| 41 | GND | 42 | PCIE_RX1P |
| 43 | PCIE_TX0N | 44 | GND |
| 45 | PCIE_TX0P | 46 | PCIE_RX0N |
| 47 | GND | 48 | PCIE_RX0P |
| | | G2 | GND |

This connector makes use of the lane reversal and polarity inversion features of the PCI Express analyzer.

# A • Specifications

## A.1 Technical Specification

Table A-1 Technical Data

| Features | Details | Comments |
|---|---|---|
| Processor | Freescale MPC8641D | Contains two e600 PowerPC processing cores @ 1.13GHz |
| RAM | Up to 4 GBytes DDR2 SDRAM with ECC | Dual memory controllers running at 266 MHz |
| ROM | Up to 1GByte Flash memory | 16 MBytes allocated to Boot Flash and the rest to User Flash.<br>Advanced sector protection features |
| NOVRAM | 128 KBytes | Non-volatile storage for data that must not be lost when power is removed.<br>Power-down Autostore functionality |
| Infrastructure | PCI Express | High bandwidth serial-interconnect. Non-blocking switch architecture |
| Ethernet ports | 2 x 10/100/1000BaseT | |
| Serial ports | 2 x RS232 debug<br>2 x RS232/422/485 Sync/Async<br>2 x RS232/422/485 Async | MPC8641D provides COM1 and COM2 debug ports<br>FPGA provides COM3 to COM6 |
| VME | Tundra Tsi148 | 64-bit VME with 2eSST support. Two programmable DMA controllers |
| USB | 2 ports | USB2.0 capable |
| SATA | 2 channels | Supports speeds of up to 1.5 Gbps |
| Discrete Digital I/O | Up to 19-bits, TTL-compatible | Able to generate edge- or level-triggered interrupts |
| SRIO | Two fixed links, two optional | Shared with PCI Express |
| PCI Express | Two optional links | Shared with SRIO |
| PMC/XMC | Two sites | |
| AFIX Site | Additional functionality | Dual MIL-STD-1553 interfaces, SCSI, Graphics, USB Flash Memory, USB2.0 routing modules |
| DMA Controllers | 4 | Available in the MPC8641D for efficiently moving large blocks of data |
| Timers | 8 x 31-bit timers | Provided by the MPC8641D. Programmable frequency with up to 15 ns resolution.<br>Ability to cascade to form larger timers |
| Watchdog timer | Two 32-bit timers | Programmable interrupt and reset thresholds |
| RTC | Time Of Day/Calendar | 1 second resolution. Standby power may be connected from the VBAT pin to maintain data during power down |
| ETI | Quarter second resolution | Logs the total accumulated time the board has been powered, and the number of power cycles |
| JTAG interface | On-card connectors | JTAG headers provided for factory test and software debug purposes |

# A.2 Electrical Specification

## A.2.1 Voltage Supply Requirements

The VPX VS3 (+5V) and P3V3_AUX supplies are required and must remain within the specified limits as defined below. If either of these supplies is outside of these specifications at power-up, then the SBC610 will fail to start. If these supplies fall outside of these limits during a powered state, then the SBC610 will be held in reset and all on-board supplies will be shut down. The VPX VS1 and VS2 supplies are not used.

The VPX ±12V_AUX supplies are not used on the SBC610 but are connected to the PMC/XMC and AFIX sites.

Table A-2 Voltage Supply Requirements

| Supply | Minimum | Nominal | Maximum |
|---|---|---|---|
| VS3 | +4.88V | +5.0V | +5.25V |
| P3V3_AUX | +3.14V | +3.3V | +3.46V |
| P12V_AUX | +11.4V | +12.0V | +12.6V |
| N12V_AUX | -11.4V | -12.0V | -12.6V |
| VBAT | +1.8V | +3.3V | +5.5V |

WARNING

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components.

## A.2.2 Power Consumption

Typical power consumption figures for SBC610 are shown below. These are given at cold-wall temperatures of +25°C and +85°C in a conduction-cooled environment.

Table A-3 Power Consumption

| Processor | Temperature | Nominal (W) | Maximum (W) |
|---|---|---|---|
| 8641D @ 1333 MHz | +25°C | 57.5 | 63.4 |
| | +85°C | 71.8 | 78.0 |
| 8640D @ 1067 MHz | +25°C | 52.2 | 55.6 |
| | +85°C | 66.6 | 71.8 |
| 8640 @ 1067 MHz | +25°C | 46.3 | 47.7 |
| | +85°C | 58 | 59.9 |

Nominal consumption was measured with both cores at the VxWorks prompt. Maximum consumption was measured with both cores running cache-resident Altivec FFT tests.

NOTE

When using XMCs/PMCs, ensure that they do not cause the specified maximum supply current to be exceeded. It may not be possible to support all combinations of XMCs/PMCs within this limit.

# A.3 Environmental Specifications

## A.3.1 Convection-cooled Boards

Table A-4 Convection-cooled Environmental Specifications

| Build Style | Temperature (°C) | Vibration | Shock | Humidity | Comments |
|---|---|---|---|---|---|
| **Standard (Level 1)** | **Operating:** 0 to +55 with airflow of 300 feet/minute. **Storage:** -50 to +100 | **Random:** $0.002g^2$/Hz from 10 to 2000 Hz **Sine:** 2g from 5 to 500 Hz | 20g peak sawtooth, 11 ms duration | Up to 95% RH | Commercial grade cooled by forced air, for use in benign environments and software development applications. Optional conformal coating |
| **Extended Temperature (Level 2)** | **Operating:** -20 to +65 with airflow of 300 feet/minute **Storage:** -50 to +100 | **Random:** $0.002g^2$/Hz from 10 to 2000 Hz **Sine:** 2g from 5 to 500 Hz | 20g peak sawtooth, 11 ms duration | Up to 95% RH with varying temperature. 10 cycles, 240 hours | As Standard but conformally coated and temperature characterized |
| **Rugged Air-cooled (Level 3)** | **Operating:** -40 to +75 with airflow of 600 feet/minute **Storage:** -50 to +100 | **Random:** $0.04g^2$/Hz from 20 to 2000 Hz, with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. | 20g peak sawtooth, 11 ms duration | Up to 95% RH with varying temperature. 10 cycles, 240 hours | Wide temperature rugged, cooled by forced air. Conformally coated for additional protection |

## A.3.2 Conduction-cooled Boards

Table A-5 Conduction-cooled Environmental Specifications

| Build Style | Temperature (°C) | Vibration | Shock | Humidity | Comments |
|---|---|---|---|---|---|
| **Rugged Conduction-cooled (Level 4)** | **Operating:** -40 to +75 at the thermal interface **Storage:** -50 to +100 | **Random:** $0.1g^2$/Hz from 15 to 2000 Hz per MIL-STD-810E Fig 514.4 – 8 for high performance aircraft. 12g RMS | 40g peak sawtooth, 11 ms duration | Up to 95% RH with varying temperature. 10 cycles, 240 hours | Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS. |
| **Rugged Conduction-cooled (Level 5)** | **Operating:** -40 to +85 at the thermal interface **Storage:** -50 to +100 | **Random**: $0.1g^2$/Hz from 15 to 2000 Hz per MIL-STD-810E Fig 514.4 – 8 for high performance aircraft. 12g RMS | 40g peak sawtooth, 11 ms duration | Up to 95% RH with varying temperature. 10 cycles, 240 hours | Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS. |

## A.4 Reliability (MTBF)

The following table shows the predicted values for reliability as Mean Time Between Failures (MTBF) and failures per million hours (fpmh) for board artwork revision 3 (changes between revision 3 and revision 4 were minor):

Table A-6 Reliability (MTBF)

| Environment | Fail Rate (Failures Per Million Hours) | MTBF (Hours) |
|---|---|---|
| Ground benign 30°C | 4.0453 | 247 200 |
| Ground fixed 40°C | 17.7327 | 56 393 |
| Ground mobile 45°C | 44.8789 | 22 282 |
| Naval sheltered 40°C | 24.3328 | 41 097 |
| Naval unsheltered 45°C | 62.7160 | 15 945 |
| Airborne inhabited cargo 55°C | 43.7000 | 22 883 |
| Airborne inhabited fighter 55°C | 60.8378 | 16 437 |
| Airborne uninhabited cargo 70°C | 116.4834 | 8585 |
| Airborne uninhabited fighter 70°C | 153.6293 | 6509 |
| Airborne rotary wing 55°C | 127.8130 | 7824 |
| Space flight 30°C | 3.1293 | 319 558 |

The predictions are carried out using MIL-HDBK-217F Notice 2, Parts Count method. To complement the 217 failure rates, some manufacturers' data is included where appropriate; $\pi Q$ values have been modified according to the ANSI/VITA51.1 Specification.

These failure rates are based only on the components and connectors fitted to the board at delivery and take no account of user fitted mezzanines.

## A.5 Mechanical Specification

### A.5.1 Dimensions

The air-cooled SBC610 is constructed on a multi-layer 6U Eurocard and conforms to the dimensions specified in IEEE1101.1.

The conduction-cooled SBC610 is constructed on a multi-layer 6U Eurocard and conforms to the dimensions specified in IEEE 1101.2

### A.5.2 Weight

The typical weight varies with build level and processor type (copper heatsinks are fitted for faster boards at higher build levels), as follows:

Table A-7 Weight

| Processor Variant | Build Level 1 | Build Level 2 | Build Level 3 | Build Level 4 | Build Level 5 |
|---|---|---|---|---|---|
| 2 | 722g | 1189g | 1189g | 698g | 1246g |
| 4 | 722g | 722g | 1189g | 698g | 1246g |
| 5 | 722g | 722g | 1189g | 698g | 698g |
| 7 | 722g | 722g | 1189g | 698g | 698g |

See the Product Codes section for more details on the Processor Variant Codes.

## A.6 Product Codes

Table A-8 Product Options

| SBC610 | - | X | X | X | X | X | X | X | X | X |
|---|---|---|---|---|---|---|---|---|---|---|

**Mechanics**

1 = 0.8" pitch, VITA 46
2 = 0.85" pitch, VITA 46
3 = 1" pitch, VITA 46
6 = 1" pitch, VITA 48
A = 0.8" pitch, VITA 48 (2LM)
B = 0.85" pitch, VITA 48 (2LM)
C = 1" pitch, VITA 48 (2LM)

**AFIX**

0 = No AFIX fitted
1 = AFIX1553 (single channel)
2 = AFIX1553 (dual channel)
3 = AFIXSG (8 bit SCSI and Graphics)
4 = AFIXSG (16 bit SCSI and Graphics)
5 = AFIX1553 (single channel with side-band signals)
6 = AFIX1553 (dual channel with side-band signals)
7 = AFIXM (1GB Flash Memory)
8 = AFIXM (2GB Flash Memory)
9 = AFIXDIO1 (Discrete I/O)
A = AFIXDIO1 (USB 3, 4 and 5 Routing)

**Software**

3 = VxWorks
4 = BIT/VxWorks
5 = U-Boot
6 = BIT/U-Boot

**PMC/XMC2 I/O Option**

1 = PMC2 I/O 1-64 + XMC2 I/O 12d (P56-P64sX12d)
2 = PMC2 I/O 1-9, 11 + XMC2 I/O Full (P56-X20d38s)
A = PMC2 I/O 1-16 + COM 3,4,5,6 + XMC2 I/O 12d
B = PMC2 I/O 1-48 + COM 5,6 + XMC2 I/O 12d

**PMC1/XMC1 I/O Options**

1 = PMC1 I/0 1-64 + XMC1 I/O 12d (P56-P64sX12d)
2 = PMC1 I/O 1-9, 11 + XMC1 I/O Full (P34-X20d38s)

**Flash**

2 = 512 MBytes
3 = 1 GByte

**SDRAM**

2 = 2 GBytes
4 = 4 GBytes

**Processor**

2 = 8641D @ 1.333 GHz
4 = 8641 @1.333 GHz
5 = 8640D @ 1.067 GHz
7 = 8640 @ 1.067 GHz

**Ruggedization Level**

1 = Level 1, 2 = Level 2, 3 = Level 3, 4 = Level 4, 5 = Level 5

The default product code is SBC610-x23211xx (where X = value range shown).

## A.7 Software Support

GEIP's software strategy allows fully integrated system-level solutions to be realized easily and with confidence. Off-the-shelf, layered software modules deliver the most from low-level hardware features while exploiting the best high level debug and run-time functionality of popular COTS operating systems and communications modules.

The software products described below build on those available for previous generations of products, so providing a common interface for technology inserts.

The GEIP software strategy ensures that customers can develop market-leading products using the O/S and development environment best suited to their long term program requirements.

### A.7.1 Boot Firmware

The Boot firmware provides a foundation layer to interface between the raw board hardware, with its highly programmable device set-ups and flexibility, and the supported Operating Systems, which require a straight-forward booting and device interface model.

The U-Boot Firmware includes comprehensive configuration facilities, interactive or auto-boot sequencing from a range of device types, automatic PCI resource allocation at initialization, PCI display/interrogation utilities and other valuable features for system integrators.

Memory or other speed and feature enhancements are seamlessly absorbed by the Boot firmware, giving the same look and feel to the O/S and the user application as the GEIP hardware models advance. This allows the constant use of latest technology in required areas without system impact. Where particular operating systems define the use of alternate boot methods (e.g. VxWorks bootroms), the Boot firmware technology is absorbed into such boot methodology.

### A.7.2 Built In Test

BIT probes from the lowest level of discrete on-board hardware up to Line Replaceable Unit level within a system, ensuring the highest degree of confidence in system integrity. BIT includes comprehensive configuration facilities, allowing automatic initialization tests to be defined for the desired mix of system functionality and options. Further tests can be invoked interactively, giving BIT a valuable role as a field service tool. Both object and source code products are available.

### A.7.3 Background Condition Screening

BCS supplements the BIT initialization test coverage with further health screening that can co-exist with a standard COTS Operating System.

In contrast to a traditional BIT-style test, the intensity and coverage of which makes it destructive to operating systems, the configurable BCS package allows functions such as periodic checksumming, memory scrubbing, and others to be tailored for operation alongside the application in on-line conditions. Results are stored in Flash in the same format as BIT results. Code is available for reading out BIT/BCS results under LynxOS and VxWorks.

## A.8 I/O Modules

The Rear Transition Module (RTM) for the SBC610 is the VPX6UX600. More information about RTMs can be found in the VPX I/O Modules manual.

LINK

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH.

VPX6UX600 Hardware Reference Manual, publication number VPX6UX600-0HH.

# B • Statement of Volatility

## B.1 Volatile Memory

The SBC610 contains volatile memory, i.e. memory in which the contents are lost when power is removed. None of this volatile memory is capable of write protection.

Table B-1 Volatile Memory

| Memory Type | Size | User Modifiable? | User Access to Data? | Function | Process to Clear |
|---|---|---|---|---|---|
| SDRAM | 2 or 4 GBytes | Yes | Yes | Contains run-time data | Power-off |
| On-die processor shared L1 cache | 2 x 32 KBytes | No | No | Improved memory performance | Power-off |
| On-die processor shared L2 cache | 1 MByte | No | No | Improved memory performance | Power-off |
| SRAM | 2 MBytes | Yes | Yes | I/O FPGA local data buffering | Power-off |
| I/O FPGA Internal SRAM | 144 KBytes | Yes | Yes | I/O FPGA local data buffering | Power-off |

Other devices may contain internal RAM used to temporarily buffer data as it passes through the device. In all cases, a power-off will cause the RAM to de-energize and the contents to be lost.

## B.2 Non-Volatile Memory

The SBC610 contains non-volatile memory, i.e. memory in which the contents are retained when power is removed.

Table B-2 Non-Volatile Memory

| Memory Type | Size | User Modifiable? | User Access to Data? | Write Protectable? | Function | Process to Clear |
|---|---|---|---|---|---|---|
| Flash | 512 MBytes or 1 GByte | Yes | Yes | Yes | Stores operating system or user data | Unprotect and erase |
| NVRAM | 128 KBytes | Yes | Yes | Yes | Stores set-up and configuration data | Unprotect and erase |
| EEPROM | 2 x 32 KBytes | Yes | Yes | Yes | PCIe Switch configuration | Unprotect and erase |
| EEPROM | 4 x 32 KBytes | No | No | Yes | PCI to PCIe Bridge configuration | N/A |
| EEPROM | 32 KBytes | Yes | Yes | Yes | SRIO Switch configuration | Unprotect and erase |
| EEPROM | 2 x 256 Bytes | No | Yes | Read-only | SDRAM configuration | N/A |
| EEPROM | 32 KBytes | Yes | Yes | Yes | Processor configuration | Unprotect and erase (board will only boot in Recovery mode) |
| EEPROM (in DIP Switch) | 6 bits | Yes | Yes | Yes | XMC GA configuration | Unprotect and set to default |
| EEPROM (in ETI) | 10 Bytes | No | No | Read-only | ETI User EEPROM | N/A |
| PROM | 1 MByte | No | No | No | I/O FPGA configuration | N/A |

# Glossary

LINK

This glossary only features terms special to this manual. Explanations of more general terms can be found in the Glossary, publication number GLOS1.

**2eSST** Two-edge Source Synchronous data Transfer.

**AMP** Asymmetric Multi-Processing.

**BMM** Board Management Microcontroller.

**GEIP** GE Intelligent Platforms.

**NVMRO** Non-Volatile Memory Read Only.

**SMP** Symmetric Multi-Processing.

**SRIO** Serial RapidIO.

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## C (continued)

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## V



## W



## X

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## Additional Resources

For more information, please visit the GE Intelligent Platforms Embedded Systems web site at:

defense.ge-ip.com

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