NANO-8044

NANO-ITX Board

User's Manual

Version 1.1

Table of Contents

How to Use This Manual

How to Use This Manual

The manual describes how to configure your NANO-8044 system board to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Host Board.

Chapter 1: System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single host board.

Chapter 2: Hardware Configuration. Show the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3: System Installation. Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

Chapter 4: BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

Chapter 5: Troubleshooting. Provide various of useful tips to quickly get NANO-8044 running with success. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual is subject to change without prior notice. These changes will be incorporated in new editions of the document. The vendor may make supplement or change in the products described in this document at any time.

Chapter 1
System Overview

1.1 Introduction

Powell Inc., a world-leading innovator in the Industrial PC (IPC) market and a member of the Intel® Communications Alliance, has launched its new NANO-8044 in response to market demand for a simplified embedded system board (ESB) that combines a smaller footprint, lower power consumption, robust computing power and with longevity support.

The NANO-8044 is specifically designed to operate at very low power consumption and low heat, so it can be a truly fanless configuration and battery operated. Base on Intel® System Controller Hub US15W, the NANO-8044 supports one 200-pin SO-DIMM memory slot for DDR2 SDRAM up to 2GB and comes with one IDE, one Type II CompactFlash® socket, one SD card (support SD 1.1 and MMC 4.1 only), dual independent display by VGA and 24-bit LVDS, one gigabit Ethernet, six USB and one PCI-E expansion slot.

Base on leading Intel® Atom solution, NANO-8044 is a compact and ultra low power dissipation board for Digital Signage, Portable Satellite, Digital Security Surveillance (**DSS**) applications…etc.

1.2 Check List

The WADE-8044 package should cover the following basic items

- ✓ One NANO-8044 NANO-ITX Main Board
- ✓ One 2-in-1 Heatsink
- ✓ One Installation Resources CD-Title
- ✓ One ATX Power Cable

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintain.

1.3 Product Specification

- **Main Processor**
  - On board Intel® ATOM™ Z510 (1.1GHz) / Z530 (1.6GHz) processor
  - CPU clock bus: Z530: 533MHz / Z510:400MHz
- **Chipset**
  Intel® System Controller Hub US15W
- **System BIOS**
  AMI BIOS
- **Main Memory**
  One 200-pin DDR2 SODIMM socket supports up to 2GB dual channel 400/533 MHz memory
- **Expansion Interface**
  One PCI-Express x 1slot
- **Serial Port**
  Support one RS232/422/485
- **USB Interface**
  Support six USB (Universal Serial Bus) ports, four on rear I/O and two on board header for internal devices. USB port6 can support USB 2.0 only base on Intel specification.
- **Compact Flash**
  - Support one Type II Compact Flash socket
  - Support boot from Compact Flash function
- **SD card**
  Support one SD card, for SD 1.1 and MMC 4.0 only
- **Audio Interface**
  Connector for Mic-In and Line-Out
- **Watch Dog Timer**
  - Support WDT function through software programming for enable/disable and interval setting
  - General system reset
- **On board VGA**
  Intel® System Controller Hub US15W integrated GMA 500 Graphic device
- **On-board Ethernet LAN**
  One Gigabit Ethernet (10/100/1000 Mbits/sec) LAN ports using Intel® 82574L PCI-Expressx1interface GbE Ethernet Controller
- **High Drive GPIO**
  On-board programmable 8-bit Digital I/O interface
- **Cooling Fans**
  Support one 3-pin power connector for system fan

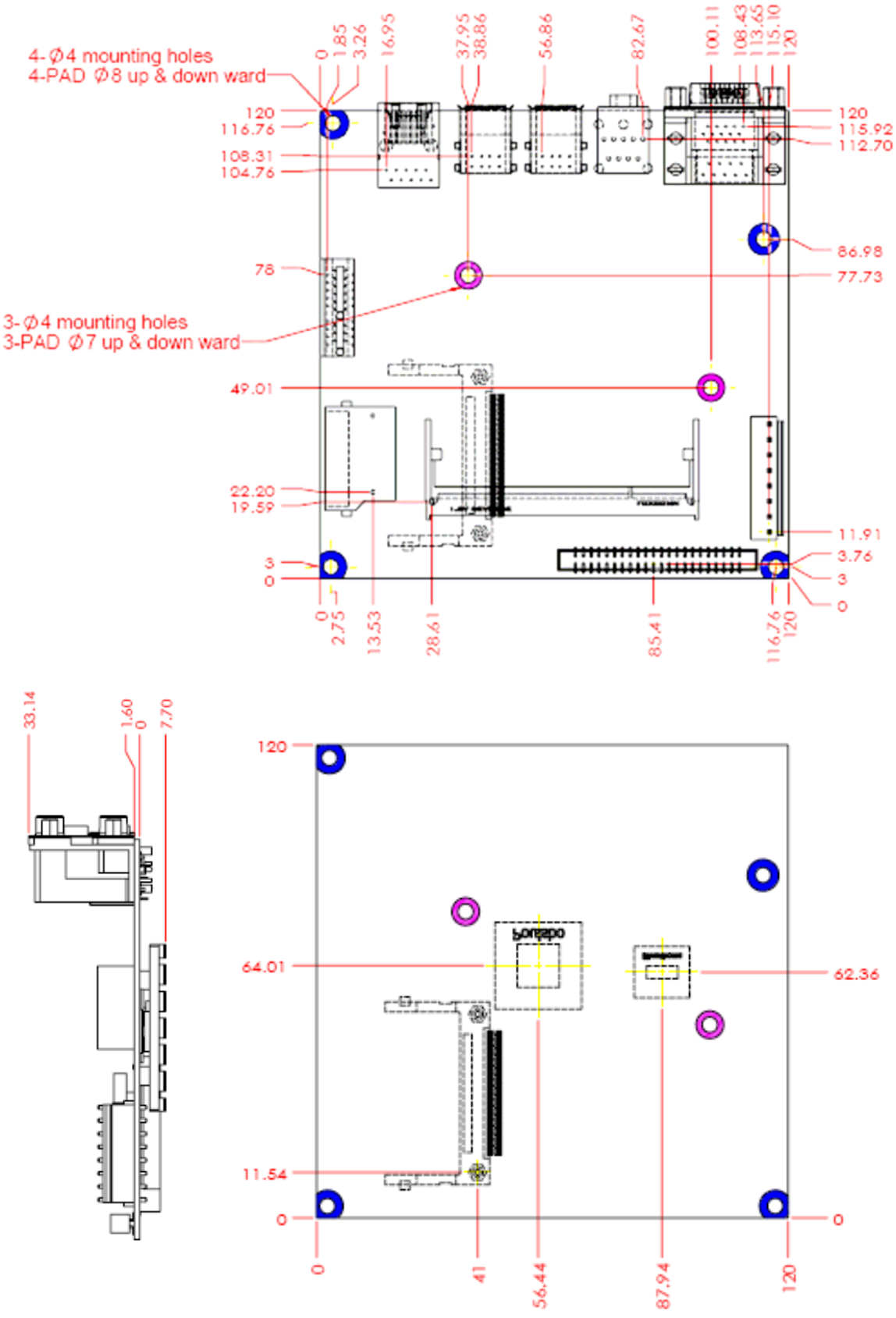
- **System Monitoring Feature**
  Monitor system temperature and major power sources.
- **Outline Dimension (L x W)**
  120mm(4.72'') x 120mm(4.72'')
- **Power Requirements**
  Configuration

CPU Type	Intel® Atom™ CPU Z510 1.10GHz FSB:400MHz L2:512K
SBC BIOS	Portwell, Inc. NANO-8044 BIOS Rev.:R1.00.E0 (08012008)
Memory	Apacer DDR2 PC4300 512MB*1 (SAMSUNG K4T51083QE-ZCD5)
VGA Card	Onboard Intel Corporation Poulsbo Embedded Graphics Chipset Function 0
VGA Driver	Intel Corporation Poulsbo Embedded Graphics Chipset Version:9.0.1.1200
LAN Card	Onboard Intel® 82574L Gigabit Network Connection
LAN Driver	Intel® 82574L Gigabit Network Connection Version:10.3.42.0
Audio Card	Onabord Realtek ALC888 High Definition Audio Controller
Audio Driver	Realtek High Definition Audio Controller Version:5.10.0.5296
Chip Driver	Intel® Chipset Device Software Version:8.8.0.1011
USB 2.0 Driver	Intel® SCH Family USB2 Enhanced Host Controller Version:8.8.0.1001
IDE HDD	Seagate ST340014A 40GB
Compact Flash	Apacer AP-CF128B-Steno
CDROM	PIONEER DVD-126A
Power Supply	PW-330ATXE-12V

Item	Power ON	Full Loading 10Min	Full Loading 30Min
System +12V	1.54A	0.38A	0.90A
System +5V	2.04A	2.96A	3.09A

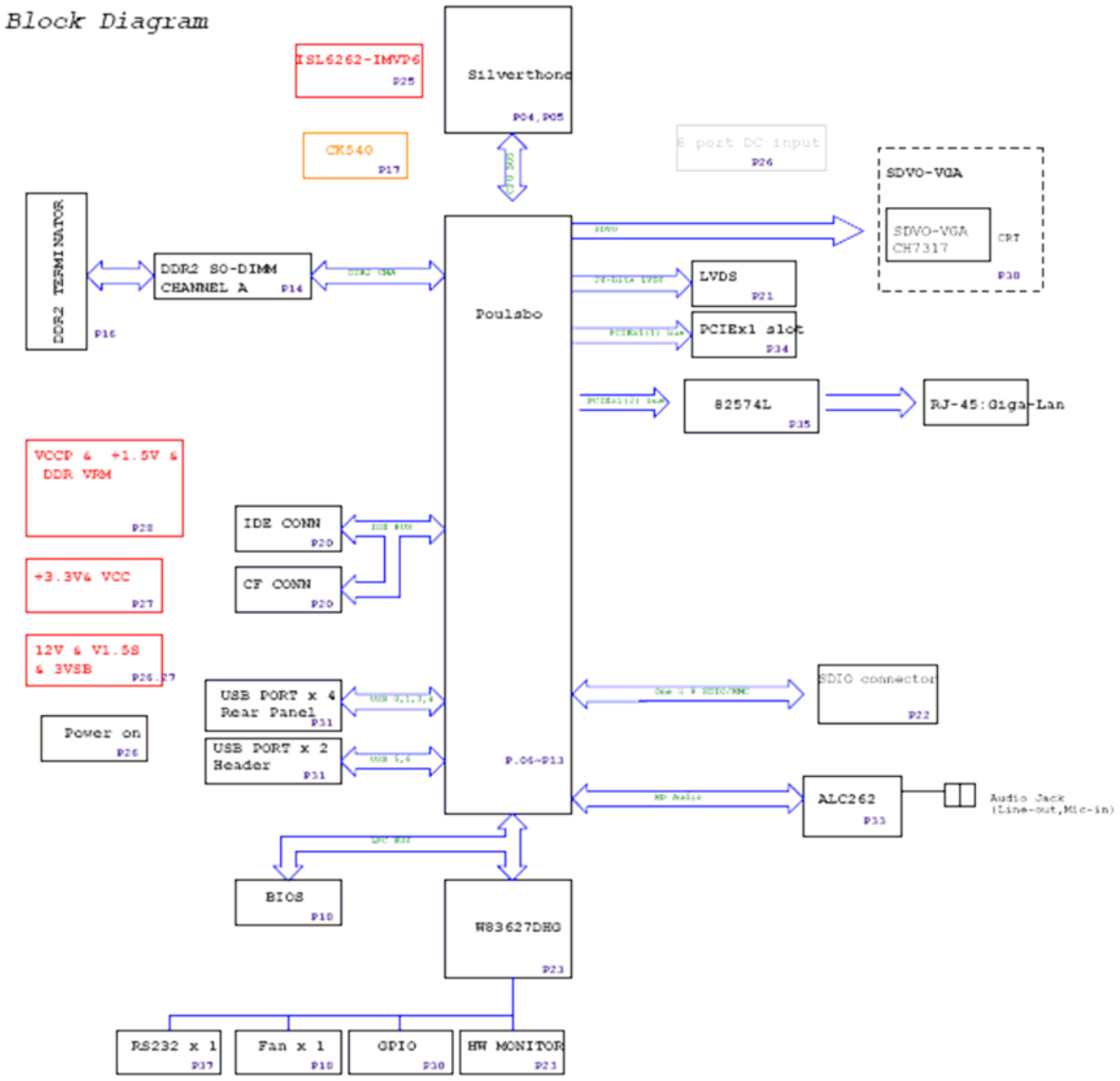
- **Operating Temperature**
  0 °C ~ 60 °C
- **Storage temperature**
  -20 ~ 80 °C
- **Relative Humidity**
  0% ~ 90%, non-condensing

1.3.1 Mechanical Drawing



1.4 System Architecture

All of details operating relations are shown in NANO-8044 System Block Diagram.



NANO-8044 System Block Diagram

Chapter 2
Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connector. All of the configuration jumpers on NANO-8044 are in the proper position. The default settings are indicated with a star sign (★).

2.1 Jumper Setting

In the following sections, **Short** means covering a jumper cap over jumper pins; **Open** or **N/C** (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 2-1 for the Jumper allocations.

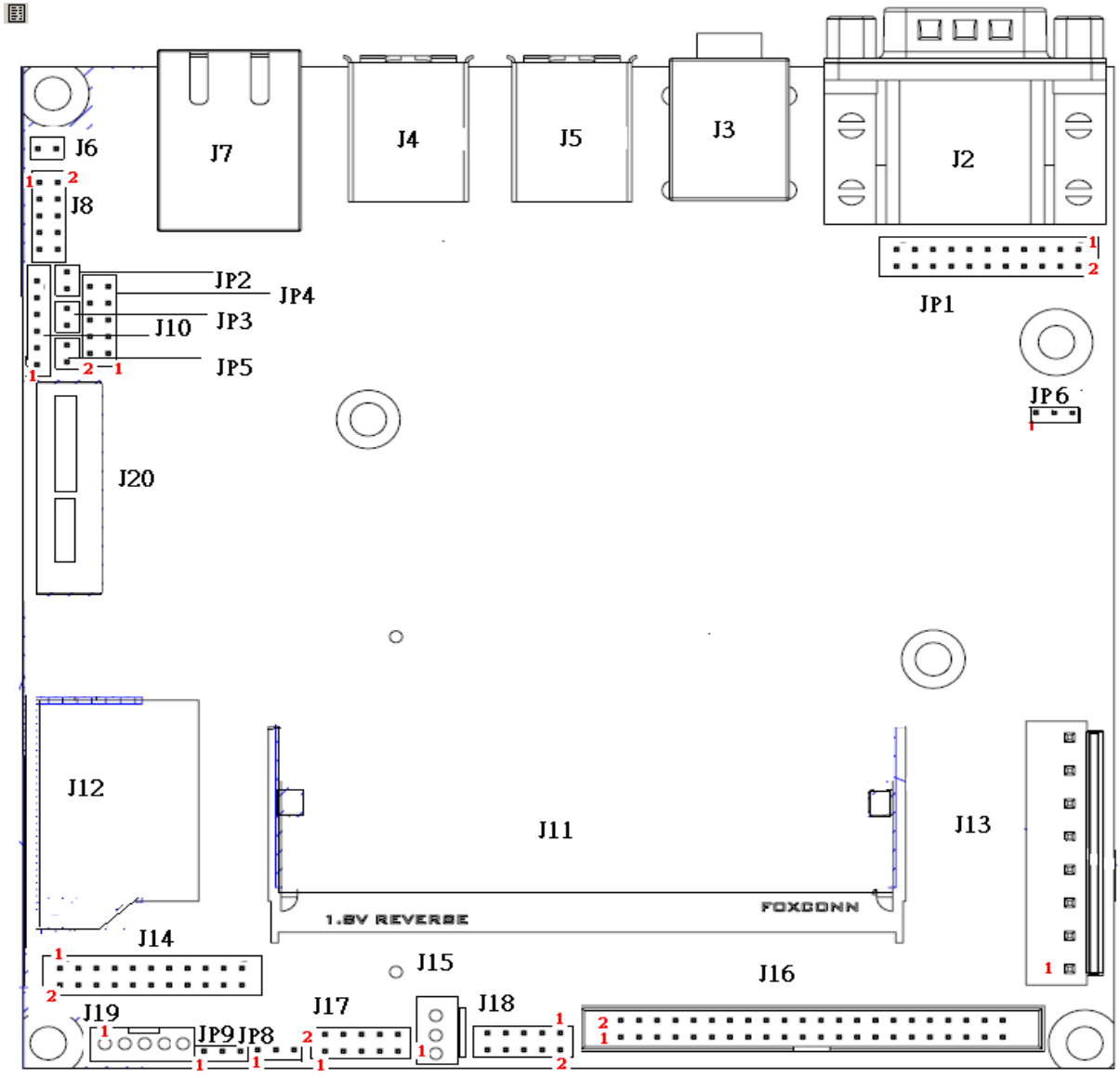


Figure 2-1 NANO-8044 Jumper and Connector Locations

JP9 : 5V / 3.3Vbacklight Inverter Power selection

JP9	Signal Description
1-2 Short	3.3V ★
2-3 Short	5V

JP8 : LCD Power Jump Setting

JP8	Signal Description
1-2 Short	3.3V ★
2-3 Short	5V

JP6 : SDVO to VGA address selection

JP6	Signal Description
1-2 Short	72h
2-3 Short	70h

Note:
The default is 70h (Internal pull-up), so jumper is not to be use.

JP5 : PM_SLPMODE jumper

JP5	Function
1-2 Short	PM_SLPMODE connect

JP4 : LPC Debug Port header

PIN No.	Signal Description	PIN No.	Signal Description
1	LPC_AD0	2	VCC3
3	LPC_AD1	4	PLT_RST#
5	LPC_AD2	6	LPC_FRAME#
7	LPC_AD3	8	LPC_PCID

JP3 : SLP_S5 jumper

JP3	Function
1-2 Short	SLP_S5 Enable

JP2 : RSMRST# jumper

JP2	Function
1-2 Short	RSMRST# Enable

JP1 : RS232/422/485 jumper setting

COM Function	Jumper setting
RS-232	5-6,9-11,10-12,15-17,16-18 ★
RS-422	3-4,7-9,8-10,13-15,14-16,21-22
RS-485	1-2,7-9,8-10,19-20

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors

Connector Function List

Connector	Description	Remark
J2	COM+VGA connector	
J3	Audio (LINE_OUT/MIC_IN) Interface connector	
J4/J5	USB connector	
J6	CMOS Clear header	
J7	RJ-45 connector	
J8	Front USB header	
J10	Micro-controller programming header	
J11	DDR2 SO-DIMM	
J12	SD/MMC connector	
J13	Power connector	
J14	LVDS Interface	
J15	Fan header	
J16	Pitch2.0 IDE header	
J17	8-bit GPIO header	
J18	Power button/Reset/HDD LED/SUS LED header	
J19	LVDS inverter header	
J20	PCIEx1 slot	

Pin Assignments of Connectors

J2 : COM+VGA connector

PIN No.	Signal Description	PIN No.	Signal Description
A1	RED	B1	DCD#1/DT1-
A2	Green	B2	RXD#1/DT+
A3	Blue	B3	TXD#1/422R+
A4	NC	B4	DTR#1/422R-
A5	GND	B5	GND
A6	VGA_AL_EN	B6	DSR#
A7	GND	B7	RTS#1
A8	GND	B8	CTS#1
A9	NC	B9	RI#1
A10	GND		
A11	NC		
A12	MONSDA		
A13	MONHSYNC		
A14	MONVSYNC		
A15	MONSCL		

J3 : Audio (LINE_OUT/MIC_IN) Interface connector

PIN No.	Signal Description	PIN No.	Signal Description
Green	LINE_OUT	Pink	MIC_IN

J4/J5 : USB connector

PIN No.	Signal Description	PIN No.	Signal Description
J4	USB port0	J5	USB port3
J4	USB port1	J5	USB port4

J6 : CMOS Clear header

PIN No.	Signal Description
1	RTC_RST#
2	Ground

J7 : RJ45 connector

PIN No.	Signal Description
RJ45	100/Giga network

J8 : Front USB header

PIN No.	Signal Description	PIN No.	Signal Description
1	USB0VCC	2	USB0VCC
3	USBD6-	4	USBD5-
5	USBD6+	6	USBD5+
7	USBGND	8	USBGND
9	NC	10	NC

PS. Pin 1,3,5,7 support USB 2.0 only.

J10 : Micro-controller download firmware header

PIN No.	Signal Description
1	Vpp
2	Vdd
3	Gnd
4	ICSPDAT
5	ICSPCLK
6	NC

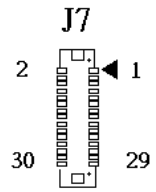
J12 : **SDIO/MMC Pin header**

PIN No.	Signal Description	PIN No.	Signal Description
1	SLOT_DATA0+	2	+3.3V
3	SLOT_ DATA 1+	4	SLOT_CLK-
5	SLOT_ DATA 2+	6	SLOT_CMD
7	SLOT_ DATA 3+	8	+3.3V
9	SLOT_ DATA 4+	10	GND
11	SLOT_ DATA 5+	12	SLOT_CD#
13	SLOT_ DATA 6+	14	SLOT_WP
15	SLOT_ DATA 7+	16	GND

J13 : Power connector

PIN No.	Signal Description	PIN No.	Signal Description
1	VCC	2	VCC
3	5VSB	4	+12V
5	PS_ON#	6	GND
7	GND	8	GND

J14 : LVDS Interface

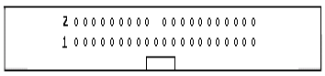


PIN No.	Signal Description	PIN No.	Signal Description
1	Ch1_DATA0+	2	Ch1_ DATA 0-
3	Ch1_ DATA 1+	4	Ch1_ DATA 1-
5	Ch1_ DATA2+	6	Ch1_DATA2-
7	Ch1_ DATA 3+	8	Ch1_ DATA 3-
9	Ch1_ CLK+	10	Ch1_ CLK-
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	NC	20	NC
21	L_BKLTCTL	22	NC
23	GND	24	NC
25	GND	26	GND
27	VDD_LVDS	28	VDD_LVDS
29	N/A	30	VDD_LVDS

J15 : Fan header

PIN No.	Signal Description
1	GND
2	FANPWM1
3	FANI01

J16 : 44-pin Hard Disk Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	R_PLT_RST#	2	GND
3	PDD7	4	PDD8
5	PDD6	6	PDD9
7	PDD5	8	PDD10
9	PDD4	10	PDD11
11	PDD3	12	PDD12
13	PDD2	14	PDD13
15	PDD1	16	PDD14
17	PDD0	18	PDD15
19	GND	20	N/C
21	PDDREQ	22	GND
23	PDIOW#	24	GND
25	PDIOR#	26	GND
27	PDIORDY	28	GND
29	PDDACK#	30	GND
31	IRQ14#	32	N/C
33	PDA1	34	GND
35	PDA0	36	PDA2
37	PDCS#1	38	PDCS#3
39	IDEACT#	40	GND
41	+5V	42	+5V
43	GND	44	N/C

J17 : 8-bits GPIO header

PIN No.	Signal Description	PIN No.	Signal Description
1	LPC_GP10	2	LPC_GP14
3	LPC_GP11	4	LPC_GP15
5	LPC_GP12	6	LPC_GP16
7	LPC_GP13	8	LPC_GP17
9	GND	10	VCC

J18 : Power button/Reset/HDD LED/SUS LED header

PIN No.	Signal Description	PIN No.	Signal Description
1	GND	2	PWR_LED
3	5V_Dual	4	SUS_LED
5	VCC3	6	HDD_LED
7	SYS_RESET#	8	GND
9	GND	10	PWR_ON_SW#

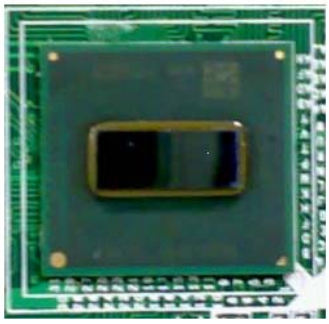
J19 : LCD Panel Power Invert

PIN No.	Signal Description
5	Back light Enable
4	Ground
3	+12V
2	Ground
1	+5V

Chapter 3
System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1 Intel ® ATOM ™ processor Z510/Z530 CPU



Configuring System Bus

NANO-8044 will automatically detect the CPU FSB 400/533MHz CMOS used. CPU speed of Intel ATOM ™ Processor for Mobile can be detected automatically.

3.2 Intel® System Controller Hub US15W

The Intel® System Controller Hub US15W is a low-power chipset in one small 22x22 mm package, It combines the Intel® Graphics Media Accelerator 500, memorycontroller, and I/O controller in a single-chip solution while featuring advanced 3D graphics and extensive I/O capabilities such as USB2.0,SDIO and PCI Express. It supports Intel® High Definition Audio and hardware video decode acceleration, a 400/533 MHz CMOS front-side bus, dual independent display.

3.3 Main Memory

NANO-8044 provides one 200-pin DDR2 SO-DIMM socket which supports 400/533 DDR2-DRAM as main memory, Non-ECC (Error Checking and Correcting), non-register functions. The maximum memory size can be up to 1GB capacity.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be either one double-sided DIMM in either one DIMM socket or one single-sided SO-DIMM in socket.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install memory module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

Note:
To maintain system stability, don't change any of DRAM parameters in BIOS setup to upgrade system performance without acquiring technical information.

Memory frequency / CPU FSB synchronization

NANO-8044 supports different memory frequencies depending on the CPU front side bus and the type of DDR2 SO-DIMM.

CPU FSB	Memory Frequency
533MHz	533/400MHz
400 MHz	400MHz

3.4 Installing the Single Board Computer

To install your NANO-8044 into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position
Step 2 : Install and configure memory module on right position
Step 3 : Place NANO-8044 into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that SBC is properly inserted and fixed by mechanism.

Note:
Please refer to section 3.4.1 to 3.4.4 to install INF/VGA/LAN/Audio drivers.

3.4.1 Chipset Component Driver

The chipset on NANO-8044 is a new chipset that a few old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows XP /VISTA, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in NANO-8044 CD-title.

3.4.2 Intel Integrated Graphics GMCH Chip

Using Intel® SCH US15W with Media Accelerator High performance graphic integrated chipset is aimed to gain an outstanding graphic performance. Shared 1MB to 8MB system DDR2 SO-DIMM Memory with Total Graphics Memory. This combination makes NANO-8044 an excellent piece of multimedia hardware.

Drivers Support

Please find Springdale GMCH driver in the NANO-8044 CD-title. Drivers support Windows XP / VISTA.

3.4.3 Intel Gigabit Ethernet Controller

Drivers Support

Please find Intel 82574L LAN (J7) drivers in Ethernet directory of NANO-8044 CD-title. The drivers support Windows XP / VISTA.

LED Indicator (for LAN status)

NANO-8044 provides two LED indicators to report Intel 82574L Gigabit Ethernet interface status. Please refer to the table below as a quick reference guide.

<table>
<tr><th rowspan="2">82574L</th><th rowspan="2">Color</th><th rowspan="2">Name of LED</th><th colspan="3">Operation of Ethernet Port</th></tr>
<tr><th colspan="2">Linked</th><th>Active</th></tr>
<tr><td>Status LED</td><td>Green</td><td>LAN Linked & Active LED</td><td colspan="2">On</td><td>Blinking</td></tr>
<tr><td rowspan="2">Speed LED</td><td>Orange</td><td rowspan="2">LAN speed LED</td><td>Giga Mbps</td><td>100 Mbps</td><td>10 Mbps</td></tr>
<tr><td>Green</td><td>Orange</td><td>Green</td><td>Off</td></tr>
</table>

3.4.4 Audio Controller

Please find Realtek ALC888 Audio driver form NANO-8044 CD-title. The drivers support Windows XP / VISTA.

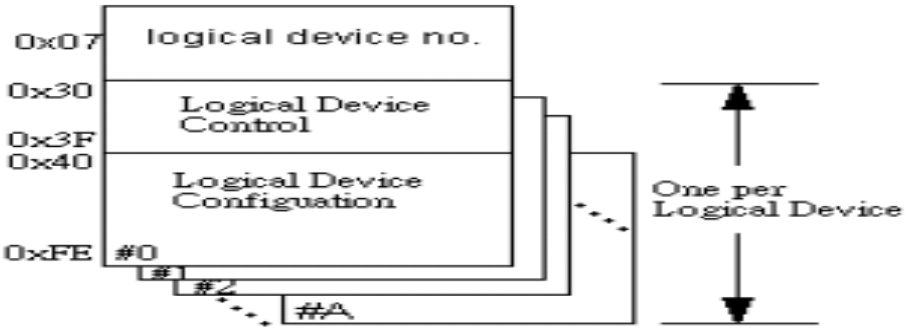
3.5 WDT Function

The algorithm of the WDT function can be simply described as a timer counting process with an output event. The Time-Out period (T_{wd}) can be set by software commands or hardware jumpers that depend on the board circuit design and may be different among the boards. This timer can be used to monitor a software hang.

Nano-8044 allows users to control WDT by issuing dynamic software commands. The WDT starts counting when it is activated. It will cause a system reset once it expires. Before WDT expires, a refreshing command with a T_{wd} can be issued to re-count WDT and continue the status monitoring. If the system encounters a software or application hang, WDT will generate a system reset after its timeout.

The related Control Registers of WDT are included in the following programming guide that is written in C language. User can write a non-zero value (defined as T_{wd}) into the Time-out Value Register (CR_T_{wd}) to enable WDT. Users can write 0x00 and then T_{wd} to CR_T_{wd} to refresh WDT. To refresh WDT, the time tolerance of refreshing interval must be considered. The smaller of T_{wd}, the more deviation of WDT and you need to include more tolerance. "Let T_{wd} be longer than 2 seconds" is the recommendation due to the limitation of Winbond W83627DHG WDT. You can call Portwell support center for reference. The value read back from CR_T_{wd} indicates the counting down value instead of the original T_{wd}. System will be reset after the Time-out Value to be counted down to zero. Users can directly fill a zero value into CR_T_{wd} to disable WDT immediately. To ensure a successful access to the desired Control Register, the following programming guide should be followed.

Programming guide :
CR: Configuration Register.
LD: Logical Device of SIO. There are 11 LDs in W83627DHG SIO.
CR00~2F: Global Control Registers. (All LDs share these CRs)
CR07: LD selection.
CR30~FF: Each LD has its own CR30~FF.



There are two I/O ports as I/O access window for configuring WDT,
1) IO port 0x2E is H/W strapped and named as EFIR (Extended Function Index Register, for identifying CR index number)
2) IO port 0x2F is H/W strapped and named as EFDR (Extended Function Data Register, for accessing desired CR)

<< How to access W83627DHG Configuration Register >>
First, it needs to enter extended function mode.
Enter extended function mode for accessing W83627DHG configuration registers:

```
outportb (EFIR, 0x87);
outportb (EFIR, 0x87);  // double IO write
```

Read Configuration Register CR_rx, and keep this byte to unsigned char al_char

```
outportb(EFIR, CR_rx ) ;
al_char = inportb(EFDR) ;
```

Write Configuration Register CR_wx with byte al_char1 ;

```
outportb (EFIR, CR_wx ) ;
outportb (EFDR, al_char1);
```

Exit extended mode after completion of configuration register access.

```
outportb(EFIR, 0xaa);
```

<< How to access W83627DHG WDT Configuration Register >>
Must enter extended function mode first, then follow the following steps for accessing WDT registers.

Step (1): CR2B_bit4P0

```
        Initialize the multiplex pin (pin89) to WDTO function
        outportb ( EFIR , 0x2B ) ;          // al_char1 : unsigned char
    al_char1 = inportb (EFDR) & 0xEF;  // CR2B_bit4P0
    outportb ( EFIR , 0x2B ) ;          // init pin 89 to WDT
    outportb ( EFDR , al_char1 ) ;
```

Step (2) : CR07_P08

```
        Ponit to LD8.
    outportb ( EFIR , 0x07 ) ;
    outportb ( EFDR , 0x08 ) ;
```

Step (3) : LD8_CR30_bit0P1

```
        Activate LD8
    outportb ( EFIR , 0x30 ) ;
    al_char1 = inportb ( EFDR ) | 0x01 ;  // CR30_bit0P1
    outportb ( EFIR , 0x30 ) ;          // Activate LD8
    outportb ( EFDR , al_char1 ) ;
```

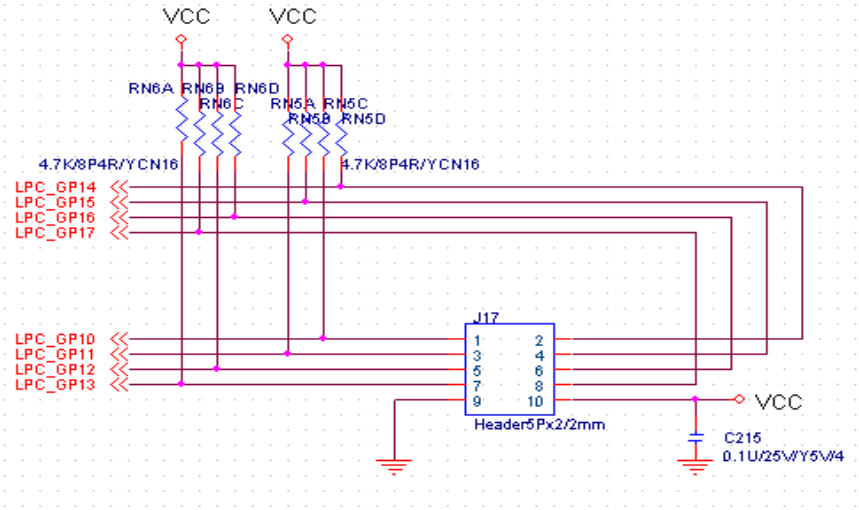
Step (4) : LD8_CRF7_bit[7,6]P[0,0]
Not allow K/B and Mouse's interrupts to reload WDT timer.

```
outportb ( EFIR , 0xF7 ) ;
al_char1 = inportb ( EFDR ) & 0x3F ;  // CRF7_bit[7,6]P[0,0]
outportb ( EFIR , 0xF7 ) ;
outportb ( EFDR , al_char1 ) ;
```

Step (5) : Refresh WDT before it expires.
Once WDT expires, system will be reset.
LD8_CRF5_bit3 : 0 : second unit
1: minute unit
LD8_CRF6: T_{wd} , "Writing 00" means "disable WDT"
1~255 time unit (time unit: second, minute)

Notes:
"CR2B_bit4P0"means " Write 0 to bit4 of Configuration Register 0x2B".

3.6 GPIO



J17 : General Purpose Input/Output Interface Connector

There are 8 GPIO pins on Nano-8044. GP10, GP11, GP12 and GP13 are dedicated GPO pins with 12mA current sink capacity at 5V signal level. The output signals have internal weak pull-high resistor, 4.7K Ohm, to 5V.The GPO signals are driven by W83627DHG GP30 ~ 33 pins.

GP14, GP15, GP16 and GP17 are dedicated GPI pins. They are first inverted and then connected to W83627DHG GP34~37 pins.

Refer to the W83627DHG data sheet to configure both input / output port , SGP30~37, by programming W83627DHG GPIO registers. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 =output, 1 = input). Invert port value by setting inversion register (0 = non -inverse, 1 = inverse). Port value is read / written through data register.
In addition, only GP30, GP31 and GP35 are designed to be able to assert PSOUT# or PME# signal to wake up the system if any of them has any transitions. There are about 16mS debounced circuit inside these 3 GPIOs and it can be disabled by programming respective bit (LD9, CR[FEh] bit 4~6).

3.6.1 Pin assignment

J17 : General Purpose I/O Connector

PIN No.	Signal Description
1	General Purpose Input Port 10
2	General Purpose Output Port 14
3	General Purpose Input Port 11
4	General Purpose Output Port 15
5	General Purpose Input Port 12
6	General Purpose Output Port 16
7	General Purpose Input Port 13
8	General Purpose Output Port 17
9	Ground
10	+5V

Programming Guide :
Must enter extended function mode (Double I/O write 0x87 to EFIR) first , then follow the following steps for accessing GPIO pins . When completion of GPIO access, Exit extended mode (I/O write 0xaa to EFIR).

```
void enter_Superio_CFG(void)
{
outportb(Superio_Addr, 0x87);
outportb(Superio_Addr, 0x87);
}
void exit_Superio_CFG(void)
{
outportb(Superio_Addr, 0xAA);
}
```

(1) Initialize W83627DHG multiplex pins to SGP32~34 function

```
enter_Superio_CFG();
   d = GET_CFG(0x2A);
   d = d & 0xFD;
   Set_CFG(0x2A, d);       //  Pin 89,90 function selected by CR2C
   d = GET_CFG(0x2C);
   d = d & 0x1F;
   Set_CFG(0x2C, d);       // Declare Pin88,89,90 as GPIO function
```

(2) Point to LD9 (for SGP30~37 GPIO port registers) and activate its function

```
Set_CFG(0x07, 0x09);          // Select logic device 09
   d = GET_CFG(0x30);
   d = d | 0x02;
   Set_CFG(0x30, d);             //Enable GPIO3
   Set_CFG(0xFE, 0x77);       //Declare GP30,GP31,GP35's triggle type is level and
//diable input de-bouncer
   Set_CFG(0xF2, 0x00);    //Declare GP30~37 without data inversion
```

(3) LD9_CRF0_PF0 ; Set SGP30~33 as GPO pins and SGP34~37 as GPI pin.

```
Set_CFG(0xF0, 0xF0);    //GP30~33 as output;GP34~GP37 as input
```

LD9_CRF1 ; Data Register for reading/writing data to GPIO pins

```
        ; E.g. if put four jumper caps on J17 pin1-2,3-4,5-6,and 7-8
        ; ( Warning : J17 pin9-10 is not allowed to be short circuit. )
        ; and then Write [1,0,1,0] to bit[3:0] , you can get [1,0,1,0] from
        ; bit[7:4].
Set_CFG(0xF1, 0x0A);    //GP30~33 output H,L,H,L
d = GET_CFG(0xF1) & 0xF0;
```

Chapter 4
BIOS Setup Information

NANO-8044 is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, NANO-8044 communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start-up.

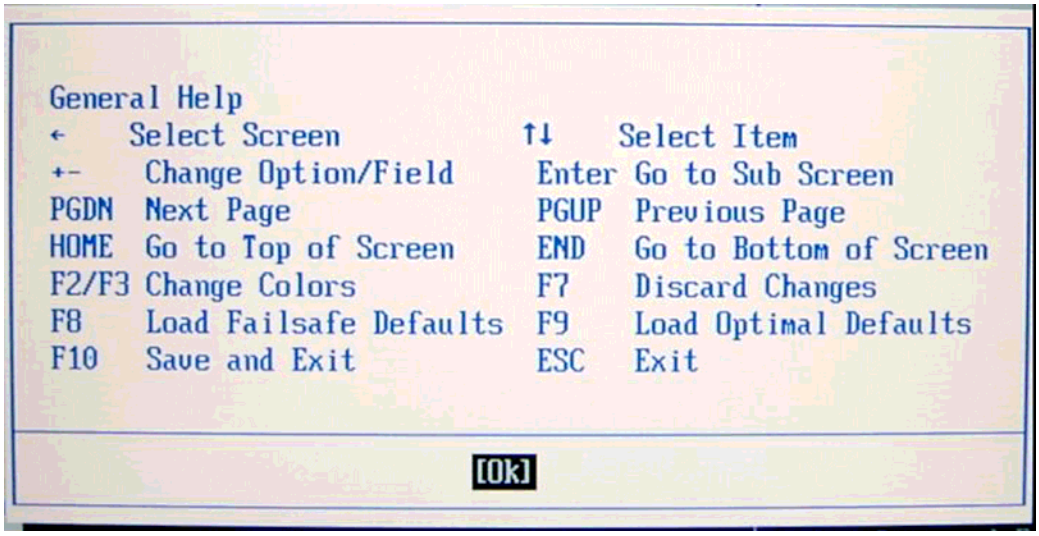
4.1 Entering Setup

Turn on or reboot the computer. When the message, "Hit <DEL> if you want to run SETUP" appears, press <Del> key to enter BIOS setup program.

If the message disappears before you respond, but you still wish to enter Setup, please restart the system to try "COLD START" again by turning it OFF and then ON, or touch the "RESET" button. You may also restart from "WARM START" by pressing <Ctrl>, <Alt>, and <Delete> keys simultaneously. If you do not press the keys at the right time and the system will not boot, an error message will be displayed and you will again be asked to,

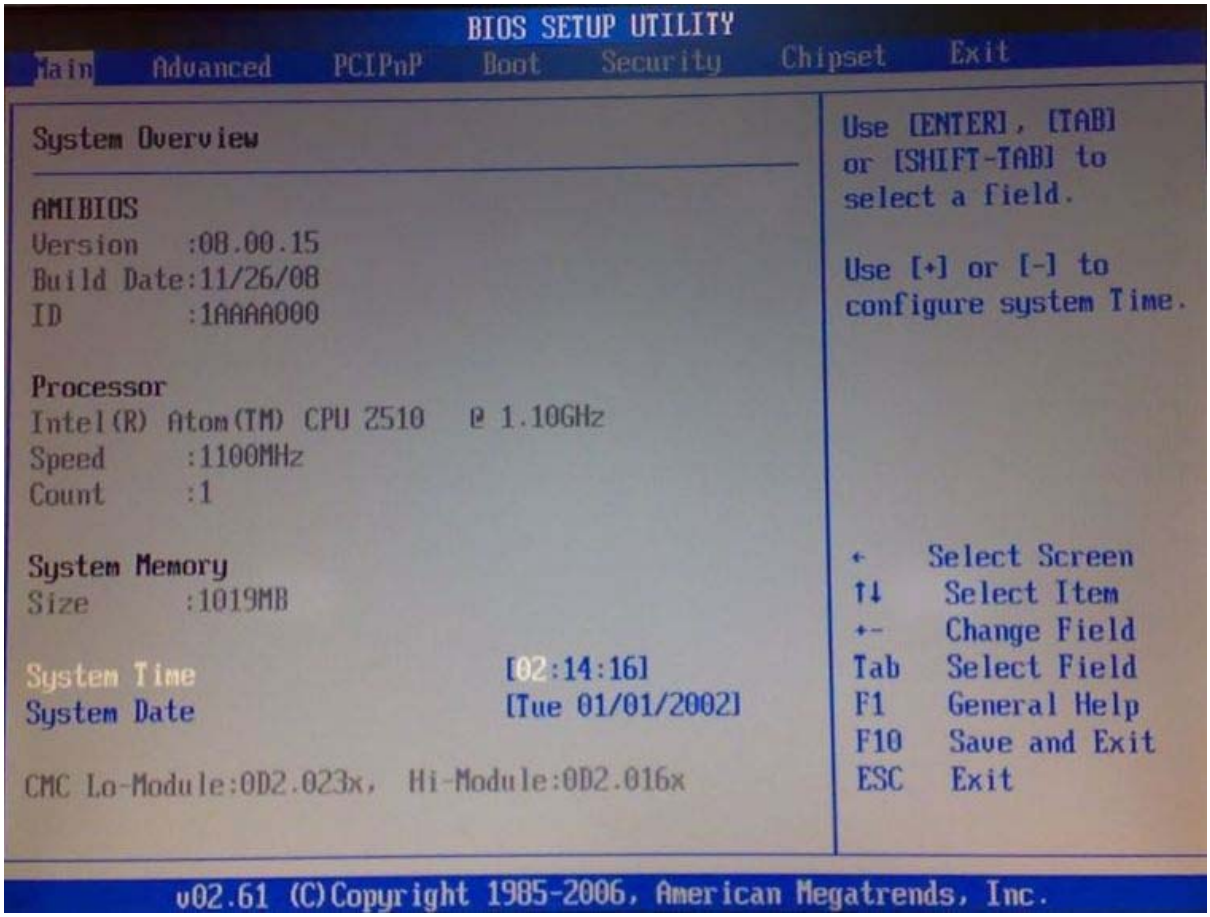
Press <F1> to Run SETUP or Resume

The BIOS setup program provides a General Help screen. You can call up this screen from any menu by simply pressing <F1>. The Help screen lists the appropriate keys to use and the possible selections for the highlighted item. Press <Esc> to exit the Help screen.



4.2 Main Menu

Use this menu for basic system configurations such as time, date etc.



AMI BIOS, Processor, System Memory

These items show the firmware and hardware specifications of your system. Read only.

System Time

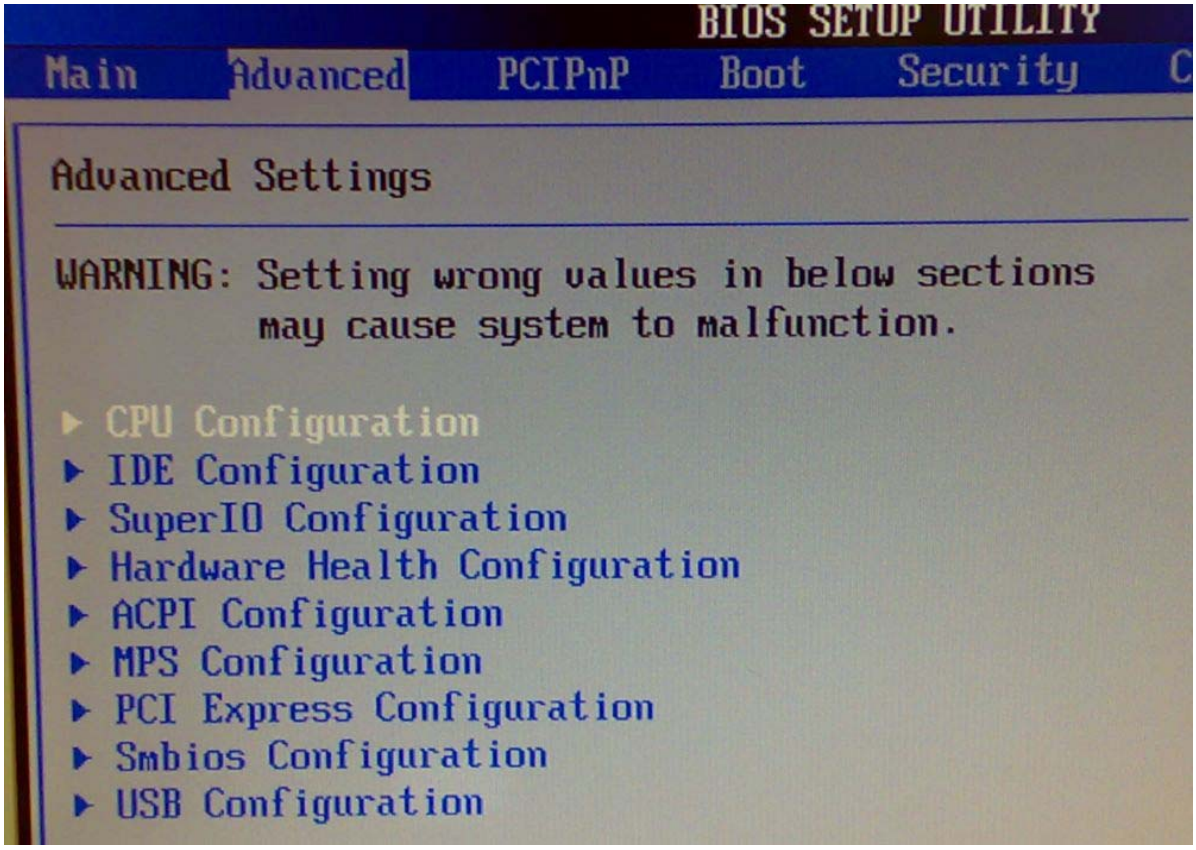
The time format is <Hour> <Minute> <Second>. Use [+] or [−] to configure system Time.

System Date

The date format is <Day>, <Month> <Date> <Year>. Use [+] or [−] to configure system Date.

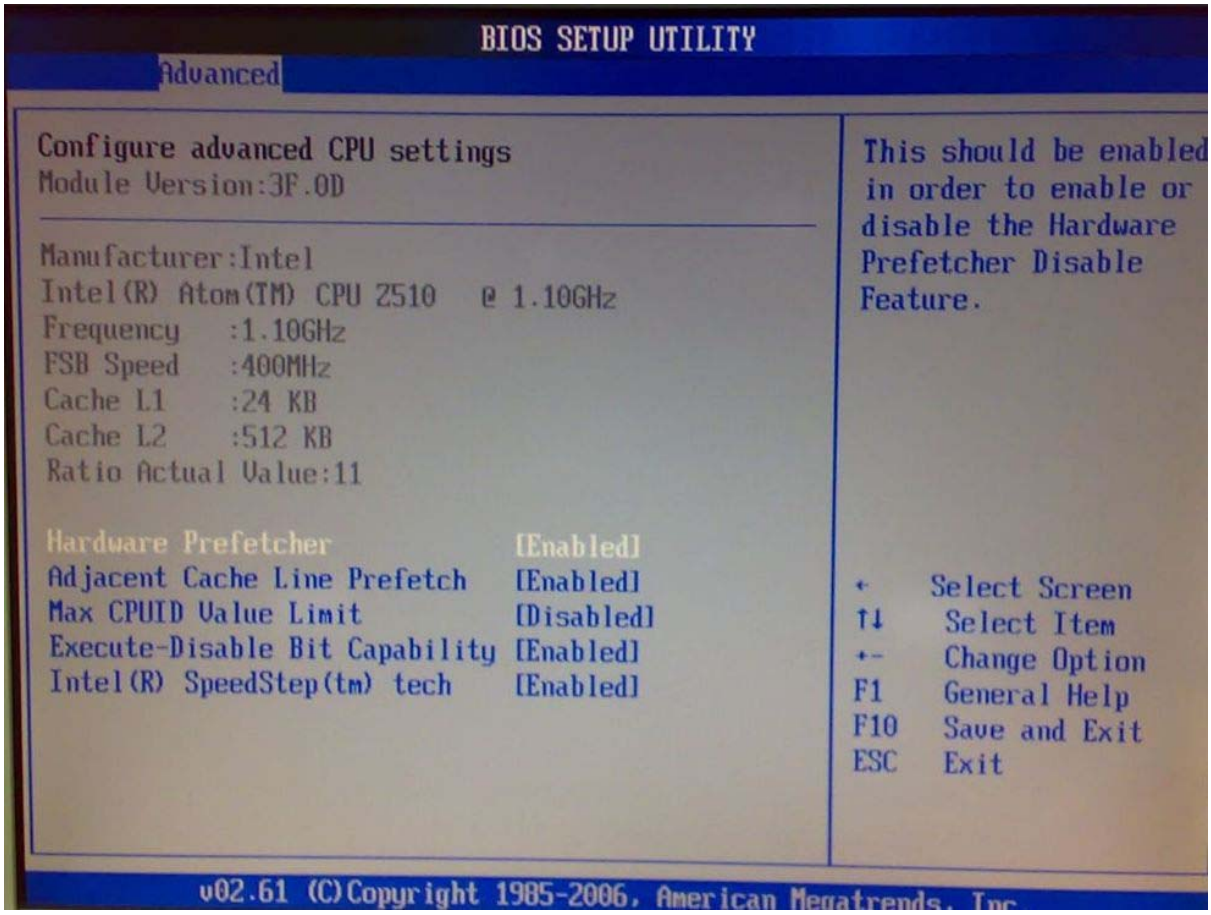
4.3 Advanced

Use this menu to set up the items of special enhanced features.



CPU Configuration

These items show the advanced specifications of your CPU. Read only.



Hardware Prefetcher

This should be enabled in order to enable or disable the Hardware Prefetcher Disable Feature.

The choice: Disabled, Enabled.

Adjacent Cache Line Prefetch

This should be enabled in order to enable or disable the Adjacent Cache Line Prefetch Disable Feature.

The choice: Disabled, Enabled.

Max CPUID Value Limit

Disable for Windows XP.

Execute-Disable Bit Capability

When disable, force the XD feature flag to always return 0.

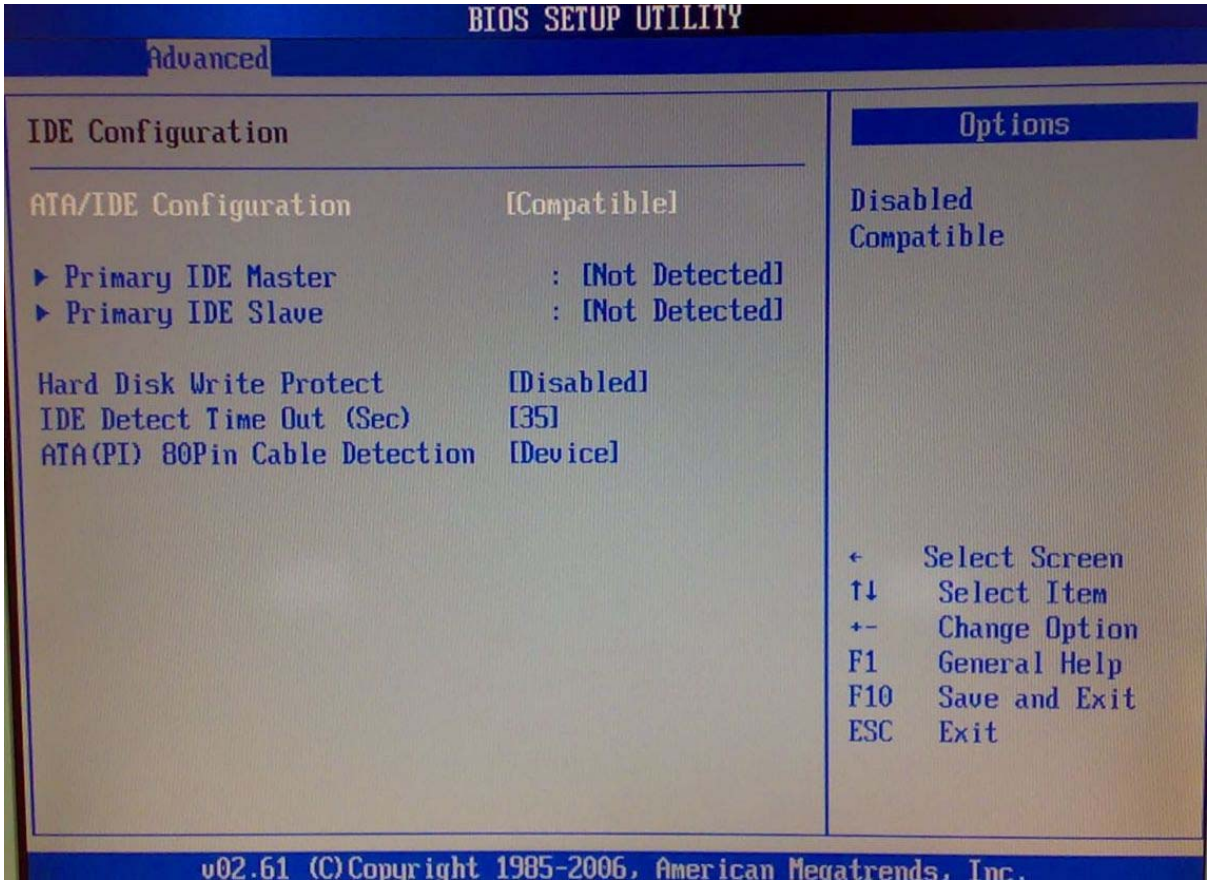
The choice: Disabled, Enabled.

Intel(R) SpeedSetup(™) tech

Disable: Disable GV3
Enable: Enable GV3

IDE Configuration

The IDE Configuration the IDE devices, such as hard disk drive or CD-ROM drive. It uses a separate sub menu to configure each hard disk drive (Master and Slave).

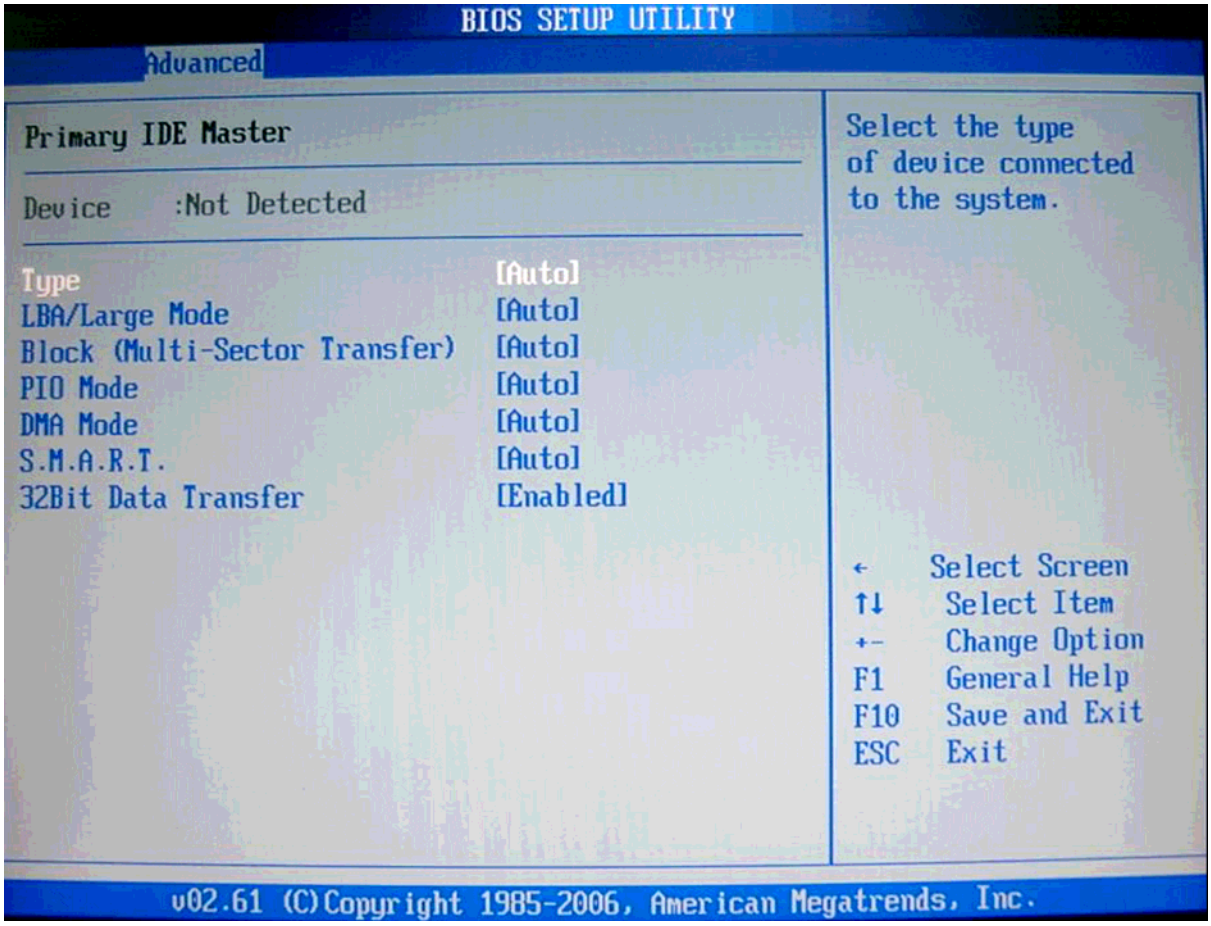


ATA/IDE Configuration

The choice: Disabled, Compatible.

Primary IDE Master/Slave

While entering setup, BIOS auto detects the presence of IDE devices. This displays shows the status of auto detection of IDE devices.



[Type] Press PgUp/<+> or PgDn/<—> to select [Manual], [None] or [Auto] type. You can use [Manual] to define your own drive type manually.

[LBA/Large Mode] Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads and Sectors.

[Block (Multi-Sector Transfer)] Any selection except Disabled determines the number of sectors transferred per block.

[PIO Mode] Indicates the type of PIO (Programmed Input/Output).

[DMA Mode] Indicates the type of Ultra DMA.

[S.M.A.R.T.] This allows you to activate the S.M.A.R.T. (Self-Monitoring Analysis & Reporting Technology) capability for the hard disks. S. M.A.R.T is a utility that monitors your disk status to predict hard disk failure. This gives you an opportunity to move data from a hard disk that is going to fail to a safe place before the hard disk becomes offline.

[32 Bit Data Transfer] Enable/Disable 32-bit Data Transfer.

Hard Disk Write Protect

Disabled/Enabled device write protection, this will be effective only if device is accessed through BIOS.

The choice: Disabled, Enabled.

IDE Detect Time Out (Sec)

Select the time out value for detecting ATA/ATAPI device (s).

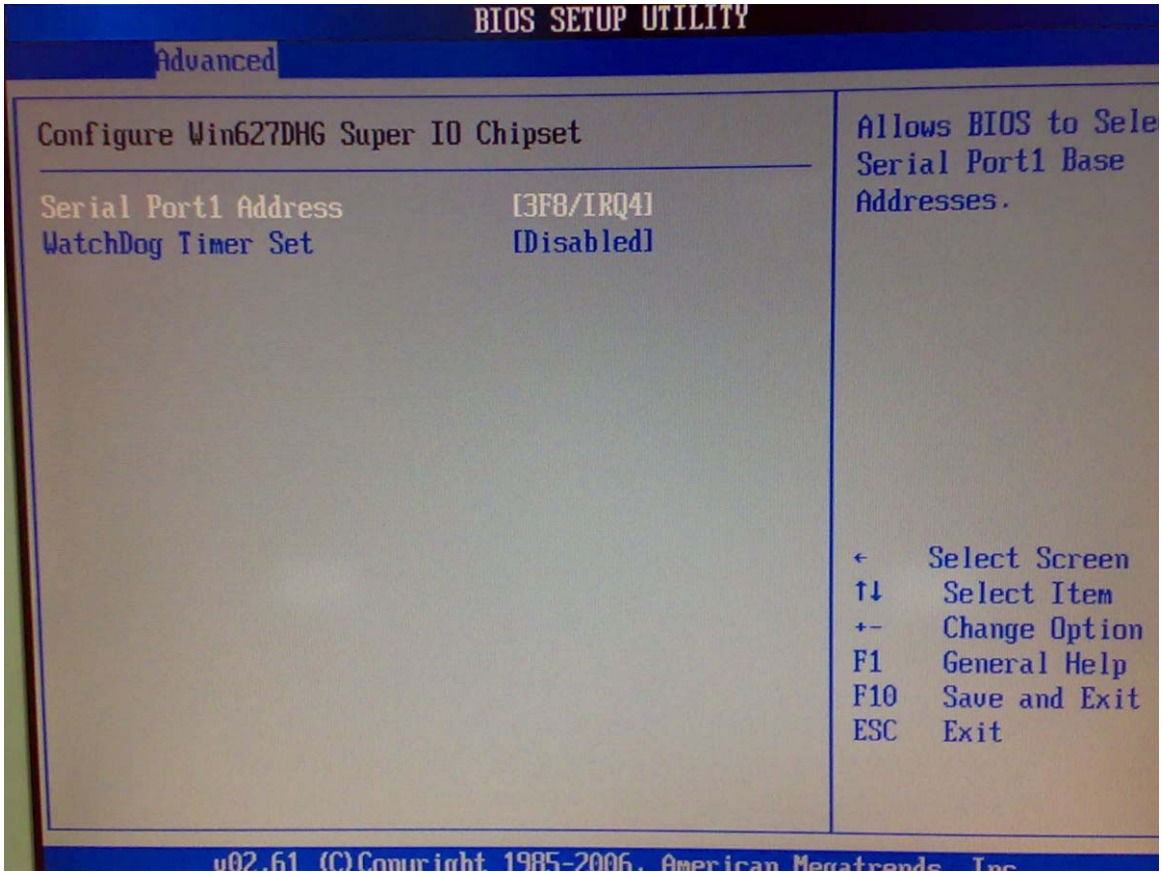
The choice: 0, 5, 10, 15, 20, 25, 30, 35.

ATA (PI) 80Pin Cable Detection

Select the mechanism for detecting 80Pin ATA (PI) cable.

The choice: Host & Device, Host, Device.

Super IO Configuration



Serial Port 1 Address

Allows BIOS Select Serial Port1 Base Addresses.

The choice: Disabled, 3F8/IRQ4.

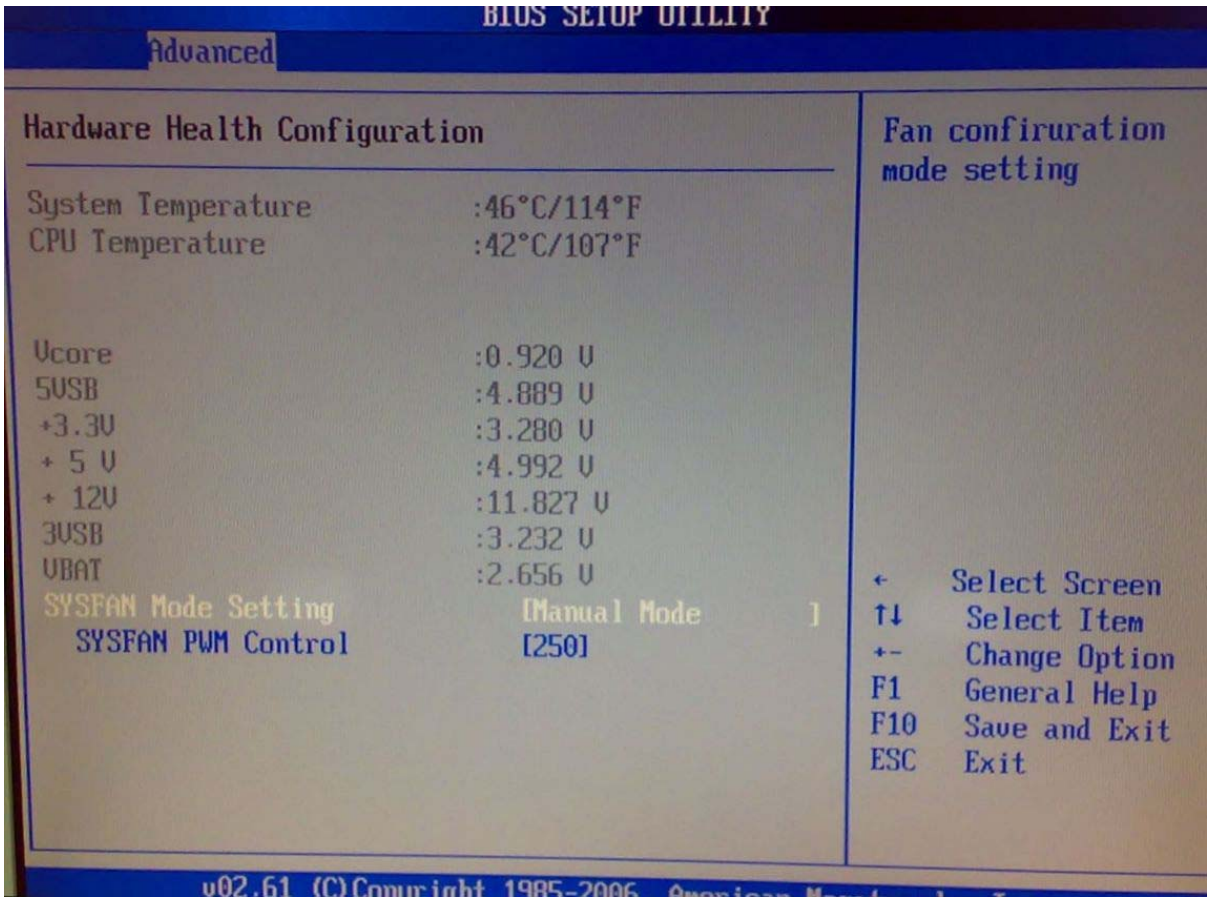
Watch Dog Timer Set

This BIOS testing option is able to reset the system according to the selected table.

The choice: Disabled, 10, 20, 30, 40 Sec, 1Min, 2Min, 4Min.

Hardware Health Configuration

Configuration / monitor the Hardware Health.



SYSFAN Mode Setting

Fan configuration mode setting.

The choice: Manual Mode, Thermal Cruise Mode.

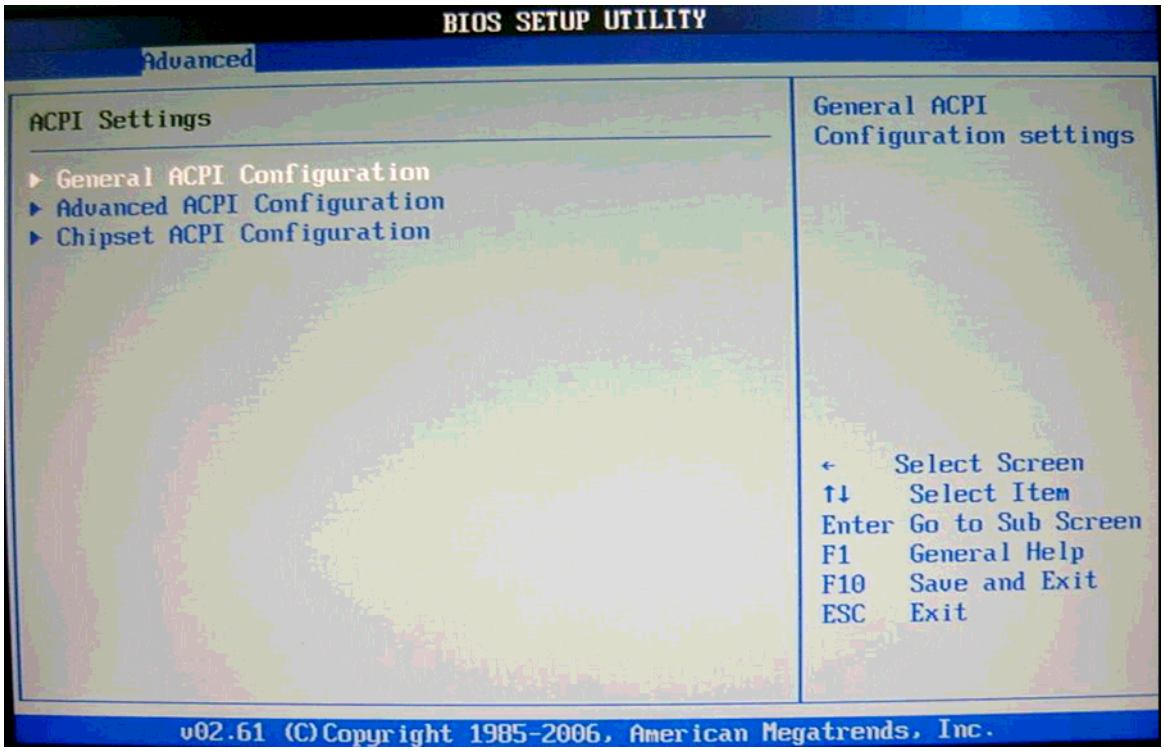
SYSFAN PWM Control

The PWM duty cycle control.

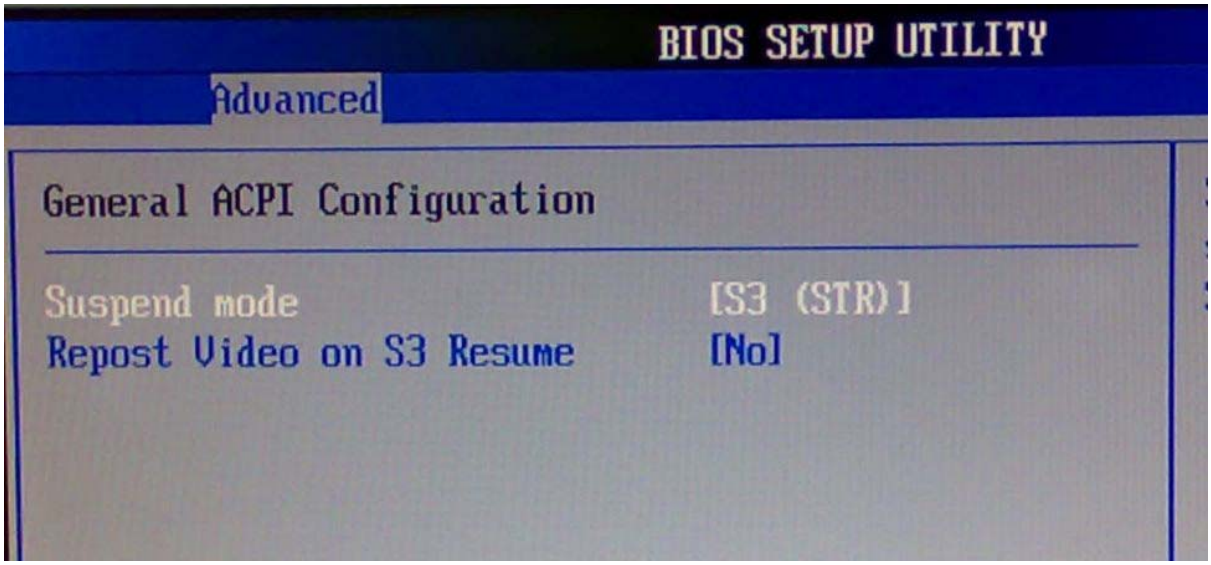
The choice: 0 to 255.

ACPI Configuration

Select for Advanced ACPI Configuration.



General ACPI Configuration



Suspend mode

This item specifies the power saving modes for ACPI function. If your operating system supports ACPI, you can choose to enter the Standby mode in S3 (STR) function through the setting of this field. Option is:

[S3 (STR)] The S3 sleep mode is a lower power state where the information of system configuration and open applications/ files is saved to main memory that remains powered while most other hardware components turn off to save energy. The information stored in memory will be used to restore the system when a "wake up" event occurs.

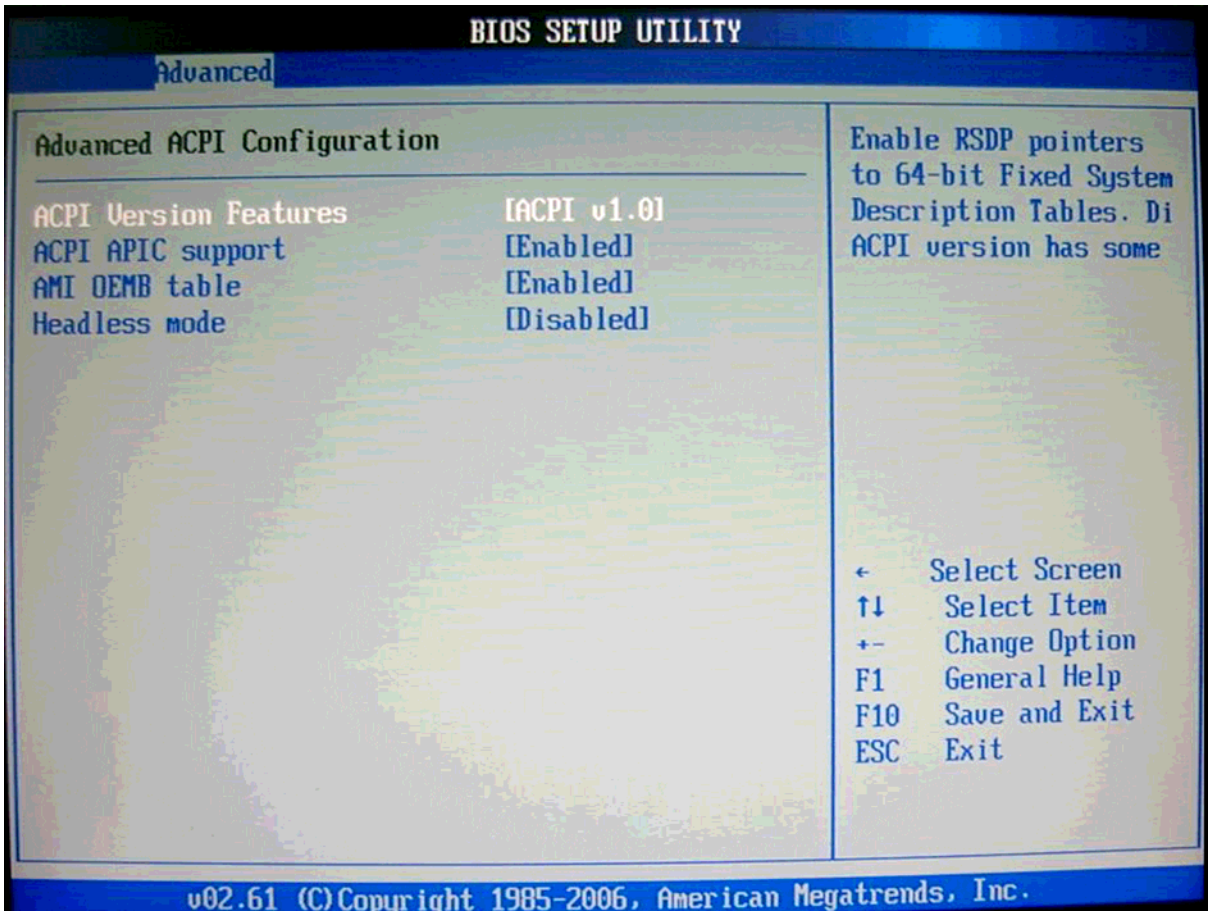
Repost Video on S3 Resume

Determines whether to invoke VGA BIOS post on S3/STR resume.

The choice: No, Yes

Advanced ACPI Configuration

Advanced ACPI Configuration settings, Use this section to configure additional ACPI options.



ACPI Version Features

Enable RSDP pointers to 64-bit Fixed System Description Tables.

The choice: ACPI v1.0 / ACPI v2.0 / ACPI v3.0.

ACPI APIC support

Include ACPI APIC table pointer to RSDT pointer list.

The choice: Disabled, Enabled.

AMI OEMB table

Include OEMB table pointer to R(X) SDT pointer list.

The choice: Disabled, Enabled.

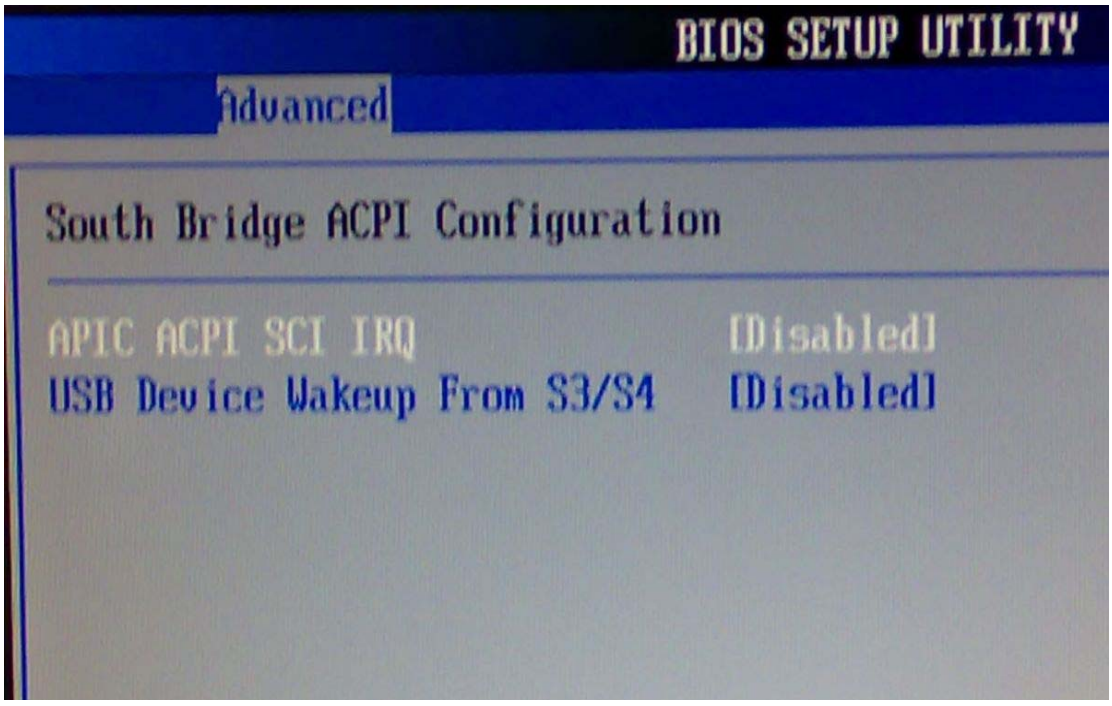
Headless mode

Enable / Disable Headless operation mode through ACPI.

The choice: Disabled, Enabled.

Chipset ACPI Configuration

Chipset ACPI related Configuration settings, Use this section to configure additional ACPI options.



APIC ACPI SCI IRQ

Enable / Disable APIC ACPI SCI IRQ.

The choice: Disabled, Enabled.

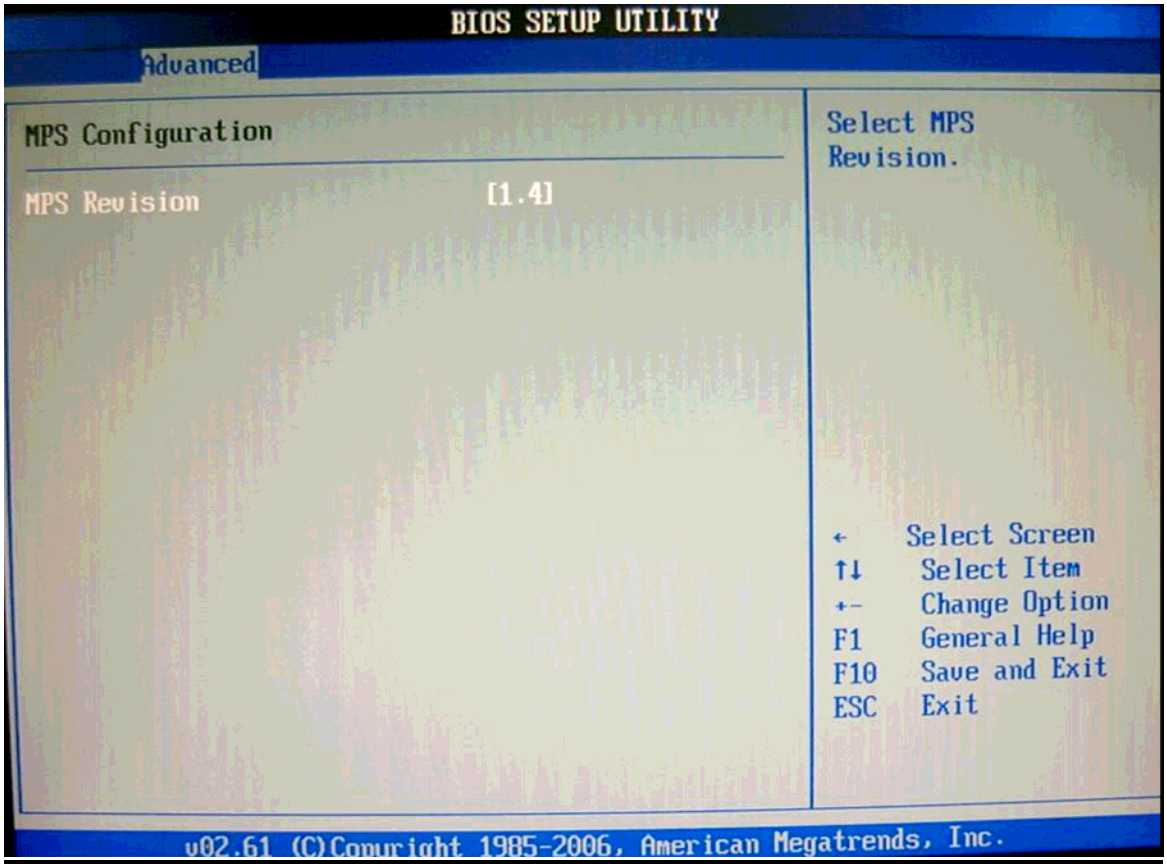
USB Device Wakeup From S3/S4

Enable / Disable USB device Wake from S3/S4 mode.

The choice: Disabled, Enabled.

MPS Configuration

Configure the Multi-Processor Table.



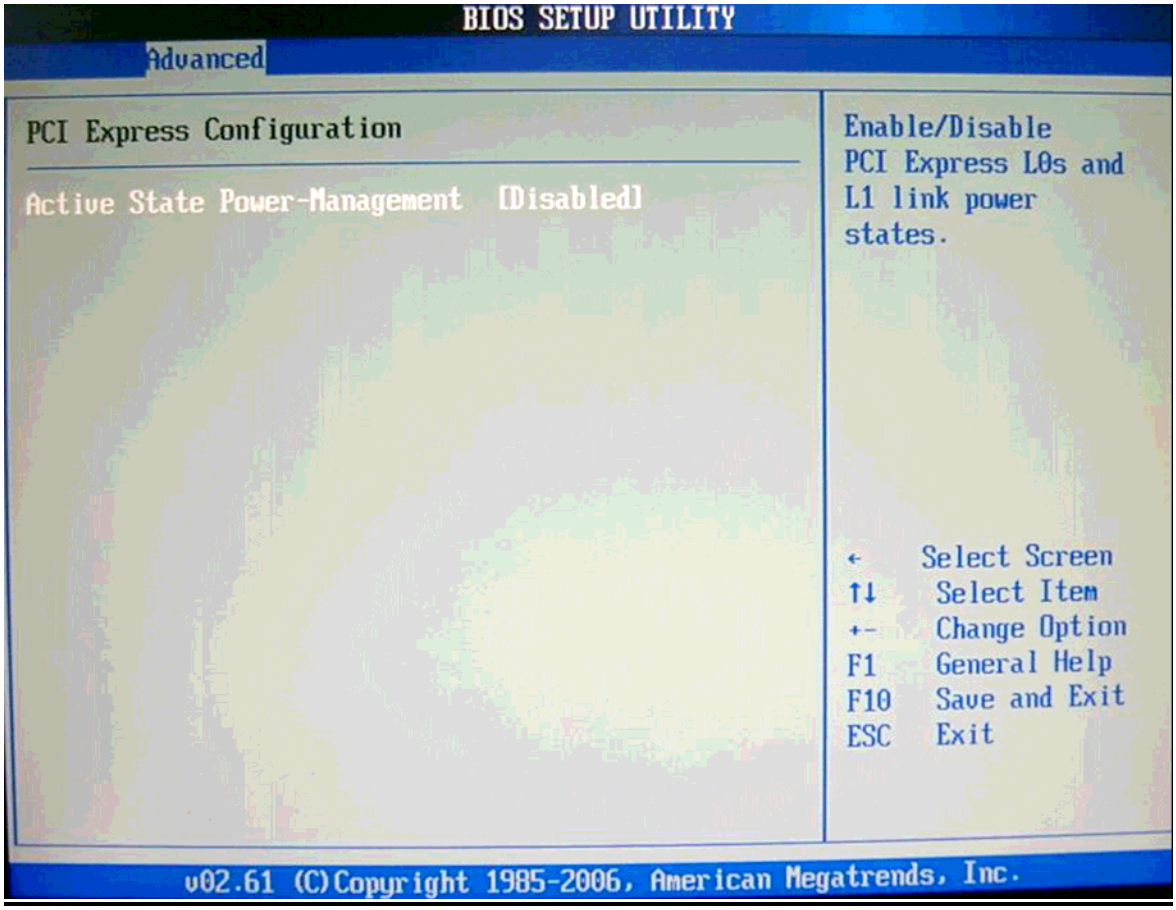
MPS Revision

This field allows you to select which MPS (Multi-Processor Specification) version to be used for the operating system. You need to select the MPS version supported by your operating system. To find out which version to use, consult the vendor of your operating system.

The choice: 1.1, 1.4.

PCI Express Configuration

Configure PCI Express Support.



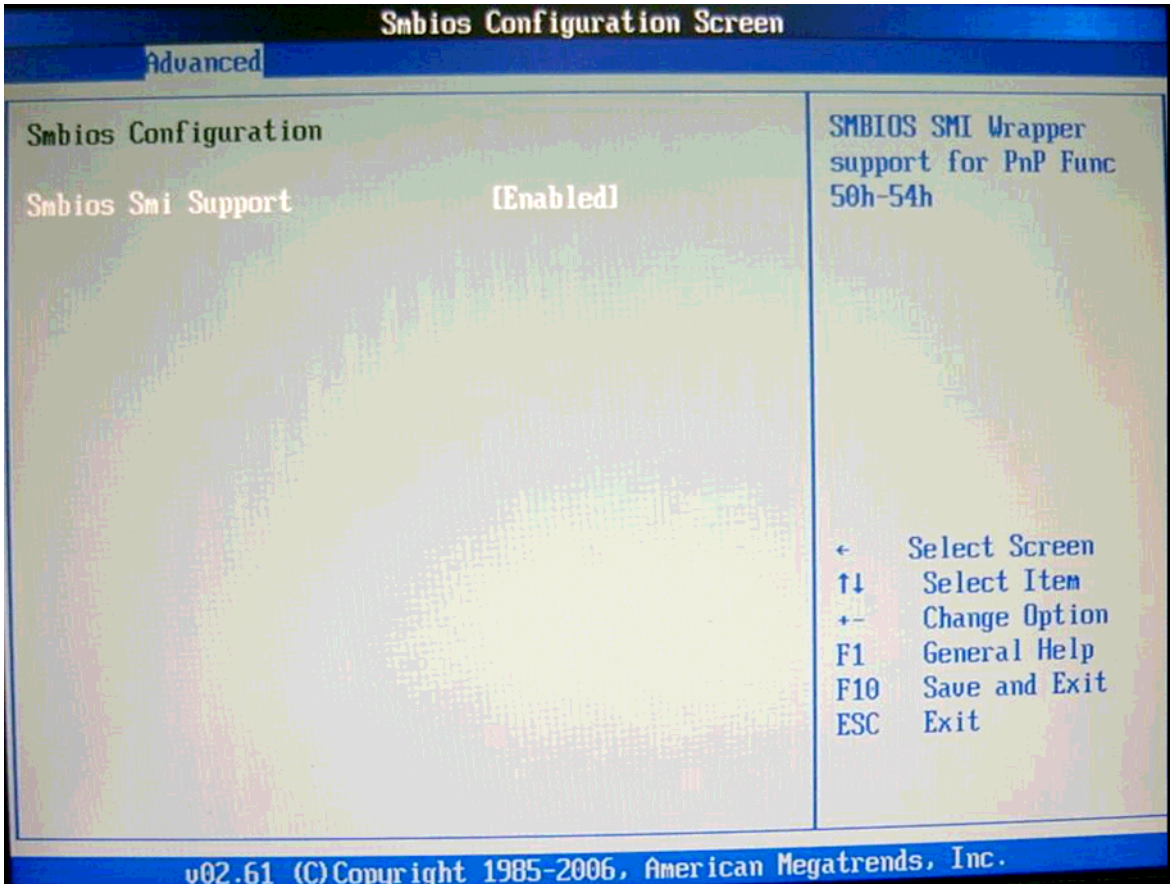
Active State Power-Management

PCI Express L0s and L1 link power states.

The choice: Disabled, Enabled.

Smbios Configuration

SMBIOS Configuration Menu.

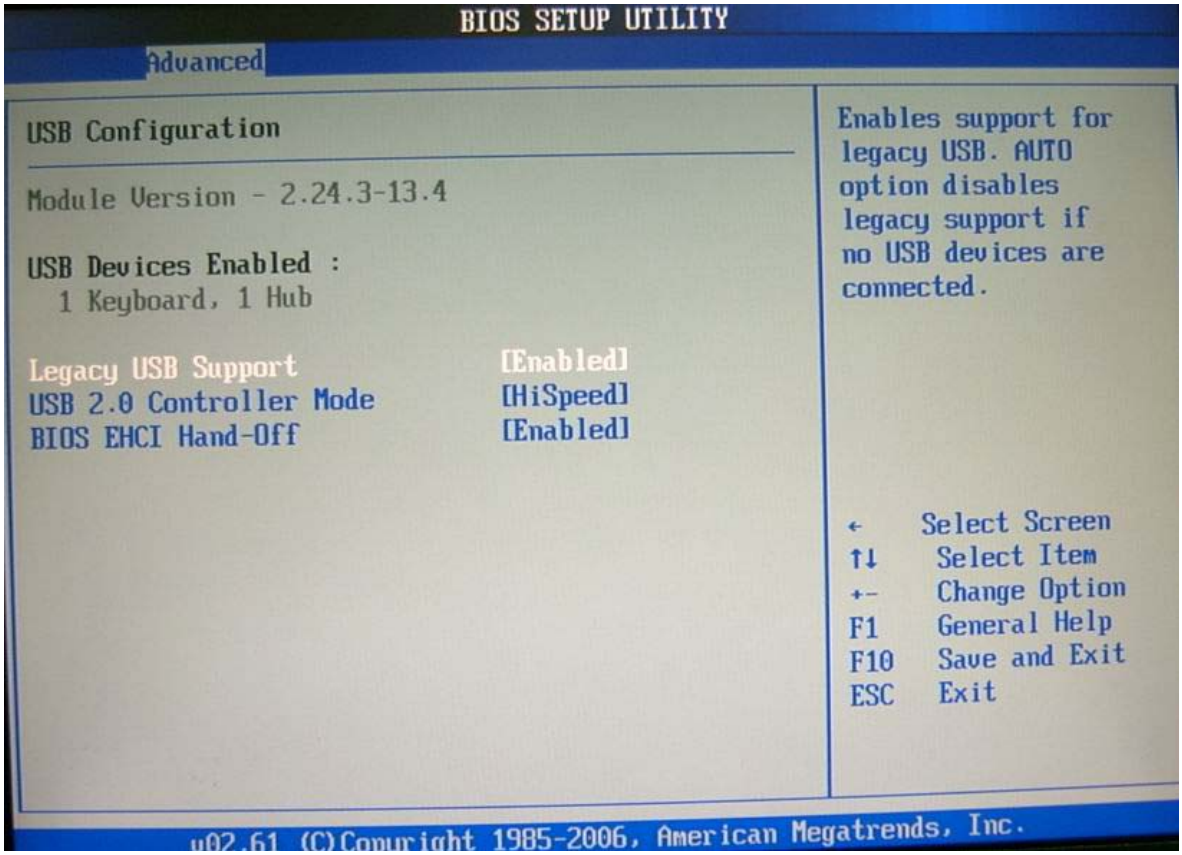


Smbios Smi Support

SMBIOS SMI Wrapper supports for PnP Func 50h-54h.

The choice: Disabled, Enabled.

USB Configuration



Legacy USB Support

Set to [Enabled] if you need to use any USB 1.1/2.0 device in the operating system that does not support or have any USB 1.1/2.0 driver installed, such as DOS and SCO Unix.

The choice: Disabled, Enabled, Auto.

USB 2.0 Controller Mode

This setting specifies the operation mode of the onboard USB 2.0 controller.

The choice: FullSpeed, HiSpeed.

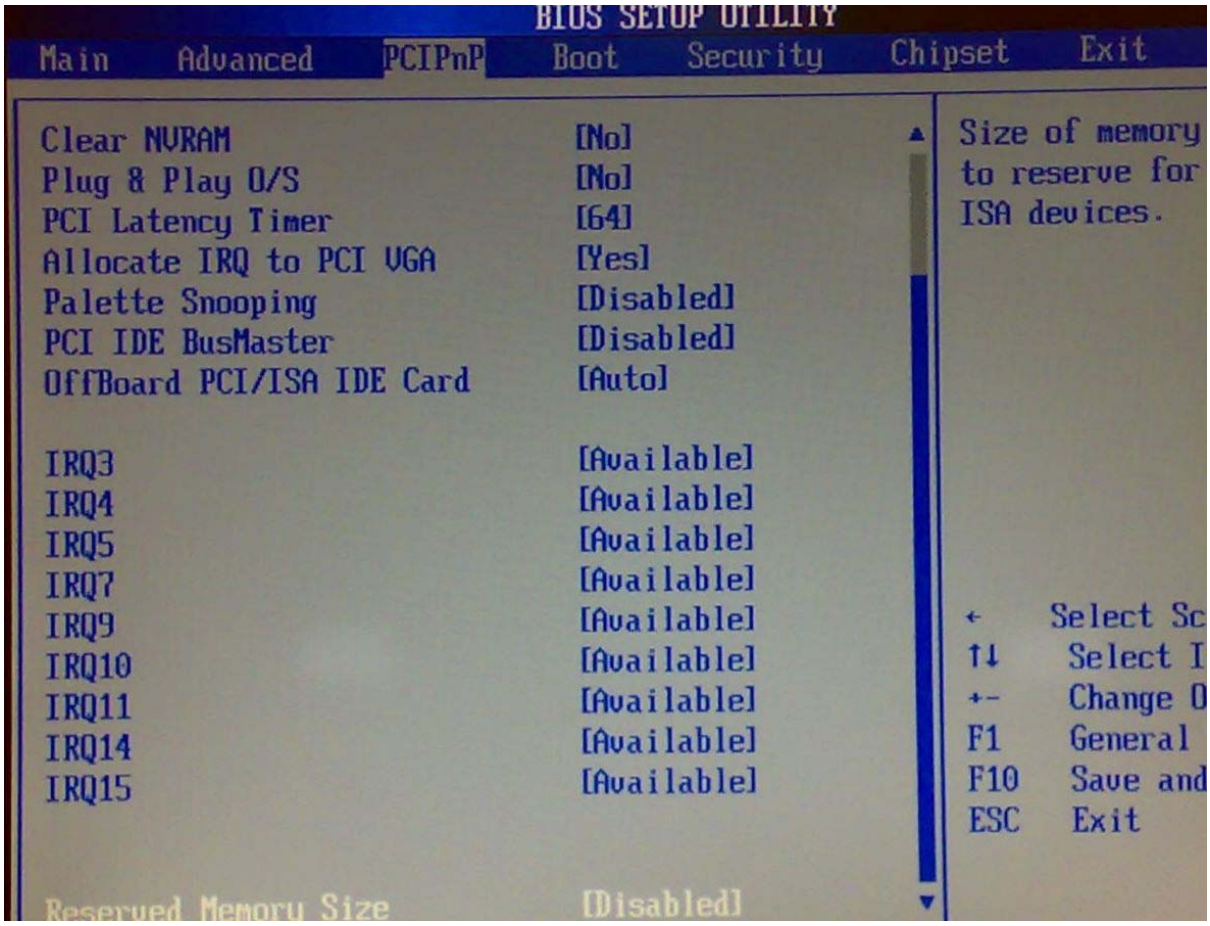
BIOS EHCI Hand-Off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.

The choice: Disabled, Enabled.

4.4 PCIPnP

Advanced PCI/PnP setting wrong values in below sections may cause system to malfunction.



Clear NVRAM

Clear NVRAM during System Boot.

The choice: No, Yes.

Plug & Play O/S

No: lets the BIOS configure all the devices in the system.
Yes: lets the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.

The choice: No, Yes.

PCI Latency Timer

Select value in units of PCI clocks for PCI device latency timer register.

The choice: 32, 64, 96, 128, 160, 192, 224, 248.

Allocate IRQ to PCI VGA

Yes: Assigns IRQ to PCI VGA card if card requests an IRQ.
No: Does not assign IRQ to PCI VGA card even if card requests an IRQ.

The choice: No, Yes.

Palette Snooping

Enabled: informs the PCI devices that an ISA graphics device is installed in the system so the card will function correctly.

The choice: Disabled, Enabled.

PCI IDE BusMaster

Enabled: Uses PCI bus mastering for reading / writing to IDE drives.

The choice: Disabled, Enabled.

OffBoard PCI/ISA IDE Card

Some PCI IDE cards may require this to be set to the PCI slot number that is holding the card. AUTO: Works for most PCI IDE cards.

The choice: Auto, PCI Slot1, PCI Slot2, PCI Slot3, PCI Slot4, PCI Slot5, PCI Slot6.

IRQ 3 / IRQ 4 / IRQ5 / IRQ7 / IRQ 9 / IRQ 10 / IRQ 11 / IRQ 14 / IRQ 15

Available: Specified IRQ is available to be used by PCI/PnP devices.
Reserved: Specified IRQ is reserved for used by Legacy ISA devices.

The choice: Available, Reserved.

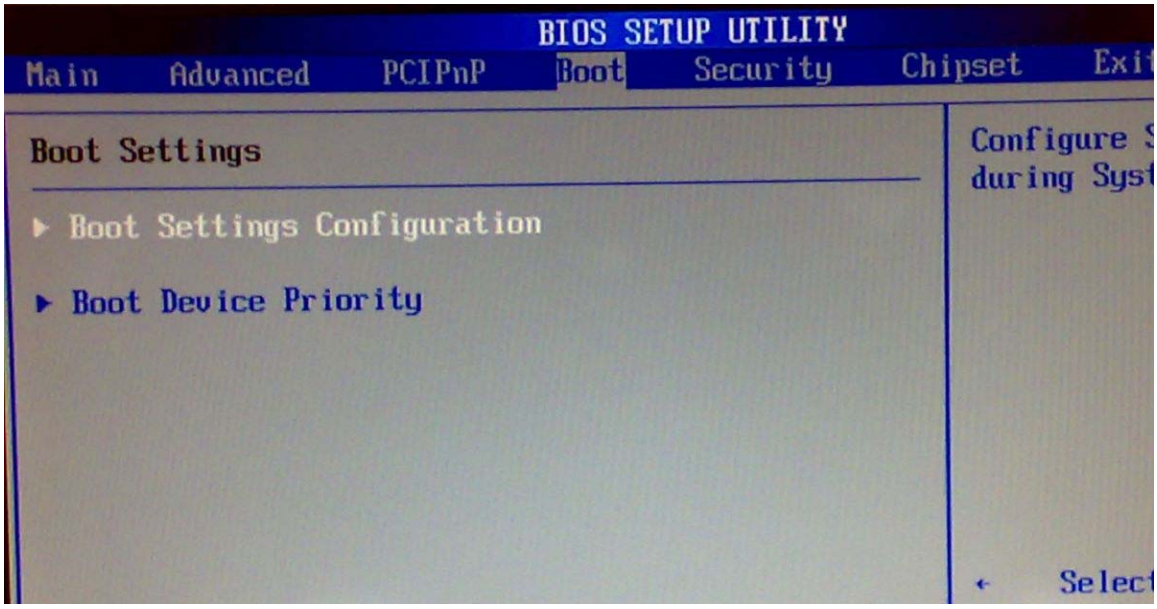
Reserved Memory Size

Select Size of memory block to reserve for legacy ISA devices.

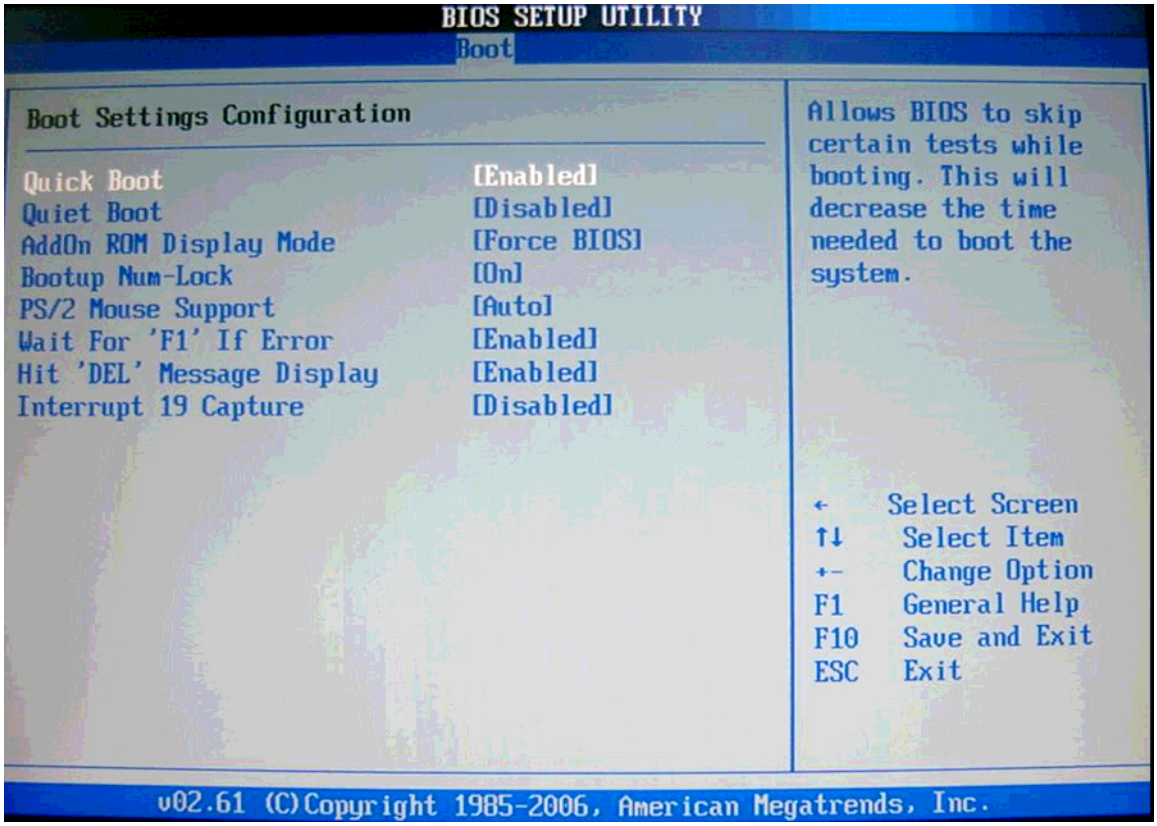
The choice: Disabled, 16K, 32K, 64K.

4.5 Boot

Use this menu to specify the priority of boot devices.



Boot Settings Configuration



Quick Boot

Enabling this setting will cause the BIOS power-on self test routine to skip some of its tests during boot up for faster system boot.

The choice: Disabled, Enabled.

Quiet Boot

This BIOS feature determines if the BIOS should hide the normal POST messages with the motherboard or system manufacturer's full-screen logo. When it is enabled, the BIOS will display the full-screen logo during the boot-up sequence, hiding normal POST messages.
When it is disabled, the BIOS will display the normal POST messages, instead of the full-screen logo.

Please note that enabling this BIOS feature often adds 2-3 seconds of delay to the booting sequence. This delay ensures that the logo is displayed for a sufficient amount of time. Therefore, it is recommended that you disable this BIOS feature for a faster boot-up time.

The choice: Disabled, Enabled.

AddOn ROM Display Mode

This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

The choice: Force BIOS, Keep Current.

Bootup Num-Lock

This setting is to set the Num Lock status when the system is powered on.
Setting to [On] will turn on the Num Lock key when the system is powered on.
Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

The choice: Off, On.

PS/2 Mouse support

Select [Enabled] if you need to use a PS/2-interfaced mouse in the operating system.

The choice: Disabled, Enabled, Auto.

Wait For 'F1' If Error

When this setting is set to [Enabled] and the boot sequence encounters an error, it asks you to press F1. If disabled, the system continues to boot without waiting for you to press any keys.

The choice: Disabled, Enabled.

Hit 'DEL' Message Display

Set this option to [Disabled] to prevent the message as follows:

Hit Del if you want to run setup
It will prevent the message from appearing on the first BIOS screen when the computer boots. Set it to [Enabled] when you want to run the BIOS Setup Utility.

The choice: Disabled, Enabled.

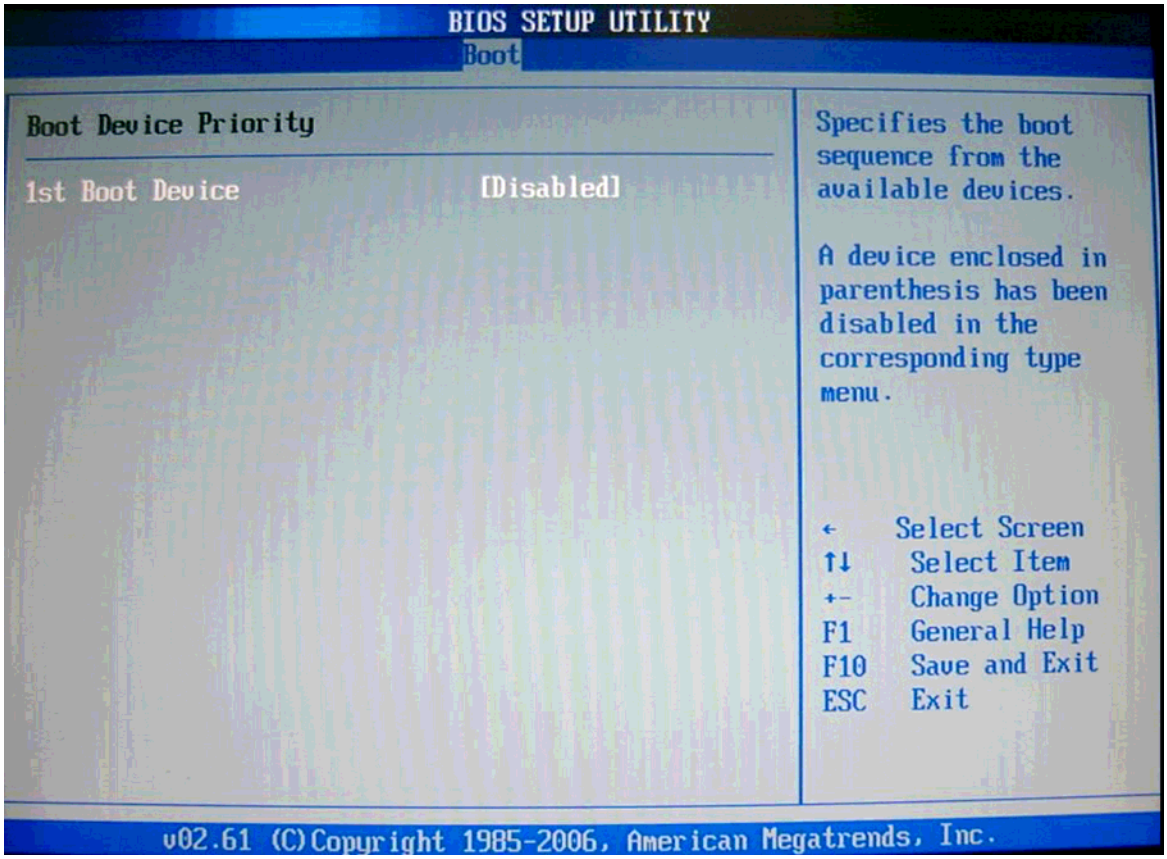
Interrupt 19 Capture

Interrupt 19 is the software interrupt that handles the boot disk function. When enabled, this BIOS feature allows the ROM BIOS of these host adaptors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's ROM setup utility, if one is available.

When disabled, the ROM BIOS of these host adaptors will not be able to "capture" Interrupt 19. Therefore, you will not be able to boot operating systems from any bootable disks attached to these host adaptors. Nor will you be able to gain access to their ROM setup utilities.

The choice: Disabled, Enabled.

Boot Device Priority



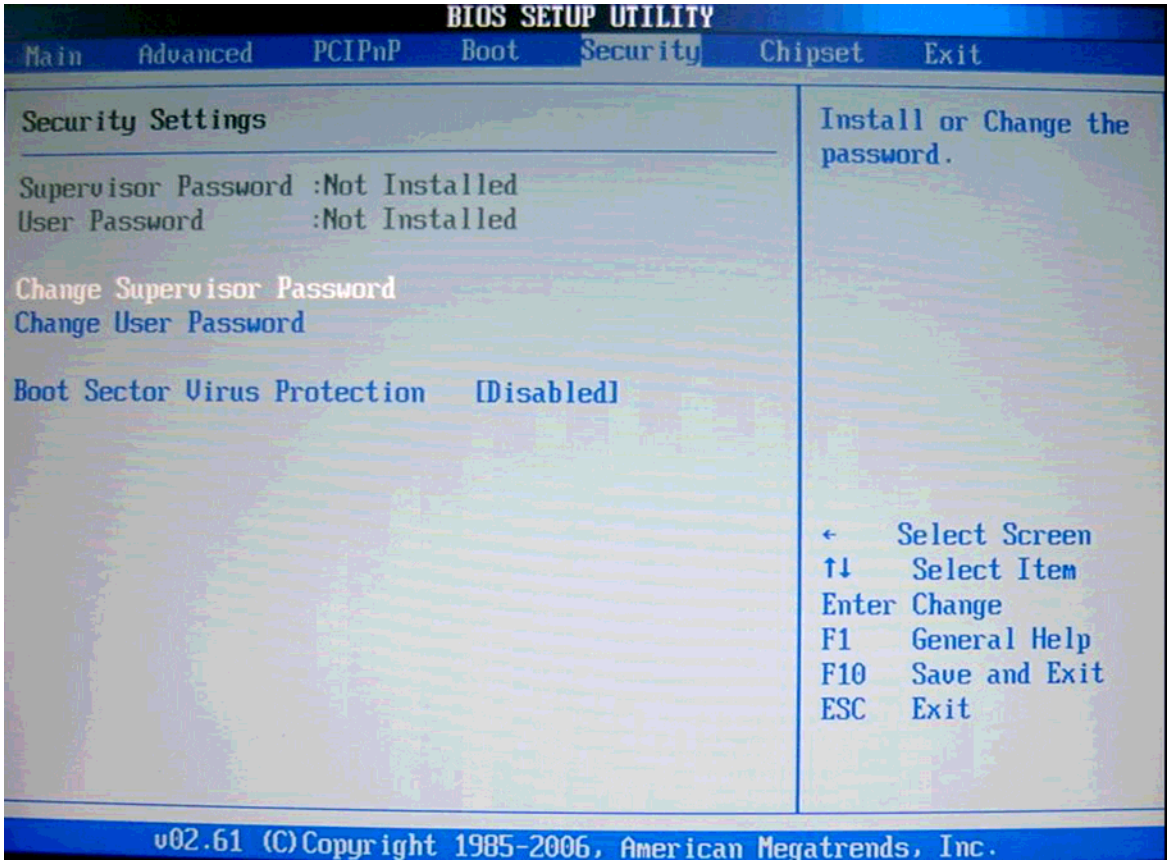
1st Boot Device

The items allow you to set the sequence of boot devices where BIOS attempts to load the disk operating system. First press <Enter> to enter the sub-menu. Then you may use the arrow keys (↑↓) to select the desired device, then press <+>, <—> or <PageUp>, <PageDown> key to move it up/down in the priority list.

The choice: (Network:IBA GE Slot 0200 v1324), Disabled.

4.6 Security

Use this menu to set supervisor and user passwords.



Supervisor Password / Change Supervisor Password

Supervisor Password controls access to the BIOS Setup utility. These settings allow you to set or change the supervisor password.

User Password / Change User Password

User Password controls access to the system at boot. These settings allow you to set or change the user password.

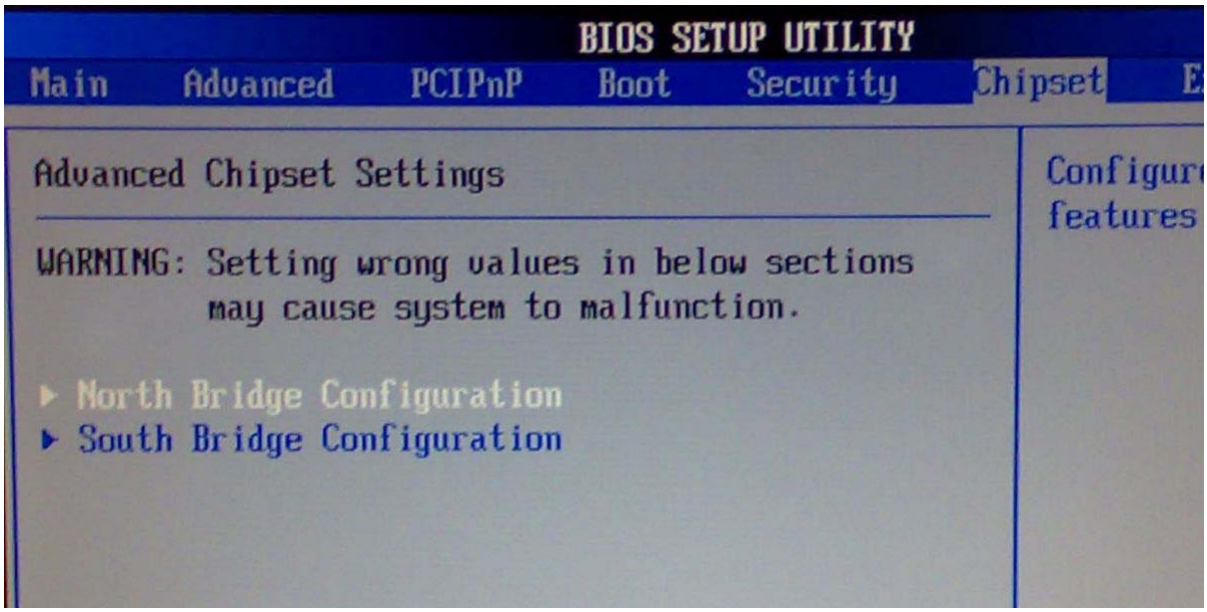
Boot Sector Virus Protection

Boot Sector Virus Protection.

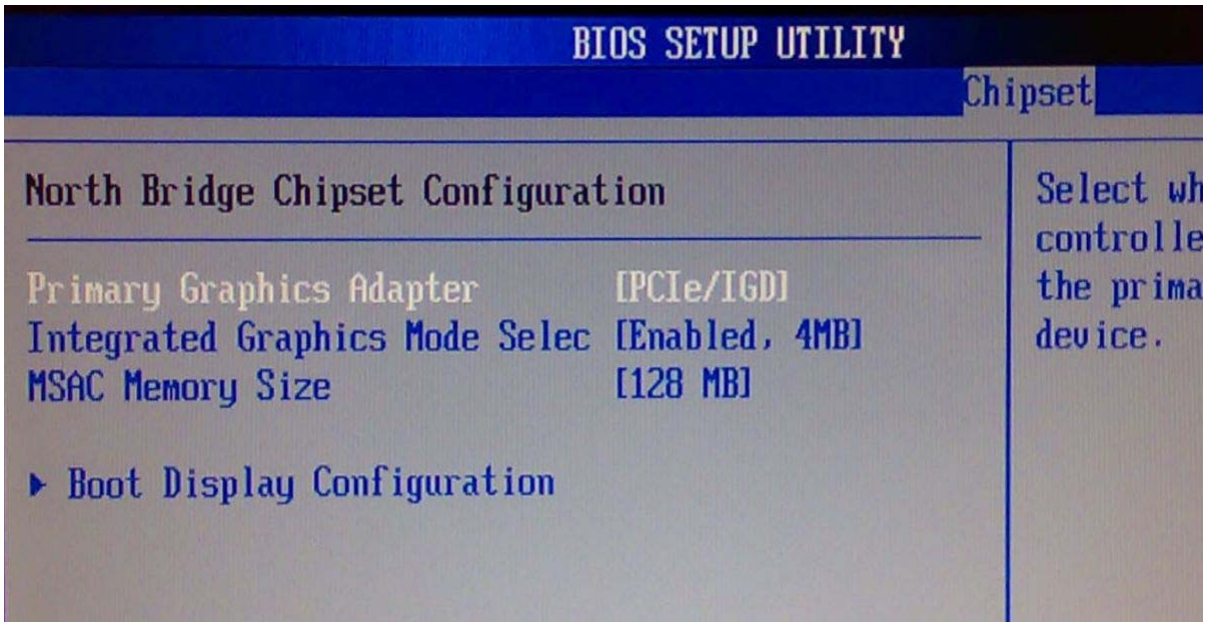
The choice: Disabled, Enabled.

4.7 Chipset

This menu controls the advanced features of the onboard Northbridge and Southbridge.



North Bridge Chipset Configuration



Primary Graphics Adapter

Select which graphics controller to use as the primary boot device.

The choice: IGD, PCIe/IGD.

Integrated Graphics Mode Selec

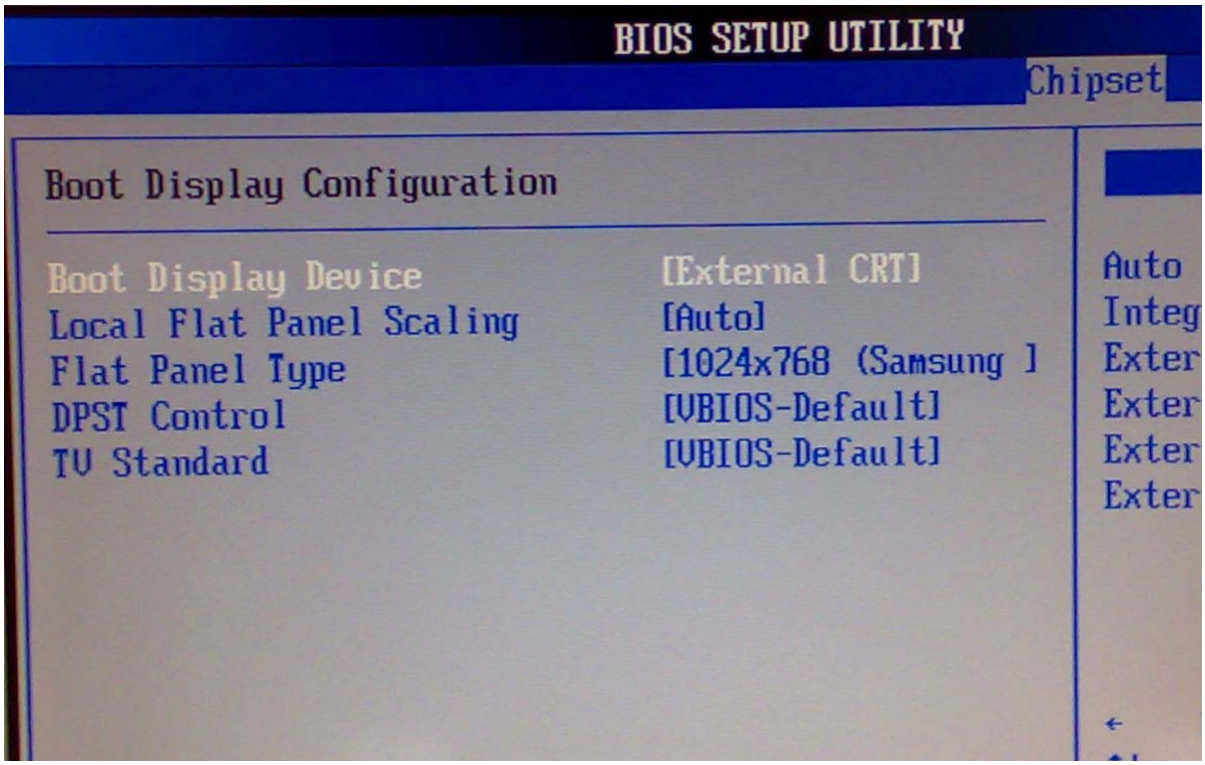
Select the amount of system memory used by the internal graphics device.

The choice: Disabled, Enabled, 1MB, Enabled, 4MB, Enabled, 8MB.

MSAC Memory Size

The choice: 128MB, 256MB.

Boot Display Configuration



Boot Display Device

The choice: Auto, Integrated LVDS, External DVI/HDMI, External TV, External CRT External LVDS.

Local Flat Panel Scaling

The choice: Auto, Forced Scaling, Disabled.

Flat Panel Type

The choice: 640x480 (generic), 800x600 (generic), 1024x768 (generic), 640x480 (NEC 8.4”), 800x600 (NEC 9”), 1024x600 (TMD 5.61”), 1024x600 (Samsung 4.8”), 1024x768 (Samsung 15”), 1280x768 (Sharp 7.2”), 1280x800 (Samsung 15.4”), 1366x768 (TMD 11.1”).

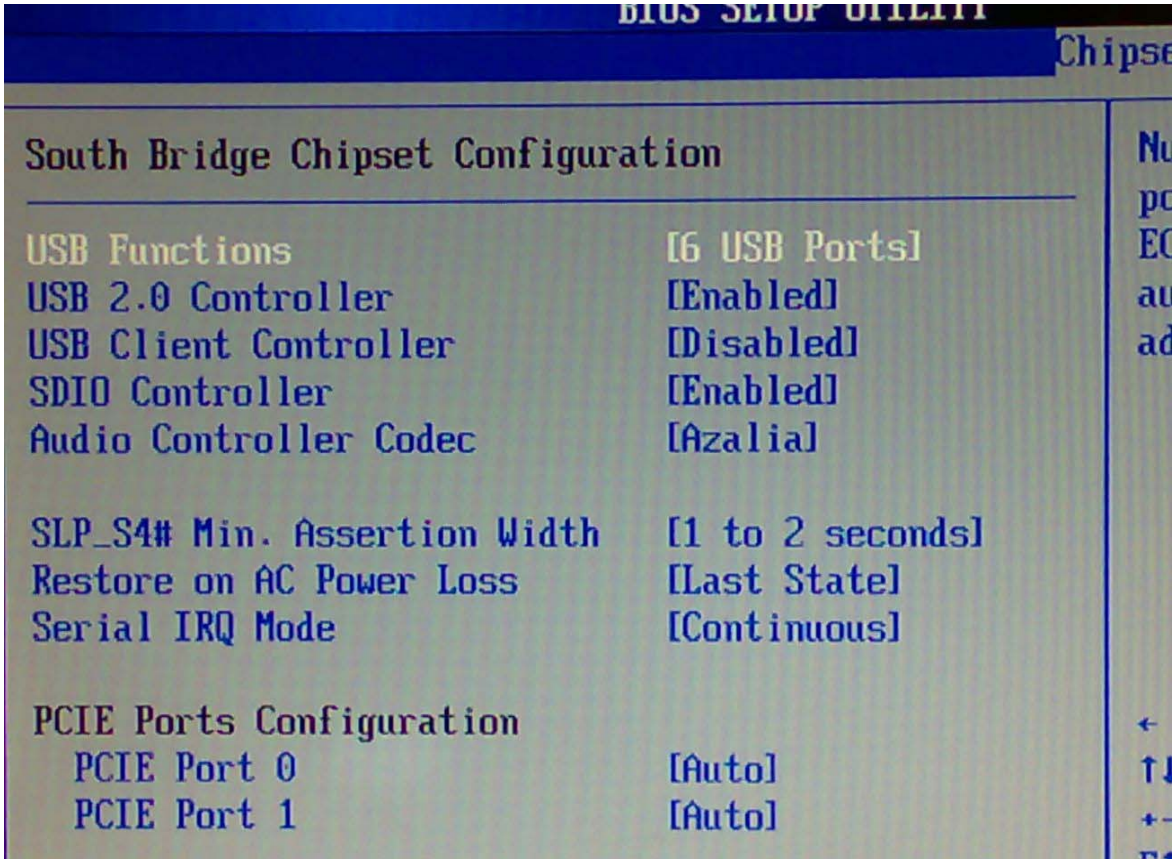
DPST Control

The choice: VBIOS-Default, DPST Disabled, DPST Enabled at Level 1~Level 5.

TV Standard

The choice: VBIOS-Default, NTSC, PAL, SECAM, SMPTE240M, ITU-R television, SMPTE295M, SMPTE296M, CEA 7702, CEA 7703.

South Bridge Chipset Configuration



USB Functions

This setting specifies the function of the onboard USB controller.

The choice: Disabled, 2 USB Ports, 4 USB Ports, 6 USB Ports.

USB 2.0 Controller

Set to [Enabled] if you need to use any USB 2.0 device in the operating system that does not support or have any USB 2.0 driver installed, such as DOS.

The choice: Enabled, Disabled.

USB Client Controller

The choice: Enabled, Disabled.

SDIO controller

The choice: Enabled, Disabled.

Audio Controller Codec

The choice: Auto, Azalia, Disabled.

SLP_S4# Min. Assertion Width

The choice: 4 to 5 seconds, 3 to 4 seconds, 2 to 3 seconds, 1 to 2 seconds.

Restore on AC Power Loss

This item allows user to configure the power status of using ATX power supply after a serious power loss occurs.

The choice: Power Off, Power On, Last State.

Serial IRQ Mode

The choice: Continuous, Quiet.

PCIE Port 0

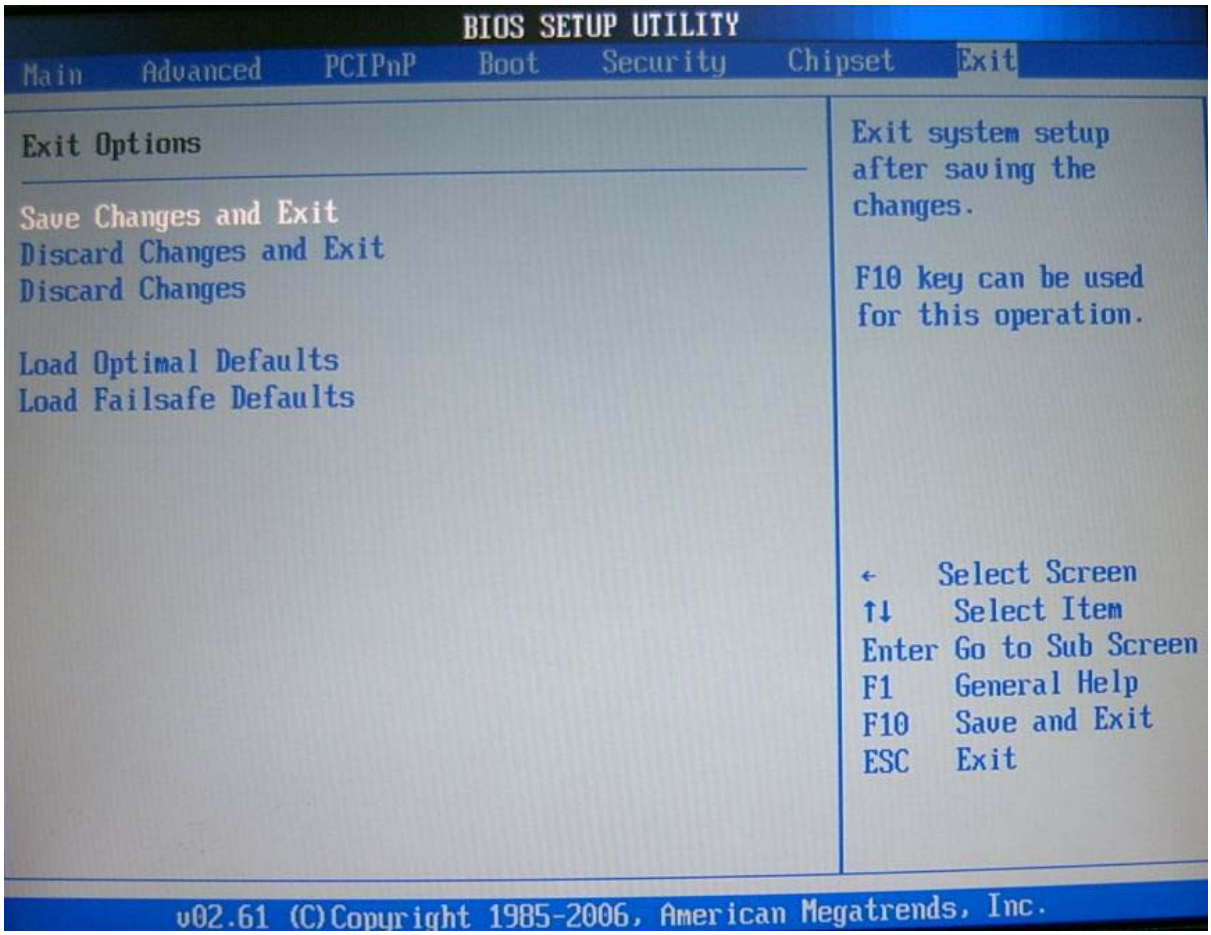
The choice: Auto, Enabled, Disabled.

PCIE Port 1

The choice: Auto, Enabled, Disabled.

4.8 Exit

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.



Save Changes and Exit

Exit System Setup and save your changes to CMOS. Pressing <Enter> on this item asks for confirmation: Save changes to CMOS and exit the Setup Utility.

Discard Changes and Exit

Abandon all changes and exit the Setup Utility.

Discard Changes

Abandon all changes and continue with the Setup Utility.

Load Optimal Defaults

Use this menu to load the default values set by the SBC manufacturer specifically for optimal performance of the SBC.

Load Failsafe Defaults

Use this menu to load the default values set by the BIOS vendor for stable system performance.

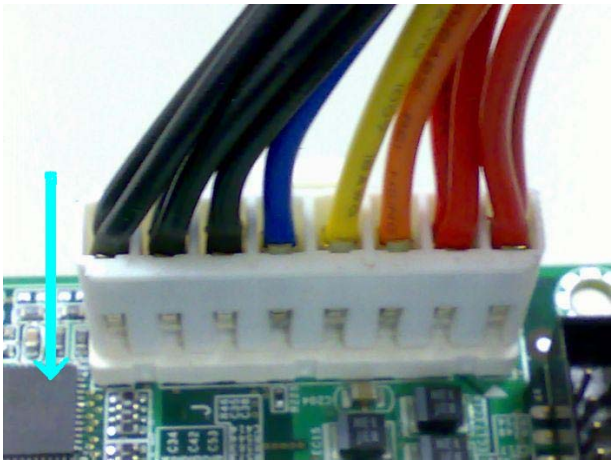
Chapter 5
Troubleshooting

This chapter provides a few useful tips to quickly get NANO-8044 running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will primarily focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

5.1 Hardware Quick Installation

ATX Power Setting

Unlike other Single board computer, NANO-8044 supports ATX only. Therefore, there is no other setting that really needs to be set up. However, there are only two connectors that must be connected—J13 (8 pins Power Connector) Figure.



5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the device cables required before turning on ATX power. 200-pin DDR2 SO-DIMM, keyboard, mouse, PATA hard disk, VGA connector, device power cables, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with NANO-8044, it is recommended, when going with the boot-up sequence, to hit "DEL" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to "**Load Optimal Defaults**", press "Enter" and chose "OK" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

Auto Detect Hard Disks

In the BIOS => Standard CMOS setup menu, pick up any one from Primary Master/Slave IDE ports, and press "Enter". Setup the selected IDE port and its access mode to "Auto". This will force system to automatically pick up the IDE devices that are being connected each time system boots up.

Improper disable operation

There are too many occasions where users disable a certain device/feature in one application through BIOS setting. These variables may not be set back to the original values when needed. These devices/features will certainly fail to be detected.

When the above conditions happen, it is strongly recommended to check the BIOS settings. Make sure certain items are set as they should be. These include the COM1 port, USB ports, external cache, on-board VGA and Ethernet.

It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are

Disable COM1 serial port to release IRQ #4
Etc…

A quick review of the basic IRQ mapping is given below for your reference.

IRQ#	Description
IRQ #0	System Counter
IRQ #1	Keyboard
IRQ #2	Programmed Controller
IRQ #3	COM2
IRQ #4	COM1
IRQ #5	Sound, Network, USB 1.0/1.1 UHCI Controller
IRQ #6	Floppy Disk Controller
IRQ #7	Printer Port (Parallel Port)
IRQ #8	CMOS / Real Time Clock
IRQ #9	ACPI Controller
IRQ #10	SCSI adapter, Video card, USB controller

IRQ #11	Network Controller
IRQ #12	PS/2 Mouse Connector
IRQ #13	Math coprocessor
IRQ #14	Primary IDE Controller
IRQ #15	Secondary IDE Controller

It is then very easy to find out which IRQ resource is ready for additional peripherals. If IRQ resource is not enough, please disable some devices listed above to release further IRQ numbers.

5.3 FAQ

Installation Problem

Question: How do I connect my keyboard and mouse if the NANO-8044 do not have PS/2 connector?

Answer: You may use USB keyboard and mouse to connect on USB interface.

Information & Support

Question: How can I connect my NANO-8044 series to panel?

Answer: First of all, you need to read the Panel spec and Inverter spec to understand which type of panel you will use on NANO-8044 series; different panel will connect to different connector; LVDS interface is J14.

Question: How can I change COM port to RS-232/RS-422/RS-485 mode?

Answer: You can short JP1 pin header to change RS-232/RS-422/RS-485 mode.

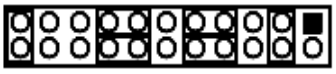
- **JP1: COM1(J2 Top) Interface Selection**

21 19 17 15 13 11 9 7 5 3 1

22 20 18 16 14 12 10 8 6 4 2

RS-232

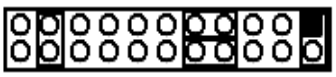
21 19 17 15 13 11 9 7 5 3 1



22 20 18 16 14 12 10 8 6 4 2

RS-422

21 19 17 15 13 11 9 7 5 3 1



22 20 18 16 14 12 10 8 6 4 2

RS-485

JP1	Function
5-6,9-11,10-12,15-17,16-18 Short	RS-232 ★
3-4,7-9,8-10,13-15,14-16,21-22 Short	RS-422
1-2,7-9,8-10,19-20 Short	RS-485

Note:
Please visit our technical web site at
http://www.portwell.com.tw
For additional technical information, which is not covered in this manual, you can mail to tsd@mail.portwell.com.tw or you can also send mail to our sales, they will be very delighted to forward them to us.

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used for your reference.

Memory Area	Size	Device Description
0000-003F	1K	Interrupt Area
0040-004F	0.3K	BIOS Data Area
0050-006F	0.5K	System Data
0070-0E2E	54K	DOS
0E2F-0F6B	5K	Program Area
0F6C-9FBF	577K	[Available]
= Conventional memory ends at 639K =		
9FC0-9FFF	1K	Extended BIOS Area
A000-AFFF	64K	VGA Graphics
B000-B7FF	32K	Unused
B800-BFFF	32K	VGA Text
C000-CE5F	57K	Video ROM
CE60- EFFF	134K	Unused
F000-FFFF	64K	System ROM

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

IRQ#	Current Use	Default Use
IRQ 0	System ROM	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	[Unassigned]	Usable IRQ
IRQ 3	[Unassigned]	Usable IRQ
IRQ 4	System ROM	COM1
IRQ 5	[Unassigned]	Usable IRQ
IRQ 6	System ROM	Diskette Event
IRQ 7	Unused	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	[Unassigned]	Usable IRQ
IRQ 10	[Unassigned]	Usable IRQ
IRQ 11	[Unassigned]	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	[Unassigned]	Usable IRQ