MPC555 Evaluation Board
Quick Reference

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SECTION 1
Preface

The EVB555 is an MPC555-based evaluation board that can be used for the development and test of microcontroller systems. The MPC555 is a member of the Motorola MPC500 PowerPC™ Risc microcontroller family. Beside its PowerPC core and the internal memory subsystem it has a number of peripheral components (eg. 2 Analog-to-Digital converters, 2 CAN controller modules, 2 Time Processor Units) onchip.

The EVB555 can be used to evaluate the capabilities of an MPC555-based microcontroller system. All special features of the MPC555 are supported. The evaluation board is a development and test platform for software and hardware for the MPC555. It can be used by software and hardware developers to test programs, tools or circuits without having to develop a complete microcontroller system themselves.

The heart of the evaluation board is the MPC555. The processor can be operated in ”single chip mode” as well as using external resources. The EVB555 evaluation board has 1 Mbyte RAM, 512 Kbyte flash memory, one port replacement unit and numerous hardware expansion possibilities. To support development and test, the evaluation board can be connected to logic analyzers, debuggers and emulators produced by different manufacturers.

SECTION 2
Technical Features of the EVB555

The following list summarizes the technical features of the EVB555 evaluation board. The architecture of the board is displayed in **Figure 2-1** on the following page.

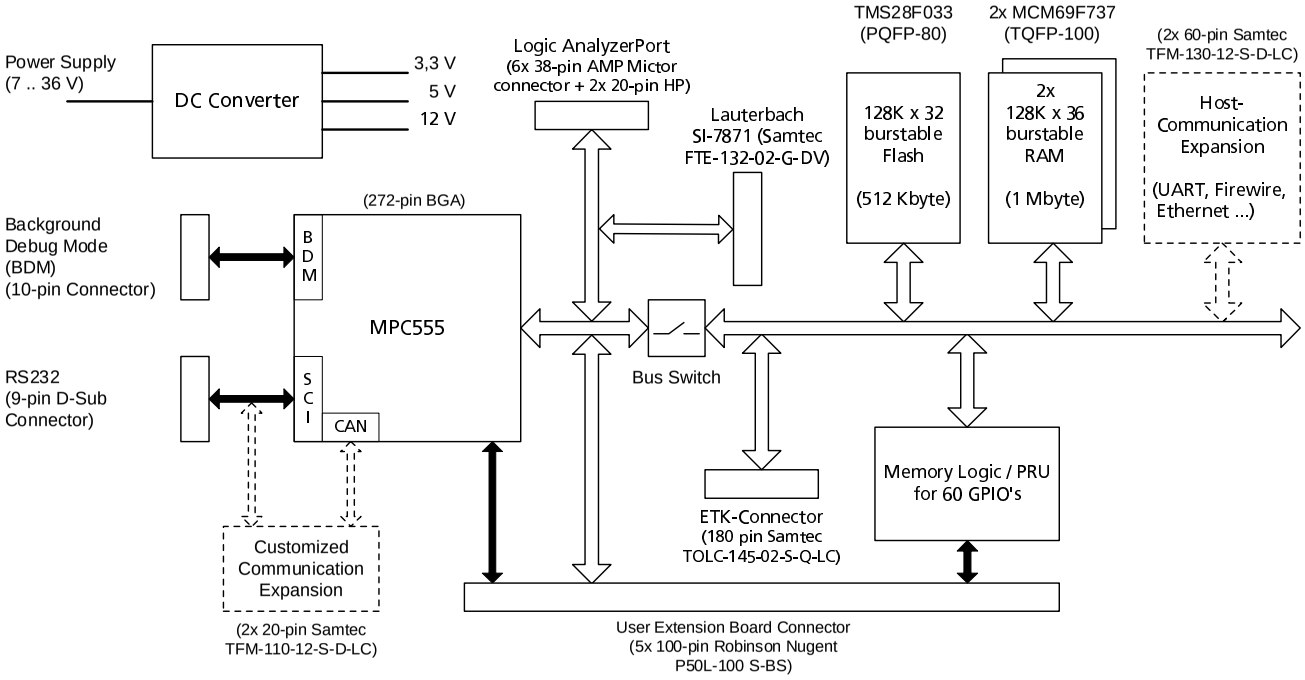
- General advantages
  - — Full function range of the MPC555 can be used
  - — Microcontroller works with variable clock rate (up to 40 MHz)
- Memory
  - — Contains 1 Mbyte fast, synchronous SRAM (32-bit wide, burstable)
  - — 512 Kbyte external flash memory (32-bit wide, burstable)
- Configurability
  - — Convenient configuration of the PLL of the microcontroller via a triple DIP switch
  - — Reset configuration of the MPC555 via a DIP switch (32 bits)
- Extensive analysis and debug support
  - — Flexible BDM interface (background debug mode) for debugging
  - — Direct connection to the ETAS emulator test probe ETKP-1
  - — Excellent analysis possibilities with 268-pin interface for logic analyzers (6 AMP Mictor and 2 berg type connector)
  - — Connection of the probe to Lauterbach Trace32 emulation and programming system
- Very good expansion capability
  - — MAPI-400 interface

    Interface as a connection to a customer-specific base-board (user extension board)
  - — Customized communication expansion

    Customer-specific expansion module, e.g. for CAN, additional serial interfaces (RS232)
  - — Host communication expansion

    Expansion module for high-speed communication to host system, e.g. via Ethernet, Firewire
  - — Port replacement unit (PRU)

    In ”external bus mode” 64 general purpose I/O pins are available that are required by the MPC555 for the bus interface.



PRU - Port Replacement Unit
ETK - Emulator Probe

Figure 2-1 Architecture of the EVB555 evaluation board

SECTION 3
Overview of the Evaluation Board

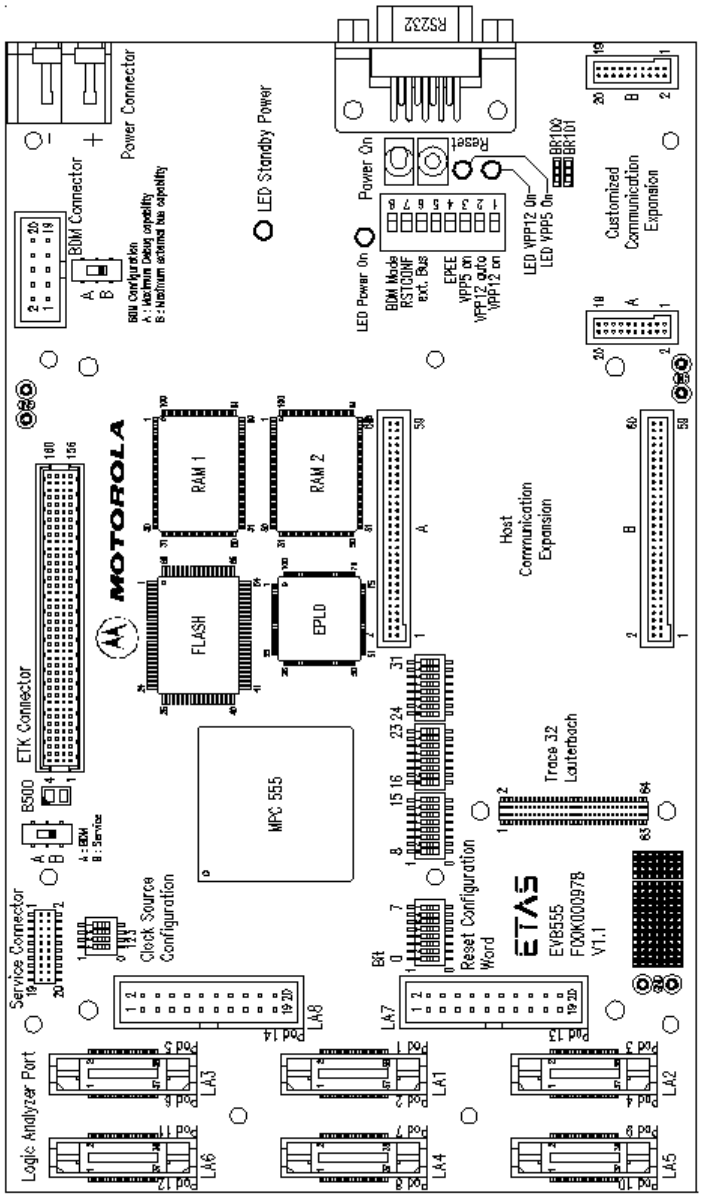


Figure 3-1 EVB555 Top

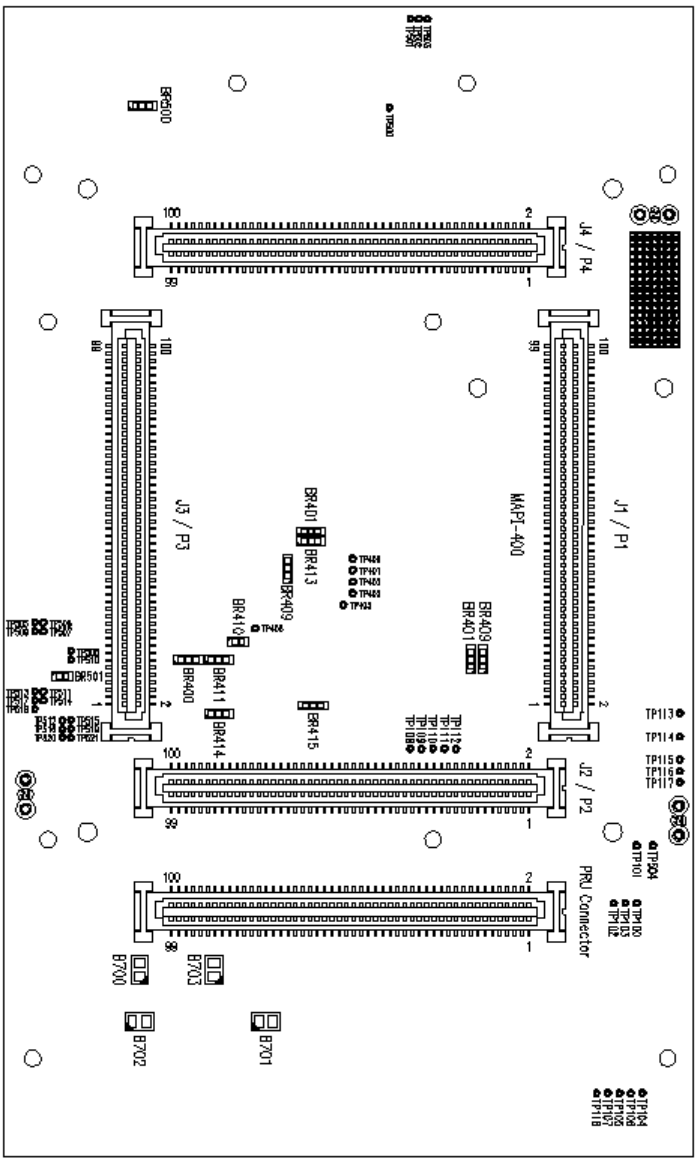


Figure 3-2 EVB555 Bottom

SECTION 4
Interfaces and Configuration Possibilities

4.1 Power Supply

4.1.1 Supply Voltage Connection

The supply voltage should be connected using 2-wire line to the Power clamp (CO102). Both solid as well as flexible wire can be used. The recommended diameter is 0.5 to 2.5 mm^2.

Observe polarity (+,-) and voltage range (7..36V)!

The current consumption at a supply voltage of 12 Volts is as follows (without external load):

- Debug mode: 120 - 150mA
- Standby mode: 20 - 30mA

Additional current is required at startup and during high I/O activity.

4.1.2 Standby

After connecting the external supply voltage, the evaluation board is in standby mode. Only the SRAMs and the standby power pin of the MPC555 are supplied with power. The MPC555 is in reset. This mode is shown by the Standby Power LED (LD703, yellow).

4.1.3 Power On

The toggle switch Power On (SW703) is used for activating the operating voltage of the EVB555. The activated state is shown by the additional LED Power On (LD702, green). All modules on the evaluation board are now supplied with power.

4.2 Single Chip/External Bus Mode

The MPC555 can be operated as a single-chip microcontroller or by using the external bus interface (16-bit or 32-bit wide). The operating mode is set using the ”SC” bits in the SIU module configuration register or in the hard reset configuration word (see MPC555 Manual).

4.2.1 Single Chip Mode

The external resources on the evaluation board, such as SRAM, flash or port replacement unit (PRU), are not used. The pins, which have a second assignment to the external bus interface are now available as general purpose I/O pins. The external bus must be disconnected in this operating mode. Set the DIP switch ”ext. Bus” (SW100-6) to ”Off” for this purpose.

4.2.2 External Bus Interface

The external bus makes it possible to use the resources of the EVB555, such as SRAM, Flash-EEPROM or host communication expansion. The pins are used here for addresses and data. Section 5.2**.** explains how the general purpose I/O lines are still available on the EVB555.

4.3 BDM Interface

The basic debug interface of the EVB555 is the background debug mode interface (BDM for short).

4.3.1 BDM Modes

Two variants are possible here for the support of the configurable use of the pins on the MPC555:

Variant A - maximum debug capability

BDM pin	MPC555 signal	MPC555 pin
1	VFLS0_MPIO3	J18
6	VFLS1_MPIO4	K18

Variant B - maximum external bus capability

BDM pin	MPC555 pin	MPC555 pin
1	IWP0_VFLS0	L2
6	IWP1_VFLS1	L1

4.3.2 BDM/JTAG Support

Due to the double-use of the same pins on the MPC555 for the BDM and the JTAG interface, only one of both interfaces can be used at the same time. The operating mode is selected via the SW102 switch (BDM/Service). The relevant configuration of the MPC555 is explained in the MPC555 User Manual.

- "BDM" setting
  The BDM interface is available at the BDM connector (CO100) .
- "JTAG" setting
  The JTAG interface is available at the Service connector (CO103). This is required for test purposes (e.g. manufacture test) and for programming the EPLD.

The SW102 switch can always remain in the BDM setting when the EVB555 is operated normally.

4.4 Programming the Flash Modules

4.4.1 External Flash

A separate programming voltage of 12V is required for programming the external Flash-EEPROM. This can be controlled and should not be connected permanently for safety reasons.

- Manual control
  The programming voltage Vpp12 can be activated with the DIP switch ”Vpp12 on” (SW100-1). It is then permanently connected to the external flash. To protect the flash memory from being overwritten by accident, the switch should be ”off” when no programming is to take place.
- Automatic control
  If the ”Vpp12 auto” option is enabled (SW100-2 on), the Vpp12 programming voltage can be switched on by the MPC555 program or by the connected ETAS emulator test probe (ETK).
  - — Control by CPU program
    Vpp12 is activated by entering ”1” in the programming voltage control register (cf. **Figure 5-2**). Vpp12 is deactivated by entering a ”0” in the register.
  - — Control by the emulator test probe (ETK)
    The ETK can activate the programming voltage by applying a high level at the SGEPEE signal (CO508, pin 137). This makes it possible for the ETK to program the external flash.

4.4.2 Internal Flash of the MPC555

Two prerequisites must be fulfilled for programming the internal flash memory of the MPC555:

1. Vpp5 (5 V) programming voltage is connected.
2. Programming is enabled by the high level at the EPEE pin.

The Vpp5 programming voltage can be applied separately by closing the ”Vpp5 on” (SW100-3) DIP switch. To protect the internal flash from being overwritten by accident, the switch should be ”off” when no programming is to take place.

Enabling programming via the EPEE pin

1. The pin can be permanently connected to a high level with the ”EPEE” (SW100-4 on) switch
2. The ETK can enable the programming mode by a high level at the SGEPEE signal (C0508, pin 137).

4.5 Interfaces for Testing and Debugging

4.5.1 Logic Analyzer Interface

The connection for the logic analyzer consists of 2 parts:

- digital signals: LA1 to LA6 (CO500 - 505) 38-pin AMP Mictor connector
- analog signals: LA7 and LA8 (CO506,507) 20-pin connector

The assignment of all Logic Analyzer interface connectors can be found in Appendix **A.2**.

4.5.2 Trace32 Lauterbach

The CO509 connector is used for connecting the trace module of the Trace32 BDM debugger (produced by Lauterbach Datentechnik GmbH). The functionality of the debugger can be expanded in this way.

4.5.3 ETK Connector

The ETK connector (CO508) is used for connecting the ETKP-1 emulator test probe (made by ETAS GmbH & Co.KG), which is widely used in automotive engineering.

The ETKP-1 is a memory emulator for 32-bit microcontroller systems and makes it possible to access data in the external and internal memory of the microcontroller while the program is running. That way, variables can be controlled and adapted at program runtime. This procedure is used, for example, in the calibration of engine ECUs in the automobile industry.

4.5.4 MAPI-400+100 Interface

The MAPI-400+100 interface makes it possible to expand the EVB555 with extensive and customer-specific hardware. For example, there could be signal converters and output drivers connected to extend the EVB555 to a test sample of a control unit for industrial use.

The interface consists of two parts.

- MAPI-400 interface
  The MAPI-400 interface (CO600 - CO603) is a standard interface for 32-bit microcontrollers made by Motorola. It makes all necessary signals, such as the address and data bus, as well as control signals, available for the expansion of the microcontroller system. The interface consists of four 100-pin sockets (Robinson Nugent P50L-100-S-BS-TGF). The assignment is shown in Appendix **A.1.1**.
- ”Port replacement unit” (PRU) connector
  This connector (CO604, Robinson Nugent P50L-100-S-BS-TGF) extends the MAPI-400 interface with signals of the port replacement unit (PRU). This means that 64 general purpose I/O pins are again available in ”external bus mode” that are required for the bus interface at the MPC555.

4.6 Reset and Reset Configuration

4.6.1 Reset Button

The Reset (SW702) button initiates a hard reset of the MPC555. When a hard reset occurs, the MPC555 terminates the current program and enters the reset state. The PLL continues to run, however. Once the button is released, the MPC555 starts to work again by reading the system configuration (hard reset configuration).

4.6.2 Hard Reset Configuration

The hard reset configuration makes it possible to influence the behavior of the MPC555 from outside. It particularly includes settings that are necessary before or during the start of the first program. The reset configuration is read by the MPC555 after the supply voltage is switched on and after a hard reset has occurred.

Setting the hard reset configuration is conveniently solved on the EVB555 by assigning the hard reset configuration word via 32 DIP switches.

Table 4-1 on the following page is a short summary of the meaning of the individual bits. For a more detailed description, please consult the MPC555 User Manual. The specified variant makes it possible to work with a BDM debugger.

Bit	Name	Description	Var. 1
0	EARB	0: internal arbitration 1: external arbitration	0
1	IP	Interrupt table location after reset 0: MSR(IP) =1 1: MSR(IP) =0	0
2	BDRV	0: reduced drive strength of bus pins 1: full drive strength of bus pins	1
3	BDIS	0: bank 0 is bootable 1: memory controller inactive	0
4:5	BPS	Boot port size 00: 32-bit 01: 8-bit 10: 16-bit 11: reserved	00
9:10	DBGC	Debug pin configuration (IWP,BI,BG,BR,BB) (6.13.1.1)	10
11	DBPC	Debug pin configuration 0: BDM 1: JTAG	0
12	ATWC	Address type <> Write enable 0: /WE 1: AT	0
13:14	EBDF	External bus division factor 00: CLKOUT = GCLK2 01: CLKOUT = GCLK2/2	00
16	PRPM	Peripheral mode enable 0: normal 1: external master	0
17:18	SC	Single chip select 00: extended chip, 32-bit data 01: extended chip, 16-bit data 10: single chip, show cycle (address) 11: single chip	00
19	ETRE	Extended table relocation 0: off 1: on	0
20	FLEN	0: internal flash disabled (boot external) 1: internal flash enabled	1
23	CLES	0: little endian swap logic inactive 1: little endian swap logic active	0
28:30	ISB	Initial internal space base (6.12.1.2)	00
31	DME	0: dual mapping disabled 1: dual mapping enabled	0

Table 4-1 Hard reset configuration word

4.6.3 Configuration of the PLL

The MPC555 can work with varying external clock generation. The configuration of the microcontroller for the clock used takes place before the operating voltage is applied.

The MODCK setting makes it possible to configure the PLL of the MPC555. Only a few of the possible settings are useful due to the design of the EVB555:

MODCK			LME	MF+1	Timing Reference
1	2	3			
0	1	0	1	5	$freq_{(OSCM)}$ = 4 MHz, limb mode enabled
1	0	0	0	1	$freq_{clkout(max)}$ = $freq_{(EXTCLK)}$, limp mode disabled
1	0	1	0	1	$freq_{clkout(max)}$ = $freq_{(EXTCLK)}$, limp mode disabled
1	1	0	0	5	$freq_{(EXTCLK)}$ = 4 MHz, limp mode disabled
1	1	1	1	1	$freq_{clkout}$=$freq_{(EXTCLK)}$, limp mode enabled

Table 4-2 PLL configuration

Please consult the MPC555 User Manual for an explanation of the PLL function and limp mode.

The standard setting for the evaluation board should be ”010”. The PLL works using the quartz crystal assembled on the EVB555 (4 MHz) whereby the limp mode is enabled.

SECTION 5
Working with the EVB555

5.1 Using External Resources

The external resources on the board (RAM, Flash-EEPROM, PRU) can be addressed through the external bus interface. The selection takes place via chip select signals. **Figure 5-1** shows the connection of the external devices to the most important bus control signals of the MPC555.

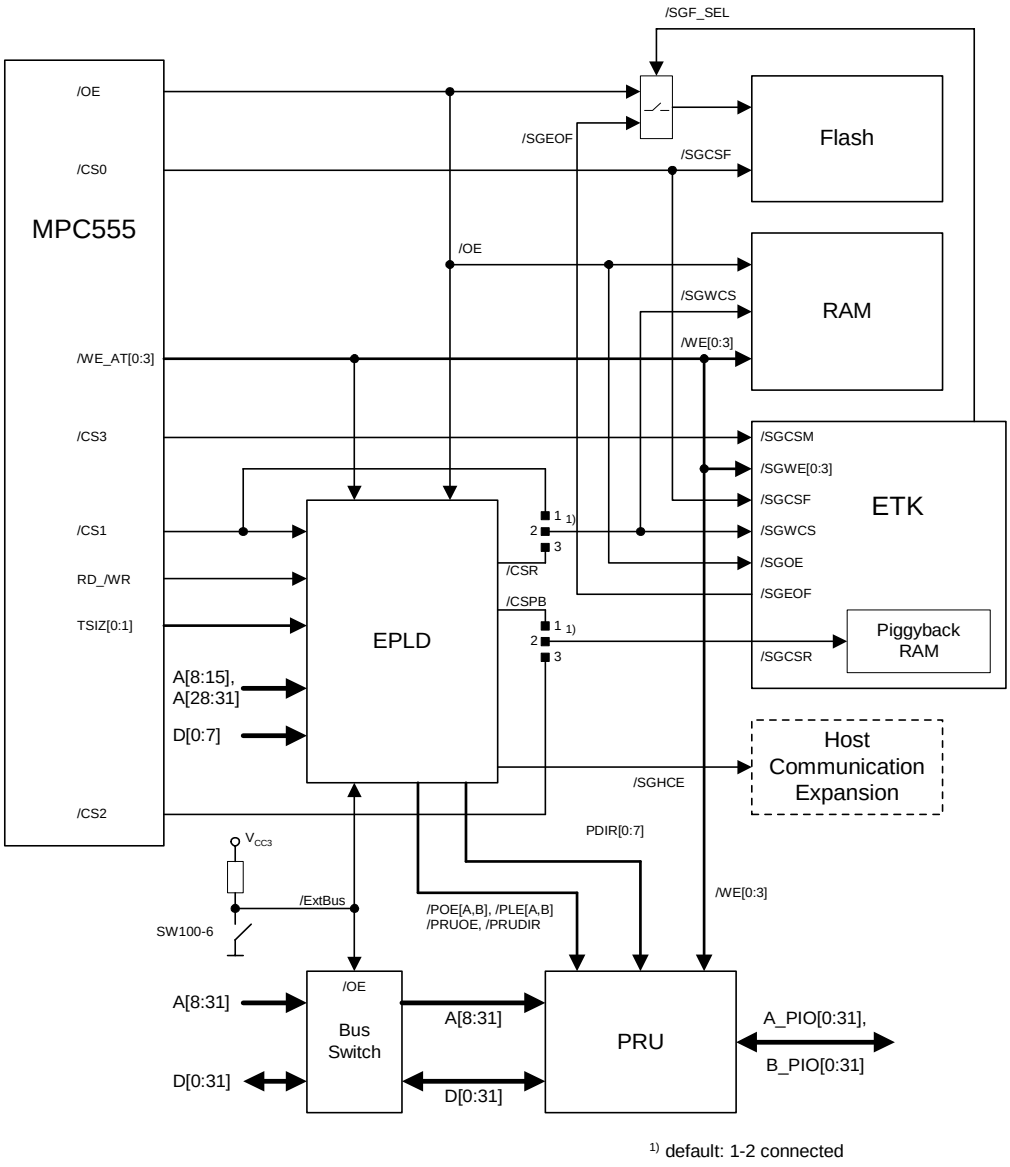
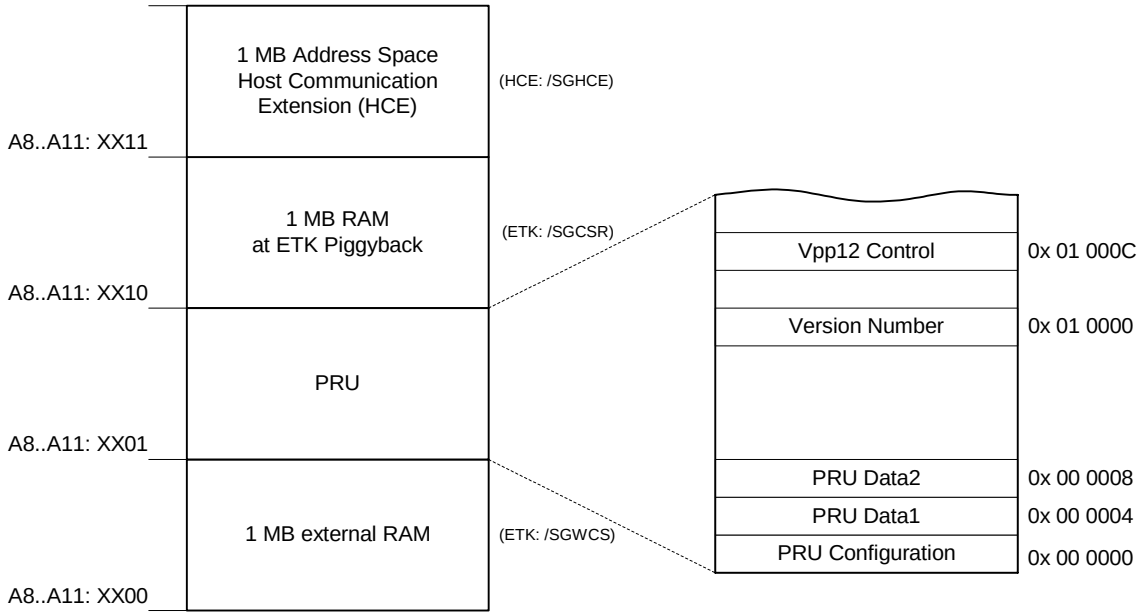


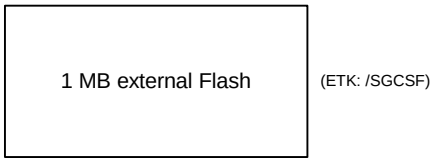
Figure 5-1 Using external resources on the EVB 555

The Flash-EPROM is selected with chip select 0 (/CS0). Chip select 1 (/CS1) is partitioned by the EPLD in ranges for the external RAM, the PRU, the RAM extension on the ETK and the Host Communication Expansion. This division takes place according to addresses and is shown below.

Chip Select 1:



Chip Select 0:



Chip Select 3:

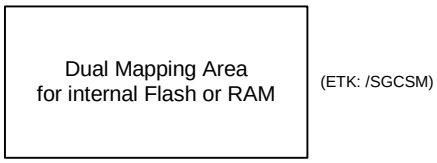


Figure 5-2 Overview of memory selection

The memory size assigned to chip select 1 (/CS1) of the MPC555 should therefore be 4 Mbyte. If the units intended for the higher addresses are not used, this area can also be selected to be smaller (e.g. only 2 Mbyte for RAM and PRU).

5.2 Working with the PRU

The port replacement unit, PRU, provides 64 general purpose I/O lines to compensate the loss of the I/O pins used for the external bus interface.

The EPLD controls the PRU and decodes the addresses for the two groups of I/O channels (A_PIO[0..31] and B_PIO[0..31]). The direction (input or output) of the I/O lines can be configured by setting the corresponding bits PRU_CONF register of the EPLD (see **Table 5-1**). If a configuration bit is set to “0“ the port is used for output whereas a value of "1" means that the port is used for input..

Configuration bit no.	I/O lines
0	A_PIO[24..31]
1	A_PIO[16..24]
2	A_PIO[8..15]
3	A_PIO[0..7]
4	B_PIO[24..31]
5	B_PIO[16..24]
6	B_PIO[8..15]
7	B_PIO[0..7]

Table 5-1 Allocation of the configuration bits

The value of an I/O line defined as input is read from address PRU_DATA1 (for A_PIO[0..31]) or PRU_DATA2 (for B_PIO[0..31]). The EPLD drives the PRU to put the values of all 32 bits per group on the bus.

For setting output values, data is written to address PRU_DATA1 or PRU_DATA2 and latched to the output ports. If a PRU read operation follows, the previously written values are read in again from the ports working as outputs.

In **Figure 5-3** the principle of the address decoding is shown.

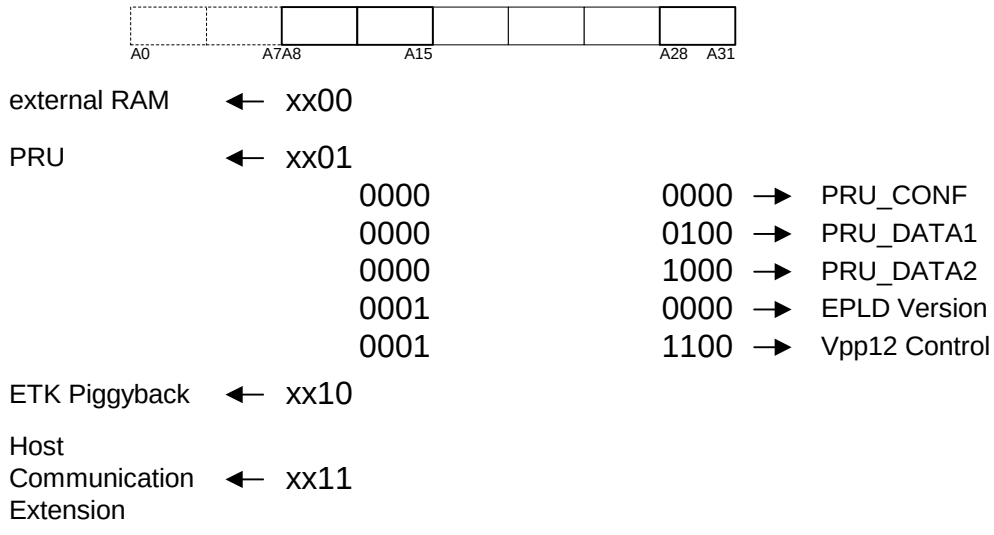


Figure 5-3 Address decoding by EPLD

5.3 Notes on the External Flash Memory

The external flash memory, which is produced by Texas Instruments, has to be configured before you can read from it. This procedure is described in the data sheet of the flash memory.

Internal clock	Bus clock	External flash usable
32MHz	32MHz	Yes
40MHz	20MHz	Yes
40MHz	40MHz	No

Table 5-2 External flash memory at different clock rates

The flash memory only works correctly at a bus clock rate of 33 MHz or less. The resulting variants for the EVB555 are shown in **Table 5-2**.

5.4 Booting on the EVB555

To be able to start a program without a BDM debugger, it is necessary to boot from non-volatile memory (i.e., from flash memory). The mode can be set via the reset configuration word (see Section **4.6.2**.). There are a few points about the EVB555 that should be observed.

The external flash memory cannot be used for booting since it does not provide a mechanism for saving its start-up configuration. It has to be configured before you can read from it.

Booting from the internal flash of the MPC555 is supported by the evaluation board. Earlier versions of the MPC555 are not, however, capable of booting from the internal flash at an internal clock rate of 20 MHz. The standard clock rate is 20 MHz, which is generated by multiplying the crystal frequency (4 MHz) with the mode clock configuration factor 5.

You can solve this problem by exchanging the external crystal. It is recommended that you replace the 4 MHz crystal by a 16 MHz type and operate the PLL of the MPC555 in 1:1 mode. In that case, you will end up with a 16 MHz rate. The value of the mode clock has to be changed to ”011” for this purpose (Section **4.6.3**). This mode is within the PLL specification and even earlier versions of the MPC555 should boot reliably from internal flash memory. If you want to operate the board in this way long-term, you should reduce the capacitor at the XFC output (C201) to 560 pF.

APPENDIX A
Connector Assignment

The following tables display the connector assignment of the EVB555 evaluation board. Only the connected pins are listed; all other pins are open.

A.1 MAPI-400+100 Interface

A.1.1 MAPI0 Interface Assignment

A.1.1.1 Assignment of J1/P1 (CO600) connector:

Pin	MPC pin	Signal name	Description corresponding to data sheet
1	C9	AAN51_PQB7	See AAN48_PQB4
3	A10	AAN52_PQA0	Analog input: passed on as a separate signal to the QADC.
5	B10	AAN53_PQA1	See AAN52_PQA0
7	A11	AAN54_PQA2	See AAN52_PQA0
9	D10	AAN55_PQA3	See AAN52_PQA0
11	C10	AAN56_PQA4	See AAN52_PQA0
13	B11	AAN57_PQA5	See AAN52_PQA0
15	D11	AAN58_PQA6	See AAN52_PQA0
17	C11	AAN59_PQA7	See AAN52_PQA0
27	D3	A_TPUCH0	A_TPUCH0 - A_TPUCH15: Time Processor Unit A channel
29	A2	A_TPUCH1	See A_TPUCH0
30	E17	MPWM0	MPWM0 - MPWM3, MPWM16 - MPWM19: Pulse width modulation
31	D4	A_TPUCH2	See A_TPUCH0
32	D18	MPWM1	See MPWM0
33	C3	A_TPUCH3	See A_TPUCH0
35	A3	A_TPUCH4	See A_TPUCH0
36	D19	MPWM2	See MPWM0
37	D5	A_TPUCH5	See A_TPUCH0
38	D20	MPWM3	See MPWM0
39	B3	A_TPUCH6	See A_TPUCH0
42	F17	MPWM16	See MPWM0
43	C4	A_TPUCH7	See A_TPUCH0
44	E18	MPWM17	See MPWM0
45	A4	A_TPUCH8	See A_TPUCH0
47	C5	A_TPUCH9	See A_TPUCH0
48	F18	MPWM18	See MPWM0
49	B4	A_TPUCH10	See A_TPUCH0
50	E19	MPWM19	See MPWM0
51	B5	A_TPUCH11	See A_TPUCH0
53	A5	A_TPUCH12	See A_TPUCH0
54	A6	A_TPUCH15	See A_TPUCH0
55	C6	A_TPUCH13	See A_TPUCH0
56	C2	A_T2CLK	to clock or gate the timer count register 2 (TCR2) within the TPU.
57	B6	A_TPUCH14	See A_TPUCH0
61	M2	/IRQ1B_SGP	Interrupt request, SGPIO, reservation: to indicate that the internal core initiated a transfer.
62	M1	/IRQ0B_SGP	Interrupt request, SGPIO
63	L3	/IRQ3B_SGP	Interrupt request, SGPIO, kill reservation, retry: indicates to a master that the cycle is terminated but should be repeated.
64	M3	/IRQ2B_SGP	Interrupt request, SGPIO, cancel reservation: to clear its reservation.
65	W18	/IRQ5B_SGP	Interrupt request, SGPIO, mode clock [1]: sampled at the negation of /PORESET in order to configure the PLL/clock mode.
66	L4	/IRQ4B_SGP	Interrupt request, SGPIO, address type: indicates one of the 16 ”address types”. The address type signals are valid at the rising edge of the clock in which the special transfer start (STS) is asserted.

Pin	MPC pin	Signal name	Description corresponding to data sheet
67	Y19	/IRQ7B_mck3	Interrupt request, mode clock [3]: similar to IRQ5B, no SGPIO
68	Y18	/IRQ6B_mck2	Interrupt request, mode clock [2]: similar to IRQ5B, no SGPIO
100	P17	VPP	Flash supply voltage (5V) used during program and erase operation of the CMF.
28, 41, 46, 71, 74, 89, 92		GND	Ground

A.1.1.2 Assignment of J2/P2 (CO601) connector:

Pin	MPC pin	Signal name	Description corresponding to the data sheet
2	D9	AAN50_PQB6	See AAN48_PQB4
4	B9	AAN49_PQB5	See AAN48_PQB4
6	A9	AAN48_PQB4	Analog input channel: passed on as a separate signal to the QADC. Port (PQB): has a synchronizer with an input enable and clock.
8	B8	AAN3_PQB3	See AAN0_PQB0
10	C8	AAN2_PQB2	See AAN0_PQB0
12			See AAN0_PQB0
14	A8	AAN0_PQB0	Multiplexed input analog channel: passed on as a separate signal to the QADC.
21	A17	MDA11	Double action: provide a path for two 16-bit input captures and two 16-bit output captures.
22	A18	MDA12	See MDA11
23	A19	MDA13	See MDA11
24	B17	MDA14	See MDA11
25	B18	MDA15	See MDA11
26	C17	MDA27	See MDA11
27	B20	MDA28	See MDA11
28	C18	MDA29	See MDA11
30	W20	/HRESETB	Hard reset: after negation of /HRESET is detected, a 16-cycle period is taken before testing an external reset. An external pull-up device is required to negate /HRESET.
31	C16	ETRIG1	External trigger input to the QADC_A and QADC_B modules. Can be configured for both QADC_A and QADC_B.
32	U18	EXTCLK	External frequency source for the chip. Must be grounded if unused.
33	B16	ETRIG2	See ETRIG1
34	N4	/BBB_IWP3	Bus busy: master is using the bus. Visible instruction queue flush status. Load/store watchpoint. 3
35	U4	/BDIPB	Burst data in progress: indicates that a data beat follows the current one.
36	N3	/BGB_LWP1	Bus grant: indicates external data bus status. Visible instruction queue flush status Load/store watchpoint
37	V2	/BIB_/STSB	Burst inhibit: ”0” → slave device is not able to support burst transfers. Special transfer start: beginning of an internal transaction in showcycle mode.
38	N2	/BRB_IWP2	Bus request: the data bus has been requested for external cycle. Visible instruction queue flush status Load/store watchpoint 2
39	V1	/BURSTB	Burst indicator: ”0” → burst transaction
40	M4	SGP_/IRQOUTB	SGPIO, interrupt out: an interrupt has been sent to external devices.
41	U3	/TSB	Transfer start: start of a bus cycle that transfers data
42	P18	EPEE	Input: will externally control the program or erase operations.
47	M19	ECK	External bus clock (EBCK): external baud clock used by SCI1 and SCI2
48	U19	ENGCLK/BUCLK	ENGCLK: engineering clock output. Full strength, half strength, disabled. Using EECLK[0:1] bits in the SCCR register. BUCLK: backup clock, less precise on-chip ring oscillator for minimum functionality.
49	N17	RXD1_QGPI	Receive data: serial input from the SCI1
50	N18	TXD1_QGPO	Transmit data: serial output from the SCI1
51	N19	RXD2_QGPI	Receive data: serial input from the SCI2
52	N20	TXD2_QGPO	Transmit data: serial output from the SCI2
61	C19	MDA30	See MDA11
65	C20	MDA31	See MDA11
66	G17	MPIO5	GPIO
67	E20	MPIO6	GPIO

Pin	MPC pin	Signal name	Description corresponding to the data sheet
68	F19	MPIO7	GPIO
69	G18	MPIO8	GPIO
70	F20	MPIO9	GPIO
71	H17	MPIO10	GPIO
72	G19	MPIO11	GPIO
73	G20	MPIO12	GPIO
74	H20	MPIO13	GPIO
75	H19	MPIO14	GPIO
76	H18	MPIO15	GPIO
88	A12	BAN0_PQB0	See AAN0_PQB0
90	B12	BAN1_PQB1	See AAN0_PQB0
92	A13	BAN2_PQB2	See AAN0_PQB0
94	A14	BAN3_PQB3	See AAN0_PQB0
96	B13	BAN48_PQB4	See AAN48_PQB4
98	C12	BAN49_PQB5	See AAN48_PQB4
100	D12	BAN50_PQB6	See AAN48_PQB4
17, 18, 43, 46, 63, 64, 83, 84		GND	Ground

A.1.1.3 Assignment of J3/P3 (CO602) connector:

Pin	MPC pin	Signal name	Description corresponding to the data sheet
2	A15	BAN51_PQB7	See AAN48_PQB4
4	B14	BAN52_PQA0	See AAN52_PQA0
6	C13	BAN53_PQA1	See AAN52_PQA0
8	B15	BAN54_PQA2	See AAN52_PQA0
10	D13	BAN55_PQA3	See AAN52_PQA0
12	C14	BAN56_PQA4	See AAN52_PQA0
14	C15	BAN57_PQA5	See AAN52_PQA0
16	D14	BAN58_PQA6	See AAN52_PQA0
18	D15	BAN59_PQA7	See AAN52_PQA0
26	H2	B_TPUCH0	B_TPUCH0 - B_TPUCH15: Time Processor Unit B channel
27	K20	A_CNRX0	TOUCAN receive data 0: serial data input
28	H1	B_TPUCH1	See B_TPUCH0
29	K19	A_CNTX0	TOUCAN transmit data 0: serial data output
30	G1	B_TPUCH2	See B_TPUCH0
32	G2	B_TPUCH3	See B_TPUCH0
33	H3	B_CNRX0	TOUCAN receive data 0: serial data input
34	G3	B_TPUCH4	See B_TPUCH0
35	H4	B_CNTX0	TOUCAN transmit data 0: serial data output
36	F1	B_TPUCH5	See B_TPUCH0
38	F2	B_TPUCH6	See B_TPUCH0
39	M20	SCK_QGP6	SCK: provides the clock from the QSPI in master mode or to the QSPI in slave mode
40	E1	B_TPUCH7	See B_TPUCH0
41	L19	MISO_QGP4	Master-in slave-out (MISO): provides serial data input to the QSPI in master mode and serial data output from the QSPI in slave mode
42	F3	B_TPUCH8	See B_TPUCH0
44	G4	B_TPUCH9	See B_TPUCH0
45	L20	MOSI_QGP5	Master-out slave-in (MOSI): provides serial data output to the QSPI in master mode, and serial data input from the QSPI in slave mode.
46	E2	B_TPUCH10	See B_TPUCH0
47	L18	PCS0_QGP	PCS0: provide QSPI peripheral chip select 0. SS: places the QSPI in slave mode. QSPI GPIO[0]: can be configured as GPIO if not needed.
48	D1	B_TPUCH11	See B_TPUCH0
50	F4	B_TPUCH12	See B_TPUCH0
51	L17	PCS1_QGP	PCS1: provide QSPI peripheral chip select 1. QSPI GPIO[1]: can be configured as GPIO if not needed.
52	D2	B_TPUCH13	See B_TPUCH0
53	M18	PCS2_QGP	See PCS1_QGP
54	E3	B_TPUCH14	See B_TPUCH0
56	C1	B_TPUCH15	See B_TPUCH0
57	M17	PCS3_QGP	See PCS1_QGP
58	B1	B_T2CLK	See A_T2CLK
62	J19	VF0_MPIO0	VF[0:2] visible instruction queue flush status: output by the chip when program instruction flow tracking is required. GPIO
64	J20	VF1_MPIO1	See VF0_MPIO0
66	J17	VF2_MPIO2	See VF0_MPIO0
67	J18	VFLS0_MPIO3	Visible history buffer flush status: to allow program instruction flow tracking.
69	K18	VFLS1_MPIO4	See VFLS0_MPIO3
71	L2	IWP0_VFLS	Instruction watchpoint. Visible history buffer flush status: output by the chip to enable program instruction flow tracking.
73	L1	IWP1_VFLS	See IWP0_VFLS

Pin	MPC pin	Signal name	Description corresponding to the data sheet
77	V19	/PORESETB	Power on reset: activated as a result of a voltage failure. The internal / PORESET is asserted only if /PORESET is asserted > 100 ns.
80	J2	TDO_DSDO	Test data out, development serial data output: the data-out line of the debug port interface.
82	K2	TDI_DSDI	Test data in, development serial data input : The data-in line for the debug port interface.
83	K1	TMS	Test mode select
85	J1	TCK_DSCK	Test clock, development serial clock: clock for the debug interface.
86	U1	TSIZ0	Transfer size: indicates the size of the requested data transfer.
87	J3	/TRSTB	Test reset: asynchronous reset to the test logic.
88	T3	TSIZ1	Transfer size: indicates the size of the requested data transfer.
89	V20	/SRESETB	Soft reset: after negation of /SRESET is detected, a 16-cycle period is taken before testing an external reset. An external pull-up device is required to negate /SRESET.
90	U17	/RSTCONF_TEXP	Reset configuration (input): the reset configuration mode will be sampled from the external data bus. Timer expired (output): status of the TEXPS bit in the PLPRCR register in the USIU.
94	K3	FRZ_/PTR	SGPIO freeze: RCPU is in debug mode program trace (/PTR): an instruction fetch is taking place.
25, 43, 65, 68, 81, 91, 95, 97		GND	Ground

A.1.1.4 Assignment of J4/P4 (CO603) connector:

Pin	MPC pin	Signal name	Description corresponding to the data sheet
3	W9	Data_SGP1	Data_SGP0 - Data_SGP31: can be sized to support 8-, 16-, 24- or 32-bit transfers. Data_SGP0 is the MSB.
4	Y9	Data_SGP0	
5	W10	Data_SGP3	
6	Y10	Data_SGP2	
7	W11	Data_SGP5	
8	Y11	Data_SGP4	
9	W12	Data_SGP7	
10	Y12	Data_SGP6	
11	W13	Data_SGP9	
12	Y13	Data_SGP8	
13	W14	Data_SGP11	
14	Y14	Data_SGP10	
17	W15	Data_SGP13	
18	Y15	Data_SGP12	
19	W16	Data_SGP15	
20	Y16	Data_SGP14	
21	W17	Data_SGP17	
22	Y17	Data_SGP16	
23	V16	Data_SGP19	
24	V17	Data_SGP18	
25	V15	Data_SGP21	
26	U16	Data_SGP20	
29	U14	Data_SGP23	
30	V14	Data_SGP22	
31	U13	Data_SGP25	
32	V13	Data_SGP24	
33	U12	Data_SGP27	
34	V12	Data_SGP26	
35	U11	Data_SGP29	
36	V11	Data_SGP28	
37	V9	Data_SGP31	
38	V10	Data_SGP30	

Pin	MPC pin	Signal name	Description corresponding to the data sheet
49	V5	Addr_SGP9	Addr_SGP8 - Addr_SGP31: 24 address lines, 16 MB address space
50	V6	Addr_SGP8	
51	V3	Addr_SGP11	
52	V4	Addr_SGP10	
53	Y2	Addr_SGP13	
54	W1	Addr_SGP12	
55	Y3	Addr_SGP15	
56	W3	Addr_SGP14	
59	Y4	Addr_SGP17	
60	W4	Addr_SGP16	
61	Y5	Addr_SGP19	
62	W5	Addr_SGP18	
63	Y6	Addr_SGP21	
64	W6	Addr_SGP20	
65	W7	Addr_SGP23	
66	V7	Addr_SGP22	
67	Y8	Addr_SGP25	
68	Y7	Addr_SGP24	
69	V8	Addr_SGP27	
70	W8	Addr_SGP26	
71	U9	Addr_SGP29	
72	U8	Addr_SGP28	
73	U6	Addr_SGP31	
74	U7	Addr_SGP30	
77	U2	/TAB	Transfer acknowledge: transfer accepted/valid
78	T2	/TEAB	Transfer error acknowledge: error occurred in the current transaction
80	N1	/WEB_AT[0]	Write enable: /WE0 is asserted if the data lane DATA[0:7] contains valid data.
81	R1	RD_/WRB	Read/write : ”1” → read, ”0” → write
82	P1	/WEB_AT[1]	Write enable: /WE1 is asserted if the data lane DATA[8:15] contains valid data.
84	P2	/WEB_AT[2]	Write enable: /WE2 is asserted if the data lane DATA[16:23] contains valid data.
85	P4	/CS0B	Chip select: /CS0 can be the global chip select for the boot device.
86	P3	/WEB_AT[3]	Write enable: /WE3 is asserted if the data lane DATA[24:31] contains valid data.
87	R4	/CS1B	Chip select
88	T1	/OEB	Output enable
89	R3	/CS2B	Chip select
91	R2	/CS3B	Chip select
95	V18	CLKOUT	Clock out: can be configured to full strength, half strength or disabled.
15, 16, 27, 28, 39, 40, 57, 58, 75, 76, 83, 93, 96 ,97		GND	Ground

The following connections are **not** on the MAPI 400 interface.

MPC pin	Signal name	Description corresponding to the data sheet
U20	XTAL	Connection to an external crystal for the internal oscillator circuitry.
T20	EXTAL	Connection to an external crystal for the internal oscillator. Must be grounded, if unused.
R19	XFC	External filter capacity: for an external capacitor filter for the PLL circuitry.
R20	VDDSYN	Power supply of the PLL circuitry
T19	VSSSYN	Power supply of the PLL circuitry
B7	VRH	High reference voltage for QADC_A and QADC_B.
A7	VRL	Low reference voltage for QADC_A and QADC_B.
T18	KAPWR	Keep alive power: 3V supply for the SRAM.

A.1.2 PRU connector (CO604) assignment

Pin	Signal name	Description corresponding to the data sheet
1	B_PIO0	B_PIO0 - B_PIO31: second group of 32 General Purpose I/O lines operated by the Port Replacement Unit
2	A_PIO0	A_PIO0 - A_PIO31: first group of 32 General Purpose I/O lines operated by the Port Replacement Unit
3	B_PIO1	See B_PIO0
4	A_PIO1	See A_PIO0
5	B_PIO2	See B_PIO0
6	A_PIO2	See A_PIO0
7	B_PIO3	See B_PIO0
8	A_PIO3	See A_PIO0
9	B_PIO4	See B_PIO0
10	A_PIO4	See A_PIO0
11	B_PIO5	See B_PIO0
12	A_PIO5	See A_PIO0
13	B_PIO6	See B_PIO0
14	A_PIO6	See A_PIO0
17	B_PIO7	See B_PIO0
18	A_PIO7	See A_PIO0
19	B_PIO8	See B_PIO0
20	A_PIO8	See A_PIO0
21	B_PIO9	See B_PIO0
22	A_PIO9	See A_PIO0
23	B_PIO10	See B_PIO0
24	A_PIO10	See A_PIO0
25	B_PIO11	See B_PIO0
26	A_PIO11	See A_PIO0
29	B_PIO12	See B_PIO0
30	A_PIO12	See A_PIO0
31	B_PIO13	See B_PIO0
32	A_PIO13	See A_PIO0
33	B_PIO14	See B_PIO0
34	A_PIO14	See A_PIO0
35	B_PIO15	See B_PIO0
36	A_PIO15	See A_PIO0
37	B_PIO16	See B_PIO0
38	A_PIO16	See A_PIO0
39	B_PIO17	See B_PIO0

Pin	Signal name	Description corresponding to the data sheet
40	A_PIO17	See A_PIO0
41	B_PIO18	See B_PIO0
42	A_PIO18	See A_PIO0
43	B_PIO19	See B_PIO0
44	A_PIO19	See A_PIO0
45	B_PIO20	See B_PIO0
46	A_PIO20	See A_PIO0
47	B_PIO21	See B_PIO0
48	A_PIO21	See A_PIO0
49	B_PIO22	See B_PIO0
50	A_PIO22	See A_PIO0
51	B_PIO23	See B_PIO0
52	A_PIO23	See A_PIO0
53	B_PIO24	See B_PIO0
54	A_PIO24	See A_PIO0
55	B_PIO25	See B_PIO0
56	A_PIO25	See A_PIO0
59	B_PIO26	See B_PIO0
60	A_PIO26	See A_PIO0
61	B_PIO27	See B_PIO0
62	A_PIO27	See A_PIO0
63	B_PIO28	See B_PIO0
64	A_PIO28	See A_PIO0
65	B_PIO29	See B_PIO0
66	A_PIO29	See A_PIO0
67	B_PIO30	See B_PIO0
68	A_PIO30	See A_PIO0
69	B_PIO31	See B_PIO0
70	A_PIO31	See A_PIO0
71	B_PIO0	See B_PIO0
72	A_PIO0	See A_PIO0
85	/EXTBUS	disconnect external resources from processor bus
86	STANDBY	switch EVB into Stanby mode
95, 96, 97, 98, 99, 100	UB2	alternative power supply path
15, 16, 27, 28, 39, 40, 57, 58, 75, 76, 83, 89, 90, 91, 92, 93, 94	GND	Ground

A.2 Assignment of Logic Analyzer Interface

A.2.1 Assignment of CO500 connector

Pin no.	LA channel	Label	Sgnal name	MPC pin	MPC signal name
6	Clk	STAT	CLKOUT	V18	CLKOUT
8	D15	ADDR	A[16]	W4	Addr_SGP16
10	D14	ADDR	A[17]	Y4	Addr_SGP17
12	D13	ADDR	A[18]	W5	Addr_SGP18
14	D12	ADDR	A[19]	Y5	Addr_SGP19
16	D11	ADDR	A[20]	W6	Addr_SGP20
18	D10	ADDR	A[21]	Y6	Addr_SGP21
20	D9	ADDR	A[22]	V7	Addr_SGP22
22	D8	ADDR	A[23]	W7	Addr_SGP23
24	D7	ADDR	A[24]	Y7	Addr_SGP24
26	D6	ADDR	A[25]	Y8	Addr_SGP25
28	D5	ADDR	A[26]	W8	Addr_SGP26
30	D4	ADDR	A[27]	V8	Addr_SGP27
32	D3	ADDR	A[28]	U8	Addr_SGP28
34	D2	ADDR	A[29]	U9	Addr_SGP29
36	D1	ADDR	A[30]	U7	Addr_SGP30
38	D0	ADDR	A[31]	U6	Addr_SGP31
5	Clk	STAT	/TS	U3	/TSB
7	D15		/PORESET	V19	/PORESETB
9	D14		KAPWR		Not to MPC555, direct to VSTBY3_3
11	D13		EXTCLK	U18	EXTCLK
13	D12		Test point 500		
15	D11	ADDR	/CS[0]	P4	/CS0B
17	D10	ADDR	/CS[1]	R4	/CS1B
19	D9	ADDR	/CS[2]	R3	/CS2B
21	D8	ADDR	/CS[3]	R2	/CS3B
23	D7	ADDR	A[8]	V6	Addr_SGP8
25	D6	ADDR	A[9]	V5	Addr_SGP9
27	D5	ADDR	A[10]	V4	Addr_SGP10
29	D4	ADDR	A[11]	V3	Addr_SGP11
31	D3	ADDR	A[12]	W1	Addr_SGP12
33	D2	ADDR	A[13]	Y2	Addr_SGP13
35	D1	ADDR	A[14]	W3	Addr_SGP14
37	D0	ADDR	A[15]	Y3	Addr_SGP15

A.2.2 Assignment of CO501 connector

Pin no.	LA channel	Label	Signal name	MPC pin	MPC signal name
6	Clk	STAT	/TA	U2	/TAB
8	D15	DATA	D[16]	Y17	Data_SGP16
10	D14	DATA	D[17]	W17	Data_SGP17
12	D13	DATA	D[18]	V17	Data_SGP18
14	D12	DATA	D[19]	V16	Data_SGP19
16	D11	DATA	D[20]	U16	Data_SGP20
18	D10	DATA	D[21]	V15	Data_SGP21
20	D9	DATA	D[22]	V14	Data_SGP22
22	D8	DATA	D[23]	U14	Data_SGP23
24	D7	DATA	D[24]	V13	Data_SGP24
26	D6	DATA	D[25]	U13	Data_SGP25
28	D5	DATA	D[26]	V12	Data_SGP26
30	D4	DATA	D[27]	U12	Data_SGP27
32	D3	DATA	D[28]	V11	Data_SGP28
34	D2	DATA	D[29]	U11	Data_SGP29
36	D1	DATA	D[30]	V10	Data_SGP30
38	D0	DATA	D[31]	V9	Data_SGP31
5	Clk	STAT	/STS	V2	/BIB_/STSB
7	D15	DATA	D[0]	Y9	Data_SGP0
9	D14	DATA	D[1]	W9	Data_SGP1
11	D13	DATA	D[2]	Y10	Data_SGP2
13	D12	DATA	D[3]	W10	Data_SGP3
15	D11	DATA	D[4]	Y11	Data_SGP4
17	D10	DATA	D[5]	W11	Data_SGP5
19	D9	DATA	D[6]	Y12	Data_SGP6
21	D8	DATA	D[7]	W12	Data_SGP7
23	D7	DATA	D[8]	Y13	Data_SGP8
25	D6	DATA	D[9]	W13	Data_SGP9
27	D5	DATA	D[10]	Y14	Data_SGP10
29	D4	DATA	D[11]	W14	Data_SGP11
31	D3	DATA	D[12]	Y15	Data_SGP12
33	D2	DATA	D[13]	W15	Data_SGP13
35	D1	DATA	D[14]	Y16	Data_SGP14
37	D0	DATA	D[15]	W16	Data_SGP15

A.2.3 Assignment of CO502 connector

Pin no.	LA channel	Label	Signal name	MPC pin	MPC signal name
6	Clk	STAT	/TEA	T2	/TEAB
8	D15	STAT	/BURST	V1	/BURSTB
10	D14	STAT	/BDIP	U4	/BDIPB
12	D13	STAT	/OE	T1	/OEB
14	D12	STAT	/WE[0]	N1	/WEB_AT[0]
16	D11	STAT	/WE[1]	P1	/WEB_AT[1]
18	D10	STAT	/WE[2]	P2	/WEB_AT[2]
20	D9	STAT	/WE[3]	P3	/WEB_AT[3]
22	D8	STAT	AT[2]	L4	/IRQ4B_SGP
24	D7	STAT	TSIZ[0]	U1	TSIZ0
26	D6	STAT	TSIZ[1]	T3	TSIZ1
28	D5	STAT	VFLS[0]	J18	VFLS0_MPIO3
30	D4	STAT	VFLS[1]	K18	VFLS1_MPIO4
32	D3	STAT	FRZ_/PTR	K3	FRZ_/PTR
34	D2	STAT	/RETRY	L3	/IRQ3B_SGP
36	D1	STAT	/SRESET	V20	/SRESETB
38	D0	STAT	/HRESET	W20	/HRESETB
5	Clk	STAT	RD_/WR	R1	RD_/WRB
7	D15		/CR	M3	/IRQ2B_SGP
9	D14		KR	M2	/IRQ1B_SGP
11	D13		/RSTCONF	U17	/RSTCONF_TEXP
13	D12		IWP[0]	L2	IWP0_VFLS
15	D11		IWP[1]	L1	IWP1_VFLS
17	D10		IWP[2]	N2	/BRB_IWP2
19	D9		IWP[3]	N4	/BBB_IWP3
21	D8		LWP[0]	M4	SGP_/IRQOUTB
23	D7		LWP[1]	N3	/BGB_LWP1
25	D6	STAT	DSCK	J1	TCK_DSCK
27	D5	STAT	DSDO	J2	TDO_DSDO
29	D4	STAT	DSDI	K2	TDI_DSDI
31	D3	STAT	Compression pin [1)]		
33	D2	STAT	VF[0]	J19	VF0_MPIO0
35	D1	STAT	VF[1]	J20	VF1_MPIO1
36	D0	STAT	VF[2]	J17	VF2_MPIO2

1) designated to be used in future by HP

A.2.4 Assignment of CO503 connector

Pin no.	LA channel	Label	Signal name	MPC pin	MPC signal name
6	Clk		SCK_QGPIO[6]	M20	SCK_QGP6
8	D15		PCS[0]_/SS_QGPIO[0]	L18	PCS0_QGP
10	D14		PCS[1]_QGPIO[1]	L17	PCS1_QGP
12	D13		PCS[2]_QGPIO[2]	M18	PCS2_QGP
14	D12		PCS[3]_QGPIO[3]	M17	PCS3_QGP
16	D11		MISO_QGPIO[4]	L19	MISO_QGP4
18	D10		MOSI_QGPIO[5]	L20	MOSI_QGP5
20	D9		TXD[1]_QGPO[1]	N18	TXD1_QGPO
22	D8		TXD[2]_QGPO[2]	N20	TXD2_QGPO
24	D7		RXD[1]_QGPI[1]	N17	RXD1_QGPI
26	D6		RXD[2]_QGPI[2]	N19	RXD2_QGPI
28	D5		MDA[4] (DA0)	A17	MDA11
30	D4		MDA[5] (DA1)	A18	MDA12
32	D3		MDA[6] (DA2)	A19	MDA13
34	D2		MDA[7] (DA3)	B17	MDA14
36	D1		MDA[8] (DA4)	B18	MDA15
38	D0		*n.c.*		
5	Clk		ECK		ECK
7	D15		MDA[9] (DA5)	C17	MDA27
9	D14		MDA[10] (DA6)	B20	MDA28
11	D13		MDA[11] (DA7)	C18	MDA29
13	D12		MDA[12] (DA8)	C19	MDA30
15	D11		MDA[13] (DA9)	C20	MDA31
17	D10		MPWM[14] (PWM0)	E17	MPWM0
19	D9		MPWM[15] (PWM1)	D18	MPWM1
21	D8		MPWM[16] (PWM2)	D19	MPWM2
23	D7		MPWM[17] (PWM3)	D20	MPWM3
25	D6		MPWM[18] (PWM4)	F17	MPWM16
27	D5		MPWM[19] (PWM5)	E18	MPWM17
29	D4		MPWM[20] (PWM6)	F18	MPWM18
31	D3		MPWM[21] (PWM7)	E19	MPWM19
33	D2		Test point 501		
35	D1		Test point 502		
37	D0		Test point 503		

A.2.5 Assignment of CO504 connector

Pin no.	LA channel	Label	Signal name		MPC pin	MPC signal name
6	Clk		ENGCLK_BUCLK		U19	ENGCLK_BUCLK
8	D15		MGPIO[0]		J19	VF0_MPIO0
10	D14		MGPIO[1]		J20	VF1_MPIO1
12	D13		MGPIO[2]		J17	VF2_MPIO2
14	D12		MGPIO[3]		J18	VFLS0_MPIO3
16	D11		MGPIO[4]		K18	VFLS1_MPIO4
18	D10		MGPIO[5]		G17	MPIO5
20	D9		MGPIO[6]		E20	MPIO6
22	D8		MGPIO[7]		F19	MPIO7
24	D7		MGPIO[8]		G18	MPIO8
26	D6		MGPIO[9]		F20	MPIO9
28	D5		MGPIO[10]		H17	MPIO10
30	D4		MGPIO[11]		G19	MPIO11
32	D3		MGPIO[12]		G20	MPIO12
34	D2		MGPIO[13]		H20	MPIO13
36	D1		MGPIO[14]		H19	MPIO14
38	D0		MGPIO[15]		H18	MPIO15
5	Clk		T2CLK	TPU_A	C2	A_T2CLK
7	D15		TPUCH[0]	TPU_A	D3	A_TPUCH0
9	D14		TPUCH[1]	TPU_A	A2	A_TPUCH1
11	D13		TPUCH[2]	TPU_A	D4	A_TPUCH2
13	D12		TPUCH[3]	TPU_A	C3	A_TPUCH3
15	D11		TPUCH[4]	TPU_A	A3	A_TPUCH4
17	D10		TPUCH[5]	TPU_A	D5	A_TPUCH5
19	D9		TPUCH[6]	TPU_A	B3	A_TPUCH6
21	D8		TPUCH[7]	TPU_A	C4	A_TPUCH7
23	D7		TPUCH[8]	TPU_A	A4	A_TPUCH8
25	D6		TPUCH[9]	TPU_A	C5	A_TPUCH9
27	D5		TPUCH[10]	TPU_A	B4	A_TPUCH10
29	D4		TPUCH[11]	TPU_A	B5	A_TPUCH11
31	D3		TPUCH[12]	TPU_A	A5	A_TPUCH12
33	D2		TPUCH[13]	TPU_A	C6	A_TPUCH13
35	D1		TPUCH[14]	TPU_A	B6	A_TPUCH14
37	D0		TPUCH[15]	TPU_A	A6	A_TPUCH15

A.2.6 Assignment of CO505 connector

Pin no.	LA channel	Label	Signal name	MPC pin	MPC signal name
6	Clk		T2CLK TPU_B	B1	B_T2CLK
8	D15		TPUCH[0] TPU_B	H2	B_TPUCH0
10	D14		TPUCH[1] TPU_B	H1	B_TPUCH1
12	D13		TPUCH[2] TPU_B	G1	B_TPUCH2
14	D12		TPUCH[3] TPU_B	G2	B_TPUCH3
16	D11		TPUCH[4] TPU_B	G3	B_TPUCH4
18	D10		TPUCH[5] TPU_B	F1	B_TPUCH5
20	D9		TPUCH[6] TPU_B	F2	B_TPUCH6
22	D8		TPUCH[7] TPU_B	E1	B_TPUCH7
24	D7		TPUCH[8] TPU_B	F3	B_TPUCH8
26	D6		TPUCH[9] TPU_B	G4	B_TPUCH9
28	D5		TPUCH[10] TPU_B	E2	B_TPUCH10
30	D4		TPUCH[11] TPU_B	D1	B_TPUCH11
32	D3		TPUCH[12] TPU_B	F4	B_TPUCH12
34	D2		TPUCH[13] TPU_B	D2	B_TPUCH13
36	D1		TPUCH[14] TPU_B	E3	B_TPUCH14
38	D0		TPUCH[15] TPU_B	C1	B_TPUCH15
5	Clk		*n.c.*		
7	D15		CNTX0_A	K19	A_CNTX0
9	D14		CNRX0_A	K20	A_CNRX0
11	D13		CNTX0_B	H4	B_CNTX0
13	D12		CNRX0_B	H3	B_CNRX0
15	D11		EPEE	P18	EPEE
17	D10		/IRQ[0]_SGPIOC[0]	M1	/IRQ0B_SGP
19	D9		/IRQ[5]_SGPIOC[5]_ MODCK[1]	W18	/IRQ5B_SGP
21	D8		/IRQ[6]_MODCK[2]	Y18	/IRQ6B_mck2
23	D7		/IRQ[7]_MODCK[3]	Y19	/IRQ7B_mck3
25	D6		TMS	K1	TMS
27	D5		/TRST	J3	/TRSTB
29	D4		*n.c.*		
31	D3		*n.c.*		
33	D2		*n.c.*		
35	D1		*n.c.*		
37	D0		*n.c.*		

A.2.7 Assignment of CO506 connector

Pin	LA channel	Label	Signal name	MPC pin	MPC signal name
3	Clk		ETRIG[1]	C16	ETRIG1
4	D15		AN[0]_ANW_PQB[0] QADC_A	A8	AAN0_PQB0
5	D14		AN[1]_ANX_PQB[1] QADC_A	D8	AAN1_PQB1
6	D13		AN[2]_ANY_PQB[2] QADC_A	C8	AAN2_PQB2
7	D12		AN[3]_ANZ_PQB[3] QADC_A	B8	AAN3_PQB3
8	D11		AN[48]_PQB[4] QADC_A	A9	AAN48_PQB4
9	D10		AN[49]_PQB[5] QADC_A	B9	AAN49_PQB5
10	D9		AN[50]_PQB[6] QADC_A	D9	AAN50_PQB6
11	D8		AN[51]_PQB[7] QADC_A	C9	AAN51_PQB7
12	D7		AN[52]_MA[0]_PQA[0] QADC_A	A10	AAN52_PQA0
13	D6		AN[53]_MA[1]_PQA[1] QADC_A	B10	AAN53_PQA1
14	D5		AN[54]_MA[2]_PQA[2] QADC_A	A11	AAN54_PQA2
15	D4		AN[55]_PQA[3] QADC_A	D10	AAN55_PQA3
16	D3		AN[56]_PQA[4] QADC_A	C10	AAN56_PQA4
17	D2		AN[57]_PQA[5] QADC_A	B11	AAN57_PQA5
18	D1		AN[58]_PQA[6] QADC_A	D11	AAN58_PQA6
19	D0		AN[59]_PQA[7] QADC_A	C11	AAN59_PQA7

A.2.8 Assignment of CO507 connector

Pin no.	LA channel	Label	Signal name	MPC pin	MPC signal name
3	Clk		ETRIG[2]	B16	ETRIG2
4	D15		AN[0]_ANW_PQB[0] QADC_B	A12	BAN0_PQB0
5	D14		AN[1]_ANX_PQB[1] QADC_B	B12	BAN1_PQB1
6	D13		AN[2]_ANY_PQB[2] QADC_B	A13	BAN2_PQB2
7	D12		AN[3]_ANZ_PQB[3] QADC_B	A14	BAN3_PQB3
8	D11		AN[48]_PQB[4] QADC_B	B13	BAN48_PQB4
9	D10		AN[49]_PQB[5] QADC_B	C12	BAN49_PQB5
10	D9		AN[50]_PQB[6] QADC_B	D12	BAN50_PQB6
11	D8		AN[51]_PQB[7] QADC_B	A15	BAN51_PQB7
12	D7		AN[52]_MA[0]_PQA[0] QADC_B	B14	BAN52_PQA0
13	D6		AN[53]_MA[1]_PQA[1] QADC_B	C13	BAN53_PQA1
14	D5		AN[54]_MA[2]_PQA[2] QADC_B	B15	BAN54_PQA2
15	D4		AN[55]_PQA[3] QADC_B	D13	BAN55_PQA3
16	D3		AN[56]_PQA[4] QADC_B	C14	BAN56_PQA4
17	D2		AN[57]_PQA[5] QADC_B	C15	BAN57_PQA5
18	D1		AN[58]_PQA[6] QADC_B	D14	BAN58_PQA6
19	D0		AN[59]_PQA[7] QADC_B	D15	BAN59_PQA7

A.3 Assignment of ETK Connectors

Pin	ETK signal name	EVB signal name	Signal description
1	UBATT	UBATT	Supply power
2	UBATT	UBATT	Supply power
3	UBATT	UBATT	Supply power
4	UBATT	UBATT	Supply power
5	GND	GND	Ground
6	GND	GND	Ground
7	GND	GND	Ground
8	USG3	VCC3	3.3V supply
9	RESERVED		*n.c.*
10	SGD0	SDATA[31]	SDATE0 - SDATA[31]: external data bus of MPC555
11	USG5	VCC5	5V supply
12	GND	GND	Ground
13	SGD1	SDATA[30]	See SDATA[31]
14	SGD2	SDATA[29]	See SDATA[31]
15	SGD3	SDATA[28]	See SDATA[31]
16	SGD4	SDATA[27]	See SDATA[31]
17	SGD5	SDATA[26]	See SDATA[31]
18	GND	GND	Ground
19	SGD6	SDATA[25]	See SDATA[31]
20	SGD7	SDATA[24]	See SDATA[31]
21	SGD8	SDATA[23]	See SDATA[31]
22	SGD9	SDATA[22]	See SDATA[31]
23	SGD10	SDATA[21]	See SDATA[31]
24	SGD11	SDATA[20]	See SDATA[31]
25	SGD12	SDATA[19]	See SDATA[31]
26	SGD13	SDATA[18]	See SDATA[31]
27	GND	GND	Ground
28	SGD14	SDATA[17]	See SDATA[31]
29	SGD15	SDATA[16]	See SDATA[31]
30	GND	GND	Ground
31	SGD16	SDATA[15]	See SDATA[31]
32	SGD17	SDATA[14]	See SDATA[31]
33	SGD18	SDATA[13]	See SDATA[31]
34	SGD19	SDATA[12]	See SDATA[31]
35	SGD20	SDATA[11]	See SDATA[31]
36	SGD21	SDATA[10]	See SDATA[31]
37	SGD22	SDATA[9]	See SDATA[31]
38	SGD23	SDATA[8]	See SDATA[31]
39	GND	GND	Ground
40	SGD24	SDATA[7]	See SDATA[31]
41	SGD25	SDATA[6]	See SDATA[31]
42	SGD26	SDATA[5]	See SDATA[31]
43	SGD27	SDATA[4]	See SDATA[31]
44	SGD28	SDATA[3]	See SDATA[31]
45	SGD29	SDATA[2]	See SDATA[31]
46	GND	GND	Ground
47	SGD30	SDATA[1]	See SDATA[31]
48	SGD31	SDATA[0]	See SDATA[31]
49	SGA0	SADDR[31]	SADDR7 - SADDR3: external address bus of MPC555
50	SGA1	SADDR[30]	See SADDR[31]
51	GND	GND	Ground

Pin	ETK signal name	EVB signal name	Signal description
52	SGA2	SADDR[29]	See SADDR[31]
53	SGA3	SADDR[28]	See SADDR[31]
54	SGA4	SADDR[27]	See SADDR[31]
55	SGA5	SADDR[26]	See SADDR[31]
56	SGA6	SADDR[25]	See SADDR[31]
57	SGA7	SADDR[24]	See SADDR[31]
58	GND	GND	Ground
59	SGA8	SADDR[23]	See SADDR[31]
60	SGA9	SADDR[22]	See SADDR[31]
61	SGA10	SADDR[21]	See SADDR[31]
62	SGA11	SADDR[20]	See SADDR[31]
63	SGA12	SADDR[19]	See SADDR[31]
64	SGA13	SADDR[18]	See SADDR[31]
65	SGA14	SADDR[17]	See SADDR[31]
66	SGA15	SADDR[16]	See SADDR[31]
67	GND	GND	Ground
68	SGA16	SADDR[15]	See SADDR[31]
69	SGA17	SADDR[14]	See SADDR[31]
70	SGA18	SADDR[13]	See SADDR[31]
71	SGA19	SADDR[12]	See SADDR[31]
72	SGA20	SADDR[11]	See SADDR[31]
73	SGA21	SADDR[10]	See SADDR[31]
74	GND	GND	Ground
75	SGA22	SADDR[9]	See SADDR[31]
76	SGA23	SADDR[8]	See SADDR[31]
77	/SGCSF	/CS[0]	Chip select flash
78	/SGCSM	/CS[3]	Chip select dual mapping
79	GND	GND	Ground
80	/SGRW	RD_/WR	Read/write : ”1” → read, ”0” → write
81	GND	GND	Ground
82	/SGRW	/OE	Output enable
83	/SGWCS	/SGWCS	Chip select SRAM
84	/SGBE0	/WE_AT[3]	Write enable: /WE3 is asserted if the data lane DATA[24:31] contains valid data.
85	/SGOEF	/SGOEF	To gate /OE of flash (flash emulation)
86	GND	GND	Ground
87	GND	GND	Ground
88	/SGBE1	/WE_AT[2]	Write enable: /WE2 is asserted if the data lane DATA[16:23] contains valid data.
89	SGSIZ0	TSIZ[1]	Transfer size: indicates the size of the requested data transfer.
90	SGSIZ1	TSIZ[0]	See TSIZ[0]
91	/SGBE2	/WE_AT[1]	Write enable: /WE1 is asserted if the data lane DATA[8:15] contains valid data.
92	/SGBE3	/WE_AT[0]	Write enable: /WE0 is asserted if the data lane DATA[0:7] contains valid data.
93	GND	GND	Ground
94	/SGINST	/IRQ4_AT2	address type 2: differentiate code or data access
95	GND	GND	Ground
96	/SGTS	/TS	Transfer start: start of a bus cycle that transfers data
97	/SGCSR	/SGCSR	Chip select for piggy-back on ETK
98	GND	GND	Ground
99	/SGTA	/TA	Transfer acknowledge: transfer accepted/valid
100	GND	GND	Ground

Pin	ETK signal name	EVB signal name	Signal description
101	/SGBDIP	/BDIP	Burst data in progress: indicates that a data beat follows the current one.
102	/SGBI	/BI_/STS	Burst inhibit: ”0” → slave device is not able to support burst transfers. Special transfer start: beginning of an internal transaction in showcycle mode.
103	/SGAACK	(TP505)	Test point 505
104	/SGBURST	/BURST	Burst indicator: ”0” → burst transaction
105	GND	GND	Ground
106	/SGRESCFG	/RSTCONF	Reset configuration: MPC555 will sample the hard reset configuration word from the external data bus.
107	GND	GND	Ground
108	RESERVED	(TP506)	Test point 506
109	/SGRES	/PORESET	Power on reset: activated as a result of a voltage failure.
110	GND	GND	Ground
111	RESERVED	(TP507)	Test point 507
112	GND	GND	Ground
113	/SGRESIN0	/HRESET	detect or force hard reset of MPC555
114	/SGRESIN1	/SRESET	detect or force soft reset of MPC555
115	GND	GND	Ground
116	SGCLK	CLKOUT	clock for peripheral device
117	GND	GND	Ground
118	RESERVED	(TP508)	Test point 508
119	GND	GND	Ground
120	RESERVED	(TP509)	Test point 509
121	RESERVED	(TP510)	Test point 510
122	GND	GND	Ground
123	SGIWP0	IWP0_VFLS0	Instruction watchpoint of MPC555
124	SGIWP1	IWP1_VFLS1	See IWP0_VFLS0
125	SGTCK	TCK_DSCK	Test clock, development serial clock: clock for the debug interface.
126	SGTMS	TMS	Test mode select
127	SGIWP2	/BR_VF1_IWP2	Bus request: the data bus has been requested for external cycle. Visible instruction queue flush status Load/store watchpoint 2
128	SGIWP3	/BB_VF2_IWP3	Bus busy: master is using the bus Visible instruction queue flush status Load/store watchpoint 3
129	SGTDI	TDI_DSDI	Test data in, development serial data input. The data-in line for the debug port interface.
130	SGTDO	TDO_DSDO	Test data out, development serial data output. The data-out line of the debug port interface.
131	GND	GND	Ground
132	SGLWP0	/IRQOUT_LWPO	interrupt out: an interrupt has been requested to all external devices. Load/store watchpoint 3
133	/SGTRST	/TRST	Test reset: asynchronous reset to the test logic.
134	GND	GND	Ground
135	SGLWP1	/BG_VF0_LWP1	Bus grant: indicates external data bus status. Visible instruction queue flush status. Load/store watchpoint
136	SGVFLS0	VFLS0_MPIO3	Visible history buffer flush status: to allow program instruction flow tracking.
137	SGEPEE	SGEPEE	MPC input: will control the Flash-EEPROM program or erase operations.
138	SGVF0	VF0_MPIO0	VF[0:2] visible instruction queue flush status: output by chip when program instruction flow tracking is required.

Pin	ETK signal name	EVB signal name	Signal description
139	SGVFLS1	VFLS1_MPIO4	See VFLS0_MPIO3
140	SGFRZ	FRZ_/PTR	SGPIO freeze: RCPU is in debug mode program trace (/PTR): an instruction fetch is performed.
141	SGVF1	VF1_MPIO1	See VF0_MPIO0
142	SGVF2	VF2_MPIO2	See VF0_MPIO0
143	GND	GND	Ground
144	RESERVED	(TP511)	Test point 511
145	/SGPOE	(TP512)	Test point 512
146	GND	GND	Ground
147	RESERVED	(TP513)	Test point 513
148	RESERVED	(TP514)	Test point 514
149	SGPDIR0	(TP515)	Test point 515
150	SGPDIR1	(TP516)	Test point 516
151	RESERVED	(TP517)	Test point 517
152	RESERVED	(TP518)	Test point 518
153	SGPDIR2	(TP519)	Test point 519
154	SGPDIR3	(TP520)	Test point 520
155	GND	GND	Ground
156	SGCLKO	EXTCLK	External frequency source for the chip.
157	/SGPWE	(TP521)	Test point 521
158	GND	GND	Ground
159	GND	GND	Ground
160	RESERVED [1)]	/SGF_SEL	

1) Resistor (0R0) to GND on the adapter (ETAP3)

A.4 Connectors and their Counterparts

A.4.1 CO 100—Background Debug Mode Interface (BDM)

CO 100	EVB555	Counterpart
Description	.100” x .100” Shrunk shrouds header, 10 pins	.100” x .100” Polarized socket, 10 pins
Manufacturer	3M	3M
Order No.	925320-01-10-10	8510-4500 JL (boardmount) CHG-2010-J01010-KCP (wiremount)

A.4.2 CO 101—RS232 Serial Interface

CO 101	EVB555	Counterpart
Description	SUBD9	SUBD 9 plug connector, 9 pins
Manufacturer	CONEC	CONEC
Order No.	164C 12969X	161A 10019X or 161A 11069X, etc.

A.4.3 CO 103—JTAG/Service

CO 103	EVB555	Counterpart
Description	Micro Strips FTS series, 2 rows, 20 pins	Micro Strips, 2 rows
Manufacturer	Samtec	Samtec
Order No.	FTS-110-01-F-DV-P	FLE-110-01-G-DV-P
Comment		JTAG

A.4.4 CO 104/105—Customized Communication Expansion (CAN)

CO 104/105	EVB555	Counterpart
Description	Micro Strips, 2 rows, 20 pins	Micro Strips, 2 rows
Manufacturer	Samtec	Samtec
Order No.	TFM 110-12-S-D-P	SFM 110-02-S-D-P
Comment		Piggyback

A.4.5 CO 106/107—Host Communication Expansion

CO 106/107	EVB555	Counterpart
Description	Micro Strips, 2 rows, 60 pins	Micro Strips, 2 rows
Manufacturer	Samtec	Samtec
Order No.	TFM-130-12-S-D-P	SFM-130-02-S-D-P
Comment		Piggyback

A.4.6 CO 500-505—Logic Analyzer Ports: Digital Signals

CO 500-505	EVB555	Counterpart
Description	MICTOR-Connector, receptacle type, 38 positions	MICTOR-Connector, plug type
Manufacturer	AMP	AMP
Order No.	Reference part no. 767 004 Product code 2429 (38 positions)	Reference part no. 767 004 Product code 2429 (38 positions)
Comment		Fitting with: HP E5346A high density termination adapter or HP E5351A high density adapter

A.4.7 CO 506/507—Logic Analyzer Ports: Analog Signals

CO 506/507	EVB555	Counterpart
Description	.100” x .100” Shrunk shrouds header, 20 pins	.100” x .100” Polarized socket, 20 pins
Manufacturer	3M	3M
Order No.	925320-01-20-10	8520-4500 JL (boardmount) CHG-2020-J01010-KCP (wiremount)

A.4.8 CO 508—ETK Connector

CO 508	EVB555	Counterpart
Description	Micro Strips, 4 rows, 160 pins	Please be sure to contact the manufacturer of your emulator probe for further information before connecting it to the EVB555.
Manufacturer	Samtec	
Order No.	MOLC-140-02-S-Q-TR	
Comment		

A.4.9 CO 509—Lauterbach Connector

CO 509	EVB555	Counterpart
Description	Micro Strips, 2 rows, 64 pins	Micro Strips, 2 rows, 64 pins
Manufacturer	Samtec	Samtec
Order No.	FTE-132-02-G-DV-P	CLE-132-01-G-DV-P

A.4.10 CO 600-603—MAPI Interface

CO 600-603	EVB555	Counterpart
Description	P50L-SMT series, socket type, 100 contacts	P50L-SMT series, plug type, 100 contacts
Manufacturer	Robinson Nugent	Robinson Nugent
Order No.	P50L-100 S-BS-TGF	P50L-100 P-AS-TGF

A.4.11 CO 604—PRU Extension

CO 604	EVB555	Counterpart
Description	P50L-SMT series, socket type, 100 contacts	P50L-SMT series, plug type, 100 contacts
Manufacturer	Robinson Nugent	Robinson Nugent
Order No.	P50L-100 S-BS-TGF	P50L-100 P-AS-TGF