

## **PCI-1758UDI**

**128-channel  
Isolated Digital Input Card**

## **PCI-1758UDO**

**128-channel  
Isolated Digital Output Card**

**User Manual**

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Part No. 2003175800

1st Edition

Printed in Taiwan

June 2004

## **Product Warranty (2 years)**

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

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1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an RMA (return merchandise authorization) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

## **CE**

The PCI-1758UD and PCI-1758UDO, have passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This kind of cable is available from Advantech. Please contact your local supplier for ordering information.

## **Technical Support and Assistance**

- Step 1. Visit the Advantech web site at **[www.advantech.com/support](http://www.advantech.com/support)** where you can find the latest information about the product.
- Step 2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
  - Product name and serial number
  - Description of your peripheral attachments
  - Description of your software (operating system, version, application software, etc.)
  - A complete description of the problem
  - The exact wording of any error messages

## **Packing List**

Before setting up the system, check that the items listed below are included and in good condition. If any item does not accord with the table, please contact your dealer immediately.

The PCI-1758U include the following items:

- 1 x PCI-1758UDI/DO card
- 1 x Companion CD-ROM (DLL driver included)
- 1 x User Manual (This manual)



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## **General Information**

This chapter gives background information on the PCI-1758UDI and PCI-1758UDO. It then shows how to configure the card to match your application and prepare it for installation on your system.

Sections include:

- Introduction
- Installation Guide
- Accessories

# Chapter 1 General Information

## 1.1 Introduction

---

Thank you for buying the PCI-1758UDI/1758UDO Digital Input/Output card. The PCI-1758UDI/1758UDO card enables powerful data acquisition (DAS) card for the PCI bus. It features a unique circuit design, and complete functions for data acquisition and control.

The PCI-1758UDI/1758UDO card provides specific functions for different user requirements:

|             |   |
|-------------|---|
| PCI-1758UDO | 128-channel Isolated Digital <b>Output</b> card |
| PCI-1758UDI | 128-channel Isolated Digital <b>Input</b> Card  |

The following sections of this chapter will provide further information about features of the DAS cards.

### 1.1.1 Features

The PCI-1758UDI/UDO DIO card provides the most requested I/O and control functions as seen below:

#### **PCI-1758UDO card**

- 128 isolated digital output channels
- High-voltage isolation on output channels (2,500 VDC )
- Wide output range (5 ~ 40 VDC )
- High-sink current for isolated output channels (90 mA max./Channel)
- Current protection for each port
- BoardID
- Output status read-back
- Digital output value retained after hot system reset
- Programmable Power-Up States
- Watchdog Timer

### **PCI-1758UDI card**

- 128 isolated digital input channels
- High-voltage isolation for input channels (2,500 VDC )
- Wide input range (5 ~ 25 VDC )
- Digital Filter function
- Board ID
- Interrupt handling capability

### **Robust Isolation (PCI-1758UDI/1758UDO)**

The PCI-1758UDI/1758UDO features a robust isolation protection for applications in industrial, lab and machinery automation. The PCI-1758UDI / 1758UDO can durably withstand a voltage up to 2,500 VDC, preventing your host system from any incidental harms.

### **Wide Input/Output Range (PCI-1758UDI / 1758UDO)**

The PCI-1758UDI has a wide range of input voltage from 5 to 25 VDC, and is suitable for most industrial applications with 12 and 24 VDC input voltage. The PCI-1758UDO also features a wide output voltage range from 5 to 40 VDC, suitable for most industrial applications with 12 / 24 VDC output voltage.

### **BoardID Switch**

The PCI-1758UDI / 1758UDO has a built-in DIP switch that helps define each card's ID when multiple cards have been installed on the same PC chassis. The BoardID switch is very useful when you are building a system with multiple PCI-1758UDI/1758UDO cards. With correct Board ID settings, you can easily identify and access each card during hardware configuration and software programming.

### **Programmable Power-Up States Function**

When powering up, the output drives on the PCI-1758UDO are disabled. All output lines are user-configurable for logic high output and logic low output. User-configurable power-up states are useful for ensuring that the PCI-1758UDO powers up in a known state. Power-up states are programmed in the EEPROM through the driver. The default settings are all set to 0. For more details, please refer to Appendix C.

### **Watchdog Timer Function**

The watchdog timer is a software configurable feature used to set critical outputs to safe states in the event of a software failure.

### **Reset Protection**

If the system has undergone a hot reset (i.e. without turning off the system power), the PCI-1758UDO can either retain outputs values of each channel, or return to its default configuration with power up status, depending on its on-board jumper setting. This function protects the system from causing wrong operations during unexpected system resets.

**Table 1.1: PCI-1758UDO/1758UDI Features Comparison**

| <b>PCI BUS Isolated Digital I/O card</b>    | <b>PCI-1758UDO</b> | <b>PCI-1758UDI</b> |
|---|--------------------|--------------------|
| 128 channel IDO                             | Y                  | -                  |
| 128 channel IDI                             | -                  | Y                  |
| BoardID                                     | Y                  | Y                  |
| 2500 VDC Isolation                          | Y                  | Y                  |
| Wide Input Range 5-25 VDC                   | -                  | Y                  |
| Wide Output Range 5-40 VDC                  | Y                  | -                  |
| Keep last status after hot reset            | Y                  | -                  |
| High Sink current (90mA/ch) on IDO channels | Y                  | -                  |
| Output status read back                     | Y                  | -                  |
| Interrupt handling                          | -                  | Y                  |

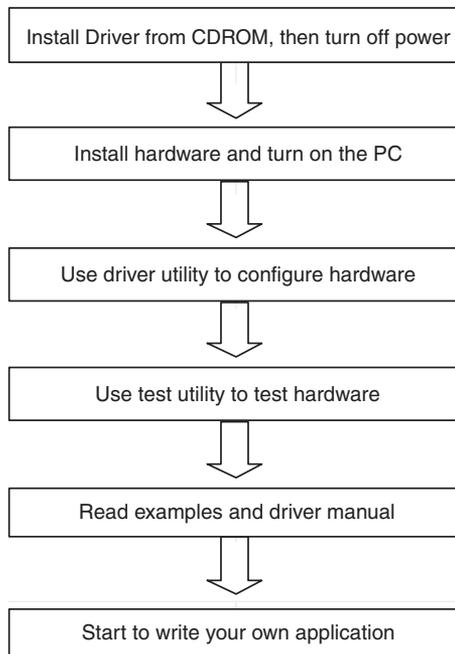
## **1.2 Installation Guide**

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Before you install your PCI-1758UDI/1758UDO card, please make sure you have the following necessary components:

- PCI-1758UDI / 1758UDO isolated digital I/O card
- PCI-1758UDI / 1758UDO User Manual
- Driver software: Advantech DLL drivers(included in the companion CD-ROM)
- Wiring cable: 100-pin MINI-SCSI HDRA-E100 cable
- Wiring board: ADAM-39100
- Computer: Personal computer or workstation with a PCI-bus slot (running Windows 98/2000/XP)

After you get the necessary components and maybe some accessories for enhanced operation for your DAS card, you can then begin the installation procedure. Figure 1-1 provides a concise flow chart to give users a broad picture of the software and hardware installation procedure.



**Figure 1.1: Installation Flow Chart**

## **1.3 Accessories**

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Advantech offers a complete set of accessory products to support the PCI-1758UDI / 1758UDO cards. These accessories include:

### **1.3.1 Wiring Cable**

PCL-101100S-1 (1m): The PCL-101100S-1 (1m) shielded cable is specially designed for the PCI-1758UDI/UDO card to provide high resistance to noise.

### **1.3.2 Wiring Terminal Board**

ADAM-39100: The ADAM-39100 is a 100-pin SCSI wiring terminal module for DIN-rail mounting. This terminal module can be readily connected to Advantech PC-LabCard products and allow easy and reliable access to individual pin connections for the PCI-1758UDI/UDO card.

## **Hardware Configuration**

This chapter has a package item checklist, proper instructions about unpacking and step-by-step procedures for card installation.

Sections include:

- Unpacking
- Hardware Installation
- Board Layout: Dimensions

# Chapter 2 Hardware Configuration

## 2.1 Unpacking

---

After receiving your PCI-1758UDI / 1758UDO package, please inspect its contents first. The package should contain the following items:

- PCI-1758UDI/1758UDO card
- Companion CD-ROM (DLL driver included)
- User Manual

The PCI-1758UDI/1758UDO card harbors certain electronic components that are vulnerable to electrostatic discharge (ESD). ESD could easily damage the integrated circuits and certain components if preventive measures are not carefully paid attention to. Before removing the card from the antistatic plastic bag, you should take following precautions to ward off possible ESD damage:

- Touch the metal part of your computer chassis with your hand to discharge static electricity accumulated on your body. Or use a grounding strap.
- Touch the antistatic bag to a metal part of your computer chassis before opening the bag.
- Take hold of the card only by the metal bracket when removing it out of the bag.

### **After taking out the card, first you should:**

- Inspect the card for any possible signs of external damage (loose or damaged components, etc.). If the card is visibly damaged, please notify our service department or our local sales representative immediately. Avoid installing a damaged card into your system.

**Also pay extra caution to the following aspects to ensure proper installation:**

- Avoid physical contact with materials that could hold static electricity such as plastic, vinyl and Styrofoam.
- Whenever you handle the card, grasp it only by its edges. DO NOT TOUCH the exposed metal pins of the connector or the electronic components.

*Note: Keep the antistatic bag for future use. You might need the original bag to store the card if you have to remove the card from the PC, or wish to transport it elsewhere.*

## **2.2 Hardware Installation**

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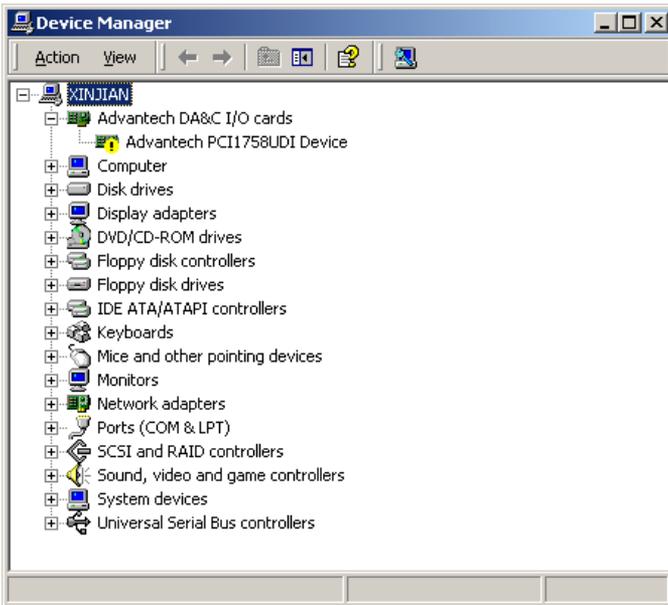
*Note: Make sure you have installed the driver first before you install the card. We strongly recommend that you install the software driver first before you install the hardware into your system, since this will guarantee a smooth and trouble-free installation process.*

When you install the PCI-1758UDI/1758UDO card, please make sure the installation of the DLL driver is complete. You can then go on to install the PCI-1758UDI/1758UDO card in any PCI slot on your computer. It is suggested that you refer to the user manual or related documentation if you have any doubt. Please follow the steps below to install the card on your system.

1. Turn off your computer and unplug the power cord and cables
2. Remove the cover of your computer.
3. Remove the slot cover on the back panel of your computer.
4. Touch a metal part on the surface of your computer to neutralize the static electricity that might be in your body.

5. Adjust DIP switch SW1 on board to set the card's BoardID.
6. Insert the PCI-1758UDI/1758UDO card into a PCI slot. Hold the card only by its edges and carefully align it with the slot. Insert the card firmly into place. Use of excessive force must be avoided, or the card might be damaged.
7. Fasten the bracket of the PCI card on the back panel rail of the computer with screws.
8. Connect appropriate accessories to the PCI card.
9. Replace the cover of your computer chassis. Re-connect the cables you removed in step 2.
10. Plug in the power cord and turn on the computer.

If your card is properly installed, you should see the device name of your card listed on the Device Manager tab. If you do see your device name listed on it but marked with an exclamation sign “!” (Fig. 2-1), it means your card has not been correctly installed. In this case, remove the card device from the Device Manager by selecting its device name and press the remove button. Then go through the driver installation process again.



**Figure 2.1: The Exclamation Mark (!) Indicates Problems**

## 2.3 Board Layout: Dimensions

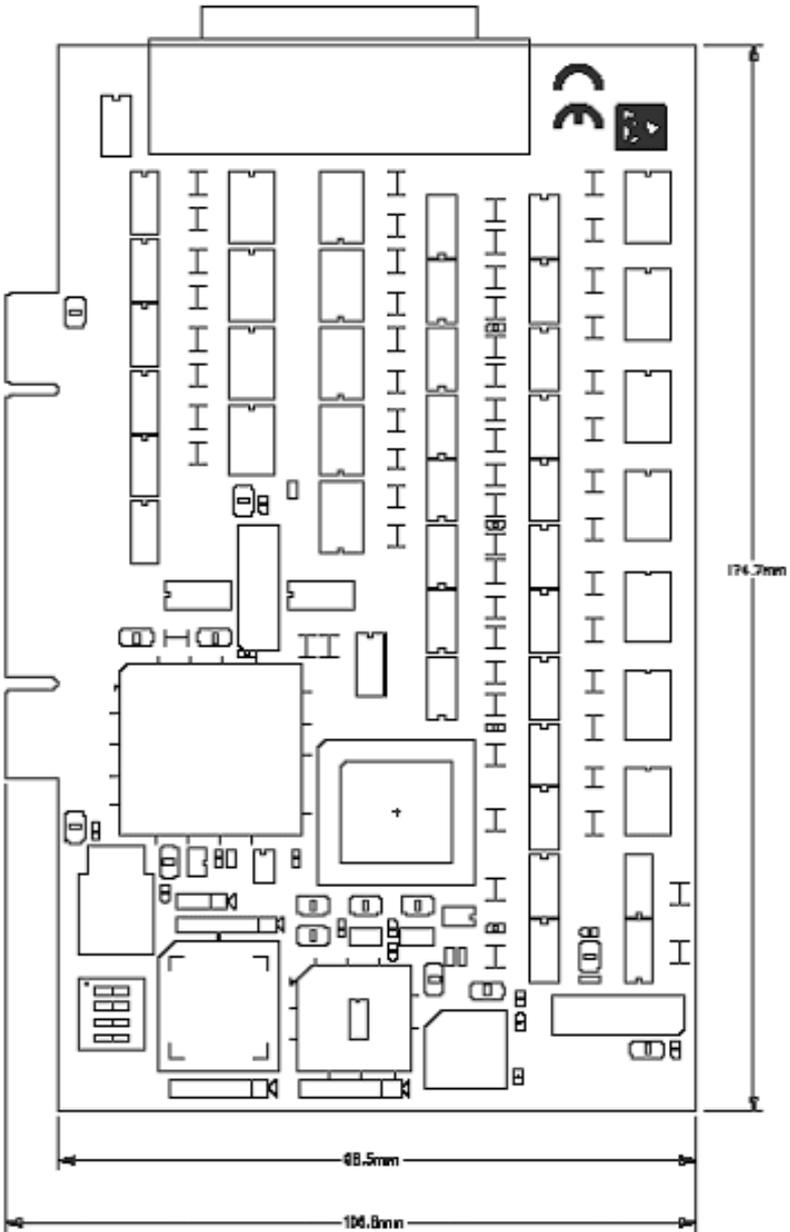


Figure 2.2: PCI-1758UDI/1758UDO Board Layout: Dimensions

### **2.3.1 Connector**

PCI-1758UDI/1758UDO has one HDRA-E100W1LFDT1EC-SL Equivalent female connector. For more details about jumpers, switches and connectors, please see Chapter 3 Pin Assignment & Jumper Setting, and Chapter 4 Operation.

## **Pin Assignments and Jumper Settings**

Maintaining signal connections is one of the most important factors in ensuring that your application system is sending and receiving data correctly. A good signal connection can avoid unnecessary and costly damage to your system and other hardware devices. This chapter provides useful information about how to connect input and output signals to the PCI-1758UDI/1758UDO via the I/O connector.

Sections include:

- Pin Assignments
- Location of Jumper and DIP Switch
- Isolated Digital Input Connections
- Isolated Digital Output Connections
- Field Wiring Considerations

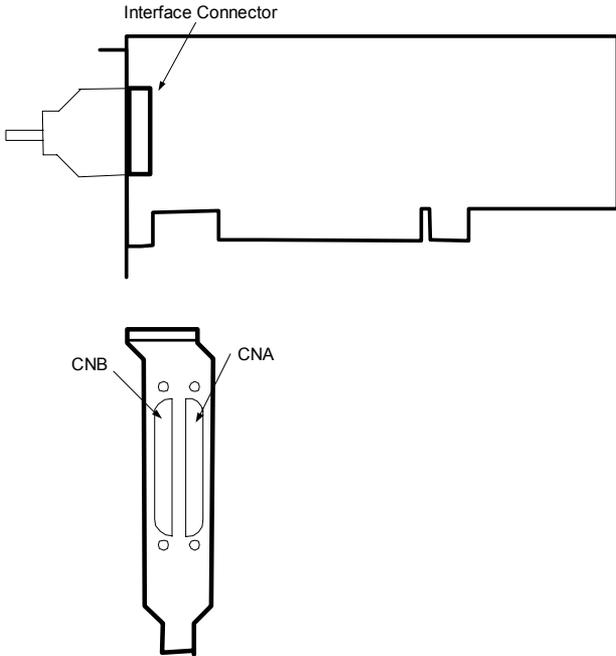
# Chapter 3 Pin Assignments & Jumper settings

## 3.1 Pin Assignments

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The I/O connectors on the PCI-1758UDI/1758UDO are one MINI-SCSI HDRA-E100 Female connectors. Figure 3-1, 3-2 shows the pin assignments for the MINI-SCSI HDRA-E100 Female connector on the PCI-1758 UDI/1758UDO, and Table 3-1, 3-2 shows its connector signal descriptions.

**Note:** *The PCL-101100S-1 (1m) shielded cable is especially designed for the PCI-1758UDI/UDO to reduce noise in the analog signal lines. Please refer to section 1.3 Accessories.*



**Figure 3.1: Connector**

| CNB      |     |    | CNA      |          |    |     |          |
|----------|-----|----|----------|----------|----|-----|----------|
| PEF_COMM | 100 | 50 | PAB_COMM | NC       | 1  | 51  | NC       |
| PEF_COMM | 99  | 49 | PAB_COMM | NC       | 2  | 52  | NC       |
| PF_IDI07 | 98  | 48 | PB_IDI07 | NC       | 3  | 53  | NC       |
| PF_IDI06 | 97  | 47 | PB_IDI06 | NC       | 4  | 54  | NC       |
| PF_IDI05 | 96  | 46 | PB_IDI05 | NC       | 5  | 55  | NC       |
| PF_IDI04 | 95  | 45 | PB_IDI04 | NC       | 6  | 56  | NC       |
| PF_IDI03 | 94  | 44 | PB_IDI03 | P0_IDI00 | 7  | 57  | P4_IDI00 |
| PF_IDI02 | 93  | 43 | PB_IDI02 | P0_IDI01 | 8  | 58  | P4_IDI01 |
| PF_IDI01 | 92  | 42 | PB_IDI01 | P0_IDI02 | 9  | 59  | P4_IDI02 |
| PF_IDI00 | 91  | 41 | PB_IDI00 | P0_IDI03 | 10 | 60  | P4_IDI03 |
| PE_IDI07 | 90  | 40 | PA_IDI07 | P0_IDI04 | 11 | 61  | P4_IDI04 |
| PE_IDI06 | 89  | 39 | PA_IDI06 | P0_IDI05 | 12 | 62  | P4_IDI05 |
| PE_IDI05 | 88  | 38 | PA_IDI05 | P0_IDI06 | 13 | 63  | P4_IDI06 |
| PE_IDI04 | 87  | 37 | PA_IDI04 | P0_IDI07 | 14 | 64  | P4_IDI07 |
| PE_IDI03 | 86  | 36 | PA_IDI03 | P1_IDI00 | 15 | 65  | P5_IDI00 |
| PE_IDI02 | 85  | 35 | PA_IDI02 | P1_IDI01 | 16 | 66  | P5_IDI01 |
| PE_IDI01 | 84  | 34 | PA_IDI01 | P1_IDI02 | 17 | 67  | P5_IDI02 |
| PE_IDI00 | 83  | 33 | PA_IDI00 | P1_IDI03 | 18 | 68  | P5_IDI03 |
| NC       | 82  | 32 | NC       | P1_IDI04 | 19 | 69  | P5_IDI04 |
| NC       | 81  | 31 | NC       | P1_IDI05 | 20 | 70  | P5_IDI05 |
| NC       | 80  | 30 | NC       | P1_IDI06 | 21 | 71  | P5_IDI06 |
| NC       | 79  | 29 | NC       | P1_IDI07 | 22 | 72  | P5_IDI07 |
| NC       | 78  | 28 | NC       | P01_COMM | 23 | 73  | P45_COMM |
| NC       | 77  | 27 | NC       | P01_COMM | 24 | 74  | P45_COMM |
| NC       | 76  | 26 | NC       | NC       | 25 | 75  | NC       |
| NC       | 75  | 25 | NC       | NC       | 26 | 76  | NC       |
| PCD_COMM | 74  | 24 | P89_COMM | NC       | 27 | 77  | NC       |
| PCD_COMM | 73  | 23 | P89_COMM | NC       | 28 | 78  | NC       |
| PD_IDI07 | 72  | 22 | P9_IDI07 | NC       | 29 | 79  | NC       |
| PD_IDI06 | 71  | 21 | P9_IDI06 | NC       | 30 | 80  | NC       |
| PD_IDI05 | 70  | 20 | P9_IDI05 | NC       | 31 | 81  | NC       |
| PD_IDI04 | 69  | 19 | P9_IDI04 | NC       | 32 | 82  | NC       |
| PD_IDI03 | 68  | 18 | P9_IDI03 | P2_IDI00 | 33 | 83  | P6_IDI00 |
| PD_IDI02 | 67  | 17 | P9_IDI02 | P2_IDI01 | 34 | 84  | P6_IDI01 |
| PD_IDI01 | 66  | 16 | P9_IDI01 | P2_IDI02 | 35 | 85  | P6_IDI02 |
| PD_IDI00 | 65  | 15 | P9_IDI00 | P2_IDI03 | 36 | 86  | P6_IDI03 |
| PC_IDI07 | 64  | 14 | P8_IDI07 | P2_IDI04 | 37 | 87  | P6_IDI04 |
| PC_IDI06 | 63  | 13 | P8_IDI06 | P2_IDI05 | 38 | 88  | P6_IDI05 |
| PC_IDI05 | 62  | 12 | P8_IDI05 | P2_IDI06 | 39 | 89  | P6_IDI06 |
| PC_IDI04 | 61  | 11 | P8_IDI04 | P2_IDI07 | 40 | 90  | P6_IDI07 |
| PC_IDI03 | 60  | 10 | P8_IDI03 | P3_IDI00 | 41 | 91  | P7_IDI00 |
| PC_IDI02 | 59  | 9  | P8_IDI02 | P3_IDI01 | 42 | 92  | P7_IDI01 |
| PC_IDI01 | 58  | 8  | P8_IDI01 | P3_IDI02 | 43 | 93  | P7_IDI02 |
| PC_IDI00 | 57  | 7  | P8_IDI00 | P3_IDI03 | 44 | 94  | P7_IDI03 |
| NC       | 56  | 6  | NC       | P3_IDI04 | 45 | 95  | P7_IDI04 |
| NC       | 55  | 5  | NC       | P3_IDI05 | 46 | 96  | P7_IDI05 |
| NC       | 54  | 4  | NC       | P3_IDI06 | 47 | 97  | P7_IDI06 |
| NC       | 53  | 3  | NC       | P3_IDI07 | 48 | 98  | P7_IDI07 |
| NC       | 52  | 2  | NC       | P23_COMM | 49 | 99  | P67_COMM |
| NC       | 51  | 1  | NC       | P23_COMM | 50 | 100 | P67_COMM |

**Figure 3.2: I/O Connector Pin Assignment for PCI-1758UDI**

| CNB      |     |    | CNA      |          |    |     |          |
|----------|-----|----|----------|----------|----|-----|----------|
| PEF_COMP | 100 | 50 | PAB_COMP | P01_COMM | 1  | 51  | P45_COMM |
| PEF_COMP | 99  | 49 | PAB_COMP | P01_COMM | 2  | 52  | P45_COMM |
| PF_IDO07 | 98  | 48 | PB_IDO07 | P01_COMM | 3  | 53  | P45_COMM |
| PF_IDO06 | 97  | 47 | PB_IDO06 | P01_COMM | 4  | 54  | P45_COMM |
| PF_IDO05 | 96  | 46 | PB_IDO05 | P01_COMM | 5  | 55  | P45_COMM |
| PF_IDO04 | 95  | 45 | PB_IDO04 | P01_COMM | 6  | 56  | P45_COMM |
| PF_IDO03 | 94  | 44 | PB_IDO03 | P0_IDO00 | 7  | 57  | P4_IDO00 |
| PF_IDO02 | 93  | 43 | PB_IDO02 | P0_IDO01 | 8  | 58  | P4_IDO01 |
| PF_IDO01 | 92  | 42 | PB_IDO01 | P0_IDO02 | 9  | 59  | P4_IDO02 |
| PF_IDO00 | 91  | 41 | PB_IDO00 | P0_IDO03 | 10 | 60  | P4_IDO03 |
| PE_IDO07 | 90  | 40 | PA_IDO07 | P0_IDO04 | 11 | 61  | P4_IDO04 |
| PE_IDO06 | 89  | 39 | PA_IDO06 | P0_IDO05 | 12 | 62  | P4_IDO05 |
| PE_IDO05 | 88  | 38 | PA_IDO05 | P0_IDO06 | 13 | 63  | P4_IDO06 |
| PE_IDO04 | 87  | 37 | PA_IDO04 | P0_IDO07 | 14 | 64  | P4_IDO07 |
| PE_IDO03 | 86  | 36 | PA_IDO03 | P1_IDO00 | 15 | 65  | P5_IDO00 |
| PE_IDO02 | 85  | 35 | PA_IDO02 | P1_IDO01 | 16 | 66  | P5_IDO01 |
| PE_IDO01 | 84  | 34 | PA_IDO01 | P1_IDO02 | 17 | 67  | P5_IDO02 |
| PE_IDO00 | 83  | 33 | PA_IDO00 | P1_IDO03 | 18 | 68  | P5_IDO03 |
| PEF_COMM | 82  | 32 | PAB_COMM | P1_IDO04 | 19 | 69  | P5_IDO04 |
| PEF_COMM | 81  | 31 | PAB_COMM | P1_IDO05 | 20 | 70  | P5_IDO05 |
| PEF_COMM | 80  | 30 | PAB_COMM | P1_IDO06 | 21 | 71  | P5_IDO06 |
| PEF_COMM | 79  | 29 | PAB_COMM | P1_IDO07 | 22 | 72  | P5_IDO07 |
| PEF_COMM | 78  | 28 | PAB_COMM | P01_COMP | 23 | 73  | P45_COMP |
| PEF_COMM | 77  | 27 | PAB_COMM | P01_COMP | 24 | 74  | P45_COMP |
| NC       | 76  | 26 | NC       | NC       | 25 | 75  | NC       |
| NC       | 75  | 25 | NC       | NC       | 26 | 76  | NC       |
| P45_COMP | 74  | 24 | P89_COMP | P23_COMM | 27 | 77  | P67_COMM |
| P45_COMP | 73  | 23 | P89_COMP | P23_COMM | 28 | 78  | P67_COMM |
| P45_COMP | 72  | 22 | P9_IDO07 | P23_COMM | 29 | 79  | P67_COMM |
| P45_COMP | 71  | 21 | P9_IDO06 | P23_COMM | 30 | 80  | P67_COMM |
| P45_COMP | 70  | 20 | P9_IDO05 | P23_COMM | 31 | 81  | P67_COMM |
| P45_COMP | 69  | 19 | P9_IDO04 | P23_COMM | 32 | 82  | P67_COMM |
| P45_COMP | 68  | 18 | P9_IDO03 | P2_IDO00 | 33 | 83  | P6_IDO00 |
| P45_COMP | 67  | 17 | P9_IDO02 | P2_IDO01 | 34 | 84  | P6_IDO01 |
| P45_COMP | 66  | 16 | P9_IDO01 | P2_IDO02 | 35 | 85  | P6_IDO02 |
| P45_COMP | 65  | 15 | P9_IDO00 | P2_IDO03 | 36 | 86  | P6_IDO03 |
| P45_COMP | 64  | 14 | P8_IDO07 | P2_IDO04 | 37 | 87  | P6_IDO04 |
| P45_COMP | 63  | 13 | P8_IDO06 | P2_IDO05 | 38 | 88  | P6_IDO05 |
| P45_COMP | 62  | 12 | P8_IDO05 | P2_IDO06 | 39 | 89  | P6_IDO06 |
| P45_COMP | 61  | 11 | P8_IDO04 | P2_IDO07 | 40 | 90  | P6_IDO07 |
| P45_COMP | 60  | 10 | P8_IDO03 | P3_IDO00 | 41 | 91  | P7_IDO00 |
| P45_COMP | 59  | 9  | P8_IDO02 | P3_IDO01 | 42 | 92  | P7_IDO01 |
| P45_COMP | 58  | 8  | P8_IDO01 | P3_IDO02 | 43 | 93  | P7_IDO02 |
| P45_COMP | 57  | 7  | P8_IDO00 | P3_IDO03 | 44 | 94  | P7_IDO03 |
| P45_COMP | 56  | 6  | P89_COMM | P3_IDO04 | 45 | 95  | P7_IDO04 |
| P45_COMP | 55  | 5  | P89_COMM | P3_IDO05 | 46 | 96  | P7_IDO05 |
| P45_COMP | 54  | 4  | P89_COMM | P3_IDO06 | 47 | 97  | P7_IDO06 |
| P45_COMP | 53  | 3  | P89_COMM | P3_IDO07 | 48 | 98  | P7_IDO07 |
| P45_COMP | 52  | 2  | P89_COMM | P23_COMP | 49 | 99  | P67_COMP |
| P45_COMP | 51  | 1  | P89_COMM | P23_COMP | 50 | 100 | P67_COMP |

**Figure 3.3: I/O Connector Pin Assignment for PCI-1758UDO**

**Table 3.1: UDI Connector**

| <b>Signal Name</b> | <b>Reference</b> | <b>Direction</b> | <b>Description</b>               |
|--------------------|------------------|------------------|----------------------------------|
| P0_IDI00~ 07       | P01_COMM         | Input            | Isolated Digital Input of port 0 |
| P1_IDI00~ 07       | P01_COMM         | Input            | Isolated Digital Input of port 1 |
| P2_IDI00~ 07       | P23_COMM         | Input            | Isolated Digital Input of port 2 |
| P3_IDI00~ 07       | P23_COMM         | Input            | Isolated Digital Input of port 3 |
| P4_IDI00~ 07       | P45_COMM         | Input            | Isolated Digital Input of port 4 |
| P5_IDI00~ 07       | P45_COMM         | Input            | Isolated Digital Input of port 5 |
| P6_IDI00~ 07       | P67_COMM         | Input            | Isolated Digital Input of port 6 |
| P7_IDI00~ 07       | P67_COMM         | Input            | Isolated Digital Input of port 7 |
| P8_IDI00~ 07       | P89_COMM         | Input            | Isolated Digital Input of port 8 |
| P9_IDI00~ 07       | P89_COMM         | Input            | Isolated Digital Input of port 9 |
| PA_IDI00~ 07       | PAB_COMM         | Input            | Isolated Digital Input of port A |
| PB_IDI00~ 07       | PAB_COMM         | Input            | Isolated Digital Input of port B |
| PC_IDI00~ 07       | PCD_COMM         | Input            | Isolated Digital Input of port C |
| PD_IDI00~ 07       | PCD_COMM         | Input            | Isolated Digital Input of port D |
| PE_IDI00~ 07       | PEF_COMM         | Input            | Isolated Digital Input of port E |
| PF_IDI00~ 07       | PEF_COMM         | Input            | Isolated Digital Input of port F |
| P01_COMM           | -                |                  | Common port of port 0 and port 1 |
| P23_COMM           | -                |                  | Common port of port 2 and port 3 |
| P45_COMM           | -                |                  | Common port of port 4 and port 5 |
| P67_COMM           | -                |                  | Common port of port 6 and port 7 |
| P89_COMM           | -                |                  | Common port of port 8 and port 9 |
| PAB_COMM           | -                |                  | Common port of port A and port B |
| PCD_COMM           | -                |                  | Common port of port C and port D |
| PEF_COMM           | -                |                  | Common port of port E and port F |
| NC                 | -                |                  | Not Used                         |

**Table 3.2: PCI-1758UDO I/O Connector Signal Description**

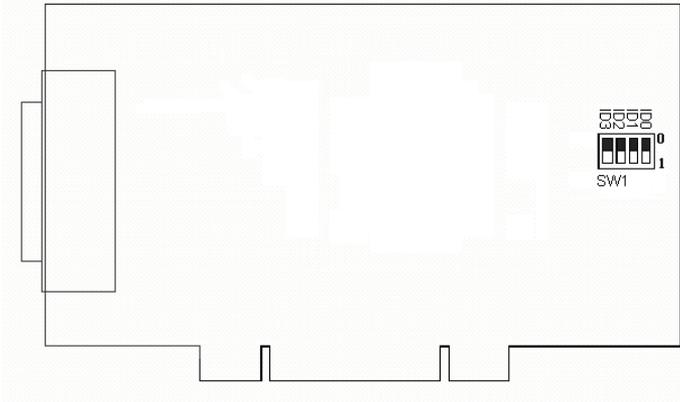
| <b>Signal Name</b> | <b>Reference</b> | <b>Direction</b> | <b>Description</b>                |
|--------------------|------------------|------------------|-----------------------------------|
| P0_IDO00~ 07       | P01_COMM         | Output           | Isolated Digital Output of port 0 |
| P1_IDO00~ 07       | P01_COMM         | Output           | Isolated Digital Output of port 1 |
| P2_IDO00~ 07       | P23_COMM         | Output           | Isolated Digital Output of port 2 |
| P3_IDO00~ 07       | P23_COMM         | Output           | Isolated Digital Output of port 3 |
| P4_IDO00~ 07       | P45_COMM         | Output           | Isolated Digital Output of port 4 |
| P5_IDO00~ 07       | P45_COMM         | Output           | Isolated Digital Output of port 5 |
| P6_IDO00~ 07       | P67_COMM         | Output           | Isolated Digital Output of port 6 |
| P7_IDO00~ 07       | P67_COMM         | Output           | Isolated Digital Output of port 7 |
| P8_IDO00~ 07       | P89_COMM         | Output           | Isolated Digital Output of port 8 |
| P9_IDO00~ 07       | P89_COMM         | Output           | Isolated Digital Output of port 9 |
| PA_IDO00~ 07       | PAB_COMM         | Output           | Isolated Digital Output of port A |
| PB_IDO00~ 07       | PAB_COMM         | Output           | Isolated Digital Output of port B |
| PC_IDO00~ 07       | PCD_COMM         | Output           | Isolated Digital Output of port C |
| PD_IDO00~ 07       | PCD_COMM         | Output           | Isolated Digital Output of port D |
| PE_IDO00~ 07       | PEF_COMM         | Output           | Isolated Digital Output of port E |
| PF_IDO00~ 07       | PEF_COMM         | Output           | Isolated Digital Output of port F |
| P01_COMM           | -                |                  | Negative external power supply    |
| P23_COMM           | -                |                  | Negative external power supply    |
| P45_COMM           | -                |                  | Negative external power supply    |
| P67_COMM           | -                |                  | Negative external power supply    |
| P89_COMM           | -                |                  | Negative external power supply    |
| PAB_COMM           | -                |                  | Negative external power supply    |
| PCD_COMM           | -                |                  | Negative external power supply    |
| PEF_COMM           | -                |                  | Negative external power supply    |
| P01_COMP           | -                |                  | Positive external power supply    |
| P23_COMP           | -                |                  | Positive external power supply    |
| P45_COMP           | -                |                  | Positive external power supply    |
| P67_COMP           | -                |                  | Positive external power supply    |
| P89_COMP           | -                |                  | Positive external power supply    |
| PAB_COMP           | -                |                  | Positive external power supply    |
| PCD_COMM           | -                |                  | Positive external power supply    |
| PEF_COMM           | -                |                  | Positive external power supply    |
| NC                 | -                | -                | Not used                          |

Note: Each PEF\_COMM pin can tolerate no more than 300 mA. Make sure that every PEF\_COMM pin is properly connected to the equipment's ground (GND).

## 3.2 Location of Jumper and DIP Switch

---

Figure 3-3, and 3-4 show the names and locations of jumpers and DIP switches on the PCI-1758UDI/1758UDO. There is one DIP switch SW1 on PCI-1758UDI. There is one DIP switch SW1 and one jumper JP1 on the PCI-1758UDO.



**Figure 3.4: Location of DIP Switch on PCI-1758UDI**



**Figure 3.5: Location of DIP Switch and Jumper on PCI-1758UDO**

### 3.3 Isolated Digital Input Connections

The PCI-1758UDI has 128 isolated digital input channels designated:

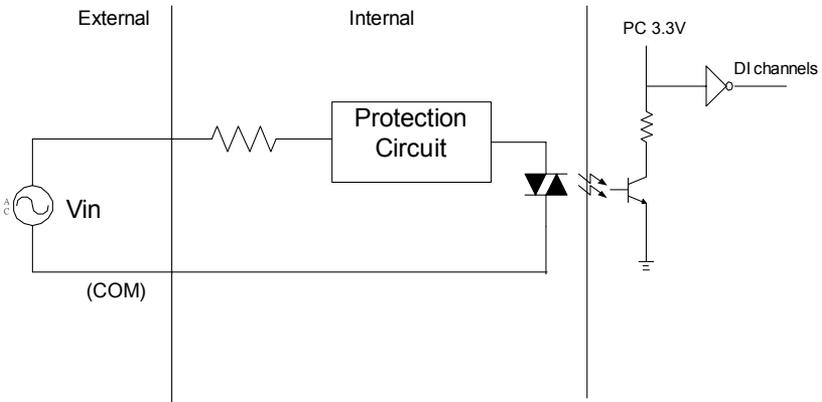
P0\_IDI00~07, P1\_IDI00~07, P2\_IDI00~07, P3\_IDI00~07,  
P4\_IDI00~07, P5\_IDI00~07, P6\_IDI00~07, P7\_IDI00~07,  
P8\_IDI00~07, P9\_IDI00~07, PA\_IDI00~07, PB\_IDI00~07,  
PC\_IDI00~07, PD\_IDI00~07, PE\_IDI00~07, PF\_IDI00~07

#### 3.3.1 Interrupt Function of the DI Signals

All 128 channels in PCI-1758UDI can be used to generate hardware interrupts. Setup the configuration of interrupts by programming the interrupt control register. For detailed information, please refer to Section 5.1 Interrupt Function.

#### 3.3.2 Isolated Inputs

Each of the isolated digital input channels accepts 5~25 VDC voltage inputs, and also accept bi-directional input. This means that you can apply positive or negative voltage to an isolated input pin. Each group of 16 channels share one common pin. Figure 3-5 shows how to connect an external input source to one of the card's isolated input channels.



**Figure 3.6: Isolated Digital Input Connection**

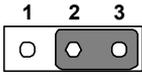
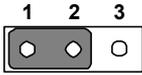
## 3.4 Isolated Digital Output Connections

The PCI-1758UDO has 128 isolated digital output channels designated P0\_IDO00~7, P1\_IDO00~7, P2\_IDO00~7, P3\_IDO00~7, P4\_IDO00~7, P5\_IDO00~7, P6\_IDO00~7, P7\_IDO00~7, P8\_IDO00~7, P9\_IDO00~7, PA\_IDO00~7, PB\_IDO00~7, PC\_IDO00~7, PD\_IDO00~7, PE\_IDO00~7, and PF\_IDO00~7.

### 3.4.1 Power On Configuration

The default configuration will be set after power is turned on. The hardware reset sets all the isolated output channels to "off" status (The current of the load can not be sink mode). So you do not need to worry about damaging external devices during system startup or reset. When the system is hot reset, the status of the isolated digital output channels can be selected by jumper JP1. Table 3-3 shows the configuration of jumper JP1.

**Table 3.3: JP3: Power On Configuration after Hot Reset**

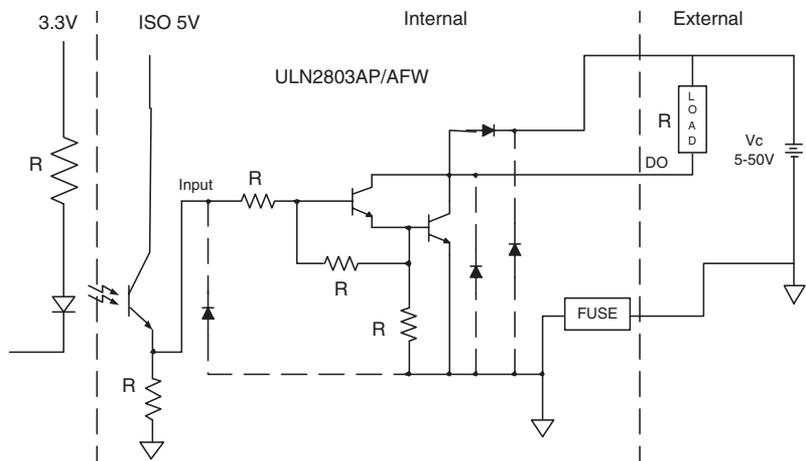
| PCI-1758UDO JP1   | Power on configuration after hot reset              |
|---|---|
|  | Keep the last digital output status after hot reset |
|  | Load Default configuration while reset              |

### 3.4.2 Isolated Outputs

Each of the isolated output channels is equipped with a Darlington transistor. All of the 16 output channels shares common collectors and integral suppression diodes for induction coil loads.

Figure 3-7 on next page shows how to connect an external output load to the card's isolated outputs..

*Note: If an external voltage (5 ~ 40 VDC) is applied to an isolated output channel while it is being used as an output channel, the current will flow from the external voltage source to the card. Please be cautious about that the current flowing through each IDO pin can not exceed 90 mA.*



**Figure 3.7: Isolated Digital Output Connection**

## 3.5 Field Wiring Considerations

When you use the PCI-1758UDI to acquire data from outside, noises in the environment might significantly affect the accuracy of your measurements if due cautions are not taken. The following measures will be helpful to reduce possible interference in the signal wires between signal sources and the PCI-1758UDI.

- Keep the signal cables away from strong electromagnetic sources such as power lines, large electric motors, circuit breakers or welding machines, since they may cause strong electromagnetic interference. Keep the analog signal cables away from any video monitor, since it can significantly affect a data acquisition system.
- If the cable travels through an area with significant electromagnetic interference, you should adopt individually shielded, twisted-pair wires as the analog input cable. This type of cable has its signal wires twisted together and shielded with a metal mesh. The metal mesh should only be connected to one point at the signal source ground.
- Avoid running the signal cables through any conduit that might have power lines in it.
- If you have to place your signal cable parallel to a power line that has a high voltage or high current running through it, try to keep a safe distance between them. Or you should place the signal cable at a right angle to the power line to minimize the disturbance.

## Operation

This chapter describes the operation of PCI-1758UDI and PCI-1758UDO. The provided software driver gives you access all of the card's functions without having to do register level programming. If you prefer to implement your own bit-level programming, please refer to the following information.

Sections include:

- Interrupt Function
- Digital Filter Function
- Watchdog Timer Function
- Power-Up States Function
- BoardID

# Chapter 4 Operation

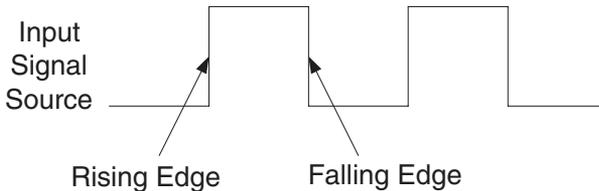
## 4.1 Interrupt Function (PCI-1758UDI)

---

PCI-1758UDI provides an interrupt function for every digital input channel. All the isolated digital input channels are connected to the interrupt circuitry. You can disable/enable the interrupt function, and select trigger type by setting the Rising Edge Interrupt Registers and Falling Edge Interrupt Registers of the PCI-1758UDI. When the interrupt request signals occur, the software will service these interrupt requests by ISR. The multiple interrupt sources provide the card with more capability and flexibility.

### 4.1.1 Interrupt Modes for Digital Input

There are four registers that control the function and status of each input interrupt signal source. They give you the ability to select different modes to match different applications. The four registers are: Interrupt State Register, Rising Edge Interrupt Register, Falling Edge Interrupt Register and Port Identify Register. The detailed functions of these registers are described in Appendix C.



*Figure 4.1: Interrupt Mode for Digital Input*

## 4.2 Digital Filter Function (PCI-1758UDI)

---

The digital filter function is used to eliminate glitches on input data and reduce the number of changes to examine and process. The filter blocks pulses that are shorter than the specified timing interval, and passes pulses that are double the length of the specified interval. Intermediate-length pulses—pulses longer than half of the interval but less than the interval, may or may not pass the filter.

The following table lists the pulse widths guaranteed to be passed and blocked.

**Table 4.1: Pulse Width Filtering**

| Filter Interval | Pulse Width Passed |            | Pulse Width Blocked |               |
|-----------------|--------------------|------------|---------------------|---------------|
|                 | Low Pulse          | High Pulse | Low Pulse           | High Pulse    |
| Tinterval       | Tinterval          | Tinterval  | (Tinterval/2)       | (Tinterval/2) |

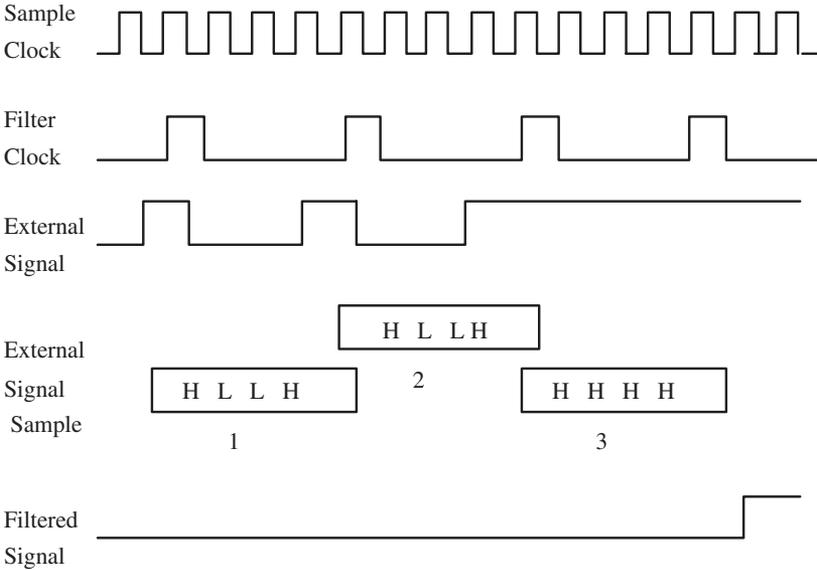
You can enable or disable filtering on every input channel as is necessary for your application. All filtered channels share the same timing interval, which ranges from 200 ns to 400 sec.

There are two clocks in the filter: the sample clock and the filter clock. The sample clock has a period of 100 ns. The filter clock is generated by a counter and has a period equal to one half of the specified timing interval. The input signal is sampled on each rising edge of the sample clock. However, a change in the input signal is recognized only if it maintains its new state for at least two consecutive rising edges of the filter clock.

The filter clock is programmable and allows you to control how long a pulse must last to be recognized by write a value to Filter interval time Preset register high 16 bits.

### 4.2.1 Digital Filtering Example

The following figure shows a filter configuration with an 800 ns filter interval (400 ns filter clock).



**Figure 4.2: Digital Filter Example**

In periods 1 and 2, the filter blocks the glitches because the external signal does not remain steadily high from one filter clock to the next. In period 3, the filter passes the transition because the external signal remains steadily high. Depending on when the transition occurs, the filter may require up to two filter clocks—one full filter interval—to pass a transition. The figure shows a rising (0 to 1) transition. The same filtering applies to falling (1 to 0) transitions.

### 4.2.2 Digital Filter Function Control Register

There are two registers that control the digital filter function and status of each channel: the Digital Filter Function Control Register and the Filter Interval Time Preset Register. For details about their functions, please refer to Appendix C.

### **4.3 Watchdog Timer Function (PCI-1758UDO)**

---

This feature is used to set critical outputs to safe states in the event of a software failure. When the watchdog timer is enabled, PCI-1758UDO has to receive a “watchdog clear” software command within the interval time specified for the watchdog timer. If it doesn’t, this is considered a loss of communication between the application and PCI-1758UDO, and the outputs go to a user-defined safe state and remain in that state until the watchdog timer is disabled and new values are written by software.

After the watchdog timer expires, the PCI-1758UDO will ignore any writes until the watchdog timer is disabled. You can set the watchdog timer timeout period through the WDT register to specify the amount of time that must elapse before the watchdog timer expires. The counter on the watchdog timer is configurable up to  $(2^{32}-1) \times 100$  ns (approximately seven minutes) before it expires.

For more details about the watchdog timer register operation, please refer to Appendix C.

### **4.4 Power-Up States Function (PCI-1758UDO)**

---

User-configurable power-up states are useful for ensuring that the PCI-1758UDO powers up in a known state. When the system is powered-up, all output lines of PCI-1758UDO are user-configurable for logic high output or logic low output. So you can predefine the outputs. This function ensures the card’s output state can be defined at any time.

Power-up states are programmed in the EEPROM with a driver. In the EEPROM Control Register you can write the predefined output data to EEPROM. The default value from the factory is all set to 0. For more details about register operations, please refer to appendix C.

## 4.5 Board ID (PCI-1758UDI/UDO)

The PCI-1758UDI/1758UDO has a built-in DIP-switch (SW1), which is used to define each card's BoardID. You can determine the BoardID on the register as shown on Table 4-5. When there are multiple cards on the same chassis, this BoardID setting function is useful for identifying each card's device number through BoardID. We set the PCI-1758UDI/1758UDO BoardID as 0 at the factory. If you need to adjust it to other BoardIDs, set SW1 while referring to Table 4-3.

**Table 4.2: Board ID Register of PCI-1758UDI/1758UDO**

| Board ID register of PCI-1758UDI |     |     |     |     |
|----------------------------------|-----|-----|-----|-----|
| Base Add.+ 56h                   | 3   | 2   | 1   | 0   |
| Abbreviation                     | ID3 | ID2 | ID1 | ID0 |
| Board ID register of PCI-1758UDO |     |     |     |     |
| Base Add.+ 1Ch                   | 3   | 2   | 1   | 0   |
| Abbreviation                     | ID3 | ID2 | ID1 | ID0 |

ID0: the least significant bit (LSB) of BoardID

ID3: the most significant bit (MSB) of BoardID

**Table 4.3: BoardID Setting (SW1)**

| Board ID(DEC) | Switch Position |     |     |     |
|---------------|-----------------|-----|-----|-----|
|               | ID3             | ID2 | ID1 | ID0 |
| 0*            | ON              | ON  | ON  | ON  |
| 1             | ON              | ON  | ON  | OFF |
| 2             | ON              | ON  | OFF | ON  |
| 3             | ON              | ON  | OFF | OFF |
| 4             | ON              | OFF | ON  | ON  |
| 5             | ON              | OFF | ON  | OFF |
| 6             | ON              | OFF | OFF | ON  |
| 7             | ON              | OFF | OFF | OFF |
| 8             | OFF             | ON  | ON  | ON  |
| 9             | OFF             | ON  | ON  | OFF |
| 10            | OFF             | ON  | OFF | ON  |
| 11            | OFF             | ON  | OFF | OFF |
| 12            | OFF             | OFF | ON  | ON  |
| 13            | OFF             | OFF | ON  | OFF |
| 14            | OFF             | OFF | OFF | ON  |
| 15            | OFF             | OFF | OFF | OFF |
| *: Default    |                 |     |     |     |

APPENDIX  
**A**

**Specifications**

# Appendix A Specifications

## A.1 Specifications

---

### A.1.1 Isolated Digital Input

|                                    |                 |              |
|------------------------------------|-----------------|--------------|
| <b>Model Name</b>                  |                 | PCI-1758UDI  |
| <b>Number of Input Channels</b>    |                 | 128          |
| <b>Interrupt Inputs</b>            |                 | 128          |
| <b>Optical Isolation</b>           |                 | 2500 VDC     |
| <b>Opto-Isolator Response Time</b> |                 | 50 $\mu$ s   |
| <b>Input Voltage</b>               | <b>VIH(max)</b> | 25 V         |
|                                    | <b>VIH(min)</b> | 5 V          |
|                                    | <b>VIL(max)</b> | 2.5 V        |
| <b>Input Resistance</b>            |                 | 3 k $\Omega$ |

### A.1.2 Isolated Digital Output

|                                    |  |                    |
|------------------------------------|--|--------------------|
| <b>Model Name</b>                  |  | PCI-1758UDO        |
| <b>Number of Input Channels</b>    |  | 128                |
| <b>Optical Isolation</b>           |  | 2500 VDC           |
| <b>Opto-Isolator Response Time</b> |  | 50 $\mu$ s         |
| <b>Supply Voltage</b>              |  | 5-40 V             |
| <b>Sink Current</b>                |  | 90 mA max./Channel |

### A.1.3 General

|                           |                  |  |                    |
|---------------------------|------------------|--|--------------------|
| <b>Model Name</b>         |                  | <b>PCI-1758UDI</b>                                 | <b>PCI-1758UDO</b> |
| <b>I/O Connector Type</b> |                  | MINI-SCSI HDRA-E100 Female                         |                    |
| <b>Dimensions</b>         |                  | 175 x 100 mm (6.9" x 3.9")                         |                    |
| <b>Power Consumption</b>  | <b>Typical</b>   | +5V@ 0.3A  | +5V@ 1.1A          |
|                           | <b>Max.</b>      | +5V@ 0.6A  | +5V@ 2.2A          |
| <b>Temperature</b>        | <b>Operating</b> | 0 ~ 60° C (32 ~ 140° F)<br>(refer to IEC 68-2-1,2) |                    |
|                           | <b>Storage</b>   | -20 ~ 70° C (-4 ~ 158° F)                          |                    |
| <b>Relative Humidity</b>  |                  | 5 ~ 95 % RH non-condensing (refer to IEC 68-2-3)   |                    |



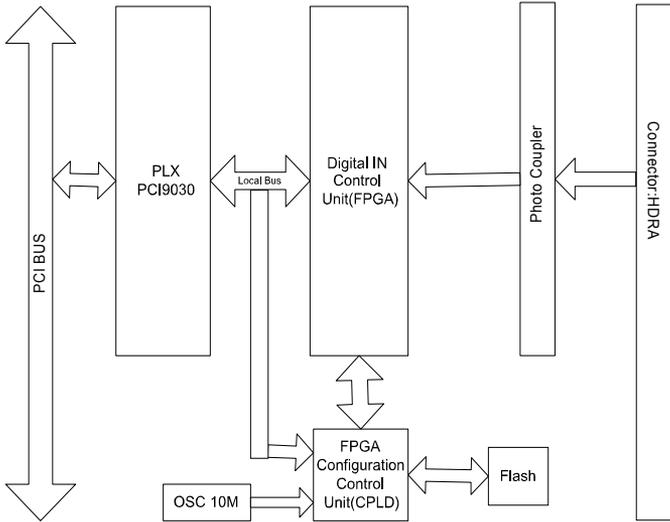
APPENDIX

# B

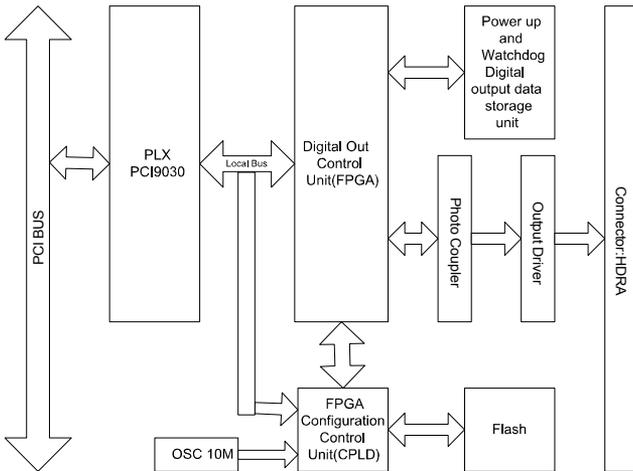
## Block Diagram

# Appendix B Block Diagram

## B.1 PCI-1758UDI Block Diagram



## B.2 PCI-1758UDO Block Diagram



APPENDIX

C

## **Register Structure and Format**

# Appendix C Register Structure & Format

## C.1 Register Structure

---

PCI-1758UDI/1758UDO is delivered with an easy-to-use 32-bit DLL driver for user programming under the Windows 98/2000/XP operating system. You are advised to program the PCI-1758UDI /1758UDO using the 32-bit DLL driver provided by Advantech to avoid the complexity of low-level programming by register.

The most important consideration in programming the PCI-1758UDI/1758UDO at the register level is to understand the function of the card's registers. The information in the following sections is provided only for those who would like to do their own low-level programming.

The PCI-1758UDI requires 84 consecutive addresses in the PC's I/O space. The address of each register is specified as an offset from the card's base address. For example, BASE+0 is the card's base address and BASE+8 is the base address plus seven bytes.

*Note*                      *All registers only support 16-bit data access.*

## C.2 PCI-1758UDI Register Format

---

### C.2.1 Register Format

| Address offset(H EX) | Register Description |                                 |
|----------------------|----------------------|---------------------------------|
|                      | Write                | Read                            |
| 0                    |                      | Digital Input Port 0 and Port 1 |
| 2                    |                      | Digital Input Port 2 and Port 3 |
| 4                    |                      | Digital Input Port 4 and Port 5 |
| 6                    |                      | Digital Input Port 6 and Port 7 |
| 8                    |                      | Digital Input Port 8 and Port 9 |
| A                    |                      | Digital Input Port A and Port B |
| C                    |                      | Digital Input Port C and Port D |
| E                    |                      | Digital Input Port E and Port F |

|    |  |  |
|----|--|--|
| 10 | DI Port 0 and Port1 Rising Edge Interrupt Register   | DI Port 0 and Port1 Rising Edge Interrupt Register   |
| 12 | DI Port 0 and Port1 Falling Edge Interrupt Register  | DI Port 0 and Port1 Falling Edge Interrupt Register  |
| 14 | DI Port2 and Port3 Rising Edge Interrupt Register    | DI Port2 and Port3 Rising Edge Interrupt Register    |
| 16 | DI Port 2 and Port3 Falling Edge Interrupt Register  | DI Port 2 and Port3 Falling Edge Interrupt Register  |
| 18 | DI Port 4 and Port5 Rising Edge Interrupt Register   | DI Port 4 and Port5 Rising Edge Interrupt Register   |
| 1A | DI Port4 and Port5 Falling Edge Interrupt Register   | DI Port4 and Port5 Falling Edge Interrupt Register   |
| 1C | DI Port 6 and Port7 Rising Edge Interrupt Register   | DI Port6 and Port7 Rising Edge Interrupt Register    |
| 1E | DI Port6 and Port7 Falling Edge Interrupt Register   | DI Port6 and Port7 Falling Edge Interrupt Register   |
| 20 | DI Port 8 and Port9 Rising Edge Interrupt Register   | DI Port 8 and Port9 Rising Edge Interrupt Register   |
| 22 | DI Port8 and Port9 Falling Edge Interrupt Register   | DI Port8 and Port9 Falling Edge Interrupt Register   |
| 24 | DI Port A and Port B Rising Edge Interrupt Register  | DI Port A and Port B Rising Edge Interrupt Register  |
| 26 | DI Port A and Port B Falling Edge Interrupt Register | DI Port A and Port B Falling Edge Interrupt Register |
| 28 | DI Port C and Port D Rising Edge Interrupt Register  | DI Port C and Port D Rising Edge Interrupt Register  |
| 2A | DI Port C and Port D Falling Edge Interrupt Register | DI Port C and Port D Falling Edge Interrupt Register |
| 2C | DI Port E and Port F Rising Edge Interrupt Register  | DI Port E and Port F Rising Edge Interrupt Register  |
| 2E | DI Port E and Port F Falling Edge Interrupt Register | DI Port E and Port F Falling Edge Interrupt Register |
| 30 | Port 0 and Port 1 Interrupt State Register           | Port 0 and Port 1 Interrupt State Register           |
| 32 | Port 2 and Port 3 Interrupt State Register           | Port 2 and Port 3 Interrupt State Register           |
| 34 | Port 4 and Port 5 Interrupt State Register           | Port 4 and Port 5 Interrupt State Register           |
| 36 | Port 6 and Port 7 Interrupt State Register           | Port 6 and Port 7 Interrupt State Register           |
| 38 | Port 8 and Port 9 Interrupt State Register           | Port 8 and Port 9 Interrupt State Register           |
| 3A | Port A and Port B Interrupt State Register           | Port A and Port B Interrupt State Register           |
| 3C | Port C and Port D Interrupt State Register           | Port C and Port D Interrupt State Register           |
| 3E | Port E and Port F Interrupt State Register           | Port E and Port F Interrupt State Register           |

|    |  |  |
|----|--|--|
| 40 | Port 0 and Port 1 Digital filter Enable Register | Port 0 and Port 1 Digital filter Enable Register |
| 42 | Port 2 and Port 3 Digital filter Enable Register | Port 2 and Port 3 Digital filter Enable Register |
| 44 | Port 4 and Port 5 Digital filter Enable Register | Port 4 and Port 5 Digital filter Enable Register |
| 46 | Port 6 and Port 7 Digital filter Enable Register | Port 6 and Port 7 Digital filter Enable Register |
| 48 | Port 8 and Port 9 Digital filter Enable Register | Port 8 and Port 9 Digital filter Enable Register |
| 4A | Port A and Port B Digital filter Enable Register | Port A and Port B Digital filter Enable Register |
| 4C | Port C and Port D Digital filter Enable Register | Port C and Port D Digital filter Enable Register |
| 4E | Port E and Port F Digital filter Enable Register | Port E and Port F Digital filter Enable Register |
| 50 |  | Interrupt of Port Identify Register              |
| 52 | Filter interval time preset low 16 bits          | Filter interval time preset low 16 bits          |
| 54 | Filter interval time preset high 16 bits         | Filter interval time preset high 16 bits         |
| 56 |  | Board ID   |

## C.2.2 Digital Input Register

Base+0x00/02/04/06/08/0A/0C/0E: Digital Input value

| Base+0x00 – 0x0E(Read) |          |          |          |          |          |          |          |          |          |          |          |          |          |          |          |
|------------------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit 15                 | Bit 14   | Bit 13   | Bit 12   | Bit 11   | Bit 10   | Bit 9    | Bit 8    | Bit 7    | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    |
| P1 IDI 7               | P1 IDI 6 | P1 IDI 5 | P1 IDI 4 | P1 IDI 1 | P1 IDI 2 | P1 IDI 1 | P1 IDI 0 | P0 IDI 7 | P0 IDI 6 | P0 IDI 5 | P0 IDI 4 | P0 IDI 1 | P0 IDI 2 | P0 IDI 1 | P0 IDI 0 |

| Base+0x00 – 0x0E (Write) |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
|--------------------------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 15                   | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| N/A                      |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |

Bit 15 – Bit 0(Read):

0: The Pn-IDIm input photo couple is inaction

1: The Pn-IDIm input photo couple is active

( n : 0 to F is for Port 0 to Port F, m : 0 to 7 is for IDI0 to IDI7 )

Base+0x00 for Port 0 and Port 1

Base+0x02 for Port 2 and Port 3

Base+0x04 for Port 4 and Port 5

Base+0x06 for Port 6 and Port 7

Base+0x08 for Port 8 and Port 9

Base+0x0A for Port A and Port B

Base+0x0C for Port C and Port D

Base+0x0E for Port E and Port F

### C.2.3 Digital Input Rising Edge Interrupt Register

Base+0x10/14/18/1C/20/24/28/2C: Digital Input Rising Edge Interrupt setting.

| Base+0x10- 0x2C (Write/Read) |         |         |         |         |         |         |         |         |         |         |         |         |         |         |         |
|------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Bit 15                       | Bit 14  | Bit 13  | Bit 12  | Bit 11  | Bit 10  | Bit 9   | Bit 8   | Bit 7   | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1   | Bit 0   |
| P1 IDI7                      | P1 IDI6 | P1 IDI5 | P1 IDI4 | P1 IDI1 | P1 IDI2 | P1 IDI1 | P1 IDI0 | P0 IDI7 | P0 IDI6 | P0 IDI5 | P0 IDI4 | P0 IDI1 | P0 IDI2 | P0 IDI1 | P0 IDI0 |

Bit 15 – Bit 0(Write):

0 : Disable the Pn-IDIm Rising Edge interrupt function

1 : Enable the Pn-IDIm Rising Edge interrupt function

( n : 0 to F is for Port 0 to Port F, m : 0 to 7 is for IDI0 to IDI7 )

Bit 15 – Bit 0(Read): Read back the setting value.

Base+0x10 for Port 0 and Port 1

Base+0x14 for Port 2 and Port 3

Base+0x18 for Port 4 and Port 5

Base+0x1C for Port 6 and Port 7

Base+0x20 for Port 8 and Port 9  
 Base+0x24 for Port A and Port B  
 Base+0x28 for Port C and Port D  
 Base+0x2C for Port E and Port F

### C.2.4 Digital Input Falling Edge Interrupt Register

Base+0x12/16/1A/1E/22/26/2A/2E: Digital Input Falling Edge Interrupt setting

| <b>Base+0x12 – 0x2E (Write/Read)</b> |         |         |         |         |         |         |         |         |         |         |         |         |         |         |         |
|--------------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Bit 15                               | Bit 14  | Bit 13  | Bit 12  | Bit 11  | Bit 10  | Bit 9   | Bit 8   | Bit 7   | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1   | Bit 0   |
| P1 IDI7                              | P1 IDI6 | P1 IDI5 | P1 IDI4 | P1 IDI1 | P1 IDI2 | P1 IDI1 | P1 IDI0 | P0 IDI7 | P0 IDI6 | P0 IDI5 | P0 IDI4 | P0 IDI1 | P0 IDI2 | P0 IDI1 | P0 IDI0 |

Bit 15 – Bit 0(Write):

0 : Disable the Pn-IDIm Falling Edge interrupt function

1 : Enable the Pn-IDIm Falling Edge interrupt function

( n : 0 to F for Port 0 to Port F, m : 0 to 7 for IDI0 to IDI7 )

Bit 15 – Bit 0(Read): Read back the setting value.

Base+0x12 for Port 0 and Port 1

Base+0x16 for Port 2 and Port 3

Base+0x1A for Port 4 and Port 5

Base+0x1E for Port 6 and Port 7

Base+0x22 for Port 8 and Port 9

Base+0x26 for Port A and Port B

Base+0x2A for Port C and Port D

Base+0x2E for Port E and Port F

## C.2.5 Interrupt State Register

Base+0x30/32/34/36/38/3A/3C/3E: Interrupt state setting.

| Base+0x30 – 0x3E (Write/Read) |         |         |         |         |         |         |         |         |         |         |         |         |         |         |         |
|-------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Bit 15                        | Bit 14  | Bit 13  | Bit 12  | Bit 11  | Bit 10  | Bit 9   | Bit 8   | Bit 7   | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1   | Bit 0   |
| P1 IDI7                       | P1 IDI6 | P1 IDI5 | P1 IDI4 | P1 IDI1 | P1 IDI2 | P1 IDI1 | P1 IDI0 | P0 IDI7 | P0 IDI6 | P0 IDI5 | P0 IDI4 | P0 IDI1 | P0 IDI2 | P0 IDI1 | P0 IDI0 |

This register can read and clear the status of the interrupt flag. If an interrupt occurs, users can check the status of 0x50 (refer to C.2.1.5) to identify in which port the interrupt occurred. Then users can read the identified port to the register from 0x30 to 0x3E to know in which bit an interrupt occurs.

If users want to clear the interrupt flag, just identify where the interrupt occurs and then write “1” into that register directly.

Bit 15 – Bit 0(Read): Read the Interrupt Flag Status

1: means an interrupt flag occurs in Pn-IDIm

0: means no interrupt flag occurs in Pn-IDIm

( n : 0 to F for Port 0 to Port F, m : 0 to 7 for IDI0 to IDI7 )

To identify in which port an interrupt occurs, please refer to the C.2.1.5

Bit 15 – Bit 0(Write): Clear the Interrupt Flag.

1: Clear the interrupt flag in Pn-IDIm

0: Keep the interrupt flag status in Pn-IDIm

Base+0x30 for Port 0 and Port 1

Base+0x32 for Port 2 and Port 3

Base+0x34 for Port 4 and Port 5

Base+0x36 for Port 6 and Port 7

Base+0x38 for Port 8 and Port 9

Base+0x3A for Port A and Port B

Base+0x3C for Port C and Port D

Base+0x3E for Port E and Port F

## C.2.6 Interrupt of Port Identify Register

Address=base address + 50.

| Base+0x50 (Read) |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
|------------------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 15           | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| PF               | PE     | PD     | PC     | PB     | PA     | P9    | P8    | P7    | P6    | P5    | P4    | P3    | P2    | P1    | P0    |

Bit0~Bit15 (Read): Identify in which port an interrupt occurs from port 0 to port F.

1: means an interrupt occurs in this port.

0: means no interrupt occurs in this port.

There are two registers which control the digital filter function and status of each channel: **Digital Filter Enable Register** and **Filter Interval Time Preset Register**.

## C.2.7 Digital Filter Function Control Register

Base+0x40/42/44/46/48/4A/4C/4E: Digital Filter Function Control Register

| Base+0x40- 0x4E (Write/Read) |         |         |         |         |         |         |         |         |         |         |         |         |         |         |         |
|------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Bit 15                       | Bit 14  | Bit 13  | Bit 12  | Bit 11  | Bit 10  | Bit 9   | Bit 8   | Bit 7   | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1   | Bit 0   |
| P1 IDI7                      | P1 IDI6 | P1 IDI5 | P1 IDI4 | P1 IDI1 | P1 IDI2 | P1 IDI1 | P1 IDI0 | P0 IDI7 | P0 IDI6 | P0 IDI5 | P0 IDI4 | P0 IDI1 | P0 IDI2 | P0 IDI1 | P0 IDI0 |

Bit 15 – Bit 0(write):

0: Disable the Pn-IDIm digital filter function

1: Enable the Pn-IDIm digital filter function

Bit 15 – Bit 0(Read):

0: Disable the Pn-IDIm digital filter function

1: Enable the Pn-IDIm digital filter function

(n: 0 to F for Port 0 to Port F, m : 0 to 7 for IDI0 to IDI7 )

Base+0x40 for Port 0 and Port 1

Base+0x42 for Port 2 and Port 3

Base+0x44 for Port 4 and Port 5  
 Base+0x46 for Port 6 and Port 7  
 Base+0x48 for Port 8 and Port 9  
 Base+0x4A for Port A and Port B  
 Base+0x4C for Port C and Port D  
 Base+0x4E for Port E and Port F

### C.2.8 Filter Interval Time Preset Register

| Base+0x52 (Write/Read)                           |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
|--|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 15   | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Filter interval time preset register low 16 bits |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |

| Base+0x54 (Write/Read)                            |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
|---|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 15  | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Filter interval time preset register high 16 bits |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |

The filter interval time is preset by writing a 32-bit value to the two registers. The high 16 bits should be written to Filter Interval Time Preset register high 16 bits and the low 16 bits should be written to Filter Interval Time Preset register low 16 bits. The value written to the two registers is calculated by the following formula:

$$T_{\text{interval}} = \text{Value} \times 200 \text{ ns}$$

**For example:**

Filter Interval Time Preset register high 16 bits =0x0001;

Filter Interval Time Preset register low 16 bits =0x0000;

Value = 0x00010000;

$$T_{\text{interval}} = \text{Value} \times 200\text{ns}=13107200\text{ns};$$

## C.3 PCI-1758 UDO Register Format

| Base Address | Register Description                 |  |
|--------------|--------------------------------------|--|
|              | Write                                | Read                                       |
| <b>0</b>     | Digital Output Port 0 and Port 1     | Digital Output Port 0 and port 1 Read Back |
| <b>2</b>     | Digital Output Port 2 and Port 3     | Digital Output Port 2 and Port 3 Read Back |
| <b>4</b>     | Digital Output Port 4 and Port 5     | Digital Output Port 4 and Port 5 Read Back |
| <b>6</b>     | Digital Output Port 6 and Port 7     | Digital Output Port 6 and Port 7 Read Back |
| <b>8</b>     | Digital Output Port 8 and Port 9     | Digital Output Port 8 and Port 9 Read Back |
| <b>A</b>     | Digital Output Port A and Port B     | Digital Output Port A and Port B Read Back |
| <b>C</b>     | Digital Output Port C and Port D     | Digital Output Port C and Port D Read Back |
| <b>E</b>     | Digital Output Port E and Port F     | Digital Output Port E and Port F Read Back |
| <b>10</b>    | Watchdog counter values low 16 bits  | Watchdog counter values low 16 bits        |
| <b>12</b>    | Watchdog counter values high 16 bits | Watchdog counter values high 16 bits       |
| <b>14</b>    | Watchdog timer control Register      | Watchdog timer state Register              |
| <b>16</b>    | Watchdog timer clear Register        | N/A  |
| <b>18</b>    | N/A                                  | N/A  |
| <b>1A</b>    | EEPROM Control Register              | EEPROM DO Status                           |
| <b>1C</b>    | N/A                                  | Board ID                                   |

### C.3.1 Digital Output Register

Base+0x00/02/04/06/08/0A/0C/0E: Digital Output Register.

| Base+0x00- 0x0E (Write/Read) |         |         |         |         |         |         |         |         |         |         |         |         |         |         |         |
|------------------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| Bit 15                       | Bit 14  | Bit 13  | Bit 12  | Bit 11  | Bit 10  | Bit 9   | Bit 8   | Bit 7   | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1   | Bit 0   |
| P1 IDO7                      | P1 IDO6 | P1 IDO5 | P1 IDO4 | P1 IDO3 | P1 IDO2 | P1 IDO1 | P1 IDO0 | P0 IDO7 | P0 IDO6 | P0 IDO5 | P0 IDO4 | P0 IDO1 | P0 IDO2 | P0 IDO1 | P0 IDO0 |

Bit 15 – Bit 0(Write):

0 : The Pn-IDOm output photo couple is inaction

1 : The Pn-IDOm output photo couple is active

Bit 15 – Bit 0(Read back):

0 : The Pn-IDOm output photo couple is inaction

1 : The Pn-IDOm output photo couple is active

( n : 0 to F for Port 0 to Port F, m : 0 to 7 for IDO0 to IDO7 )

Base+0x00 for Port 0 and Port 1

Base+0x02 for Port 2 and Port 3

Base+0x04 for Port 4 and Port 5

Base+0x06 for Port 6 and Port 7

Base+0x08 for Port 8 and Port 9

Base+0x0A for Port A and Port B

Base+0x0C for Port C and Port D

Base+0x0E for Port E and Port F

### C.3.2 Watchdog Counter Value Register

Base+0x10/12: Watchdog Counter Value Register.

| Base+0x10 (Write/Read)              |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
|-------------------------------------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 15                              | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Watchdog counter values low 16 bits |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |

| Base+0x12 (Write/Read)               |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
|--------------------------------------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit 15                               | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Watchdog counter values high 16 bits |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |

Watchdog timer Interval = WDT x 100ns

For example:

Watchdog timer values high 16 bits Register=0x0001;

Watchdog timer values low 16 bits Register=0x0000;

WDT=0x00010000;

Watchdog timer Interval = WDT x 100ns=6553600ns;

### C.3.3 Watchdog State/Control Register

Base+0x14 : WDT function setting

| Base+0x14 (Write) |            |        |
|-------------------|------------|--------|
| Bit 15 – Bit 2    | Bit 1      | Bit 0  |
| N/A               | WDT INT EN | WDT En |

Bit 0:

0 : Disable WDT function

1 : Enable WDT function

(When the WDT is enable then the watch dog timer (WDT) in PCI-1758UDO start count down from the value set in Base+0x10h and Base+0x12h)

Bit 1:

0 : Disable WDT interrupt function when WDT count down to 0

1 : Enable WDT interrupt function when WDT count down to 0

| <b>Base+0x14 (Read)</b> |                  |              |              |
|-------------------------|------------------|--------------|--------------|
| <b>Bit 15 – Bit 3</b>   | <b>Bit 2</b>     | <b>Bit 1</b> | <b>Bit 0</b> |
| N/A                     | WDT Timeout flag | WDT INT EN   | WDT En       |

Bit 0: Read the status of WDT En

Bit 1: Read the status of WDT INT EN

Bit 2:

0 : WDT current value is not 0

1 : WDT current value is 0

### **C.3.4 Watchdog Timer Clear Register**

Base+0x16 : Watchdog timer reset Register

| <b>Base+0x16 (Write)</b> |              |
|--------------------------|--------------|
| <b>Bit 15 – Bit 1</b>    | <b>Bit 0</b> |
| N/A                      | WDI          |

Bit 0:

0 : Reset the Watchdog Timer to pre-set value

1 : Keep the Watchdog Timer current state

*Note It is recommended that you implement the function in base+0x1A through the driver instead of through this register directly.*

### **C.3.5 EEPROM Control/DO state Register**

Base+0x1A : EEPROM DO state Register

| <b>Base+0x1A (Read)</b> |              |
|-------------------------|--------------|
| <b>Bit 15 – Bit 1</b>   | <b>Bit 0</b> |
| N/A                     | DO           |

Bit 0:

EEPROM DO state

| <b>Base+0x1A (Write)</b> |              |              |              |              |
|--------------------------|--------------|--------------|--------------|--------------|
| <b>Bit 15 – Bit 4</b>    | <b>Bit 3</b> | <b>Bit 2</b> | <b>Bit 1</b> | <b>Bit 0</b> |
| N/A                      | CS           | CLK          | DI           | DO           |

Through this register user can set the power up status and watchdog timer overflow states in the eeprom.

- CS: eeprom select
- CLK: eeprom clk
- DI: eeprom data in
- DO: eeprom data out
- The data format of EEPROM:

| <b>Address</b> | <b>Stored data description</b> | <b>Stored data class</b>           |
|----------------|--------------------------------|------------------------------------|
| 0x00           | P1_IDO & P0_IDO                | Digital output power up values     |
| 0x01           | P3_IDO & P2_IDO                |                                    |
| 0x02           | P5_IDO & P4_IDO                |                                    |
| 0x03           | P7_IDO & P6_IDO                |                                    |
| 0x04           | P9_IDO & P8_IDO                |                                    |
| 0x05           | PB_IDO & PA_IDO                |                                    |
| 0x06           | PD_IDO & PC_IDO                |                                    |
| 0x07           | PF_IDO & PE_IDO                |                                    |
| 0x10           | P1_IDO & P0_IDO                | Digital output WDT overflow values |
| 0x11           | P3_IDO & P2_IDO                |                                    |
| 0x12           | P5_IDO & P4_IDO                |                                    |
| 0x13           | P7_IDO & P6_IDO                |                                    |
| 0x14           | P9_IDO & P8_IDO                |                                    |
| 0x15           | PB_IDO & PA_IDO                |                                    |
| 0x16           | PD_IDO & PC_IDO                |                                    |
| 0x17           | PF_IDO & PE_IDO                |                                    |

## C.4 Board ID Register (For UDO and UDI)

You can determine the BoardID on the register as shown on table below. When there are multiple cards on the same chassis, this BoardID setting function is useful for identifying each card's device number through BoardID. We set the PCI-1758UDI/1758UDO BoardID as 0 at the factory. If you need to adjust it to other board ID, set the SW1 by referring to the table.

| Board ID register of PCI-1758UDI |     |     |     |     |
|----------------------------------|-----|-----|-----|-----|
| Base Add.+ 56h                   | 3   | 2   | 1   | 0   |
| Abbreviation                     | ID3 | ID2 | ID1 | ID0 |
| Board ID register of PCI-1758UDO |     |     |     |     |
| Base Add.+ 1Ch                   | 3   | 2   | 1   | 0   |
| Abbreviation                     | ID3 | ID2 | ID1 | ID0 |

ID0: the least significant bit (LSB) of Board ID

ID3: the most significant bit (MSB) of Board ID

| Board ID Setting (SW1) |                 |     |     |     |
|------------------------|-----------------|-----|-----|-----|
| Board ID(DEC)          | Switch Position |     |     |     |
|                        | ID3             | ID2 | ID1 | ID0 |
| 0*                     | ON              | ON  | ON  | ON  |
| 1                      | ON              | ON  | ON  | OFF |
| 2                      | ON              | ON  | OFF | ON  |
| 3                      | ON              | ON  | OFF | OFF |
| 4                      | ON              | OFF | ON  | ON  |
| 5                      | ON              | OFF | ON  | OFF |
| 6                      | ON              | OFF | OFF | ON  |
| 7                      | ON              | OFF | OFF | OFF |
| 8                      | OFF             | ON  | ON  | ON  |
| 9                      | OFF             | ON  | ON  | OFF |
| 10                     | OFF             | ON  | OFF | ON  |
| 11                     | OFF             | ON  | OFF | OFF |
| 12                     | OFF             | OFF | ON  | ON  |
| 13                     | OFF             | OFF | ON  | OFF |
| 14                     | OFF             | OFF | OFF | ON  |
| 15                     | OFF             | OFF | OFF | OFF |
| *: Default             |                 |     |     |     |

