R32C/100 Series

Using DMAC II with Chained Transfer

REJ05B1415-0100
Rev.1.00
July 30, 2010

1. Abstract

This document describes the setting method to perform a chained transfer using DMAC II.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

- MCUs: R32C/116 Group
  R32C/117 Group
  R32C/118 Group

This application note can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the above groups. Check the manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Outline

In a chained transfer, a data transfer is sequentially performed according to a DMAC II index (transfer information) linked with the previous transfer.
Table 3.1 lists selectable functions when using chained transfer mode, and the settings in this document. Table 3.2 lists the number of transfers and transfer sources in this document, and the DMAC II triggers. Figure 3.1 shows an operation example of a chained transfer when using an INT0 interrupt to trigger DMAC II.

Table 3.1 Selectable Functions when Using Chained Transfer Mode and Document Settings

Item	Selectable Function	Setting
Transfer sizes	8 bits 16 bits	8 bits
Transfer sources	Immediate data Memory	Memory
Source addressing	Non-incrementing addressing Incrementing addressing	Incrementing addressing
Destination addressing	Non-incrementing addressing Incrementing addressing	Non-incrementing addressing
Transfer modes	Single transfer Burst transfer	Single transfer
Calculation transfer	Calculation not used Calculation used	Calculation not used
DMA II transfer complete interrupt	Interrupt not generated Interrupt generated	Interrupt not generated

Table 3.2 Number of Transfers and Transfer Sources, and DMAC II Triggers

Item	Settings
Number of transfers	5 times + 5 times
Transfer sources	DMAC II index (1): 11h, 22h, 33h, 44h, 55h DMAC II index (2): FFh, EEh, DDh, CCh, BBh
DMAC II trigger	INT0 interrupt

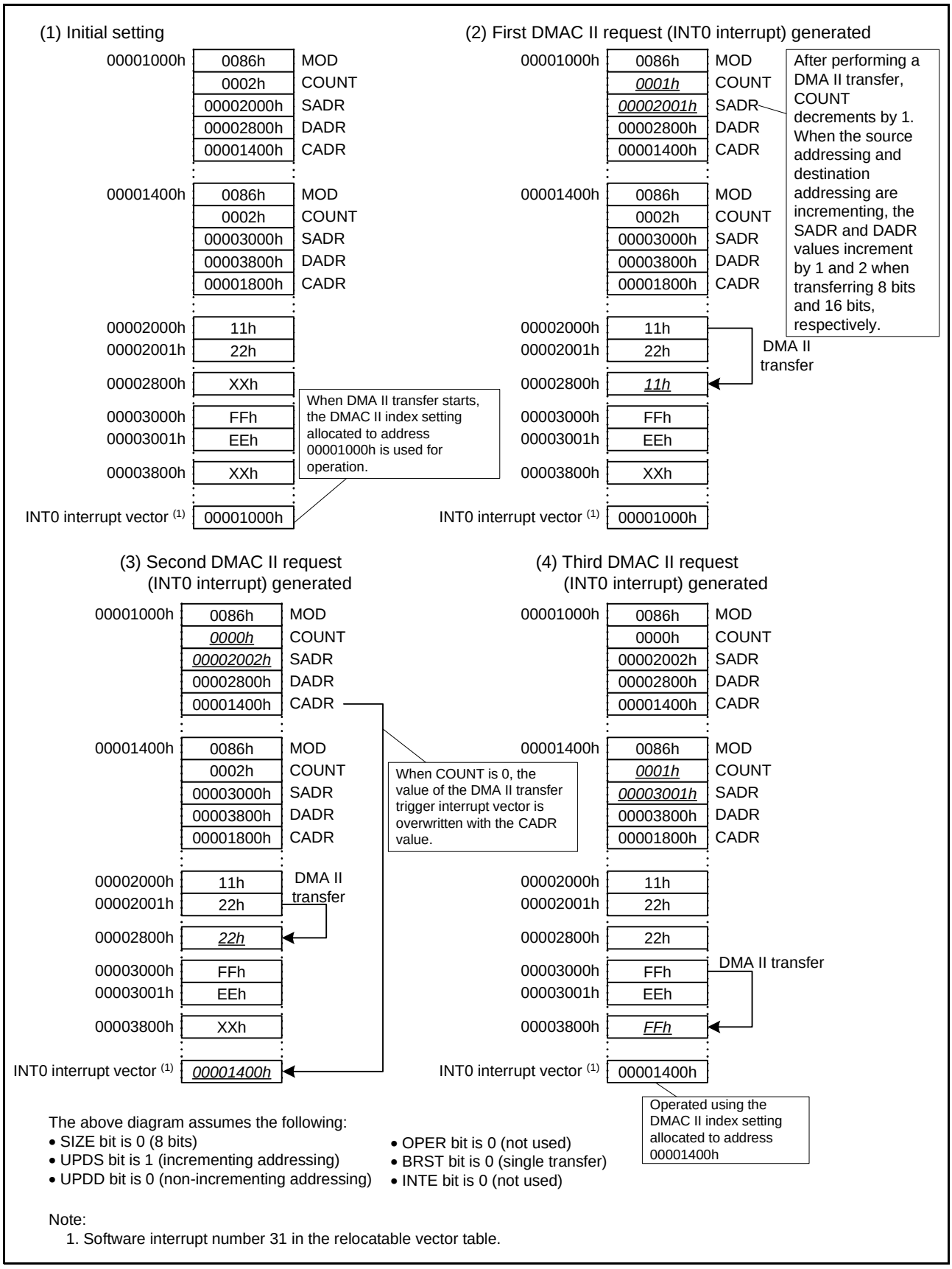


Figure 3.1 Operation Example of Chained Transfer Using an INT0 Interrupt to Trigger DMAC II

4. Settings

This chapter explains the settings for performing a chained transfer using DMAC II.

4.1 DMAC II Settings

To activate DMAC II, set the following:

- Registers RIPL1 and RIPL2
- DMAC II index
- The interrupt control register of the peripheral function triggering DMAC II
- The relocatable vector of the peripheral function triggering DMAC II
- The IRLT bit in the IIOiIE register if the intelligent I/O interrupt is used (i = 0 to 11). Refer to the hardware user's manual for details on the IIOiIE register.

4.1.1 Registers RIPL1 and RIPL2

When the DMAII bits in both the RIPL1 and RIPL2 registers are set to 1 (DMA II transfer selected) and the FSIT bits are set to 0 (normal interrupt selected), DMAC II is activated by an interrupt request from any peripheral function with bits ILVL2 to ILVL0 in the corresponding interrupt control register set to 111b (level 7). Registers RIPL1 and RIPLS should be set with the same value.

Table 4.1 lists the setting values of registers RIPL1 and RIPL2 as used in this document.

Table 4.1 Setting Values of Registers RIPL1 and RIPL2

Register Symbol	Setting Value	Remarks
RIPL1, RIPL2	20h	• Bits RLVL2 to RLVL0 are 000b (level 0) • FSIT bit is 0 (use interrupt request level 7 for normal interrupt) • DMAII bit is 1 (use interrupt request level 7 for DMA II transfer) • b7 and b6 are 0

4.1.2 DMAC II Index

The DMAC II index is a data table of 16 to 24 bytes when performing a chained transfer. The data table stores parameters for transfer mode, transfer counter, source address, operation address as an address to be calculated, destination address, chained transfer base address, and DMA II transfer complete interrupt vector address. This DMAC II index should be allocated on the RAM.
Figure 4.1 shows the DMAC II index as set in this document.

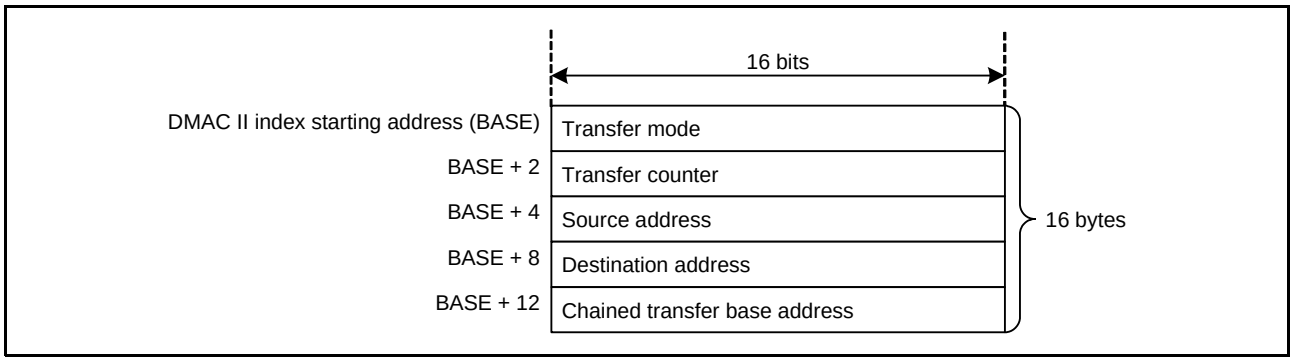


Figure 4.1 DMAC II Index Configuration When Using Memory-to-memory Transfer and Chained Transfer, and Not Using DMA II Transfer Complete Interrupt

The following is an explanation of the DMAC II index contents as shown in Figure 4.1.

- Transfer mode (MOD)
  2-byte data is required to set transfer mode.
- Transfer counter (COUNT)
  2-byte data is required to set the number of transfers to be performed.
- Source address (SADR)
  4-byte data is required to set a source address in a memory.
- Destination address (DADR)
  4-byte data is required to set a destination address in a memory.
- Chained transfer base address (CADR)
  4-byte data is required to set BASE, the starting address of the DMAC II index for the next transfer.

4.1.3 Interrupt Control Register of the Peripheral Function

Set bits ILVL2 to ILVL0 in the interrupt control register for the peripheral interrupt triggering DMAC II to 111b (level 7).

4.1.4 Relocatable Vector Table of the Peripheral Function

Set the starting address of the DMAC II index to the interrupt vector for the peripheral function interrupt triggering DMAC II. In this document, the DMAC II trigger is the INT0 interrupt.
Figure 4.2 shows an example of setting the asm function in a C language program. In this example, the DMAC II index (dm_index) is set to the relocatable vector table.

```
asm( "   .rvector 31, _dm_index" );     // Define DMAC II Index (Software Interrupt Number 31)
```

Figure 4.2 Setting Example for the Relocatable Vector Table of the Peripheral Function When Using the INT0 Interrupt to Trigger DMAC II

To use the chained transfer, allocate the relocatable vector table on the RAM.
Figure 4.3 shows an example of allocating the relocatable vector on the RAM in a C language program. This example uses the memcpy function, so include “string.h” in the standard library.

```
memcpy(ram_vect,S_VECTOR,256*4);  // Copy the relocatable vector table on the RAM
asm("   ldc     #_ram_vect, intb    ");    // The relocatable vector table should be located on the RAM
```

Figure 4.3 Allocating the Relocatable Vector Table on the RAM

When the transfer counter (COUNT) reaches 0000h, the value of the interrupt vector for the peripheral function interrupt triggering DMAC II is overwritten with the DMAC II index chained transfer base address (CADR).

4.2 Setting Procedure

Figure 4.4 shows the DMAC II chained transfer setting procedure. Refer to section 4.3 “Detailed Settings” for details on each step.

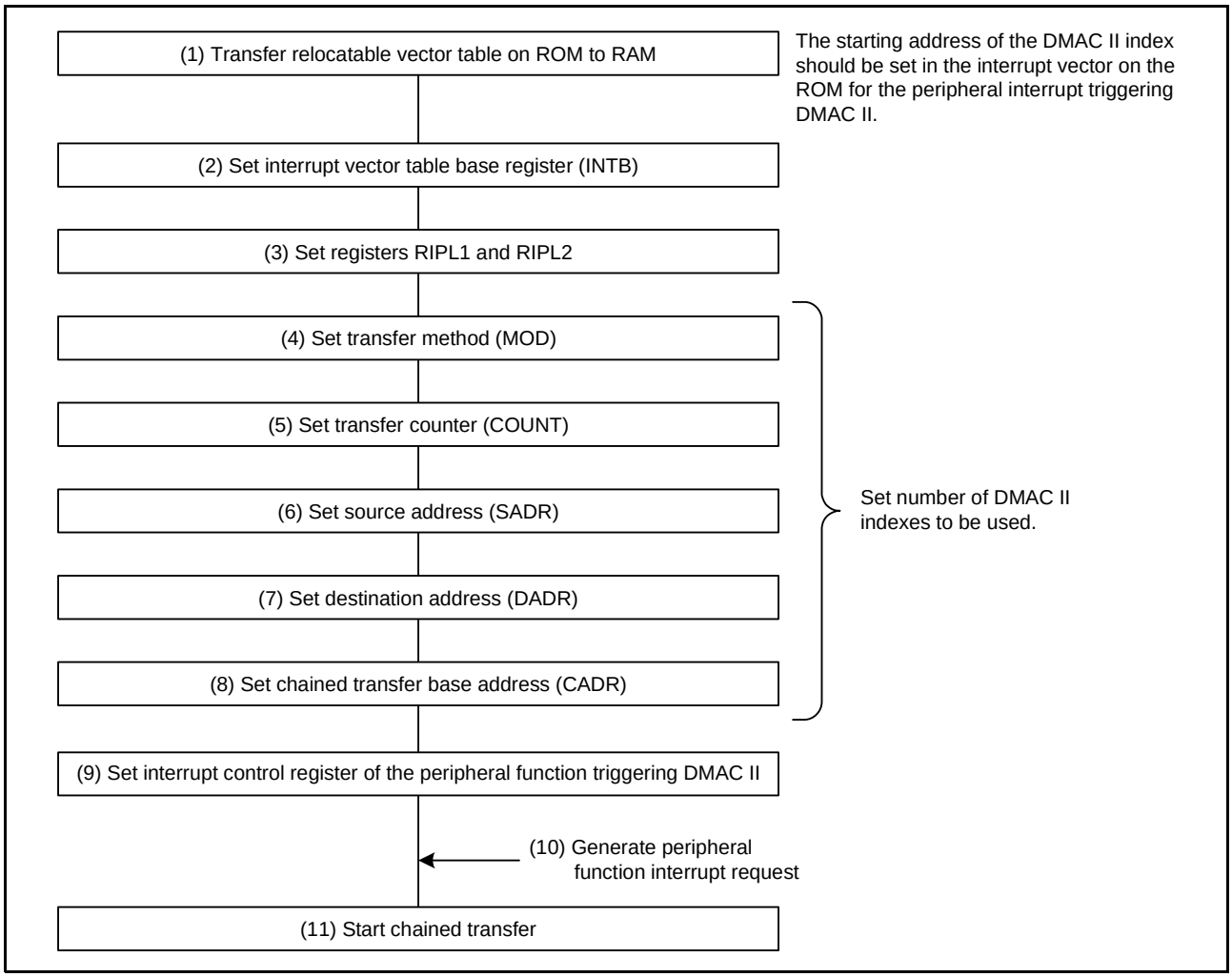


Figure 4.4 DMAC II Chained Transfer Setting Procedure

4.3 Detailed Settings

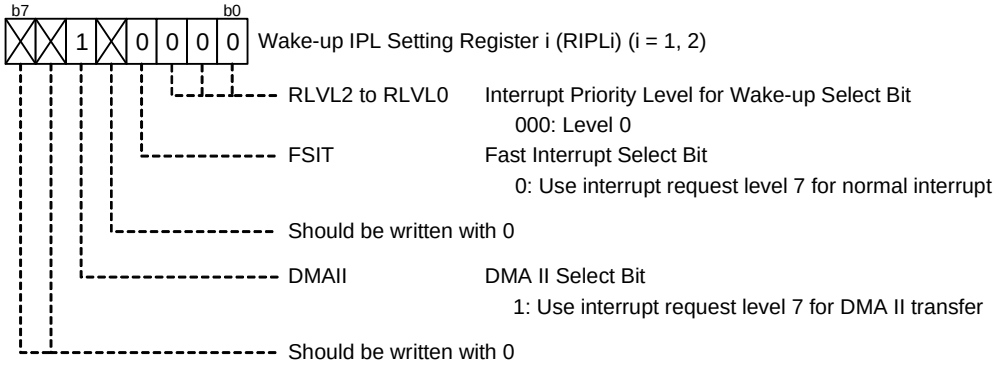
(1) Transfer relocatable vector table on ROM to RAM.

Transfer the relocatable vector table from ROM to RAM. The starting address of the DMAC II index should be set in the interrupt vector on the ROM for the peripheral function interrupt triggering DMAC II.

(2) Set the interrupt vector table base register (INTB).

In the INTB register, set the start address of the relocatable vector table allocated on the RAM.

(3) Set registers RIPL1 and RIPL2.



Registers RIPL1 and RIPL2 should be set with the same value.

Bits ILVL2 to ILVL0 in the interrupt control register should be set after the DMAII bit is set. DMAC II transfer is not affected by the I flag or the IPL.

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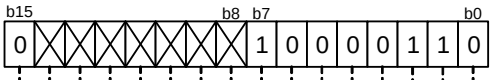
(4) Set the transfer mode (MOD).

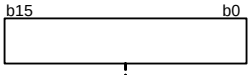
Allocate on the RAM.



Transfer Mode (MOD)

SIZE	Transfer Size Select Bit	0: 8 bits
IMM	Transfer Source Select Bit	1: Memory
UPDS	Source Addressing Select Bit	1: Incrementing addressing
UPDD	Destination Addressing Select Bit	0: Non-incrementing addressing
OPER	Calculation Transfer Select Bit	0: Not used
BRST	Burst Transfer Select Bit	0: Single transfer
INTE	DMA II Transfer Complete Interrupt Select Bit	0: Not used
CHAIN	Chained Transfer Select Bit	1: Used
Should be written with 0		
MULT	Multiple Transfer Select Bit	0: Not used

(5) Set the transfer counter (COUNT).



Transfer counter (COUNT)

Set the number of transfers to be performed

Transfers are not performed when the transfer counter is set to 0000h.

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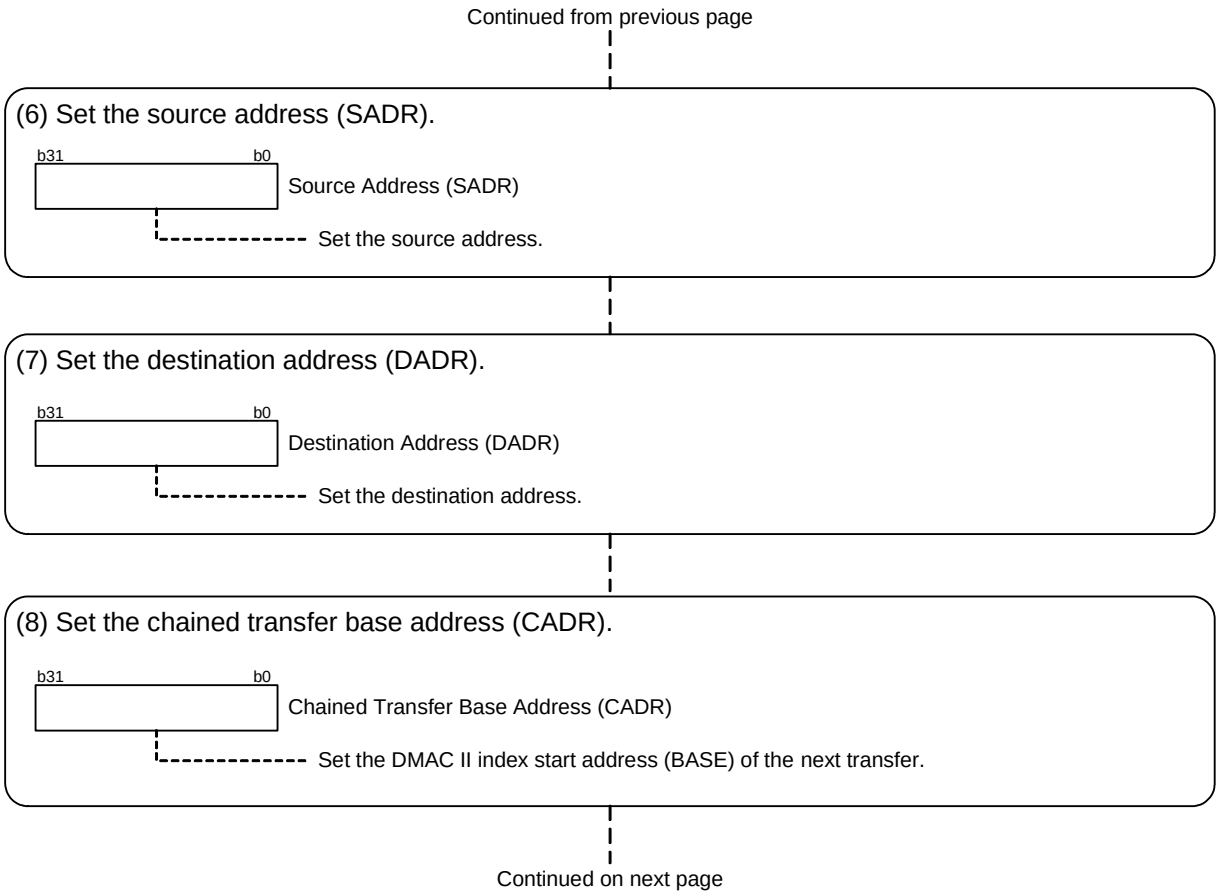
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(6) Set the source address (SADR).
b31
b0
Source Address (SADR)
Set the source address.
(7) Set the destination address (DADR).
b31
b0
Destination Address (DADR)
Set the destination address.
(8) Set the chained transfer base address (CADR).
b31
b0
Chained Transfer Base Address (CADR)
Set the DMAC II index start address (BASE) of the next transfer.
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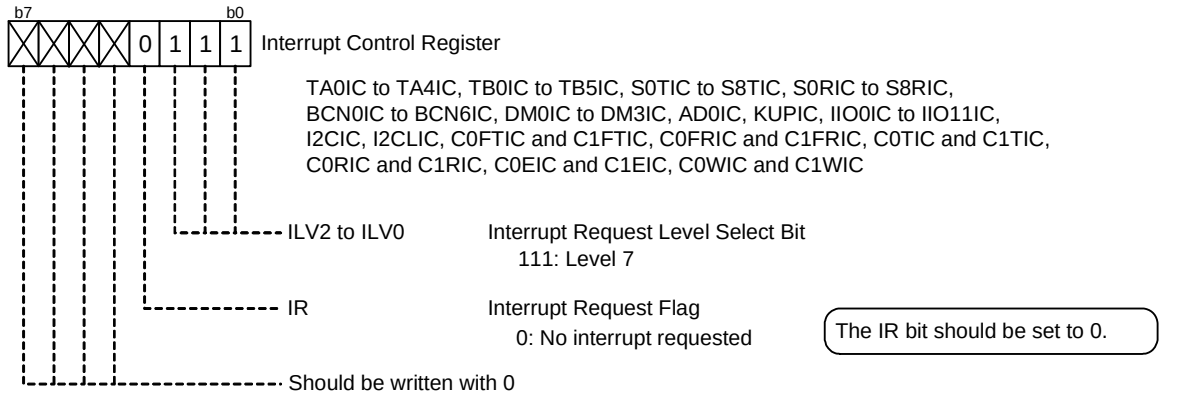
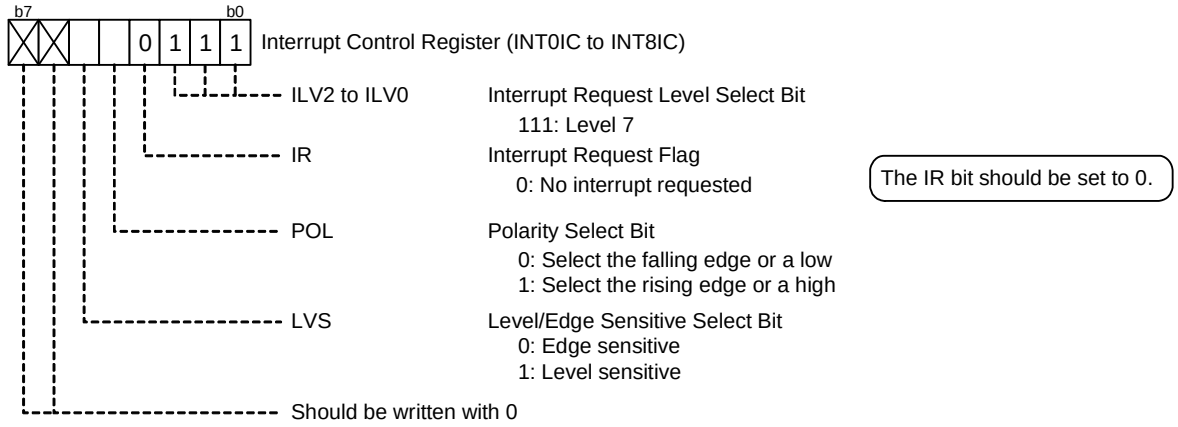
(9) Set the interrupt control register of the peripheral function triggering DMAC II.

To trigger DMAC II using peripheral function interrupts, set all bits ILVL2 to ILVL0 (level 7) to 111b.





The POL bit should be set to 0 (select the falling edge or a low) to set the corresponding bit in registers IFSR0 and IFSR1 to 1 (both edges).

When using the LVS bit to select the level sensitive, the corresponding bit in registers IFSR0 and IFSR1 should be set to 0 (one edge).

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(10) Generate peripheral function interrupt request.

Generate an interrupt request for the peripheral function interrupt set to trigger DMAC II.

(11) Start chained transfer.

When the peripheral function interrupt request is received and DMAC II chained transfer starts, the transfer counter (COUNT) decrements by 1. When COUNT reaches 000h, the peripheral function interrupt relocatable vector value is overwritten with the chained transfer base address (CADR), and the next DMAC II index is started.

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

5.1 Explanation

The following explains the sample program operation.

(1) Allocating the relocatable vector table on the RAM
The relocatable vector table on the ROM is transferred to RAM. After allocating it to RAM, the start address of the relocatable vector table is set to the interrupt vector table base register (INTB).

(2) Setting the DMAC II index
Two DMAC II indexes are set. One CHAIN bit is set to 1 (used), and the other is set to 0 (not used).

(3) Setting the DMA II trigger
The INT0 interrupt control register is set as the DMA II trigger.

(4) Operation after starting DMA II transfer
After generating a transfer request, when the transfer counter (COUNT) is 0000h, the chained transfer base address (CADR) value is overwritten by the interrupt vector value. All subsequent transfers follow the DMAC II index (chained transfers not used) indicated by the overwritten interrupt vector value.

5.2 Program Flowchart

The sample program is configured with the main function. Figure 5.1 shows the main function flowchart.

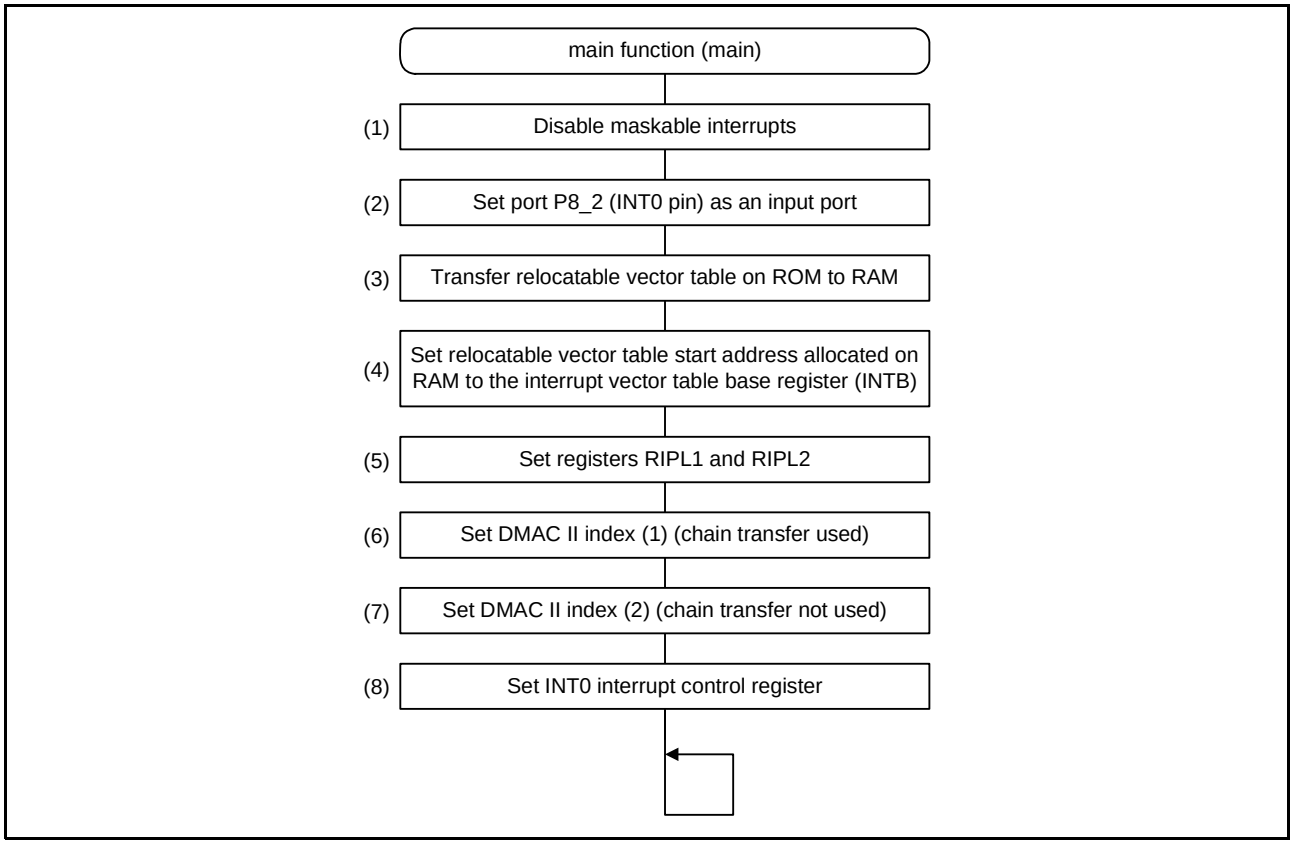

Figure 5.1 main Function Flowchart

6. Reference Documents

R32C/116 Group User's Manual: Hardware Rev.1.00
R32C/117 Group User's Manual: Hardware Rev.1.00
R32C/118 Group User's Manual: Hardware Rev.1.00
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler User's Manual
R32C/100 Series C Compiler Package V.1.02
C Compiler User's Manual Rev.2.00
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Revision History	R32C/100 Series Using DMAC II with Chained Transfer

Rev.	Date	Description	
		Page	Summary
1.00	July 30, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

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1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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