Acromag®

Series IP340 and IP341 Industrial I/O Pack Simultaneous Sample and Hold Module

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The Industrial I/O Pack (IP) Series IP340 (12-bit) and IP341 (14-bit) modules are precision, single size IP, simultaneous sampling analog input boards. Sixteen differential analog input channels are provided with an input range of ±10 volts.

The 16 differential analog voltage input channels are converted as two banks of eight channels. After the first bank of eight channels are simultaneously converted, the second bank of 8 channels can then be simultaneously converted as a group at the time specified in a user programmable delay counter.

All 16-channels share a generous 512-sample FIFO buffer, from which digitized values are read. Since all channels share the same FIFO, data tagging is implemented for easy identification of corresponding channel data. To minimize CPU interaction, FIFO interrupt generation is also supported upon reaching a FIFO programmable threshold condition.

The IP340 and IP341 modules interface to the VMEbus, PCIbus, or ISAbus, carrier boards. Up to five units may be mounted on the PCIbus carrier board to provide up to 80 differential analog input channels per PCI system slot.

The IP340/1 utilizes state of the art Surface-Mounted Technology (SMT) to achieve its wide functionality and is an ideal choice for a wide range of industrial and scientific applications that require, high-performance analog inputs.

The IP340 and IP341 modules are available in standard and extended temperature range modules as follows:

Model	Resolution	512 Sample FIFO Buffer	Temperature Range
IP340	12-bit	Yes	0 to +70°C
IP340E	12-bit	Yes	-40°C to +85°C
IP341	14-bit	Yes	0 to +70°C
IP341E	14-bit	Yes	-40°C to +85°C

KEY IP340/341 FEATURES

- **ADC 12-Bit and 14-Bit Resolution** - Eight individual 12-bit (IP340) and 14-bit (IP341) successive approximation Analog to Digital Converters (ADC) with integral sample and hold are utilized.
- **8µsec Conversion Time** - A maximum conversion rate of 125KHz is supported.
- **512 Sample FIFO Buffer -** A single 512 sample deep FIFO is available for buffering data from the 16 differential channels. This allows the external processor to service more tasks within a given time. Data tagging is implemented for easy channel data identification.
- **Interrupt Upon FIFO Threshold Condition** - FIFO interrupt generation is also supported. Upon reaching a FIFO programmable threshold condition an interrupt can be generated, to minimize CPU interaction.
- **FIFO Full, Empty, and Threshold Reached Flags-** FIFO Full, Empty, and Threshold Reached flag bits are available to implement software polling schemes for FIFO buffer data control.
- **Programmable Control of Channels Converted** - Up to 16 differential analog inputs are monitored. Channels 0 to 7 are simultaneously converted followed by the simultaneous conversion of channels 8 to 15. Channels may be individually enabled/disabled for simultaneous conversion.
- **User Programmable Conversion Timer** - A programmable conversion timer is available to control the time between simultaneous conversion of new banks of channel data. For example, channels 0-7 are converted immediately upon trigger and then channels 8-15 are converted after a user programmable delay from the start of the first eight channels. An overall count value is also used to control when conversions will start again with the first eight channels. Supports a maximum interval of 2.09 seconds.
- **Continuous Conversion Mode** - All channels selected for conversion are continually digitized with the interval between conversions controlled by the programmed conversion timer registers. Scanning is initiated by a software or external trigger. Scanning is stopped by software control.
- **Single Cycle Conversion Mode** - All channels selected for conversion are digitized once with the time between channels 0 to 7 and group 8 to 15 controlled by a programmable timer. Single cycle conversion mode is initiated by a software or external trigger.
- **External Trigger Input or Output** - The external trigger is assigned to a field I/O line. This external trigger may be configured as an input, output, or disabled. As an output this signal provides a means to synchronize other modules to a single IP340 or IP341 timer reference.
- **Precision On Board Calibration Voltages** - Calibration autozero and autospan precision voltages are available to permit host computer correction of conversion errors. The calibration voltage can be converted and then compared to the expected value stored in on board memory. Calibration voltages include: 0V (local analog ground), and a precision 5 volt reference.
- **Fault Protected Input Channels** - Analog input overvoltage protection to +/-25V power on and +/-40V with power off.

INDUSTRIAL I/O PACK INTERFACE FEATURES

- **High density -** Single-size, industry standard, IP module footprint. Four/five units mounted on a carrier board provide up to 64/80 differential channels in a single system slot.
- **Local ID** - Each IP module has its own 8-bit ID information which is accessed via data transfers in the "ID Read" space.
- **16-bit and 8-bit I/O** - Port register Read/Write is performed through data transfer cycles in the IP module I/O space.
- **High Speed** - Access times for all data transfer cycles are described in terms of "wait" states - 0 wait state is required for reading and writing all control registers and ID values. Interrupt select cycles also require 0 wait states for reading the interrupt vector. One wait state is typically required for read of the channel data FIFO ports (see the Specifications section for detailed information).

SIGNAL INTERFACE PRODUCTS

(See Appendix for more information on compatible products)

This IP module will mate directly to any industry standard IP carrier board (including Acromag's AVME9670 and AVME9630/9660 3U/6U VMEbus carrier boards). Additionally, PC/AT carrier boards are also supported (see the Acromag Model APC8620 PCIbus carrier board). A wide range of other Acromag IP modules are available to serve your signal conditioning and interface needs.

The cables and termination panels, described in the following paragraphs, are also available. For optimum performance with the IP340 and IP341 analog input modules, use of the shortest possible length of shielded output cable is recommended. Since all connections to field signals are made through the carrier board which passes them to the individual IP modules, you should consult the documentation of your carrier board to ensure compatibility with the following interface products.

Cables:

Model 5025-551-X (Shielded Cable), or Model 5025-550-X (Non-Shielded Cable): A Flat 50-pin cable with female connectors at both ends for connecting AVME9630/9660, APC8610, or APC8620 carrier boards, to Model 5025-552 termination panels. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications. The "-X" suffix of the model number is used to indicate the length in feet.

Model 5028-187 (SCSI-2 to Flat Ribbon Cable, Shielded): A round 50 conductor shielded cable with a male SCSI-2 connector at one end and a flat female ribbon connector at the other end. The cable is used for connecting AVME9670 with the TRANS-200, or other compatible carrier boards, to Model 5025-552 termination panels.

Termination Panels:

Model 5025-552: A DIN-rail mountable panel that provides 50 screw terminals for universal field I/O termination. Connects to Acromag AVME9670, AVME9630/9660, APC8610, or APC8620 carrier boards, via flat 50-pin ribbon cable (Model 5025-550-X or 5025-551-X).

VME64x Transition Module:

Model TRANS-200: This module plugs into the rear backplane directly behind the AVME9670 carrier board. The field I/O connections are made through the backplane to P0 and P2 connectors of the carrier board and then routed to four SCSI-2 connectors on the transition module (marked IP module slots "A through D") for rear exit from the card cage. It is available for use in VME64x bus card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VME64x bus mechanical dimensions and IEEE Standard (1101.11-1998), with a printed circuit board depth of 80mm, which is a standard transition module depth. The transition module connects to Acromag Termination Panel (Model 5025-552) using SCSI-2 to Flat Ribbon Cable, Shielded (Model 5028-187) to the rear of the card cage, and to AVME9670 boards within the card cage.

VME Transition Module:

Model TRANS-GP: This module repeats field I/O connections of IP modules A through D for rear exit from a VMEbus card cage. It is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. It connects to Acromag Termination Panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within the card cage, via flat 50-pin ribbon cable (cable Model 5025-550 or 5025-551).

INDUSTRIAL I/O PACK SOFTWARE LIBRARY

Acromag provides an Industrial I/O Pack Software Library diskette to simplify communication with the board (Model IPSW-LIB-M03, MSDOS format). Example software functions are provided. All functions are written in the "C" programming language and can be linked to your application. Refer to the "README.TXT" file in the root directory and the "INFO340.TXT" file in the "IP340" subdirectory on the diskette for more details.

IP MODULE OLE CONTROL SOFTWARE

Acromag provides a software product (sold separately) consisting of IP module OLE (Object Linking and Embedding) drivers for Windows 95®, and Windows NT® compatible application programs (Model IPSW-OLE-PCI, MSDOS format). This software provides individual drivers that allow Acromag IP modules and our personal computer carriers to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Borland Delphi®, Microsoft® Office® 97 applications and others. The OLE controls provide a high-level interface to IP modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the OLE controls. These functions are intended for use in conjunction with an Acromag personal computer carrier and consist of a Carrier OLE Control, and an OLE control for each Acromag IP module, as well as, a generic OLE control for non-Acromag IP modules.

IP MODULE VxWORKS SOFTWARE

Acromag provides a software product (sold separately) consisting of IP module VxWorks® drivers. This software (Model IPSW-API-VXW MSDOS format) is composed of VxWorks® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9670, AVME9660/9630, APC8610, and APC8620. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag IP modules and carriers.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. However, it is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed IP modules, within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The dense packing of the IP modules to the carrier board restricts air flow within the card cage and is cause for concern. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

BOARD CONFIGURATION

Power should be removed from the board when installing IP modules, cables, termination panels, and field wiring. Refer to Mechanical Assembly Drawing 4501-434 and the following discussion for configuration and assembly instructions.

Software Configuration

Software configurable control registers are provided for control of external trigger mode, conversion mode, timer control, channel enable, and interrupt mode selection. No hardware jumpers are required for control of these functions. These control registers must also be configured as desired before starting analog input conversions. Refer to section 3 for programming details.

CONNECTORS

Connectors of the IP340 and IP341 modules consist of one IP module field I/O connector, and one IP module logic connector. These interface connectors are discussed in the following sections.

IP Field I/O Connector (P2)

P2 provides the field I/O interface connections for mating IP modules to the carrier board. P2 is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the module to provide additional stability for harsh environments (see Mechanical Assembly Drawing 4501-434). The field and logic side connectors are keyed to avoid incorrect assembly.

P2 pin assignments are unique to each IP model (see Table 2.1) and normally correspond to the pin numbers of the field I/O interface connector on the carrier board (you should verify this for your carrier board). When reading Table 2.1 note that channel designations are abbreviated to save space. For example, channel 0 is abbreviated as “+CH00” & “-CH00” for the + & - connections, respectively.

Table 2.1: IP340 Field I/O Pin Connections (P2)

Pin Description	Number	Pin Description	Number
+CH00	1	-CH08	26
-CH00	2	COMMON	27
COMMON	3	+CH09	28
+CH01	4	-CH09	29
-CH01	5	COMMON	30
COMMON	6	+CH10	31
+CH02	7	-CH10	32
-CH02	8	COMMON	33
COMMON	9	+CH11	34
+CH03	10	-CH11	35
-CH03	11	COMMON	36
COMMON	12	+CH12	37
+CH04	13	-CH12	38
-CH04	14	COMMON	39
COMMON	15	+CH13	40
+CH05	16	-CH13	41
-CH05	17	COMMON	42
COMMON	18	+CH14	43
+CH06	19	-CH14	44
-CH06	20	COMMON	45
COMMON	21	+CH15	46
+CH07	22	-CH15	47
-CH07	23	COMMON	48
COMMON	24	EXT TRIGGER*	49
+CH08	25	SHIELD	50

Notes:
1. * Indicates that the signal is active low.

Analog Inputs: Noise and Grounding Considerations

Differential inputs require two leads (+ and -) per channel, and provide rejection of common mode voltages. This allows the desired signal to be accurately measured. However, the signal being measured cannot be floating--it must be referenced to analog common on the IP module and be within the normal input voltage range.

Differential inputs are the best choice when the input channels are sourced from different locations having slightly different ground references and when minimizing noise and maximizing accuracy are key concerns. See Drawing 4501-882 for analog input connections for differential ended inputs. Shielded cable of the shortest length possible is also strongly recommended.

The IP module is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the carrier board and backplane. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections. This is particularly important for analog inputs when a high level of accuracy/resolution is needed. Contact your Acromag representative for information on our many isolated signal conditioning products that could be used to interface to the IP340 and IP341 input modules.

External Trigger Input/Output

The external trigger signal on pin 49 of the P2 connector can be programmed as an input, output, or disabled.

The external trigger will accept a TTL compatible external trigger signal when programmed as an input. The external trigger must be a 5 Volt logic, TTL-compatible, debounced signal referenced to analog common. The external trigger signal is an active low edge sensitive signal. That is, the external trigger signal will trigger the module on the falling edge. Once the external trigger signal has been driven low, it should remain low for a minimum of 500nano-seconds.

The external trigger signal will generate triggers to allow synchronization of multiple IP340 or IP341 modules when programmed as an output. The external trigger output is a 500nano-second active low trigger signal driven from the module.

The external trigger signal can also be disabled. This prevents external noise from falsely triggering the module. See section 3.0 for programming details to make use of this signal.

IP Logic Interface Connector (P1)

P1 of the IP module provides the logic interface to the mating connector on the carrier board. This connector is a 50-pin female receptacle header (AMP 173279-3 or equivalent) which mates to the male connector of the carrier board (AMP 173280-3 or equivalent). This provides excellent connection integrity and utilizes gold-plating in the mating area. Threaded metric M2 screws and spacers are supplied with the IP module to provide additional stability for harsh environments (see Drawing 4501-434 for assembly details). Field and logic side connectors are keyed to avoid incorrect assembly. The pin assignments of P1 are standard for all IP modules according to the Industrial I/O Pack Specification (see Table 2.2).

Table 2.2: Standard Logic Interface Connections (P1)

Pin Description	Number	Pin Description	Number
GND	1	GND	26
CLK	2	+5V	27
Reset*	3	R/W*	28
D00	4	IDSEL*	29
D01	5	***DMAReq0****	30
D02	6	MEMSEL*	31
D03	7	***DMAReq1****	32
D04	8	IntSel*	33
D05	9	***DMAck0****	34
D06	10	IOSEL*	35
D07	11	***RESERVED***	36
D08	12	A1	37
D09	13	***DMAEnd****	38
D10	14	A2	39
D11	15	***ERROR****	40
D12	16	A3	41
D13	17	INTReq0*	42
D14	18	A4	43
D15	19	***INTReq1****	44
BS0*	20	A5	45
BS1*	21	***STROBE****	46
-12V	22	A6	47
+12V	23	ACK*	48
+5V	24	***RESERVED***	49
GND	25	GND	50

An Asterisk (*) is used to indicate an active-low signal.

BOLD ITALIC Logic Lines are NOT USED by this IP Model.

3.0 PROGRAMMING INFORMATION

ADDRESS MAPS

This manual is presented using the “Big Endian” byte ordering format. Big Endian is the convention used in the Motorola 68000 microprocessor family and is the VMEbus convention. In Big Endian, the lower-order byte is stored at odd-byte addresses. Thus, byte accesses are done on odd address locations. The Intel x86 family of microprocessors use the opposite convention, or “Little Endian” byte ordering. Little Endian uses even-byte addresses to store the low-order byte. As such, use of this module on a PC carrier board will require the use of the even address locations to access the 8-bit data, while a VMEbus carrier requires the use of odd address locations.

IDENTIFICATION SPACE - (Read Only, 32 Odd-Byte Addresses)

Each IP module contains identification (ID) information that resides in the ID space per the IP module specification. This area of memory contains 32 bytes of information at most. Both fixed and variable information may be present within the ID space. Fixed information includes the "IPAC" identifier, model number, and manufacturer's identification codes. Variable information includes unique information required for the module. The module’s ID information space does not contain any variable (e.g. unique calibration) information. ID space bytes are addressed using only the odd addresses in a 64 byte block (on the “Big Endian” VMEbus). Even addresses are used on the “Little Endian” PC ISA bus and PCI bus. The module’s ID space contents are shown in Table 3.1. Note that the base-address for the IP module ID space (see your carrier board instructions) must be added to the addresses shown to properly access the ID space. Execution of an ID space read requires 0 wait states.

Table 3.1: IP340 ID Space Identification (Format I)

Hex Offset From ID Base Address	ASCII Character Equivalent	Numeric Value (Hex)	Field Description
01	I	49	All IP's have 'IPAC'
03	P	50	
05	A	41	
07	C	43	
09		A3	Acromag ID Code
0B		28=IP340 29=IP341	IP Model Code[1]
0D		00	Not Used (Revision)
0F		00	Reserved
11		00	Not Used (Driver ID Low Byte)
13		00	Not Used (Driver ID High Byte)
15		0C	Total Number of ID PROM Bytes
17		1B=IP340 7A =P341	CRC
19 to 3F		yy	Not Used

Notes (Table 3.1):

1. The IP model number is represented by a two-digit code within the ID space (for example the IP340 is represented by 28 Hex IP model code).

I/O SPACE ADDRESS MAP

This board is addressable in the Industrial Pack I/O space to control the conversion of analog inputs from the field. As such, three types of information are stored in the I/O space: control, status, and data.

The I/O space may be as large as 64, 16-bit words (128 bytes) using address lines A1 to A6, but the IP340/IP341 uses only a portion of this space. The I/O space address map for the IP340 and IP341 is shown in Table 3.2. Note that the base address for the IP module I/O space (see your carrier board instructions) must be added to the addresses shown to properly access the I/O space.

Table 3.2: IP340/IP341 I/O Space Address Memory Map[2]

Hex Base Adr+	MSB D15 D08	LSB D07 D00	Hex Base Adr+
00	Control Register		01
02	Channel Enable Control		03
04	Conversion Timer Bits 15 to 0		05
06	Not Used Bits-15 to 08	Conversion Timer Bits 23 to 16	07
08	High Bank Timer Bits 15 to 0		09
0A		High Bank Timer Bits 23 to 16	0B
0C	FIFO Full Interrupt Threshold		0D
0E	Not Used Bits-15 to 08	Interrupt Vector	0F
10	Not Used Bits-15 to 01	Start Convert	11
12	FIFO Channel Data Port		13
14		FIFO Data Tag Port	15
16	Rd Wr~ / Address Port	Reference Voltage Write Data Port	17
18	Reference Voltage Read Data Port	Wr Busy / Rd Comp	19
1A	Reserved[3]	Not Used[1]	1B
1C	Not Used[1] ⇓		1D
7E	Not Used[1]		7F

Notes (Table 3.2):

1. The IP will not respond to addresses that are "Not Used".
2. All Reads and writes are 0 wait states (except read from FIFO ports which require 2 wait states worst case and 0 wait states typically).
3. This byte is reserved for use at the factory to enable writing of the reference voltage.

Control Register (Read/Write, 00H)

This read/write register is used to: enable single or continuous conversions, select conversion of calibration voltages or field analog signals, control external trigger input/output mode, enable/disable interrupts, monitor FIFO status, and issue a software reset to the module.

Table 3.3: Channel Control/Status Register

BIT	FUNCTION
1, 0	00 = Conversions are disabled. 01 = Enable Single Conversion Mode. A single conversion is initiated per software start convert or external trigger. The internal channel timer controls the start conversion of channels 8-15. 10 = Enable Continuous Conversion Mode. Conversions are initiated by a software start convert or external trigger and continued by internal hardware triggers generated at the frequency set by the interval timer registers. 11 = Reserved
3, 2	00 = All Channels Differential Input. 01 = Auto Zero Calibration Voltage Input. 10 = Auto Span Calibration Voltage. 11 = Reserved
5, 4	00 = External Trigger Disable. 01 = External Trigger Set as Input. 10 = External Trigger Set as Output. 11 = Reserved. As an output Internal Timer triggers are driven on the External trigger pin of the field I/O connector. The External Trigger output signal can be used to synchronize the conversion of multiple modules. A single master IP340 or IP341 must be selected for External Trigger output and Continuous Conversion mode while all other modules are selected for External Trigger input and Single Conversion mode. The external trigger signals (pin 49 of the field I/O) must be wired together for all synchronized modules. Also, the High Bank Timer must be programmed with the same value on all synchronized modules. The External Trigger input can be sensitive to external EMI noise which can cause erroneous external triggers. If External Trigger Input or output is not required, the External Trigger should be configured as Disabled.
6	0 = Disable Interrupt 1 = Enable Interrupt If enabled via this bit an interrupt request from the module will be issued to the system if the FIFO contains more than the threshold number of bytes selected via the threshold register. The interrupt request will remain active until the interrupt condition is removed, or by disabling interrupts via this bit. The interrupt condition can be removed by reading the channel data from the FIFO buffer (thus reducing the number of samples below the set threshold).
7	Not Used
8 Status	0 = FIFO Empty 1 = FIFO Not Empty
9 Status	0 = FIFO has less than or equal number of samples as defined by the threshold register. 1 = FIFO Threshold Reached. This bit is set when the FIFO contains more than the number of data samples set by the threshold register.
10	0 = FIFO Not Full

BIT	FUNCTION
Status	1 = FIFO Full
14-11	Not Used
15	1 = Software Reset Issued.

The software reset will clear this control register, the channel enable register, counters, the FIFO Threshold register, and FIFO buffer.

The function of each of the control register bits are described in Table 3.3. This register can be read or written with either 8-bit or 16-bit data transfers. A power-up or software channel reset sets all control register bits to 0.

Channel Enable Control Register (Read/Write, 02H)

The Channel Enable Control register (bits-15 to 0) is used to select the channels desired for conversion. Only those channels enabled are stored into the channel data FIFO. When the channel's corresponding bit is set high, per the table below, the channel's converted data is tagged and stored into the FIFO. For example, to enable channels 15, 11, and 7 through 0 the Channel Enable register must be set as 88FF hex.

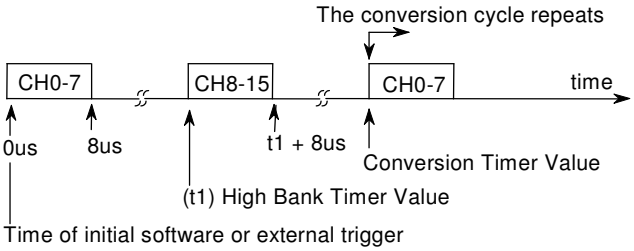
Reading or writing to this register is possible via 16-bit or 8-bit data transfers and will require zero wait states. This register's contents are cleared upon reset.

Channel Enable Control Register							
MSB							LSB
15	14	13	12	11	10	09	08
Ch15	Ch14	Ch13	Ch12	Ch11	Ch10	Ch09	Ch08
MSB							LSB
07	06	05	04	03	02	01	00
Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	Ch0

Conversion Timer Register (Read/Write)

Timed periodic triggering can be used to achieve precise time intervals between conversions. The Conversion Timer register is a 24 bit register value that controls the interval time between conversions of all enabled channels. The least significant 16-bits of this registers are accessed at offset 04 hex and the most significant 8-bits are at offset 06 hex.

The Channel Conversion Timer is used to control the frequency at which the conversion cycle is repeated for all enabled channels. For example upon software or external trigger, channels 0 to 7 are simultaneously converted. The time programmed into the High Bank Conversion Timer Register then determines when channels 8 to 15 are simultaneously converted. The cycle repeats when the time programmed into Conversion Timer determines when channels 0 to 7 will again be simultaneously converted. Thus, the Conversion Timer value must always be greater then the High Bank Conversion Timer value by at least 8µ seconds. If Continuous Conversions are selected via the Control register, then conversions will continue until disabled. See figure 1 for an illustration of the sequence of conversions describe in this paragraph.



Where: High Bank Timer Value must be > 8µ seconds
Conversion Timer Value must be > t1 + 8µ seconds

Figure1: Time line of channel bank conversions

The 24-bit Conversion Timer value divides an 8 MHz clock signal. The output of this Conversion Timer is used to precisely generate periodic trigger pulses to control the frequency at which all enabled channels are converted. The time period between trigger pulses is described by the following equation:

$$\frac{\text{Conversion Timer Value} + 1}{8{,}000{,}000Hz} = \text{T in seconds}$$

To calculate the conversion timer value the following equation can be used. Note, this gives the value in decimal. It must still be converted to hex before it is written to the Conversion Timer register.

$$\text{Conversion Timer Value} = (\text{T seconds} \times 8{,}000{,}000\text{Hz}) - 1$$

Where:
T = the desired time period between trigger pulses in seconds.
Conversion Timer Value can be a minimum of 63 decimal if only channels 0 to 7 are enabled for conversion. If any channels in the upper bank (channels 8 to 15) are also enabled, then the minimum value is 127 decimal. The maximum value is 16,777,214 decimal.

The maximum period of time which can be programmed to occur between simultaneous conversions is (16,777,214 + 1) ÷ 8,000,000 = 2.097151875 seconds. The minimum time interval which can be programmed to occur is (63 + 1) ÷ 8,000,000 = 8.0µ seconds. This minimum of 8.0µ seconds is defined by the minimum conversion time of the hardware given only channels 0 to 7 are enabled for conversions. If any channel from channels 8 to 15 are enabled for conversion, then the minimum time that the Conversion Timer can be programmed is 127 decimal. This minimum time of 16µ seconds allows 8µ seconds for channels 0 to 7 and 8µ seconds for channels 8 to 15.

The 8µ seconds maximum sample rate corresponds to a maximum sample frequency of 125KHz. The maximum analog input frequency should be band limited to one half the sample frequency. An anti-aliasing filter should be added to remove unwanted signals above 1/2 the sample frequency in the input signal for critical applications.

Read or writing the Conversion Timer register is possible with either 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

High Bank Timer Register (Read/Write)

The High Bank Timer register is a 24 bit register that controls when the upper bank of channels 8 to 15 are converted. The least significant 16-bits of this register are at offset 08 hex, and the most significant 8-bits are at offset 0A hex in the lower byte location.

The High Bank Timer is used to control the delay after channels 0 to 7 are converted until channels 8 to 15 are simultaneously converted. For example, upon software or external trigger channels 0 to 7 are simultaneously converted. Then, the time programmed into this counter determines when channels 8 to 15 will be simultaneously converted. See figure 1 for an illustration of this sequence of events.

If a channel within the 8 to 15 bank is enabled in the Channel Enable Control register, then the High Bank Timer register must be programmed with a delay. If this register is left as zero erroneous operation will result.

The 24-bit High Bank Timer value divides an 8 MHz clock signal. The output of this Timer is used to precisely generate periodic trigger pulses to control the frequency at which the bank of channels 8 to 15 are simultaneously converted. The time period between trigger pulses is described by the following equation:

$$\frac{\text{High Bank Timer Value} + 1}{8{,}000{,}000 Hz} = \text{T in seconds}$$

Where:
T = the desired time period between trigger pulses in seconds.
High Bank Timer Value can be minimum of 63 decimal. The maximum value is 16,777,150 decimal.

The maximum period of time which can be programmed to occur between conversions is (16,777,150 + 1) ÷ 8,000,000 = 2.097143875 seconds. The minimum time interval which can be programmed to occur is (63 + 1) ÷ 8,000,000 = 8.0µ seconds. This minimum of 8.0µ seconds is defined by the minimum conversion time of the hardware. This gives channels 0 to 7 eight micro seconds to complete their simultaneous conversion. Then channels 8 to 15 can be simultaneously converted.

Read or writing the High BankTimer register is possible with either 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

FIFO Full Interrupt Threshold (Read/Write, 0CH)

The FIFO Full Interrupt Threshold register is a 9-bit register that is used to control when an interrupt will be generated. When the FIFO contains more samples than the FIFO Full Interrupt Threshold value an interrupt will be issued. This register allows selection of any FIFO depth level. When this level is exceeded it will cause an interrupt to be generated to the system. This interrupt indicates that new data is available in the FIFO.

An interrupt request will remain asserted to the system as long as the FIFO threshold is exceeded and interrupts are enabled. The interrupt request can be removed by 1) disabling interrupts on the IP module or 2) reading the FIFO until it has the same number or fewer samples in it than defined by the threshold register.

Note, interrupts must first be enabled in the interrupt enable register of the control register. Reading or writing to this register is possible via 16-bit or 8-bit data transfers. This register's contents are cleared upon reset.

Interrupt Vector Register (Read/Write, 0FH)

The Interrupt Vector Register can be written with an 8-bit interrupt vector. This vector is provided to the carrier and system bus upon an active INTSEL* (interrupt acknowledge cycle). Reading or writing to this register is possible via 16-bit or 8-bit data transfers.

Interrupt Vector Register							
MSB							LSB
07	06	05	04	03	02	01	00

The Interrupt Vector register can be used as a pointer to an interrupt handling routine. The vector is an 8-bit value and can be used to point to any one of 256 possible locations to access the interrupt handling routine.

An interrupt can be enabled for generation when the number of samples in the FIFO exceeds that set by the FIFO Interrupt Threshold register. Interrupts generated by the module use interrupt request line INTREQ0* (Interrupt Request 0). The module will release the INTREQ0* signal after the FIFO buffer has fewer samples than the set threshold or if interrupts are disabled.

This register's contents are cleared upon reset.

Start Convert Register (Write Only, 11H)

The Start Convert register is write-only and is used to trigger conversions by setting data bit-0 to a logic one. This method of starting conversions is most useful for its simplicity and for when precise time of conversion is not critical. Typically, software triggering is used for initiating the first conversion. The desired mode of data acquisition must first be configured by setting the following registers to the desired values and modes: Control, Interrupt Vector, and Conversion Timers.

This register can be written with either a 16-bit or 8-bit data value. Data bit-0 must be a logic one to initiate data conversions.

Start Convert Register							
Not Used							Start Convert
07	06	05	04	03	02	01	00

FIFO Channel Data Port (Read Only, 12H)

All channels share a 512 sample deep FIFO buffer. The FIFO samples are 16-bit data values. Reading of the FIFO is possible via 16-bit data transfers only. The FIFO will be cleared by implementing a software or hardware reset.

Since all channels share the same FIFO, channel data tagging is implemented. The tag value identifies the channel to which the data corresponds.

Reading the FIFO Channel Data port causes both the channel data value and its corresponding tag to be available. If it

is necessary to identify the channel to which the data corresponds, then the FIFO Data Tag port must be read after the FIFO data is read.

Care should be taken when reading data from the FIFO buffer to insure the FIFO is not empty when a new read is initiated. The FIFO Empty status bit can be read, in the control register, prior to reading the FIFO to avoid reading erroneous data.

If the FIFO becomes full and is not read before new data is written to the FIFO, the new data will be written to the FIFO over-writing old data. Thus, you will always get the most recent data available.

It is recommended that interrupts be enabled upon meeting the FIFO's set threshold condition.

Read accesses to this register typically require one wait state and can be a maximum of 2 wait states when a FIFO write overlaps a FIFO read.

FIFO Data Tag Port (Read Only, 15H)

All channels share the same 512 sample FIFO. As such, channel data tagging is implemented to assist in identifying the channel corresponding to the FIFO data read. The hardware tags each FIFO location with a channel number, so you can easily match data and its source channel.

The tag value identifies the channel to which the data corresponds and must be read after reading the FIFO Channel Data port.

Analog Input and Corresponding Digital Output Codes

The output data coding is in binary two's compliment. The digital output code corresponding to each of the given ideal analog input values is given in binary two's complement format in Table 3.4. Note that the 12 and 14 bit data values are left justified within the 16-bit word. For the 12-bit IP340 the least significant 4 bits will be returned as zero when read. Also, for the 14-bit IP341 the least significant 2 bits will be returned as zero when read.

Table 3.4: Digital Output Codes and Input Voltages

DESCRIPTION	ANALOG INPUT			
Model	**IP340 (12-bit)**		**IP341 (14-bit)**	
Least Significant Bit Weight	4.88mV		1.22mV	
+ Full Scale Minus One LSB	9.995117 Volts	7FF0 hex	9.998779 Volts	7FFC hex
Midscale	0V	0000h	0V	0000h
One LSB Below Midscale	-4.88mV	FFF0 hex	-1.22mV	FFFC hex
Minus Full Scale	-10V	8000 hex	-10V	8000 hex

Reference Voltage Access Register (Write, 16H)

This register is used to initiate a read of the reference voltage value. The reference voltage value is provided so that software can adjust and improve the accuracy of the analog input voltage over the uncalibrated state. The reference voltage is precisely measured at the factory and then stored to this location at the addresses given in table 3.5.

The Reference Voltage Access Register is a write-only register and is used to configure and initiate a read cycle to the Reference Voltage memory. Setting bit-15 of this register high, to a "1", initiates a read cycle.

The address of the Reference Voltage to be read must be specified on bits 14 to 8 of Reference Voltage Access register.

Most Significant Byte of Reference Voltage Access Reg	
Read or Write~	Address
15	14, 13, 12, 11, 10, 9, 8

The reference voltage is stored in memory as a null terminated ASCII character string. For example if the value 4.99835 were stored to memory the corresponding ASCII characters would be 34, 2E, 39, 39, 38, 33, 35, 00 as shown in Table 3.5. Note, the ASCII equivalent of a decimal point is 2E and the null character is 00. The memory should be read starting at address 00 until the null ASCII character is read. This string can then be converted into a float by using your compiler's ATOF function.

Table 3.5: Reference Voltage Address Memory Map

Address (Hex)							
00	01	02	03	04	05	06	07
Example Reference Value							
4	.	9	9	8	3	5	null
ASCII Characters As Stored In Memory							
34	2E	39	39	38	33	35	00

The address corresponding to each of the reference voltage digits is given in hex. The most significant digit is stored at address 00 hex.

For additional details on the use of the reference voltage, refer to the "Data Correction" section.

Write accesses to the Reference Voltage Access register require zero wait states and are possible via 16-bit data transfers only. Storing the reference voltage value to memory is normally only performed at the factory.

A software or hardware reset has no affect on this register.

Reference Voltage Read Data/Status Register (Read, 18H)

The Reference Voltage Read Data/Status register is a read-only register and is used to access the read data and determine the status of a read cycle initiated by the Reference Voltage Access register. In addition, this register is used to determine the status of a write cycle to the memory. When bit-1 of this register is set it indicates the memory is busy completing a write cycle.

All read accesses to this Data/Status register initiate an approximately 1millisecond access to the memory. **Thus, you must wait 1 millisecond after reading this Data/Status register before a new read or write cycle to the memory can be initiated, (an EEPROM latency limitation).**

A read request of the memory, initiated through the Reference Voltage Access register, will provide the addressed digit of the reference voltage on data bits 15 to 8 of the Reference Voltage Data/Status register. Although the read request via the Reference Voltage Access register is accomplished in less then 800n seconds, typically, the reference voltage digit will not be available in the Reference Voltage Data/Status register for approximately 2.5 milliseconds.

Bit-0 of the Reference Voltage Data/Status register is the read complete status bit. This bit will be set high to indicate that the requested reference voltage digit is available on data bits 15 to 8 of the Reference Voltage Data/Status register. This bit is cleared upon initiation of a new read access of the memory or upon issue of a hardware reset.

Writes to Reference Voltage memory require a special enable code. Writes to memory are normally only performed at the factory. The module should be returned to Acromag if the reference voltage must be re-measured and stored to memory.

A write operation to the memory, initiated via the Reference Voltage Access register, will take approximately 5 milliseconds. Bit-1 of the Reference Voltage Data/Status register serves as a write operation busy status indicator. Bit-1 will be set high upon initiation of a write operation and will remain high until the requested write operation has completed. New read or write accesses to the memory, via the Reference Voltage Access register, should not be initiated unless the write busy status bit-1 is clear (set low to 0). A hardware reset of the IP module will also clear this bit.

Read accesses to the Reference Voltage Data/Status register require zero wait states and are possible via 16-bit data transfers only. A software or hardware reset will clear all bits to zero.

MODES OF CONVERSION

The IP340 and IP341 provide two methods of analog input operation for maximum flexibility with different applications. The following sections describe the features of each method and how to best use them.

Single Conversion Mode

In Single Conversion mode of operation, conversions are initiated by a software or external trigger. Upon the trigger, channels 0 to 7 will be simultaneously converted. Then, after the time programmed into the High Bank Timer has been reached, channels 8 to 15 will be simultaneously converted. All channels enabled in the Channel Enable Control register will be tagged with their channel number and stored to FIFO memory. No additional conversions will be initiated unless a new software or external trigger is generated.

To select this mode of operation bits 1 and 0 of the Channel Control register must be set to digital code “01”. Then, issuing a software start convert or external trigger will initiate conversions. The Conversion Timer is not used in this mode of operation. Also, the High Bank Timer is not needed if channels 8 to 15 are disabled.

This mode of operation can be used to initiate conversions based up external triggers. This can be used to synchronize multiple IP modules to a single module running in a continuous conversion mode. The external trigger of a IP340 or IP341 “master” must be programmed as an output. The external trigger signal of that module must then be connected to the external trigger signal of all other modules that are to be synchronized. These other modules must be programmed for Single Conversion mode and external trigger input. Also, the High Bank Timer must be programmed with the same value on all synchronized modules. Data conversion can then be initiated via the Start Convert bit of the master IP module configured for continuous conversion mode.

Continuous Conversion Mode

In the Continuous Conversion mode of operation, the hardware controls the continuous conversions of all enabled channels. All channels 0 to 15 are converted at the rate specified by the Conversion Timer. Channels 8 to 15 are converted after channels 0 to 7. The time programmed into the High Bank Timer specifies how long after channels 0 to 7 are converted before channels 8 to 15 are converted.

To initiate this mode of operation bits 1 and 0 of the Channel Control register must be set to digital code “10”. Then, issuing a software start convert or external trigger will initiate the continuous conversions of all enabled channels.

The interrupt capability of the IP module can be employed as a means to indicate to the system that the 512 sample FIFO is almost full (depending on the threshold selected) and must be read before data is over-written.

Alternatively, a polling method could be used. The FIFO Empty, Full, and Threshold Reached bits in the Control/Status register can be polled. When the flags indicate that new FIFO data is available the FIFO should be read before data is over-written.

PROGRAMMING CONSIDERATIONS

The IP340 and IP341 provide different methods of analog input acquisition to give the user maximum flexibility for each application. Examples are presented in the following sections to illustrate programming the different modes of operation.

Single Conversion Mode Example

This example will enable channels 0, 3, and 8 through 15 for the single conversion mode of operation. Conversions can be initiated via software or external trigger. Channels 8 to 15 will be simultaneously converted 16µ seconds after channels 0 and 3.

1. Execute Write of 0011H to the Control Register at Base Address + 00H.
   a) Single Conversion is enabled.
   b) External and Software generated triggers are enabled.

2. Execute Write of FF09H to the Channel Enable Control register at Base Address + 02H. This will enable channels 0, 3, and 8 through 15 for conversion.

3. Execute Write of 007FH to the High Bank Timer at Base Address + 08H.

4. Execute Write of 00H to the High Bank Timer at Base Address + 0AH.

5. Execute Write of 0001H to the Start Convert Bit at Base Address + 10H. This starts the simultaneous conversion of channels 3 and 0. Then, 16µ seconds later, channels 8 to 15 are simultaneously converted.

Continuous Conversion Mode with Interrupt Example

This example will enable channels 0 through 13 for the continuous conversion mode of operation. Interrupts are enabled and an interrupt threshold of 430 samples is programmed. The Conversion Timer will be set for an 80µ second interval. The High Bank Timer is set to activate the simultaneous conversion of channels 8 through 13 at 23µ seconds after channels 0 to 7. Conversions can be initiated via software or external trigger.

This example assumes that the IP module is installed onto an Acromag AVME9630/60 carrier board (consult your carrier board documentation for compatibility details).

1. Clear the global interrupt enable bit in the carrier board status register by writing a "0" to bit 3.

2. Write the interrupt vector to the IP340 or IP341 Module at base address + 0EH.

3. Write to the carrier board interrupt Level Register to program the desired interrupt level per bits 2,1, & 0.

4. Write "1" to the carrier board IP Interrupt Clear Register corresponding to the desired IP interrupt request being configured.

5. Write "1" to the carrier board IP Interrupt Enable Register bit corresponding to the IP interrupt request to be enabled.

6. Enable interrupts for the carrier board by writing a "1" to bit 3 (the Global Interrupt Enable Bit) of the carrier board's Status Register.

7. Execute Write of 0052H to the Channel Control Register at Base Address + 00H.
   a) Continuous Conversion mode is selected.
   b) External and Software generated triggers are enabled.
   c) Interrupts are enabled.

8. Execute Write of 3FFFH to the Channel Enable Control register at Base Address + 02H. This will enable channels 0 through 13 for conversion.

9. Execute Write of 27FH to the Conversion Timer Register at Base Address + 04H.
   a) This sets the Conversion Timer to 639 decimal as needed for an 80µ second interval.

10. Execute Write of 00H to the Conversion Timer Register at Base Address + 06H.
    a) The most significant bits of the Conversion Timer are set to zero.

11. Execute Write of 00B7H to the High Bank Timer Register at Base Address + 08H.
    a) This sets the High Bank Timer to 183 decimal as needed for a 23µ seconds delay after channels 0 through 7. Note: (183+1) ÷ 8,000,000 = 23µ seconds.

12. Execute Write of 00H to the High Bank Timer at Base Address + 0AH.

13. Execute Write of 1AEH to the FIFO Full Interrupt Threshold register at Base Address + 0CH.
    a) The IP340 or IP341 will issue an interrupt to the system when more than 430 samples are present in the FIFO.

14. Execute Write of 0001H to the Start Convert Bit at Base Address + 10H.
    a) This starts the simultaneous conversion of channels 0 to 7. Then, after 23µ seconds channels 8 through 13 are simultaneously converted. The cycle repeats every 80µ seconds.

General Sequence of Events for Processing an Interrupt

1. The IP340 or IP341 asserts the Interrupt Request 0 Line (INTREQ0*) as long as the FIFO contains more samples than that set in the FIFO threshold register.
2. The AVME9630/60 carrier board acts as an interrupter in making the VMEbus interrupt request (IRQx*) corresponding to the IP interrupt request.
3. The VMEbus host (interrupt handler) asserts IACK* and the level of the interrupt it is seeking on A01-A03.
4. When the asserted VMEbus IACKIN* signal (daisy-chained) is passed to the AVME9630/60, the carrier board will check if the level requested matches that specified by the host. If it matches, the carrier board will assert the INTSEL* line to the appropriate IP together with (carrier board generated) address bit A1 to select which interrupt request is being processed (A1 low corresponds to INTREQ0*).
5. The IP340 or IP341 puts the interrupt vector on the local data bus (D00-D07 for the D08 [O] interrupter) and asserts ACK* to the carrier board. The carrier board passes this along to the VMEbus (D08[O]) and asserts DTACK*.
6. The host uses the vector to form a pointer to an interrupt service routine for the interrupt handler to begin execution.

7. Example of Generic Interrupt Handler Actions:
   a) Disable the interrupting IP by writing "0" to the appropriate bit in the AVME9630/60 IP Interrupt Enable Register.
   b) Service the interrupt (read FIFO data).
   c) Clear the interrupting IP by writing a "1" to the appropriate bit in the AVME9630/60 IP Interrupt Clear register.
   d) Enable the interrupting IP by writing "1" to the appropriate bit in the AVME9630/60 IP Interrupt Enable Register.
8. The interrupt is released when the FIFO no longer has more samples than that set by the Threshold register. The interrupt request is also released if interrupts are disabled.

USE OF CALIBRATION REFERENCE SIGNAL

A Reference voltage signal for analog input calibration has been provided to improve the accuracy over the uncalibrated state. The use of software calibration allows the elimination of hardware calibration potentiometers traditionally used in precision analog front ends.

Software calibration uses some fairly complex equations. **Acromag provides you with the Industrial I/O Pack Software Library diskette to make communication with the board and calibration easy. It relieves you from having to turn the equations of the following sections into debugged software calibration code.** The functions are written in the "C" programming language and can be linked into your application. Refer to the "README.TXT" file in the root directory and the "INFO340.TXT" file in the "IP340" subdirectory on the diskette for details.

In addition, Acromag provides two software products (sold separately) which also make communication with the board and calibration easy. The first product is IP module OLE (Object Linking and Embedding) drivers for Windows 95®, and Windows NT® compatible application programs (Model IPSW-OLE-PCI, MSDOS format). The second product is IP module VxWorks® (real time operating system) drivers (Model IPSW-API-VXW, MSDOS format).

Uncalibrated Performance

The uncalibrated performance is affected by two primary error sources. These are the Instrumentation Amplifier (IN-AMP) and the Analog to Digital Converter (ADC). The untrimmed IN-AMP and ADC have significant offset and gain errors (see specifications in chapter 6) which reveal the need for software calibration.

Calibrated Performance

Very accurate calibration of the IP340 and IP341 can be accomplished by using the calibration reference voltage and auto zero (analog ground reference) present on the board. The five volt reference and the analog ground reference are used to determine two points of a straight line which defines the analog input characteristic. The exact value of the five volt reference is stored in on board memory to provide the most accurate calibration.

The IP340 and IP341 have eight separate ADC circuits. As such, each of the first eight channels will have their own unique offset and gain errors. Note, channels 8 through 15 share the gain and offset values of channels 0 through 7. The five volt reference (Auto Span Calibration Voltage) and the ground reference (Auto Zero voltage) will need to be selected and converted through each of the eight channels to determine the corrected value as given in equation 1.

Equation (1) following is used to correct the actual ADC data (i.e. the uncorrected bit count read from the ADC) making use of the stored reference voltage.

$$\text{CorrectValue} = \left[\text{CountRead} - \text{Count}_{0V}\right] \times \left[\frac{\text{5VRefConstant}}{\text{Count}_{5V} - \text{Count}_{0V}}\right] \quad (1)$$

Where:

5VRefConstant = 204.8 x 5VrefValue (IP340)
819.2 x 5VrefValue (IP341)

Count_{5V} = Actual ADC Data Read With 5 Volt Calibration Voltage Applied

Count_{0V} = Actual ADC Data Read With Auto Zero Calibration Voltage Applied

CountRead = Uncorrected ADC Data Read For Channel Undergoing Correction.

The **5VRefValue** represents the five volt reference value as it is read from stored memory via the Reference Voltage Access register and the Reference Voltage Read Data/Status register.

The **5VRefConstant** is equal to the five volt reference value as read from stored memory (5VRefValue) multiplied by 204.8 for an IP340 or multilplied by 819.2. for an IP341.

The Count_{5V} and Count_{0V} reference voltages should not be determined immediately after startup but after the module has reached a stable temperature (about 20 minutes) and updated periodically (e.g. once an hour, or more often if ambient temperatures change) to obtain the best accuracy. Note that several readings (e.g. 100) of the reference voltages should be taken via the ADC and averaged to reduce the measurement uncertainty, since these points are critical to the overall system accuracy.

Calibration Programming Example

Assume that channels 0 through 3 are enabled, and corrected input channel data is desired. The calibration parameters (Count_{5V} and Count_{0V}) need to be determined for channels 0 through 3 before the analog field signals can be corrected. Note that channel 0 and 8 share the same INAMP and ADC and thus share the same Count_{5V} and Count_{0V} values. This is also true for channels 1 and 9, 2 and 10, etc..

Determination of the Count_{0V} Value

1. Execute Write of 0046H to the Control Register at Base Address + 00H.
   a) Continuous Mode Enabled
   b) Auto Zero Calibration Voltage Selected (Count_{0V})
   c) External Trigger Disabled
   d) Interrupt Enabled

2. Execute Write of 000FH to the Channel Enable Control Register at Base Address + 02H. This will permit the Auto Zero values corresponding to channels 0 to 3 to be stored in the data FIFO.

3. Execute Write of BFH to the Conversion Timer register at Base Address + 04H. This sets the interval time between conversions to 24µ seconds.

4. Execute Write of 18FH to the FIFO Full Threshold register at Base Address + 0CH. Since interrupts are enabled in the control register, an interrupt request will be issued when 400 values of the Auto Zero calibration voltage have been stored in the FIFO. This corresponds to 100 values for each of the four channels enabled.

5. Execute Write of 0001H to the Start Convert Bit at Base Address + 10H. This starts the continuous mode of conversions.

6. Upon system interrupt execute write of 00H to the Control register at Base Address + 00H. This disables conversion. Software must calculate a $Count_{0V}$ value for each channel 0 to 3, by averaging the 100 values for each channel.

Determination of the $Count_{5V}$ Value

7. Execute Write of 004AH to the Control Register at Base Address + 00H.
   a) Continuous Mode Enabled
   b) Auto Span Calibration Voltage Selected ($Count_{5V}$)
   c) External Trigger Disabled
   d) Interrupt Enabled

8. Writing the Channel Enable register, Conversion Timer Value, and the FIFO Full Threshold is not necessary because they need not change from that programmed in the previous steps.

9. Execute Write 0001H to the Start Convert Bit at Base Address + 10H. This starts the continuous mode of conversions.

10. Upon system interrupt execute write of 00H to the Control register at Base Address + 00H. This disables conversions. Software must calculate a $Count_{5V}$ value for each channel 0 to 3, by averaging the 100 values for each channel.

Read the Reference Voltage Value From Memory

11. Read the reference voltage memory to retrieve the unique reference voltage value (5VRefValue). To obtain the reference voltage value the ASCII characters comprising the reference voltage must be read until the null (terminating) character "00" is read. To read the most significant digit, the Reference Voltage Access register must be written with data value 8000H at Base Address + 16H. The data can be read by polling the Reference Voltage Read Data/Status register. When bit 0 of the Reference Voltage Read Data/Status register is set to logic high, then the data on bits 15 to 8 contains the most significant byte of the reference voltage value.

    To initiate a read of the second memory location of the reference voltage value, the Reference Voltage Access register must be written with data value 8100H at Base Address + 16H. When bit 0 of the Calibration Coefficient Status register is set to logic high, then the data on bits 15 to 8 of this register contains the decimal point byte of the reference voltage value.

    This procedure must continue until the null ASCII character is read from memory.

12. Since $Count_{0V}$, $Count_{5V}$, and 5VRefValue are known, corrected input data values can now be determined.

Start Conversion Of Differential Input Channel Data

13. Execute Write of 0042H to Control Register at Base Address + 00H.
   a) Continuous Mode Enabled
   b) Channel Differential Input Selected
   c) External Trigger Disabled
   d) Interrupt Enabled

14. Execute Write 0001H to the Start Convert Bit at Base Address + 10H. This starts the continuous mode of conversions. Continuous simultaneous conversions of channels 0 to 3 are implemented and corresponding results are stored in the FIFO Buffer.

15. Upon system interrupt the FIFO buffer at Base Address + 12H must be read. The data read should be corrected per equation 1 of this section.

4.0 THEORY OF OPERATION

This section contains information regarding the hardware of the IP340 and IP341. A description of the basic functionality of the circuitry used on the board is also provided. Refer to the Block Diagram shown in Drawing 4501-881 as you review this material.

FIELD ANALOG INPUTS

The field I/O interface to the carrier board is provided through connector P2 (refer to Table 2.3). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2 for connection recommendations). Ignoring ground loops may cause operation errors, and with extreme abuse, possible circuit damage. Refer to Drawing 4501-882 for example wiring and grounding connections.

Analog inputs and calibration voltages are selected via analog multiplexers. IP module control logic drives the select signals of the multiplexer as required per the programming of the control register.

Up to 16 differential inputs can be monitored. The multiplexer stage directs one of two groups of eight channels for simultaneous conversion. Channels 0 to 7 are simultaneously selected and converted as a group by eight individual ADC's, and channels 8 to 15 are also simultaneously converted as a group.

The output of the multiplexer stage feeds an instrumentation amplifier (INAMP) stage. The INAMP has a fixed gain of one. The INAMPs high input impedance allows measurement of analog input signals without loading the source. The INAMP takes in the channel's + and - inputs and outputs a single ended voltage proportional to it.

The output of the INAMP feeds an Analog to Digital Converter (ADC). The ADC is a state of the art, 12-bit (IP340) or 14-bit (IP341) successive approximation converter with a built-in sample and hold circuit. The sample and hold circuit goes into the hold mode when a conversion is initiated. This maintains the selected channel's voltage constant until the ADC has accurately digitized the input. Then, it returns to sample mode to re-acquire the analog signal. Once a conversion has been completed, control logic on the module automatically and simultaneously serially reads the digitized values corresponding to the eight channels. While the digitized values are read the input is in the acquire mode. Digital noise generated by reading the newly digitized values will not be present when the ADC transitions into the hold mode since the analog signal is allowed to settle for an interval after the digitized values are read. This pipelined mode of operation facilitates a maximum system throughput with minimum system noise.

The board contains two precision voltage references and a ground (autozero) reference for use in calibration. A 2.5 volt reference is used by the ADC. A 5 volt reference is used to provide accurate auto span voltage for offset and gain correction of the ADC and INAMP.

LOGIC/POWER INTERFACE

The logic interface to the carrier board is made through connector P1 (refer to Table 2.4). The P1 interface also provides +5V and ±12V power to the module. Note that the DMA control, INTREQ1∗, ERROR∗, and STROBE∗ signals are not used.

A Field Programmable Gate-Array (FPGA) installed on the IP Module provides an interface to the carrier board per IP Module specification ANSI/VITA 4 1995. The interface to the carrier board allows complete control of all IP340 and IP341 functions.

IP INTERFACE LOGIC

IP interface logic is imbedded within the FPGA. This logic includes: address decoding, I/O and ID read/write control circuitry, and ID storage implementation.

Address decoding of the six IP address signals A(1:6) is implemented in the FPGA, in conjunction with the IP select signals, to identify access to the IP module's ID or I/O space. In addition, the byte strobes BS0∗ and BS1∗ are decoded to identify low byte, high byte, or double byte data transfers.

The carrier to IP module interface implements access to both ID and I/O space via 16 or 8-bit data transfers. Read only access to ID space provides the identification for the individual module (as given in Table 3.1) per the IP specification. Read and write accesses to the I/O space provide a means to control the module.

Access to both ID and I/O spaces are implemented with zero wait states read or write data transfers, except for read access to the FIFO buffers. Read cycles to the FIFO buffers require two wait states worst case, but typically will be implemented with zero wait states.

Two wait state reads of the FIFO buffers will only be implemented when the read overlaps with a FIFO write of new digitized data from the ADC. The FIFO read operation will wait for a previously started FIFO write operation without causing the FIFO read to take more than the worst case two wait states. The FIFO write will commence immediately after the read has completed.

CONVERSION CONTROL LOGIC

All logic to control data conversions is imbedded in the IP module's FPGA. The control logic of the module is responsible for controlling the user specified mode of operation. Once the IP module has been configured, the control logic performs the following:

- Controls Multiplexers for selection of channel data.
- Controls serial transfer of data from the eight ADC's to the FPGA FIFO memory.
- Provides external or internal trigger control.
- Controls read and write access to the reference voltage value stored in memory.
- Controls issue of interrupt requests to the carrier and responds to interrupt select cycles.
- Provides status on FIFO Full, Empty, and programmable Threshold conditions.

MULTIPLEXER CONTROL CIRCUITRY

The analog input is multiplexed into the ADC. The multiplexer allows the programmable selection of analog channel data or the auto span and auto zero calibration voltages. When selected for differential input of analog channel data, channels 0 to 7 are automatically selected for simultaneous conversion first. Then, shortly after these signals are sampled by the ADC, the multiplexer control circuitry switches channels 8 to 15 as input to the ADC's.

DATA TRANSFER FROM ADC TO FPGA

A 16-bit serial shift register is implemented in the IP module's FPGA for each of the eight channels. Internal FPGA counters are used to synchronize the transfer of digitized data from the A/D converters to the FIFO memory. Only the channels enabled for conversion are stored in FIFO memory and tagged for channel identification.

CONVERSION COUNTER

The ADC conversion rate is controlled by a conversion counter, which is a 24-bit counter implemented in the FPGA. The counter provides variable time periods up to 2.0889 seconds. The output of this counter is compared to the value stored in the Conversion Timer register to trigger the start of new conversions for the continuous mode of operation. The output of the conversion counter is also compared to the value stored in the High Bank Timer register to determine when the second bank of channels (8 through 15) are to be simultaneously triggered for conversion.

EXTERNAL TRIGGER

The external trigger connections are made via pin 49 of the P2 Field I/O Connector. For all modes of operation, when the external trigger is enabled as an input via bits 4 and 5 of the channel's control register, the falling edge of the external trigger will initiate simultaneous conversions for channels 0 to 7. Once the external trigger signal has been driven low, it should remain low for a minimum of 250n seconds for proper external trigger operation. The external trigger input signals must be TTL compatible. The IP340/IP341 uses a diode clamping circuit to protect the board from external trigger signals that violate the 5 volt logic (TTL) requirement.

As an output, an active-low TTL signal is driven from the IP module. The trigger pulse generated is low for 500n seconds, typical. See section 3.0 for programming details to make use of this signal.

INTERRUPT CONTROL LOGIC

The IP340/IP341 can be configured to generate an interrupt using a programmable FIFO Threshold level. When the FIFO has more samples than the set threshold the IP interrupt signal INTREQ0* is issued to the carrier to request an interrupt. An 8-bit interrupt service routine vector is provided during an interrupt acknowledge cycle on data lines D0 to D7. The interrupt is released when the FIFO no longer has more samples than that set by the Threshold register. The interrupt request is also released if interrupts are disabled.

REFERENCE VOLTAGE MEMORY CONTROL LOGIC

The FPGA of the IP340/IP341 module contains control logic that implements read and write access to reference voltage memory. The reference voltage memory (EEPROM) contains an ASCII null terminated string that represents the exact voltage of the on board reference circuit.

IP Module Software

Acromag also provides a software diskette (sold separately) of IP module Object Linking and Embedding (OLE) drivers for Windows 95®/NT® compatible application programs (Model IPSW-OLE-PCI, MSDOS format). This software provides individual drivers that allow all IP modules and the APC8620 carrier to be easily integrated into Windows® application programs, such as Visual C++™, Visual Basic®, Borland Delphi®, Microsoft® Office® 97 applications and others. The OLE controls provide a high-level interface to IP modules, eliminating the need to perform low-level reads/writes of registers, and the writing of interrupt handlers—all the complicated details of programming are handled by the OLE controls. These functions are intended for use in conjunction with an Acromag personal computer carrier and consist of a carrier OLE control, and an OLE control for each Acromag IP module, as well as, a generic OLE control for non-Acromag IP modules.

In addition, Acromag provides a software product (sold separately) consisting of IP module VxWorks® drivers. This software (Model IPSW-API-VXW MSDOS format) is composed of VxWorks® (real time operating system) libraries for all Acromag IP modules and carriers including the AVME9660/9630, APC8610, and APC8620. The software is implemented as a library of "C" functions which link with existing user code to make possible simple control of all Acromag IP modules and carriers.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be easily damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board. When a board is first produced and when any repair is made, it is tested, placed in a burn-in room at elevated temperature, and retested before shipment.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in Section 2, Preparation For Use, have been followed. Also, refer to the documentation of your carrier board to verify that it is correctly configured. Replacement of the module with one that is known to work correctly is a good technique to isolate a faulty module.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

Acromag's Application Engineers can provide further technical assistance if required. When needed, complete repair services are also available from Acromag.

6.0 SPECIFICATIONS

PHYSICAL

Physical Configuration…….. Single Industrial Pack Module.
Length..... 3.880 in. (98.5 mm).
Width..... 1.780 in. (45.2 mm).
Board Thickness..... 0.062 in. (1.59 mm).
Max Component Height..... 0.290 in. (7.37 mm).
Connectors:
P1 (IP Logic Interface)..... 50-pin female receptacle header (AMP 173279-3 or equivalent).
P2 (Field I/O)..... 50-pin female receptacle header (AMP 173279-3 or equivalent).

Power Requirements		Module IP340/E	Module IP341/E
5V[1] (±5%)	Typical	65mA	76mA
	Max.	98mA	114mA
+12V (±5%)	Typical	7mA	7mA
	Max.	11mA	11mA
-12V (±5%)	Typical	-6mA	-6mA
	Max.	-10mA	-10mA

Note:
1. Maximum rise time of 100m seconds.

ENVIRONMENTAL

Operating Temperature..... Standard Unit 0 to +70°C. "E" suffixed units -40°C to +85°C.
Relative Humidity..... 5-95% Non-Condensing.
Storage Temperature..... -55°C to +125°C.

Non-Isolated..... Logic and field commons have a direct electrical connection.

Radiated Field Immunity[2] (RFI). Designed to comply with IEC1000-4-3 Level 3 (10V/m, 80 to 1000MHz AM & 900MHz. keyed) and European Norm EN50082-1 with error less than ±0.25% of FSR.

Electromagnetic Interference Immunity[2] (EMI)…….. Error is less than ±0.5% of FSR under the influence of EMI from switching solenoids, commutator motors, and drill motors.

Electrostatic Discharge Immunity[2] (ESD)…….. Complies with IEC1000-4-2, Level 3 (8KV/4KV air/direct discharge) to the enclosure port, 1KV direct to I/O, and European Norm EN50082-1.

Surge Immunity…….. Not required for signal I/O per European Norm EN50082-1.

Electric Fast Transient Immunity[2](EFT)…….. Complies with IEC1000-4-4 Level 2 (0.5KV at field input and output terminals) and European Norm EN50082-1.

Radiated Emissions[2]…….. Meets or exceeds European Norm EN50081-1 for class A equipment.

Warning: This is a class A product. In a domestic environment this product may cause radio interference in which the user may be required to take adequate measures.

Note:
2. Reference Test Conditions: Temperature 25°C, 100K conversions/second, using Acromag's AVME9660 VMEbus IP carrier with a 1 meter shielded cable length connection to the field analog input signals.

Reliability Prediction

Mean Time Between Failure….. MTBF = 594,899 hours Using MIL-HDBK-217F, Notice 2.

ANALOG INPUTS

Input Channels…….. Two Banks of Eight Channels (Channels 0-7 and 8-15). The Channels of Each Bank are Simultaneously Converted.
Input Overvoltage Protection…. +/-25 Volts Power On
+/-40 Volts Power Off
Data Format…….. Binary two's complement format left justified within the 16-bit word

Maximum Source Impedance[3]	Maximum Operating Frequency	Channels in Operation
2.2KΩ	125KHz	0 to 7 & 8 to 15
6KΩ	50KHz	0 to 7 & 8 to 15
25KΩ	12.5KHz	0 to 7 & 8 to 15
50KΩ	6.25KHz	0 to 7 & 8 to 15
100KΩ	3.12KHz	0 to 7 & 8 to 15
1MΩ	125KHz	0 to 7 only

Note:
3. A low source impedance is required at the maximum operating frequency when channels 0 to 7 and 8 to 15 are in use. This is due to the leakage current experienced when the input multiplexer switches between the lower bank channels 0 to 7 and the high bank channels 8 to 15.

ADC Spec's

Conversion Rate…….. 125KHz
Input Voltage Range…….. ±10 Volts
Data Format…….. Binary 2's Complement

IP340

ADC..... Analog Devices AD7895
ADC Resolution..... 12 Bits
No Missing Codes..... 12 Bits
Differential Nonlinearity..... ±1 LSB Maximum
Gain Error[4]..... ±2 LSB Maximum
Bipolar Zero Error[4]..... ±3 LSB Maximum

IP341

ADC..... Analog Devices AD7894
ADC Resolution..... 14 Bits
No Missing Codes..... 14 Bits
Differential Nonlinearity..... -1 to +1.5 LSB Maximum
Gain Error[4]..... ±6 LSB Maximum
Bipolar Zero Error[4]..... ±8 LSB Maximum

Instrumentation Amplifier

INAMP..... Burr-Brown INA128
Nonlinearity..... ±0.001% of FSR Maximum
Offset Voltage[4]..... ±550µ Volt Maximum
Gain Error[4]..... ±0.024% Maximum
Settling Time..... 7µ seconds Typical to 0.01%

Note:
4. Software calibration eliminates these error components.

5 Volt Calibration Reference Voltage

Temperature Drift..... 2ppm/°C Typical, 5ppm/°C Max.

Maximum Overall Calibrated Error @ 25°C

IP340 Max. Total Error[5]	IP341 Max. Total Error[5]
±1.6 LSB	±2.4 LSB
0.039% Span	0.014% Span

The maximum corrected (i.e. calibrated) error is the worst case accuracy possible. It is the sum of error components due to ADC quantization of the low and high calibration signals, instrumentation amplifier, and ADC linearity error at 25°C. For critical applications multiple input samples should be averaged to improve performance.

Note:
5. Software calibration must be performed in order to achieve the specified accuracy. Follow the output connection recommendations of Chapter 2, to keep non-ideal grounds from degrading overall system accuracy.

Input Noise IP341[6]..... 1 LSB rms, Typical.
Input Noise IP340[6]..... 0.5 LSB rms, Typical.
FIFO Buffer..... 512 Samples
Interrupt..... Vectored interrupt on programmed FIFO Threshold Met Condition.

Note:
6. Reference Test Conditions: Temperature 25°C, 125K conversions/second, using Acromag's APC8629 PCI bus IP carrier with a 2 meter cable length connection to the field analog input signal.

External Trigger Input/Output

As An Input:..... Negative edge triggered. Must be an active low 5 volt logic TTL compatible, debounced signal referenced to digital common. Conversions are triggered within 500n seconds of the falling edge. Minimum pulse width is 250n seconds.
As An Output..... Active low 5 volt logic TTL compatible output is generated. The trigger pulse is low for typically 500n seconds.

INDUSTRIAL I/O PACK COMPLIANCE

Specification..... This device meets or exceeds all written Industrial I/O Pack specifications per ANSI/VITA 4 1995 for 8MHz operation for Format I Modules.

Electrical/Mechanical
Interface..... Single-Size IP Module.

I/O Space Read/Write..... 16-bit, 8-bit:
ID Space Read..... 16-bit, 8-bit (low byte) Supports Type 1, 32 bytes per IP (consecutive odd byte addresses).
Memory Space..... Not Used.
Interrupts..... 8-bits (low byte) Generates INTREQ0* interrupt request per IP and interrupt acknowledge cycles via access to IP INT space.
Access Times (8MHz Clock):
ID Space Read..... 0 wait states (250ns cycle).
FIFO Buffer Read..... 2 wait states maximum (500ns), 1-wait states typical (375ns)
Registers Read/Write..... 0 wait states (250ns cycle).
Interrupt Read/Write..... 0 wait states (250ns cycle).

APPENDIX

CABLE: MODEL 5025-550-x (Non-Shielded)
MODEL 5025-551-x (Shielded)

Type: Flat Ribbon Cable, 50-wires (female connectors at both ends). The '-x' suffix designates the length in feet (12 feet maximum). Choose shielded or unshielded cable according to model number. The unshielded cable is recommended for digital I/O, while the shielded cable is recommended for optimum performance with precision analog I/O applications.
Application: Used to connect a Model 5025-552 termination panel to the AVME9630/9660 non-intelligent carrier board A-D connectors (both have 50-pin connectors).
Length: Last field of part number designates length in feet (user-specified, 12 feet maximum). It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50-wire flat ribbon cable, 28 gage. Non-Shielded cable model uses Acromag Part 2002-211 (3M Type C3365/50 or equivalent). Shielded cable model uses Acromag Part 2002-261 (3M Type 3476/50 or equivalent).
Headers (Both Ends): 50-pin female header with strain relief. *Header* - Acromag Part 1004-512 (3M Type 3425-6600 or equivalent). *Strain Relief* - Acromag Part 1004-534 (3M Type 3448-3050 or equivalent).
Keying: Headers at both ends have polarizing key to prevent improper installation.
Schematic and Physical Attributes: For Non-Shielded cable model, see Drawing 4501-462. For Shielded cable model, see Drawing 4501-463.
Shipping Weight: 1.0 pound (0.5Kg) packaged.

TRANSITION MODULE: MODEL TRANS-GP

Type: Transition module for AVME9630/9660 boards.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME card cages. This module is available for use in card cages which provide rear exit for I/O connections via transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VMEbus mechanical dimensions, except for shorter printed circuit board depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9630/9660 boards within card cage, via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Schematic and Physical Attributes: See Drawing 4501-465.
Field Wiring: 100-pin header (male) connectors (3M 3433-D303 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Connections to AVME9630/9660: 50-pin header (male) connectors (3M 3433-1302 or equivalent) employing long ejector latches and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to AVME9630/9660 boards within the card cage via flat 50-pin ribbon cable (cable Model 5025-550-X or 5025-551-X).
Mounting: Transition module is inserted into a 6U-size, single-width slot at the rear of the VMEbus card cage.
Printed Circuit Board: Six-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40 to +85°C.
Storage Temperature: -55°C to +105°C.
Shipping Weight: 1.25 pounds (0.6Kg) packaged.

CABLE: MODEL 5028-187 (SCSI-2 to Flat Ribbon, Shielded)

Type: Round shielded cable, 50-wires (SCSI-2 male connector at one end and a flat female ribbon connector at the other end). The cable length is 2 meters (6.56 feet). This shielded cable is recommended for all I/O applications (both digital I/O and precision analog I/O).
Application: Used to connect Model 5025-552 termination panel to the TRANS-200 Transition Module. The transition module then connects to all four IP module slots to the rear of the AVME9670 (Slots A-D).
Length: Standard lenght is 2 meters (6.56 feet). Consult factory for other lenghts. It is recommended that this length be kept to a minimum to reduce noise and power loss.
Cable: 50 conductors, 28 AWG on 0.050 inch centers (permits mass termination for IDC connectors), foil/braided shield inside a PVC jacket.
Connectors: (One End): SCSI-2, 50-pin male connector with backshell and spring latch hardware.
(Other End): IDC, 50-pin female connector with strain relief.
Keying: The SCSI-2 connector has a "D Shell" and the IDC connector has a polarizing key to prevent improper installation.
Schematic and Physical Attributes: See Drawing 4501-758.
Electrical Specifications: 30 VAC per UL and CSA (SCSI-2 connector spec.'s). 1 Amp maximum at 50% energized (SCSI-2 connector spec.'s).
Operating Temperature: -20°C to +80°C.
Storage Temperature: -40°C to +85°C.
Shipping Weight: 1.0 pound (0.5Kg), packed.

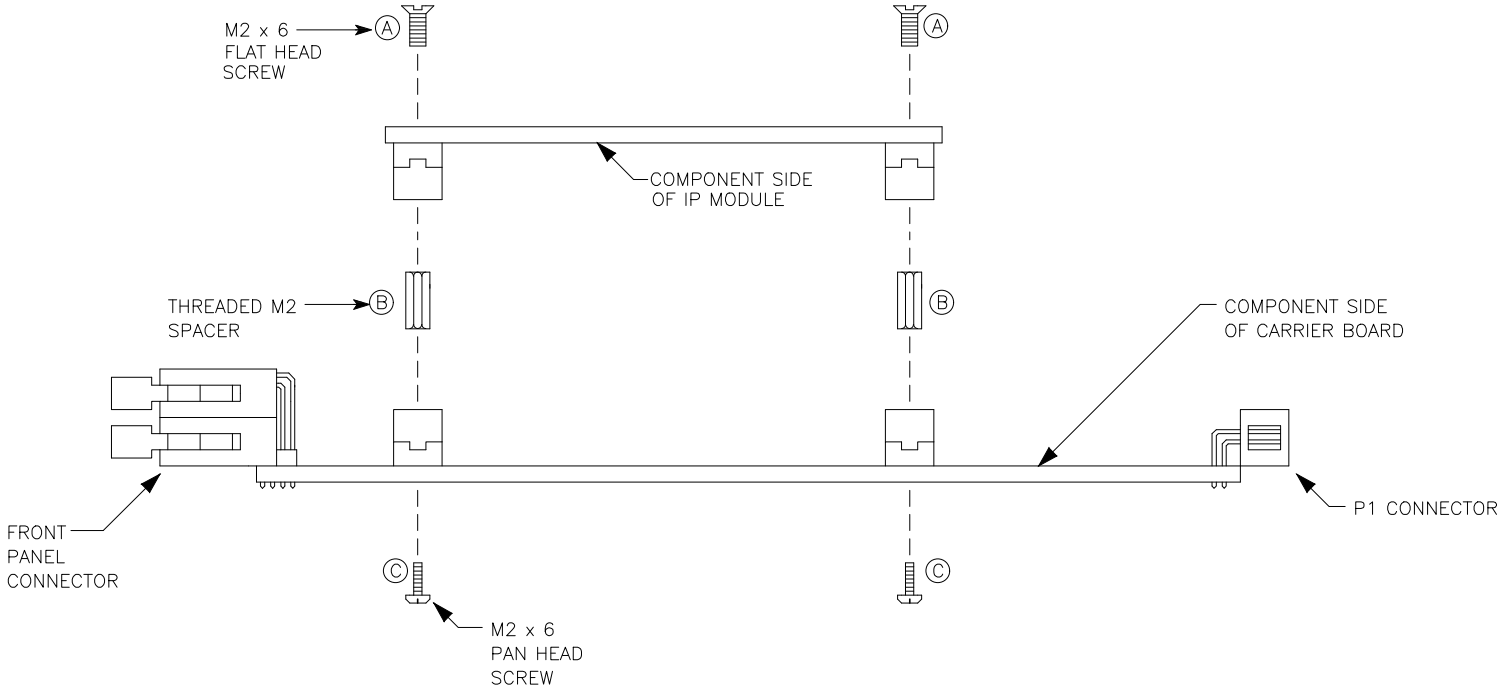
VME64x TRANSITION MODULE: MODEL TRANS-200

Type: Transition module for AVME9670 board.
Application: To repeat field I/O signals of IP modules A through D for rear exit from VME64x card cages. This module is available for use in card cages which provide rear exit for I/O connections via 80 mm wide transition modules (transition modules can only be used in card cages specifically designed for them). It is a double-height (6U), single-slot module with front panel hardware adhering to the VME64x bus mechanical dimensions and IEEE Standard (1101.11-1998), for 80 mm depth. Connects to Acromag termination panel 5025-552 from the rear of the card cage, and to AVME9670 boards within card cage, via connectors RP0 and RP2.
Schematic and Physical Attributes: See Drawing 4501-760.
Electrical Specifications: 30 VAC per UL and CSA (SCSI-2 connector spec.'s). 1 Amp maximum at 50% energized (SCSI-2 connector spec.'s).
Field Wiring: Four SCSI-2, 50-pin female connectors (AMP 787082-5 or equivalent) employing latch blocks and 30 micron gold in the mating area (per MIL-G-45204, Type II, Grade C). Connects to Acromag termination panel 5025-552 from the rear of the card cage via round shielded cable (Model 5028-187).
Connections to AVME9670: Connections are made though the PC board connectors RP0 (95 pin female with upper ground shield) and RP2 (160 pin female). The transition module plugs directly behind the AVME9670 board into the VME64x bus backplane within the card cage system.

Mounting: Transition module is inserted into a 6U-size, 80 mm width slot at the rear of the VME64Xbus card cage. (Directly behind AVME9670 board)
Printed Circuit Board: Eight-layer, military-grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +85°C.
Storage Temperature: -40°C to +85°C.
Shipping Weight: 1.25 pounds (0.6Kg) packed.

TERMINATION PANEL: MODEL 5025-552

Type: Termination Panel For AVME9630/9660, APC8610, or APC8620 Boards
Application: To connect field I/O signals to the Industrial I/O Pack (IP). *Termination Panel:* Acromag Part 4001-040 (Phoenix Contact Type FLKM 50). The 5025-552 termination panel facilitates the connection of up to 50 field I/O signals and connects to the AVME9630/9660 3U/6U, APC8610, or APC8620 non-intelligent carrier boards (field connectors only) via a flat ribbon cable (Model 5025-551-x). The A-D connectors on the carrier board connect the field I/O signals to the P2 connector on each of the Industrial I/O Pack modules. Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-50) correspond to P2 (pins 1-50) on the Industrial I/O Pack (IP). Each Industrial I/O Pack (IP) has its own unique P2 pin assignments. Refer to the IP module manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-464.
Field Wiring: 50-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.
Connections to AVME9630/9660, APC8610, or APC8620: P1, 50-pin male header with strain relief ejectors. Use Acromag 5025-551-x cable to connect panel to VME board. Keep cable as short as possible to reduce noise and power loss.
Mounting: Termination panel is snapped on the DIN mounting rail.
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.
Operating Temperature: -40°C to +100°C.
Storage Temperature: -40°C to +100°C.
Shipping Weight : 1.25 pounds (0.6kg) packaged.

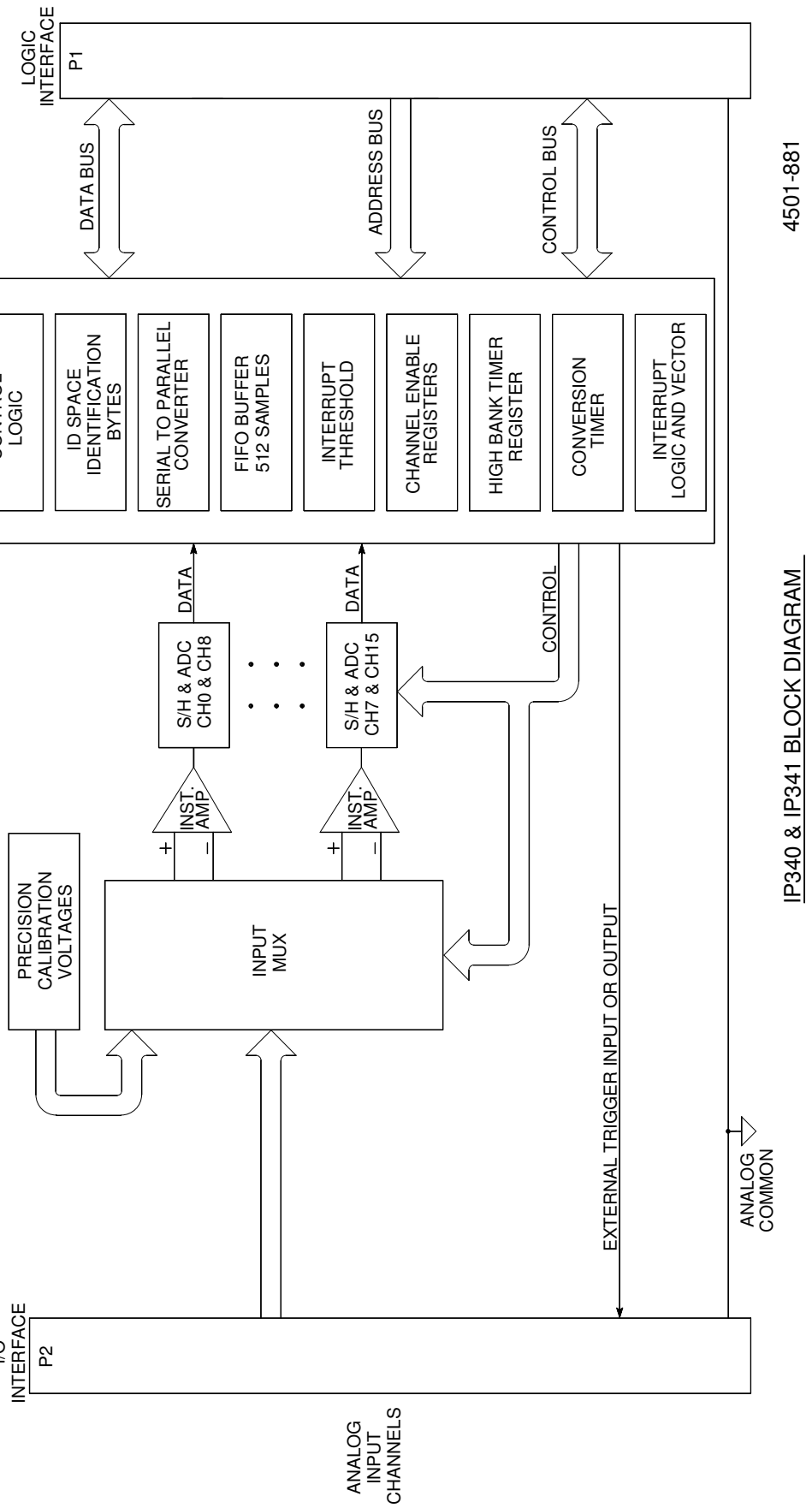


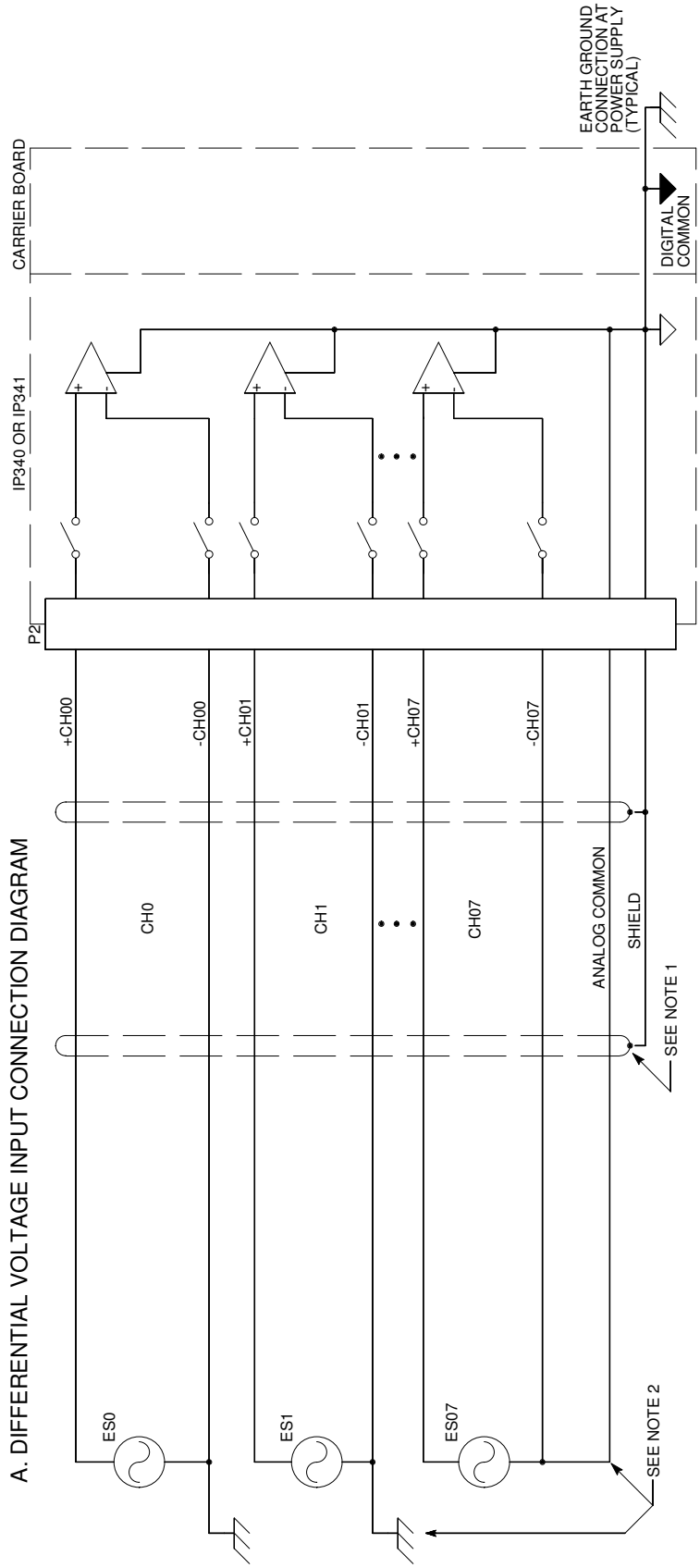
ASSEMBLY PROCEDURE:

1. THREADED SPACERS ARE PROVIDED FOR USE WITH AVME 9630/9660 CARRIER BOARDS (SHOWN). CHECK YOUR CARRIER BOARD TO DETERMINE ITS REQUIREMENTS. MOUNTING HARDWARE PROVIDED MAY NOT BE COMPATIBLE WITH ALL TYPES OF CARRIER BOARDS.
2. INSERT FLAT HEAD SCREWS (ITEM A) THROUGH SOLDER SIDE OF IP MODULE AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES) UNTIL HEX SPACER IS COMPLETELY SEATED. THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.
3. CAREFULLY ALIGN IP MODULE TO CARRIER BOARD AND PRESS TOGETHER UNTIL CONNECTORS AND SPACERS ARE SEATED.
4. INSERT PAN HEAD SCREWS (ITEM C) THROUGH SOLDER SIDE OF CARRIER BOARD AND INTO HEX SPACERS (ITEM B) AND TIGHTEN (4 PLACES). THE RECOMMENDED TORQUE IS 0.226 NEWTON METER OR 2 INCH POUNDS. OVER TIGHTENING MAY DAMAGE CIRCUIT BOARD.

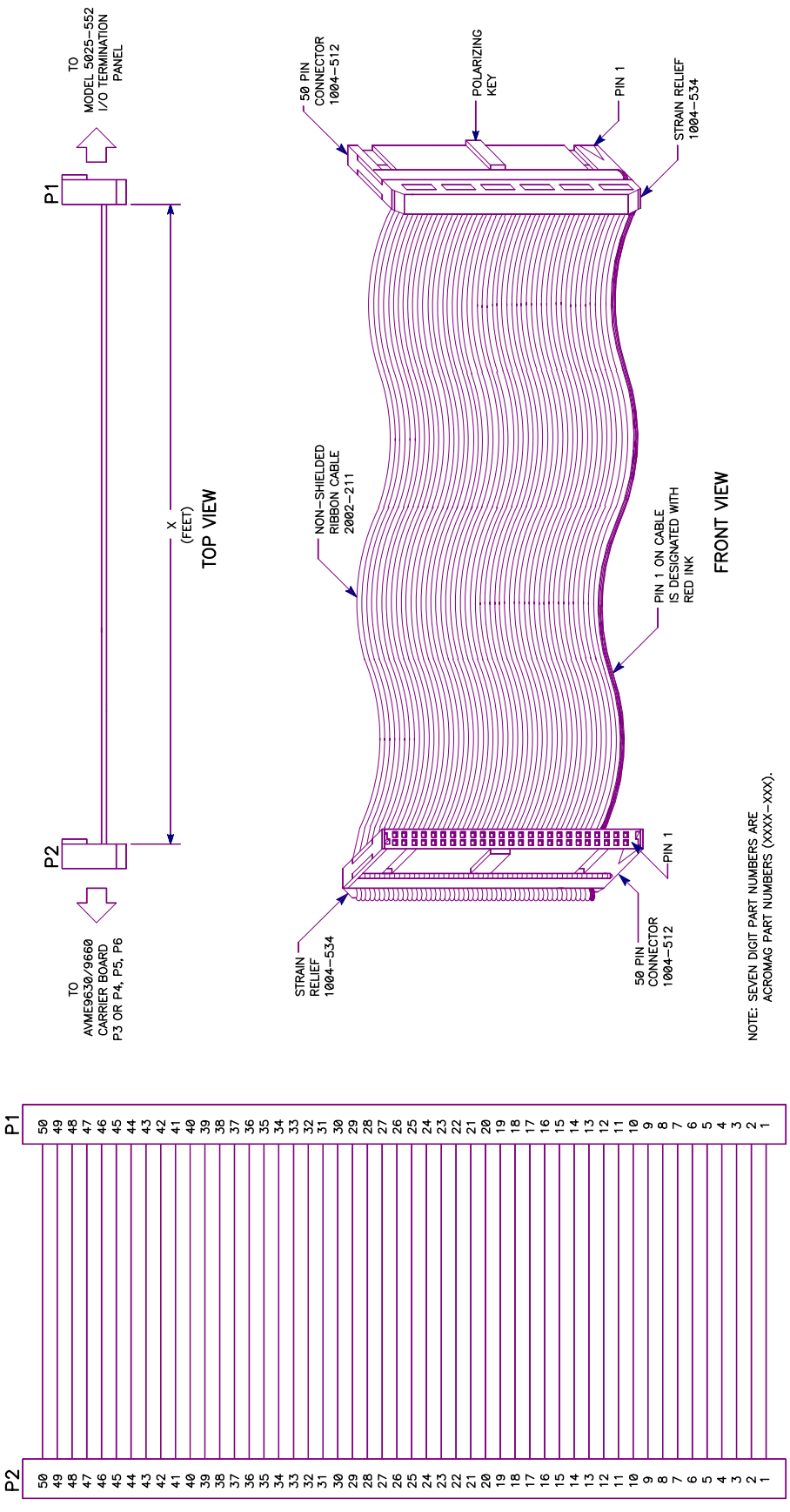
IP MODULE TO CARRIER BOARD MECHANICAL ASSEMBLY

4501-434C


LOGIC INTERFACE
P1
DATA BUS
ADDRESS BUS
CONTROL BUS
4501-881
FPGA
CONTROL LOGIC
ID SPACE IDENTIFICATION BYTES
SERIAL TO PARALLEL CONVERTER
FIFO BUFFER 512 SAMPLES
INTERRUPT THRESHOLD
CHANNEL ENABLE REGISTERS
HIGH BANK TIMER REGISTER
CONVERSION TIMER
INTERRUPT LOGIC AND VECTOR
DATA
DATA
CONTROL
S/H & ADC CH0 & CH8
S/H & ADC CH7 & CH15
INST. AMP.
INST. AMP.
+
–
+
–
PRECISION CALIBRATION VOLTAGES
INPUT MUX
EXTERNAL TRIGGER INPUT OR OUTPUT
ANALOG COMMON
I/O INTERFACE
P2
ANALOG INPUT CHANNELS
IP340 & IP341 BLOCK DIAGRAM



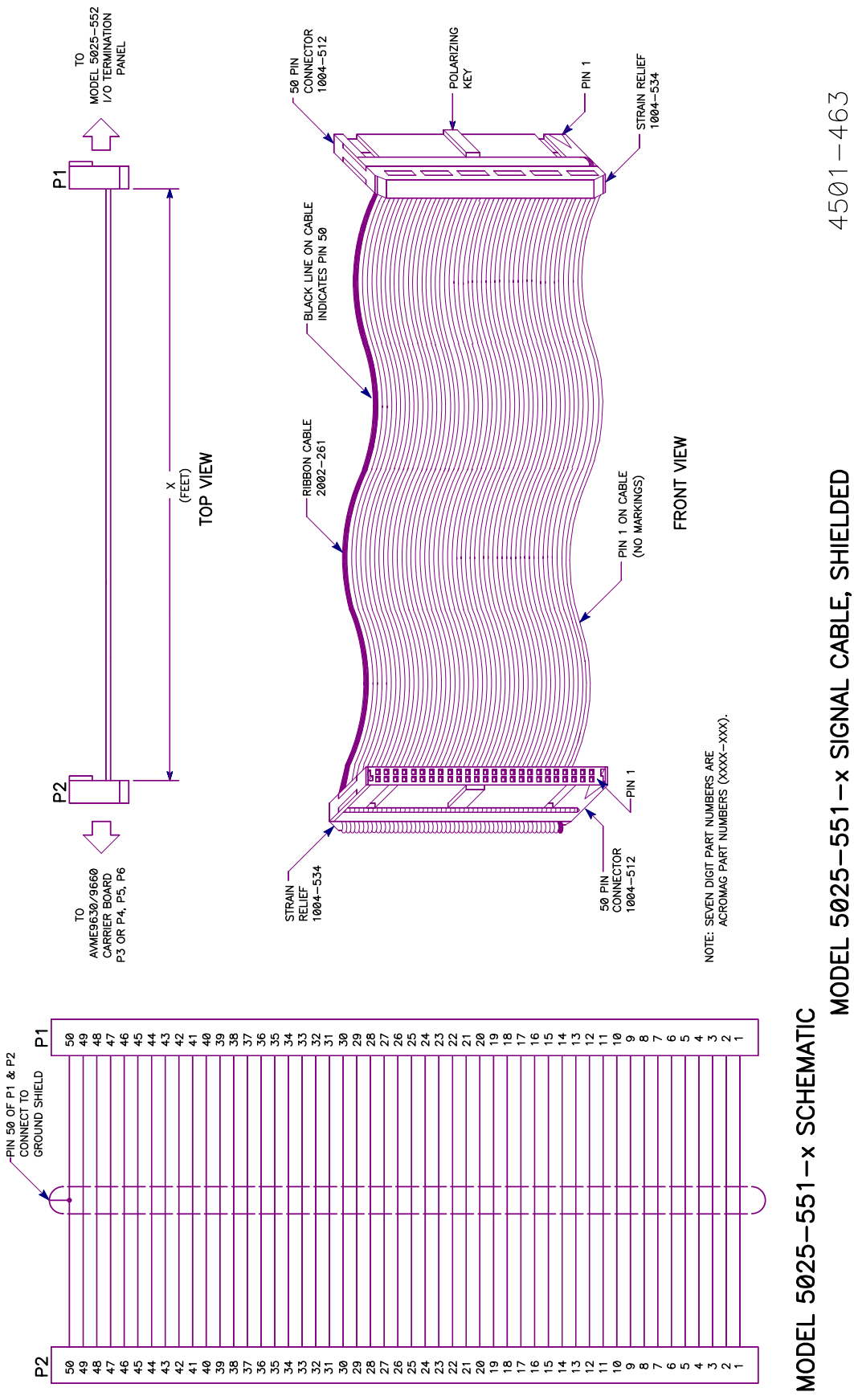
NOTES:
1. SHIELDED CABLE IS RECOMMENDED FOR LOWEST NOISE. SHIELD IS CONNECTED TO GROUND REFERENCE AT ONE END ONLY TO PROVIDE SHIELDING WITHOUT GROUND LOOPS.
2. REFERENCE CHANNELS TO ANALOG COMMON, IF THEY WOULD OTHERWISE BE FLOATING. CHANNELS ALREADY HAVING A GROUND REFERENCE MUST NOT BE CONNECTED TO ANALOG COMMON, TO AVOID GROUND LOOPS.



MODEL 5025-550-x SCHEMATIC

MODEL 5025-550-x SIGNAL CABLE, NON-SHIELDED

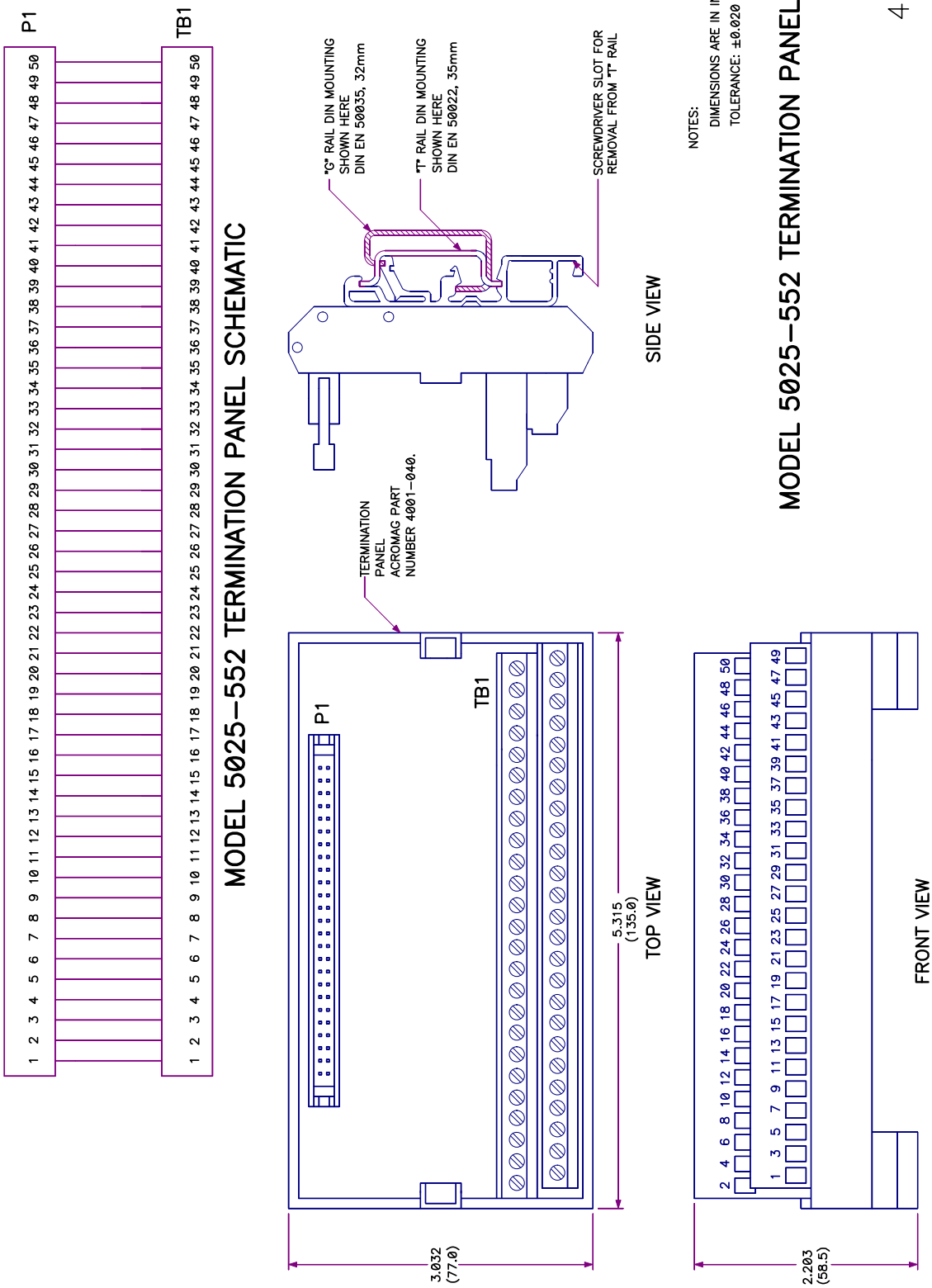
4501-462

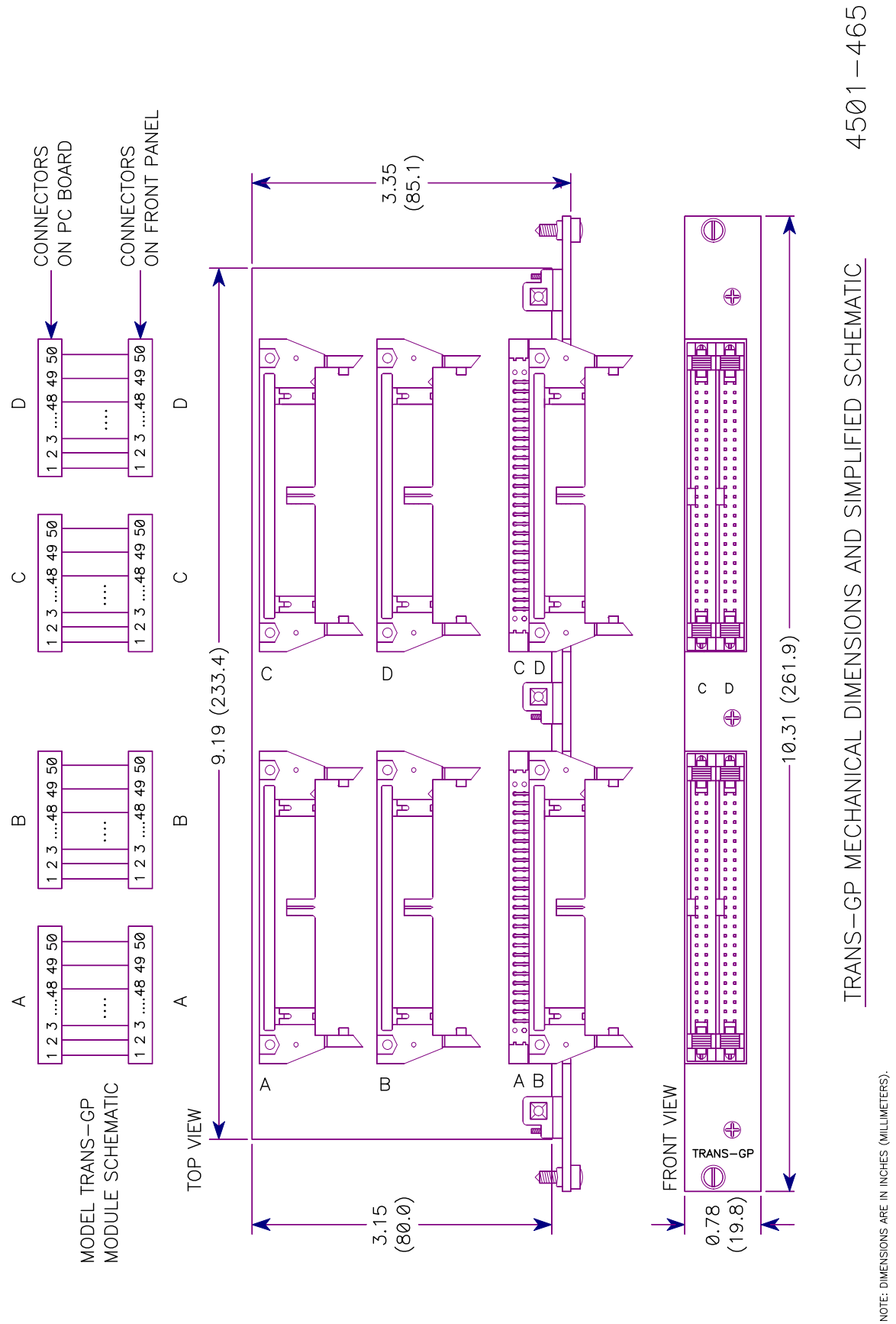


MODEL 5025-551-x SCHEMATIC

MODEL 5025-551-x SIGNAL CABLE, SHIELDED

4501-463


P1
TB1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
MODEL 5025-552 TERMINATION PANEL SCHEMATIC
"G" RAIL DIN MOUNTING SHOWN HERE DIN EN 50035, 32mm
"T" RAIL DIN MOUNTING SHOWN HERE DIN EN 50022, 35mm
SCREWDRIVER SLOT FOR REMOVAL FROM "T" RAIL
SIDE VIEW
NOTES:
DIMENSIONS ARE IN INCHES (MILLIMETERS).
TOLERANCE: ±0.020 (±0.5).
MODEL 5025-552 TERMINATION PANEL
4501-464
TERMINATION PANEL ACROMAG PART NUMBER 4001-040.
P1
TB1
5.315 (135.0)
3.032 (77.0)
TOP VIEW
2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50
1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49
2.203 (58.5)
FRONT VIEW


4501-465
TRANS-GP MECHANICAL DIMENSIONS AND SIMPLIFIED SCHEMATIC
CONNECTORS ON PC BOARD
CONNECTORS ON FRONT PANEL
A
B
C
D
1 2 3 ....48 49 50
MODEL TRANS-GP MODULE SCHEMATIC
TOP VIEW
9.19 (233.4)
3.35 (85.1)
3.15 (80.0)
A
B
C
D
A B
C D
FRONT VIEW
TRANS-GP
10.31 (261.9)
0.78 (19.8)
NOTE: DIMENSIONS ARE IN INCHES (MILLIMETERS).