Mini-ITX

i852GM4-DCQI

Intel® Celeron® M Mini ITX Main Board

User's Manual

1st Ed – 23 August 2007

FCC Statement

THIS DEVICE COMPLIES WITH PART 15 FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS:

(1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE.

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

THIS EQUIPMENT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS "A" DIGITAL DEVICE, PURSUANT TO PART 15 OF THE FCC RULES.

THESE LIMITS ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST HARMFUL INTERFERENCE WHEN THE EQUIPMENT IS OPERATED IN A COMMERCIAL ENVIRONMENT. THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTATLLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE HARMFUL INTERFERENCE TO RADIO COMMUNICATIONS.

OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE HARMFUL INTERFERENCE IN WHICH CASE THE USER WILL BE REQUIRED TO CORRECT THE INTERFERENCE AT HIS OWN EXPENSE.

Notice

This guide is designed for experienced users to setup the system within the shortest time. For detailed information, please always refer to the electronic user's manual.

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Headquarters
Advansus Corp.
No.1, Alley 20, Lane 26, Rueiguang Road,
Neihu District, Taipei 114,
Taiwan
Tel : +886-2-2792-7818
Fax : +886-2-2794-7306
http://www.Advansus.com.tw
E-mail: service@Advansus.com.tw

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This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advansus, or which have been subject to misuse, abuse, accident or improper installation. Advansus assumes no liability under the terms of this warranty as a consequence of such events. Because of Advansus high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If any of Advansus products is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details. If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU type and speed, Advansus products model name, hardware & BIOS revision number, other hardware and software used, etc.) Note anything abnormal and list any on-screen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information available.
3. If your product is diagnosed as defective, obtain an RMA (return material authorization) number from your dealer. This allows us to process your good return more quickly.
4. Carefully pack the defective product, a complete Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Contents

1. Getting Started

1.1 Safety Precautions

Warning!

Always completely disconnect the power cord from your chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

Caution!

Always ground yourself to remove any static charge before touching the CPU card. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

1.2 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped: Onboard Intel® Celeron® M 600MHz w/512K 2nd Level Cache

- 1 x i852GM onboard Intel® Celeron® M 600 MHz with 0K L2 Cache
- 1 x CD-ROM or DVD-ROM contains the followings:
  - User's Manual (this manual in PDF file)
  - Ethernet driver and utilities
  - VGA drivers and utilities
  - Audio drivers and utilities
- 1 x Cable set contains the followings:
  - 1 x IDE HDD cable (40-pin, pitch 2.54mm)
  - 2 x Serial ATA cable (34-pin, pitch 2.54mm)
  - 2 x Serial port cable with 3 DB9P(M) (10-pin, pitch 2.54mm)
  - 1 x I/O shield

If any of the above items is damaged or missing, contact your retailer.

1.3 Document Amendment History

Revision	Date	By	Comment
1st	Aug. 2007		Initial Release

1.4 Manual Objectives

This manual describes in detail the Advansus Technology i852GM4 Main Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with i852GM4 series or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

1.5 System Specifications

System	
Model	**i852GM4-DCQI**
CPU	Onboard Intel uFC-BGA 479 Celerom M 600MHz w/512K 2nd Level Cache with 0.13um process technology
FSB	400 MHz
BIOS	Award 4 Mb Flash BIOS
System Chipset	Intel® 82852GM GMCH/ 82801DB ICH4
I/O Chip	Winbond W83627EHG-A
System Memory	One 184-pin DIMM socket supports up to 1 GB DDR 200/266 SDRAM
SSD	One CompactFlash Type I/II socket
Watchdog Timer	Reset: 1 sec.~255 min. and 1 sec. or 1 min./step
H/W Status Monitor	Monitoring CPU temperature, voltage, and cooling fan status. Auto throttling control when CPU overheats
Expansion	One PCI slot (PCI Rev. 2.2 compliant) supports 3 PCI master
S3	S3 Support
SmartFan Control	YES
I/O	
MIO	1 x EIDE (Ultra DMA 100), 2 x SATA, 4 x RS-232, 1 x K/B, 1 x Mouse, (COM1~4 with Power output)
USB	6 x USB 2.0
DIO	16-bit General Purpose I/O for DI and DO
IEEE-1394A **Extra SATA Chips**	Silicon Image Sil 3512 supports 2 SATA with 150 MB/s transfer rate.

i852GM4-DCQI

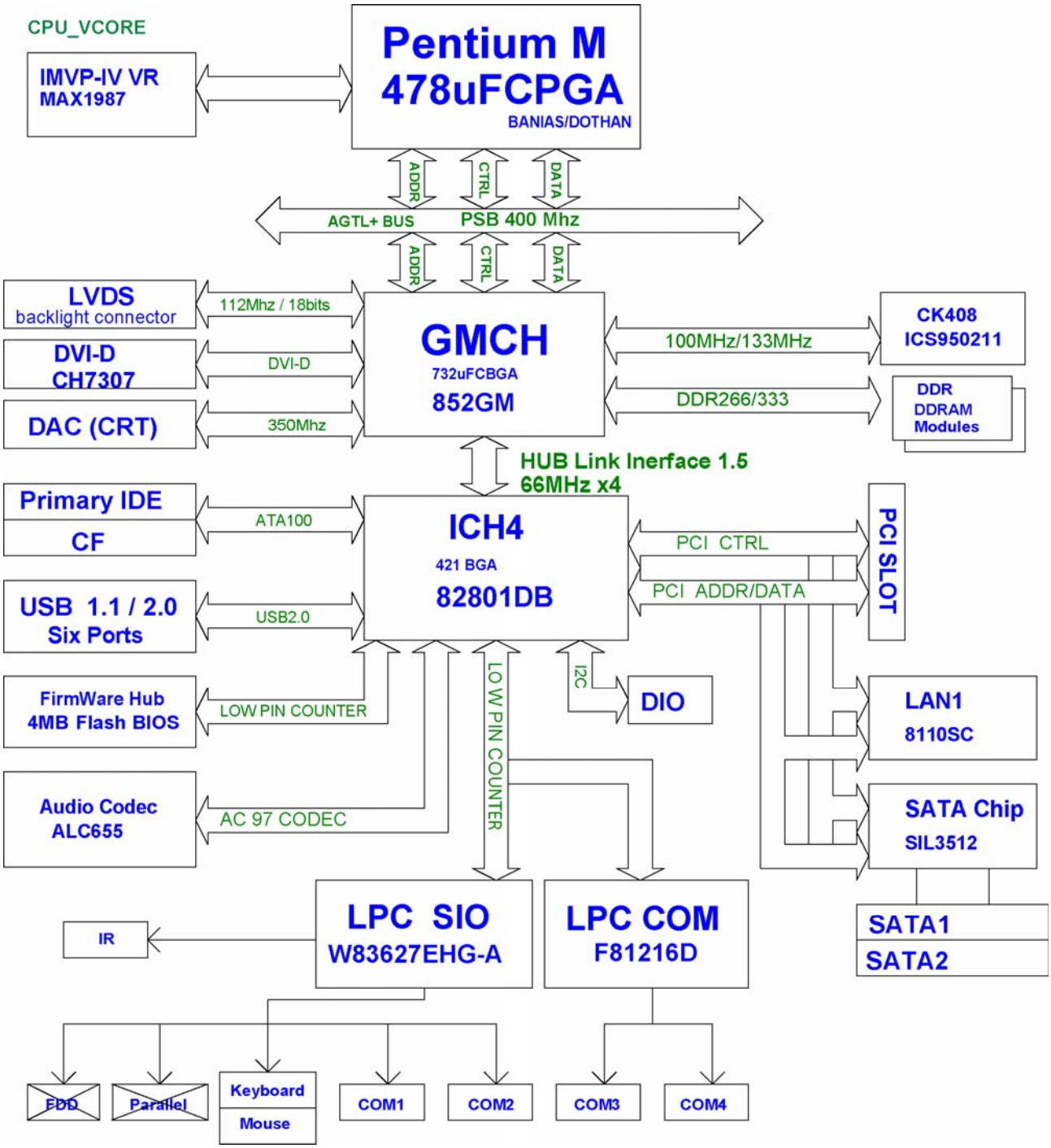
Display	
Model	**i852GM4-DCQI**
Chipset	Intel® 82852GM GMCH integrated Extreme Graphics 2 controller
Display Memory	Intel® DVMT 2.1 supports up to 64 MB video memory
Resolution	CRT mode: 1600 x 1200 @ 32 bpp (85 Hz) LCD/Simultaneous mode: 1600 x 1200 @ 32 bpp (85 Hz)
Dual Display	CRT + LVDS, or CRT + DVI
VGA/LCD Interface	N/A
LVDS	Intel® 852GM supports Single channel 18/ (24) -bit/Dual-channel 36-bit LVDS
DVI	Chrontel CH7301 DVI transmitter up to 135M pixels/second
Audio	
Audio Codec	Realtek ALC655 supports 5.1 ch. Audio (3 jacks)
Audio Interface	Mic in, Line in, Line out
Audio Amplifer	TPA3005D2 Stereo 5Watt per channel
Ethernet	
LAN1	Realtek RTL8110SC Gigabit LAN

Mechanical & Environmental	
Model	**i852GM4-DCQI**
Power Type	AT/ATX
Operation Temperature	0~60° C (32~140° F)
Operating Humidity	0%~90% relative humidity, non-condensing
Size (L x W)	6.69" x 6.69" (170 mm x 170 mm)
Weight	0.88 lbs (0.4 Kg)

1.6 Architecture Overview

1.6.1 Block Diagram

The following block diagram shows the architecture and main components of i852GM4-DCQI.



The following sections provide detail information about the functions provided onboard.

1.6.2 Intel RG82855GME and FW82801DB

The Intel 855GM/855GME GMCH components provide the processor interface, DDR SDRAM interface, display interface, and Hub interface. The Intel 855GME also has an option for AGP external graphics port, in addition to integrated graphics support for added board flexibility options.

The Intel 855GM GMCH is in a 732-pin Micro-FCBGA package and contains the following functionality listed below:

- AGTL+ host bus supporting 32-bit host addressing with Enhanced Intel SpeedStep technology support
- Supports a single channel of DDR SDRAM memory
- System memory supports DDR200/266 MHz (SSTL_2) DDR SDRAM
- Integrated graphics capabilities: Display Core frequency at 133 MHz or 200 MHz
- Render Core frequency at 100 MHz ,133 MHz, and 200 MHz
- Provides supports four display ports: one progressive scan analog monitor, dual channel LVDS interface and two DVO port.

The Intel 855GME GMCH is in a 732-pin Micro-FCBGA package and contains all features listed above and the additional functionality list below:

- Display Core frequency at 133 MHz, 200 MHz, or 250 MHz
- Render Core frequency at 100 MHz ,133 MHz, 166 MHz, 200 MHz, or 250 MHz
- System memory supports 200/266/333- MHz (SSTL_2) DDR SDRAM.
- Enhanced Power Management Graphics features

The GMCH IGD provides a highly integrated graphics accelerator delivering high performance 2D, 3D, and video capabilities. With its interfaces to UMA using a DVMT configuration, an analog display, a LVDS port, and two digital display ports (e.g. flat panel), the GMCH can provide a complete graphics solution.

The GMCH also provides 2D hardware acceleration for block transfers of data (BLTs). The BLT engine provides the ability to copy a source block of data to a destination and perform raster operations (e.g., ROP1, ROP2, and ROP3) on the data using a pattern, and/or another destination. Performing these common tasks in hardware reduces CPU load, and thus improves performance. High bandwidth access to data is provided through the system memory interface. The GMCH uses Tiling architecture to increase system memory efficiency and thus maximize effective rendering bandwidth. The Intel 855GM/855GME GMCH improves 3D performance and quality with 3D Zone rendering technology. The Intel 855GME GMCH also supports Video Mixer rendering and Bi-Cubic filtering.

The Intel 855GM/855GME GMCH has four display ports, one analog and three digital. With these interfaces, the GMCH can provide support for a progressive scan analog monitor, a dedicated dual channel LVDS LCD panel, and two DVO devices. Each port can transmit data according to one or more protocols. The data that is sent out the display port is selected from one of the two possible sources, Pipe A or Pipe B.

The Intel 855GM/855GME GMCH have an integrated dual channel LFP Transmitter interface to support LVDS LCD panel resolutions up to UXGA The display pipe provides panel up-scaling to fit a smaller source image onto a specific native panel size, as well as provides panning and centering support. The LVDS port is only supported on Pipe B. The LVDS port can only be driven by Pipe B, either independently or simultaneously with the Analog Display port. Spread Spectrum Clocking is supported: center and down spread support of 0.5%, 1%, and 2.5% utilizing an external SSC clock.

The DVO B/C interface is compliant with the DVI Specification 1.0. When combined with a DVI compliant external device (e.g. TMDS Flat Panel Transmitter, TV-out encoder, etc.), the GMCH provides a high-speed interface to a digital or analog display (e.g. flat panel, TV monitor, etc.). The DVO ports are connected to an external display device. Examples of this are TV-out encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device. The GMCH provides two DVO ports that are each capable of driving a 165-MHz pixel clock at the DVO B or DVO C interface. When DVO B and DVO C are combined into a single DVO port, then an effective pixel rate of 330 MHz can be achieved. The DVO B/C ports can be driven by Pipe A or Pipe
B. If driven on Pipe B, then the LVDS port must be disabled.

The ICH4 is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI Bus and integrates many of functions needed in today's PC platform. The GMCH and ICH4 communicate over a dedicated hub interface. The 82801DB ICH4 functions and capabilities include:

- PCI Rev. 2.2 compliant with support for 33MHz PCI operations
- Supports up to 6 Request/Grant pairs (PCI slots)
- Power management logic support
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated IDE controller; Ultra ATA/100/66/33
- USB host interface; 3 host controllers and supports 6 USB ports; includes a EHCI high-speed 2.0 USB controller

- Integrated LAN controller
- System Management Bus (SMBus) compatible with most IC devices; ICH4 has both bus master and slave capability
- AC '97 2.3 compliant link for audio and telephony codecs; up to 6 channels
- Low Pin Count (LPC) interface
- FWH Interface (FWH Flash BIOS support)
- Alert on LAN* (AOL and AOL2)

1.6.3 Intel RG82852GM and FW82801DB

The Intel 852GM GMCH component provides the processor interface, DDR SDRAM interface, display interface, and Hub Interface in an Intel 852GM chipset platform. The Intel 852GM GMCH is optimized for the Mobile Intel Pentium 4 Processor-M, Mobile Intel Celeron processor and Intel Celeron M processor. It supports a single channel of DDR SDRAM memory. Intel 852GM Chipset contains advanced power management logic. The Intel 852GM Chipset platform supports the fourth generation mobile I/O Controller Hub to provide the features required by a mobile platform.

The Intel 852GM GMCH is in a 732-pin Micro-FCBGA package and contains the following functionality:

- Supports single Intel processor configurations at 400-MHz or 3 GB/s
- 1.2-1.30-V AGTL+ host bus supporting 32-bit host bus addressing with Enhanced Intel SpeedStep® technology (Intel Celeron M processor and Intel Celeron Processor do not support Enhanced Intel SpeedStep Technology).
- System Memory supports 200/266-MHz (SSTL_2) DDR DRAM Up to 1 GB (with 256-Mb technology and two SO-DIMMs) of PC1600/2100 DDR SDRAM without ECC
- Integrated graphics capabilities, including 3D rendering acceleration and 2D hardware acceleration
- Integrated 350-MHz, 24-bit RAMDAC with pixel resolution up to 1600x1200 at 85-Hz and up to 1920x1440 @ 60 Hz
- One Dedicated Dual Channel LFP LVDS interface with frequency range of 25 MHz to 112 MHz (single channel/dual channel) for support up to SXGA+ (1400x1050 @ 60 Hz) panel resolutions with maximum pixel depth of 18-bpp
- Integrated PWM (Pulse Width Modulation) interface for LFP backlight inverter control for panel brightness
- One 165-MHz, 12-bit, DVO interface for TV-out encoder and DVI (LVDS transmitter and TMDS transmitter) support I^2C and DDC channels supported
- Dual Pipe Independent Display with Tri-view support through LFP, DVO, and CRT
- Deeper Sleep state support

- Distributed arbitration for highly concurrent operation
- Three USB host controllers provide high performance peripherals with 480 Mbps of bandwidth, while enabling support for up to six USB 2.0 ports. This results in a significant increase over previous integrated 1-4 port hubs at 12 Mbps
- The latest AC ’97 implementation delivers 20-bit audio for enhanced sound quality and full surround sound capability. Integrated audio solutions continue to enjoy success as a very cost-effective, yet high-performance solution
- LAN Connect Interface (LCI) provides flexible network solutions such as 10/100 Mbps Ethernet and 10/100 Mbps Ethernet with LAN manageability
- Dual Ultra ATA/100 controllers, coupled with the Intel® Application Accelerator – a performance software package – support faster IDE transfers to storage devices
- Intel Application Accelerator software provides additional performance over native ATA drivers by improving I/O transfer rates and enabling faster O/S load time, resulting in accelerated boot times
- Communication and Network Riser (CNR) offers flexibility in system configuration with a baseline feature set that can be upgraded with an audio card, modem card, or network card

1.6.4 DRAM Interface (Intel RG855GME)

The 855GME GMCH system memory controller directly supports the following:

- One channel of PC1600/2100/2700 DDR SDRAM memory
- DDR SDRAM devices with densities of 128-Mb, 256-Mb, and 512-Mb technology
- Up to 1 GB (512-Mb technology) SDRAM

1.6.5 DRAM Interface (Intel RG852GM)

The 852GM GMCH system memory controller directly supports the following:

- One channel of PC1600/2100 DDR SDRAM memory
- DDR SDRAM devices with densities of 128-Mb, 256-Mb, and 512-Mb technology
- Variable page sizes of 2-kB, 4-kB, 8-kB, and 16-kB. Page size is individually selected for every row and a maximum of 16 pages may be opened simultaneously

1.6.6 PCI Interface

The ICH4 PCI interface provides a 33 MHz, Rev. 2.2 compliant implementation. All PCI signals are 5V tolerant, except PME#. The ICH2 integrates a PCI arbiter that supports up to six external PCI bus masters in addition to the internal ICH4 requests.

1.6.7 IDE Interface (Bus Master Capability and Synchronous DMA Mode)

The fast IDE interface supports up to four IDE devices providing an interface for IDE hard disks and ATAPI devices. Each IDE device can have independent timings. The IDE interface supports PIO IDE transfers up to 16 Mbytes/sec and Ultra ATA transfers up 100 Mbytes/sec. It does not consume any ISA DMA resources. The IDE interface integrates 16x32-bit buffers for optimal transfers.

The ICH4's IDE system contains two independent IDE signal channels. They can be electrically isolated independently. They can be configured to the standard primary and secondary channels (four devices). There are integrated series resistors on the data and control lines.

Access to these controllers is provided by two standard IDC 40-pin connectors.

1.6.8 USB 2.0

The ICH4 contains an Enhanced Host Controller Interface (EHCI) compliant host controller that supports USB high-speed signaling. High-speed USB 2.0 allows data transfers up to 480Mb/s which is 40 times faster than full-speed USB. The ICH4 also contains three Universal Host Controller Interface (UHCI) controllers that support USB full-speed and low-speed signaling.

The ICH4 supports 6 USB 2.0 ports. All six USB ports are high-speed, full-speed, and low-speed capable. ICH4's port-routing logic determines whether a USB port is controlled by one of the UHCI controllers or by the EHCI controller.

1.6.9 Realtek ALC655 Audio Codec

VIA Technologies' VT1616TM 18-bit audio codec conforms to the AC'97 2.2 specifications. The VT1616 integrates Sample Rate Converters on all channels and can be adjusted in 1Hz increments. There is a provision in hardware for down-mixing the 6 channels into stereo when only two end points are available. The analog mixer circuitry integrates a stereo enhancement to provide a pleasing 3D surround sound effect for stereo media. This codec is designed with aggressive power management to achieve low power consumption. When used with a 3.3V analog supply, power consumption is further reduced. The primary applications for this part are desktop and portable personal computers multimedia subsystems.

1.6.10 Chrontel CH7009A TV/DVI Transmitter

The Chrontel CH7009A is a display controller device which accepts a digital graphics input signal, and encodes and transmits data through a DVI (DFP can also be supported) or TV output (analog composite, s-video or RGB). The device accepts data over one 12-bit wide variable voltage data port which supports five different data formats including RGB and YCrCb.

The DVI processor includes a low jitter PLL for generation of the high frequency serialized clock, and all circuitries are required to encode, serialize and transmit data. The CH7009 comes in versions able to drive a DVI display at a pixel rate of up to 165MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device.

The TV-Out processor performs non-interlace to interlace conversion with scaling and flicker filters, and encode the data into any of the NTSC or PAL video standards. The scaling and flicker filter is adaptive and programmable to enable superior text display. Eight graphics resolutions are supported up to 1024 by 768 with full vertical and horizontal underscan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. Support is provided for Macrovision^{TM} and RGB bypass mode which enables driving a VGA CRT with the input data.

1.6.11 Ethernet

1.6.11.1 Realtek RTL8100C Ethernet Controller

The Realtek RTL8100C(L) is a highly integrated, cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T and Power Interface (ACPI), PCI power management for modern operating systems that are cpable of Operating System-Directed Power Management (OSPM) to achieve that most efficient power management possible. The RTL8100C(L) does not support CardBus mode (the RTL8139C does).

In addition to the ACPI feature, the RTL8100C(L) also supports remote wake-up (including AMD magic Packet, LinkChg, and Microsoft® wake-up frame) in both ACPI and APM (Advanced Power Management) environments. The RTL8100C(L) is capable of performing an internal reset through the application of auxiliary power. When auxiliary power is applied and the main power remains off, the RTL8100C(L) is ready and waiting for a Magic Packet or Link Change to wake the system up. Also, the LWAKE pin provides 4 output signals (active high, active low, positive pulse, and negative pulse). The versatility of the RTL8100C(L) LWAKE pin provides motherboards, with Wake-On-LAN (WOL) functionality.

The RTL8100C(L) also supports Analog Auto-Power-down. The analog part of the RTL8100C(L) can be shut down temporarily according to user requirements, or when the RTL8100C(L) is in a power down state with the wakeup function disabled. When the analog part is shut down and the IsolateB pin is low (i.e. the main power is off), both the analog and digital parts stop functioning and the power consumption of the RTL8100C(L) is negligible.

The RTL8100C(L) also supports an auxiliary power auto-detect function, and will auto-configure related bits of its PCI power management registers in PCI configuration space.

PCI Vital Product Data (VPD) is also supported to provide hardware identifier information. The information may consist of part number, serial number, OEM brand name, and other detailed information.

1.6.11.2 Realtek RTL8100S Gigabit Ethernet Controller

The Realtek RTL8110SB(L) LOM Gigabit Ethernet controllers (RTL8110SB (128 QFP) & RTL8110SBL (128 LQFP)) combine a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, 32-bit PCI bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, they offer high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The devices support the PCI v2.3 bus interface for host communications with power management and are compliant with the IEEE 802.3 specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. They also support an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

They support the Advanced Configuration Power management Interface (ACPI)--power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)--to achieve the most efficient power management possible. PCI Message Signaled Interrupt (MSI) is also supported.

In addition to the ACPI feature, the RTL8110SB(L) support remote wake-up (including AMD Magic Packet, Re-LinkOk, and Microsoft® Wake-up frame) in both ACPI and APM (Advanced Power Management) environments. The LWAKE pin provides four different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality. To support WOL from a deep power down state (e.g. D3cold, i.e. main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8110SB(L).

The RTL8110SB(L) is fully compliant with Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE 802 IP Layer 2 priority encoding and 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server. Also, the devices boost their PCI performance by supporting PCI Memory Read Line & Memory Read Multiple when transmitting, and Memory Write and Invalidate when receiving. To better qualify for server use, the RTL8110SB(L) support the PCI Dual Address Cycle (DAC) command when the assigned buffers reside at a physical memory address higher than 4 Gigabytes.

1.6.12 Winbond W83627HF

The Winbond W83627F/HF is made to fully comply with Microsoft PC98 and PC99 Hardware Design Guide. Moreover, W83627F/HF is made to meet the specification of PC98/PC99's requirement in the power management: ACPI and DPM (Device Power Management). Super I/O chip provides features as the following:

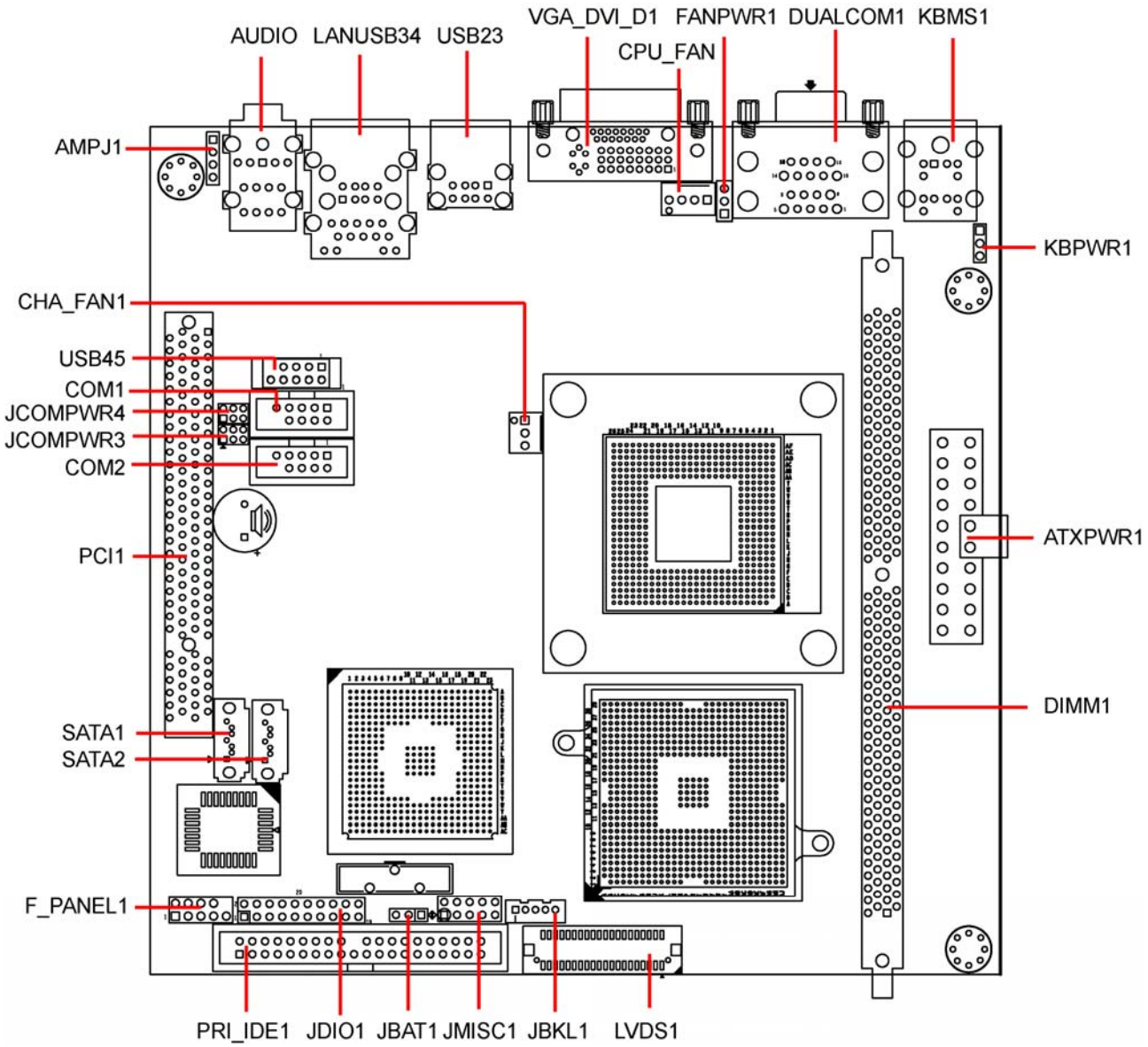
- Meet LPC Spec. 1.0
- Support LDRQ# (LPC DMA), SERIRQ (serial IRQ)
- Include all features of Winbond I/O W83977TF and W83977EF
- Integrate Hardware Monitor functions
- Compliant with Microsoft PC98/PC99 Hardware Design Guide.
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input

1.6.13 Compact Flash Interface

A Compact Flash type II connector is connected to the secondary IDE controller. The Compact Flash storage card is IDE compatible. It is an ideal replacement for standard IDE hard drives. The solid-state design offers no seek errors even under extreme shock and vibration conditions. The Compact Flash storage card is extremely small and highly suitable for rugged environments, thus providing an excellent solution for mobile applications with space limitations. It is fully compatible with all consumer applications designed for data storage PC card, PDA, and Smart Cellular Phones, allowing simple use for the end user. The Compact Flash storage card is O/S independent, thus offering an optimal solution for embedded systems operating in non-standard computing environments. The Compact Flash storage card is IDE compatible and offers various capacities.

2. Hardware Configuration

2.1 Product Overview



2.2 Installation Procedure

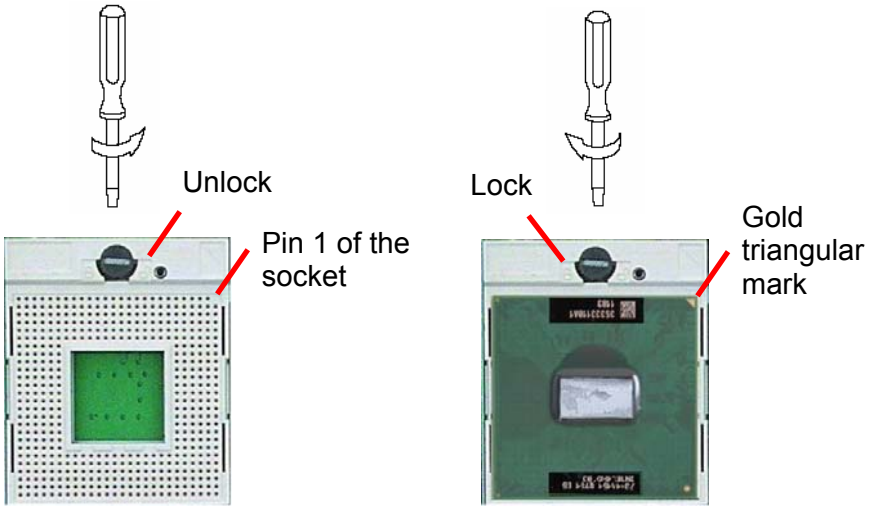
This chapter explains you the instructions of how to setup your system.

1. Turn off the power supply.
2. Insert the DIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the ATXPWR.
5. Turn on the power.
6. Enter the BIOS setup by pressing the delete key during boot up. Use the "LOAD BIOS DEFAULTS" feature. The ***Integrated Peripheral Setup*** and the ***Standard CMOS Setup*** Window must be entered and configured correctly to match the particular system configuration.
7. If TFT panel display is to be utilized, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

2.2.1 Processor Installation

2.2.1.1 Installing Pentium M CPU

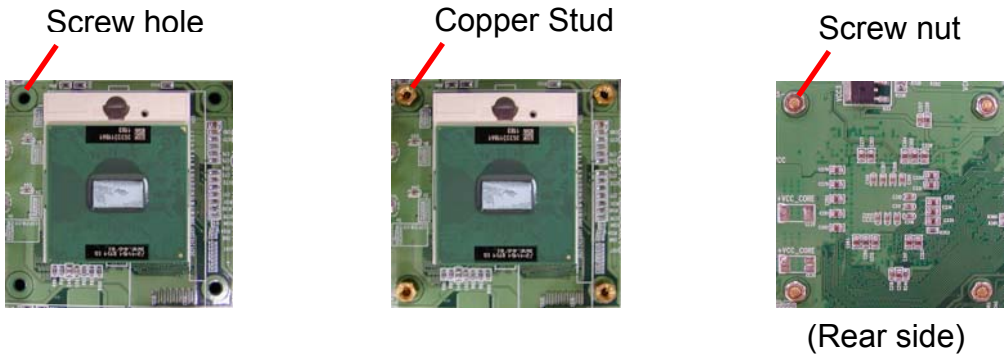
- The processor socket comes with a screw to secure the processor, please unlock the screw first.
- Position the CPU above the socket and the gold triangular mark on the CPU must align with pin 1 of the CPU socket. Then Insert the CPU gently seated in place.
- Turn the screw to the lock position.



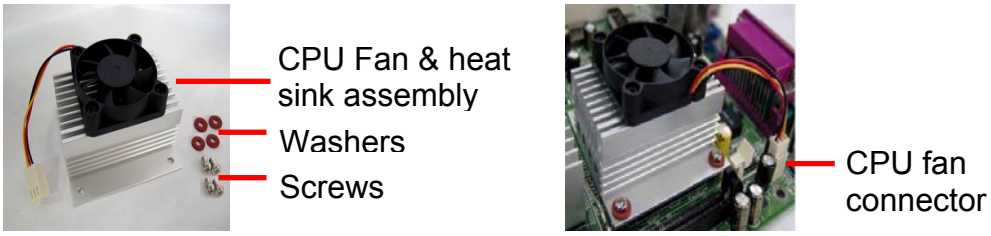
Note: Do not force the CPU into the socket. It may bend the pins and damage the CPU.

2.2.1.2 Installing the Fan and Heat Sink

- Insert the copper studs to the screw holes around the CPU socket from the top through the rear side of the board with screw nuts fastened.



- Match and place the CPU fan and heat sink assembly on the top of the CPU and copper studs. Tighten the screws into the copper studs through washers and the screw holes around the heat sink.
- Place the CPU Fan Connector.



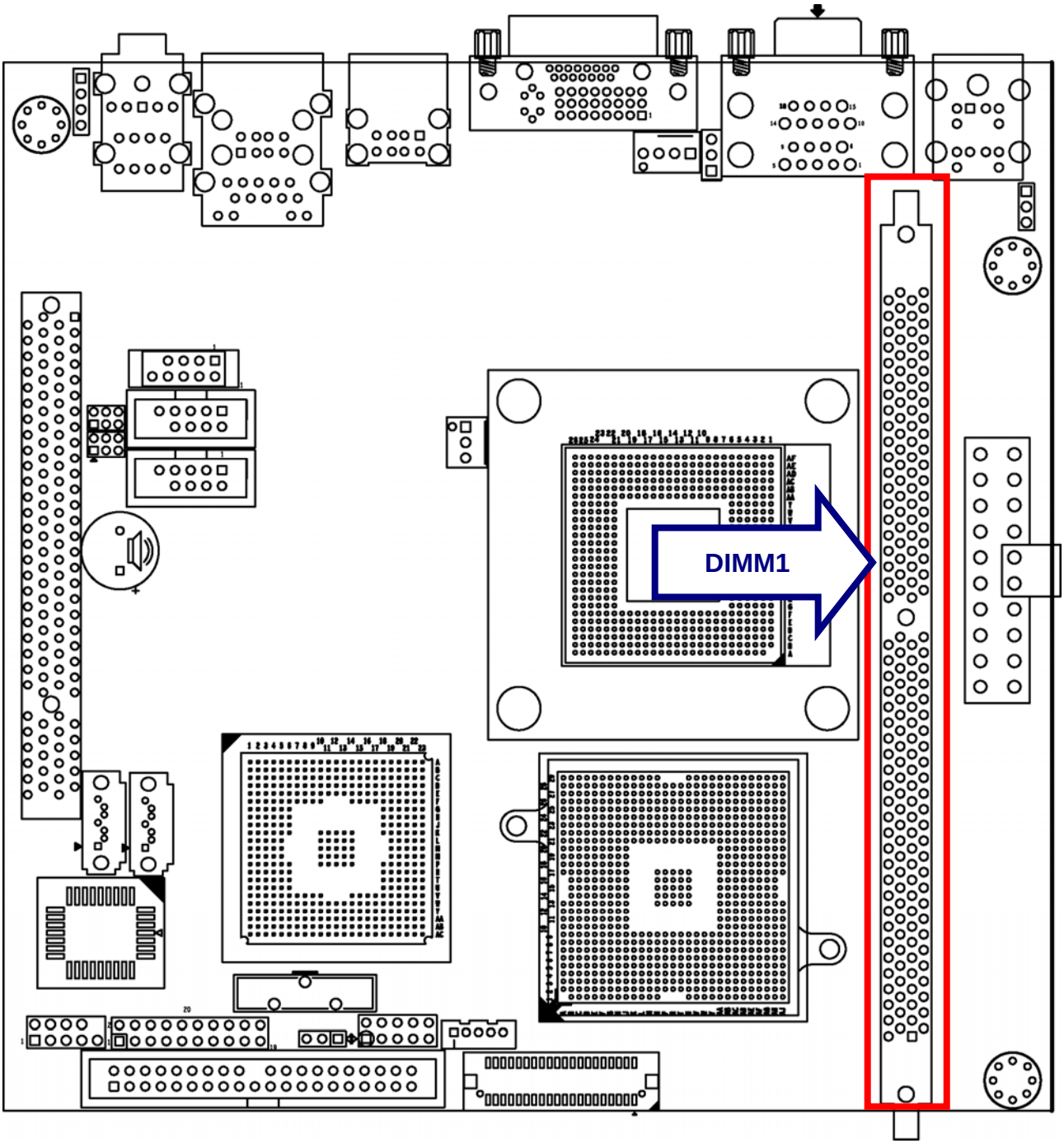
Note: Make sure the CPU fan and heat sink assembly and the CPU top surface are in total contact to avoid CPU overheating problem that would cause the system to hang or unstable

2.2.1.3 Removing CPU

- Disconnect the CPU fan connector.
- Remove the CPU fan and heat sink assembly first.
- Unfasten the copper studs from the board.
- Unlock the Pentium M processor.
- Carefully lift up the existing CPU to remove it from the socket.
- Follow the steps of installing a CPU to change to another one.

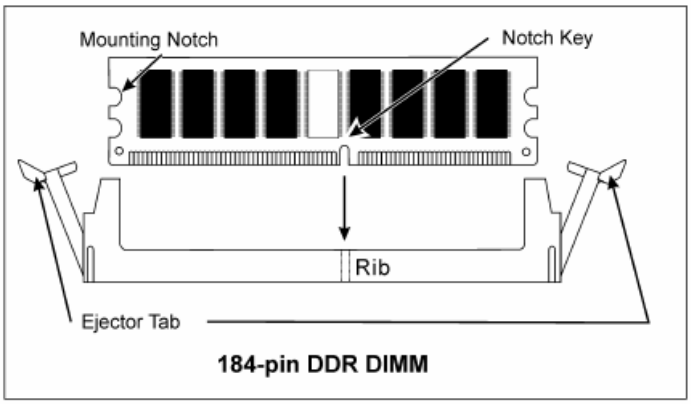
2.2.2 Main Memory

i852GM4 provides one 184-pin DIMM socket to support DDR SDRAM. The total maximum memory size is 1GB.

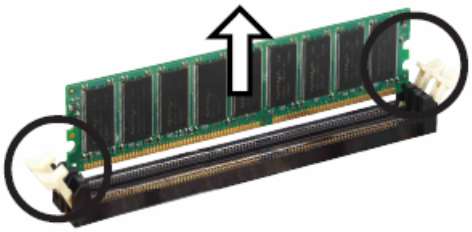


Make sure to unplug the power supply before adding or removing DIMMs or other system components. Failure to do so may cause severe damage to both the board and the components.

- Locate the DIMM slot on the board.
- Hold two edges of the DIMM module carefully. Keep away of touching its connectors.
- Align the notch key on the module with the rib on the slot.
- Firmly press the modules into the slot automatically snaps into the mounting notch. Do not force the DIMM module in with extra force as the DIMM module only fit in one direction.



- To remove the DIMM modules, push the two ejector tabs on the slot outward simultaneously, and then pull out the DIMM module.



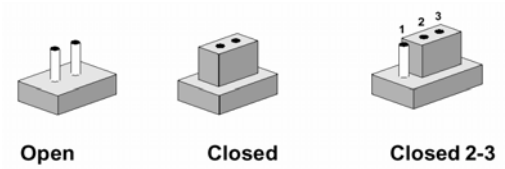
Note: (1) Please do not change any DDR SDRAM parameter in BIOS setup to increase your system's performance without acquiring technical information in advance.

(2) Static electricity can damage the electronic components of the computer or optional boards. Before starting these procedures, ensure that you are discharged of static electricity by touching a grounded metal object briefly.

2.3 Jumper and Connector List

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” a jumper you connect the pins with the clip. To “open” a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



The jumper settings are schematically depicted in this manual as follows:

A pair of needle-nose pliers may be helpful when working with jumpers.

Connectors on the board are linked to external devices such as hard disk drives, a keyboard, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

The following tables list the function of each of the board's jumpers and connectors.

Jumpers

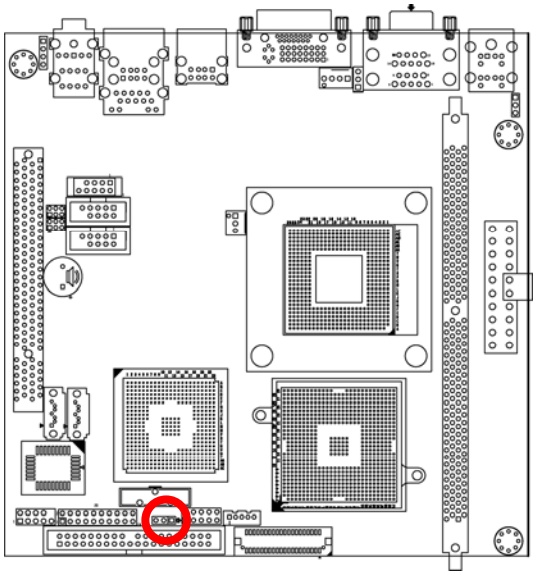
Label	Function	Note
JBAT1	Clear CMOS	3 x 1 header, pitch 2.54mm
JCOMPWR3	COMA pin 9 signal select	3 x 2 header, pitch 2.0mm
JCOMPWR4	COMB pin 9 signal select	3 x 2 header, pitch 2.0mm
KBPWR1	Keyboard Power select	3 x 1 header, pitch 2.54mm

Connectors

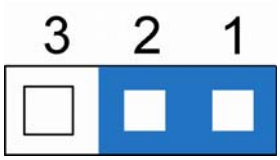
Label	Function	Note
AMPJ1		4 x 1 header, pitch 2.54mm
ATXPWR1	ATX Power connector	ATX power connector
AUDIO	Audio connector	Phone jack x 3
CHA_FAN1	System fan connector	3 x 1 wafer, pitch 2.54mm
COM1	Serial port A connector	5 x 2 header, pitch 2.54mm
COM2	Serial port B connector	5 x 2 header, pitch 2.54mm
CPU_FAN	CPU fan connector	4 x 1 wafer, pitch 2.54mm
DIMM1	184-pin DDR SDRAM DIMM socket	
DUALCOM1	Serial port1 connector Serial port 2 connector	D-sub 9-pin, male D-sub 9-pin, male
FAN_PWR1	CPU fan connector	3 x 1 header, pitch 2.54mm
F_PANEL1	Front panel connector	5 x 2 header, pitch 2.54mm
JBKL1	LCD inverter connector	5 x 1 wafer, pitch 2.0mm
JDIO1	Digital input/output connector	10 x 2 header, pitch 2.54mm
JMISC1	Miscellaneous setting connector	5 x 2 header, pitch 2.54mm
KBMS1	PS/2 keyboard & mouse connector	6-pin Mini-DIN x 2
LANUSB34	RJ-45 Ethernet / USB 0 & 1 connector	
LVDS1	LVDS connector	HIROSE DF 13-40DP-1.25V
PCI1	PCI slot	
PRI_IDE1	Primary IDE connector	20 x 2 header, pitch 2.54mm
SATA1	SATA connector	
SATA2	SATA connector	
USB23	USB connector 2 & 3	
USB45	USB connector 4 & 5	
VGA_DVI-D1	VGA connector DVI connector	D-sub 15-pin, female D-sub 24-pin, female

2.4 Setting Jumpers & Connectors

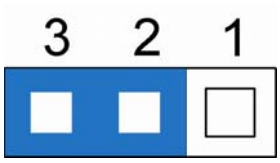
2.4.1 Clear CMOS (JBAT1)



Protect*

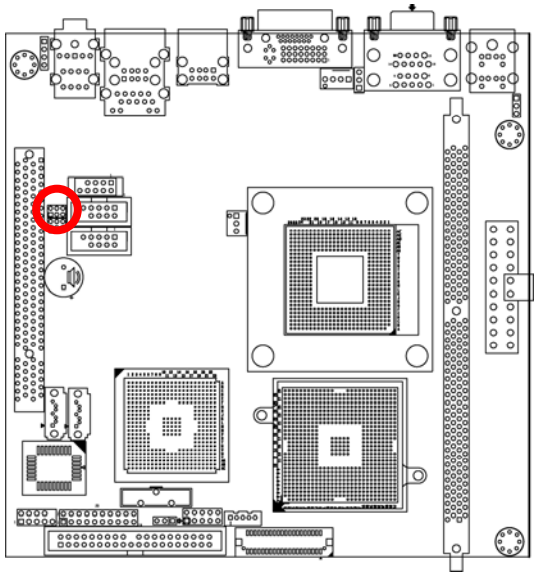


Clear CMOS



*** Default**

2.4.2 COMA Pin 9 Signal Select (JCOMPWR1)



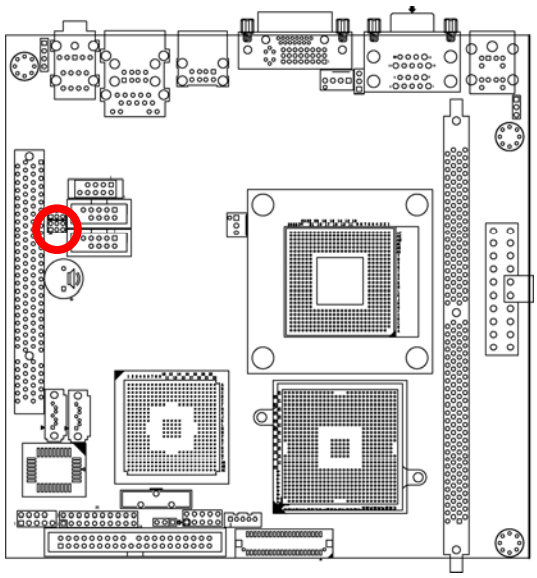
+5V

+12V

Ring*

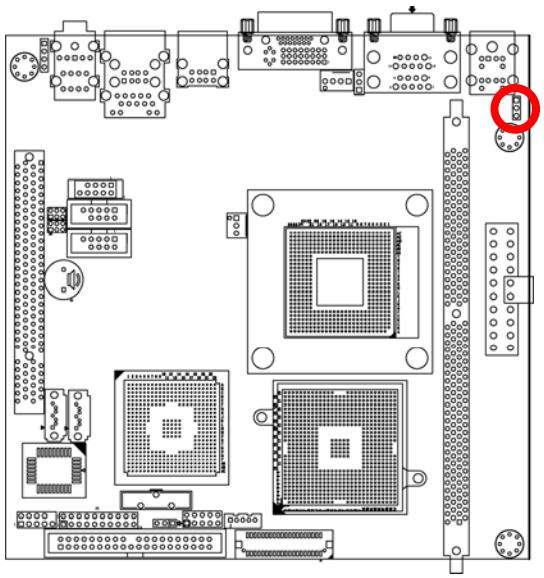
*** Default**

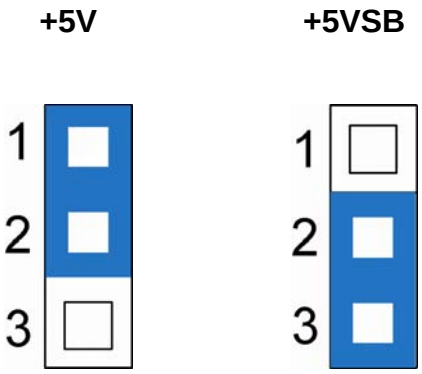
2.4.3 COMB Pin 9 Signal Select (JCOMPWR2)



*** Default**

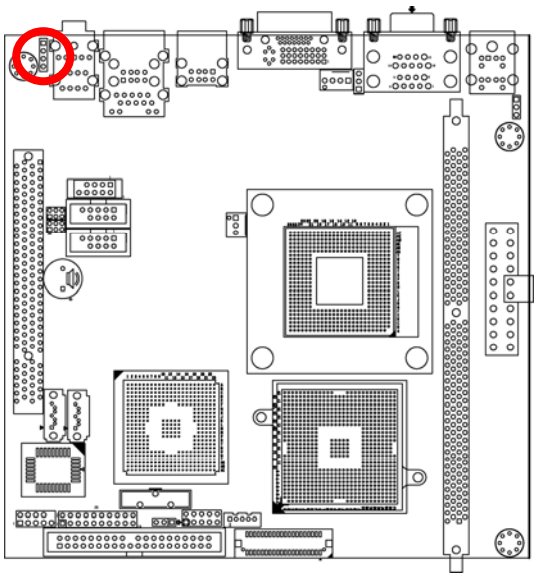
2.4.4 Keyboard Power Select (KBPWR1)





*** Default**

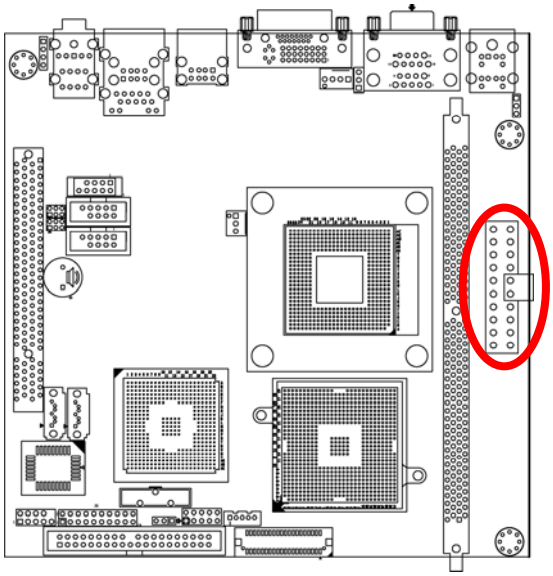
2.4.5 (AMPJ1)

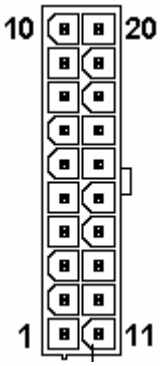


Signal	PIN
	1
	2
	3
	4

*** Default**

2.4.6 ATX Power Connector (ATXPWR1)



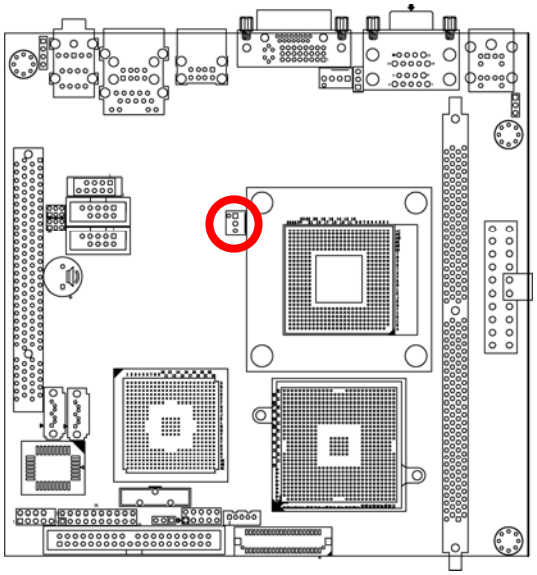


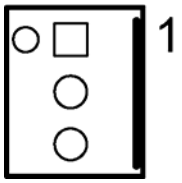
Signal	PIN	PIN	Signal
+12V	10	20	+5V
VCCSB	9	19	+5V
PWROK	8	18	-5V
GND	7	17	GND
+5V	6	16	GND
GND	5	15	GND
+5V	4	14	PS_ON
GND	3	13	GND
+3.3V	2	12	-12V
+3.3V	1	11	+3.3V

2.4.7 Audio Connector (AUDIO)

Port	Description
Audio-In	Connects a tape player or other audio sources.
Audio-Out	Connects a headphone or a speaker.
Microphone	Connects a microphone.

2.4.8 System Fan Connector (CHA_FAN1)



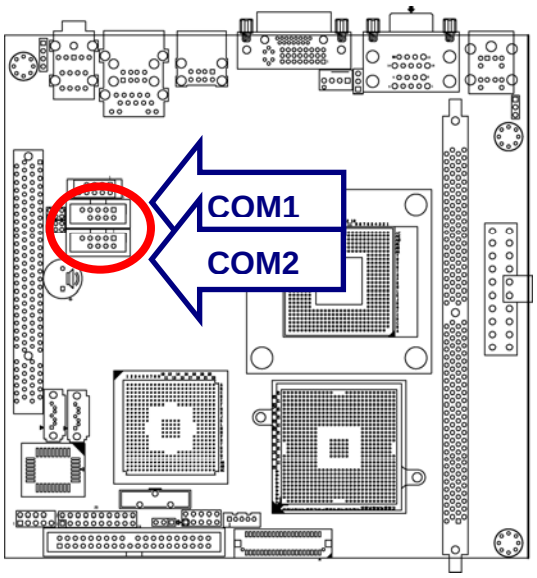


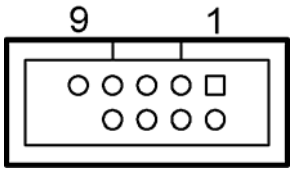
Signal	PIN
Sense	1
Power pin	2
GND	3

2.4.8.1 Signal Description – System Fan Connector (CHA_FAN1)

Signal	Signal Description
TAC	Fan speed monitor

2.4.9 Serial Port A/B Connector (COM1, COM2)



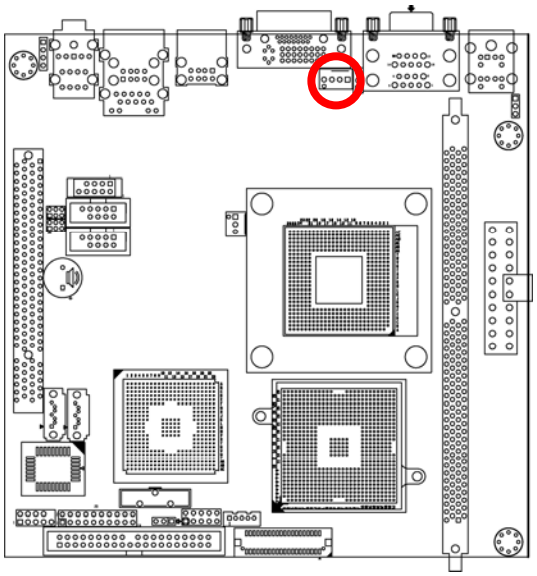


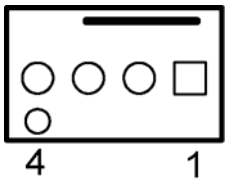
Signal	PIN	PIN	Signal
DCD	1	2	RxD
TxD	3	4	DTR
GND	5	6	DSR
RTS	7	8	CTS
RI	9		

2.4.9.1 Signal Description – Serial Port A/B Connector (COM1, COM2)

Signal	Signal Description
TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone ringing signal.

2.4.10 CPU Connector (CPU_FAN)



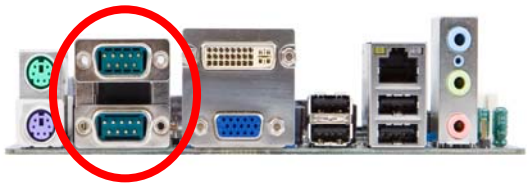


Signal	PIN
GND	1
Power pin	2
Sense	3
PWM input	4

2.4.10.1 Signal Description – CPU Fan Connector (CPU_FAN)

Signal	Signal Description
TAC	Fan speed monitor

2.4.11 Serial Port 1/2 Connector (DUALCOM1)

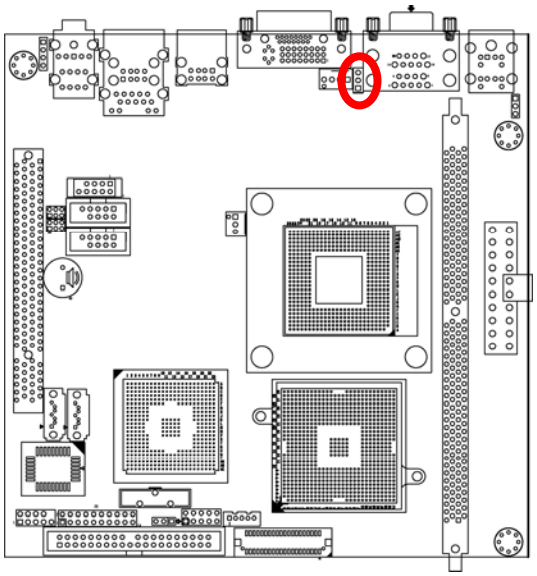


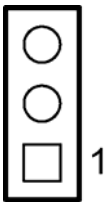
Signal	PIN	PIN	Signal
DCD	1	2	RxD
TxD	3	4	DTR
GND	5	6	DSR
RTS	7	8	CTS
RI/+5V/+12V	9	10	NC

2.4.11.1 Signal Description – Serial Port 1/2 Connector (DUALCOM1)

Signal	Signal Description
TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone ringing signal.

2.4.12 CPU Connector (FAN_PWR1)



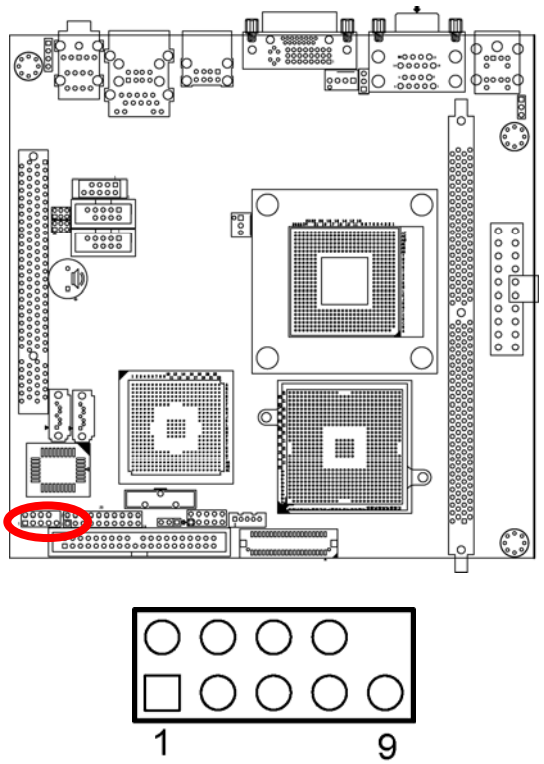


Signal	PIN
TAC	3
+12V	2
GND	1

2.4.12.1 Signal Description – CPU Fan Connector (FAN_PWR1)

Signal	Signal Description
TAC	Fan speed monitor

2.4.13 Front Panel Connector (F_PANEL1)

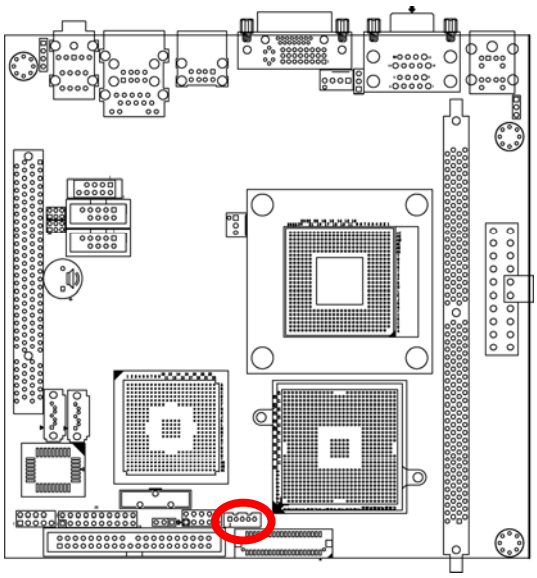


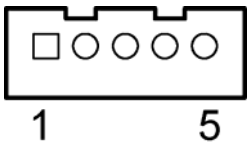
Signal	PIN	PIN	Signal
HDD_LED+	1	2	PWR_LED+
HDD_LED-	3	4	PWR_LED-
GND	5	6	PWR_BUT
RESET	7	8	GND
NC	9		

2.4.13.1 Signal Description – Front Panel Connecter (F_PANEL1)

PIN No.	Description
1, 3	HDD LED
2, 4	Power-On
5, 7	Reset SW
6, 8	Power SW

2.4.14 LCD Inverter Connector (JBKL1)





Signal	PIN
+12V	1
GND	2
ENBKL	3
VR	4
+5V	5

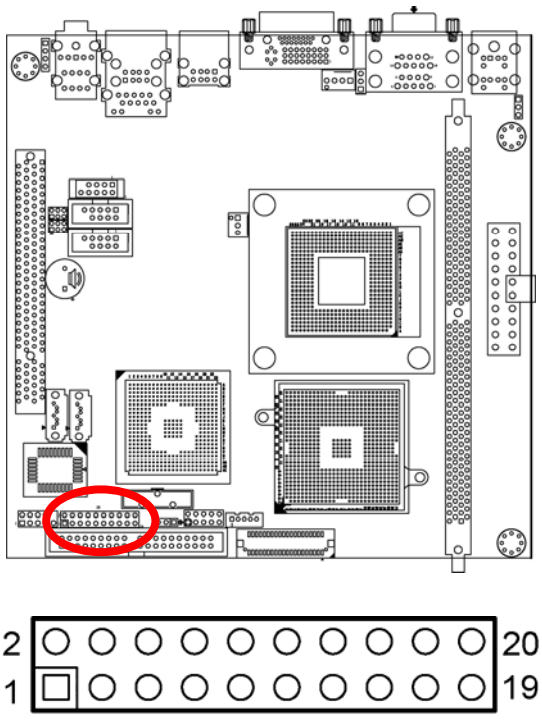
Note:

For inverters with adjustable Backlight function, it is possible to control the LCD brightness through the VR signal controlled by **JMISC**. Please see the **JMISC** section for detailed circuitry information.

2.4.14.1 Signal Description – LCD Inverter Connector (JBKL1)

Signal	Signal Description
VR	Vadj = 0.75V ~ 4.25V (Recommended: 4.7KΩ, >1/16W)
ENBKL	LCD backlight ON/OFF control signal

2.4.15 Digital Input / Output Connector (JDIO1)

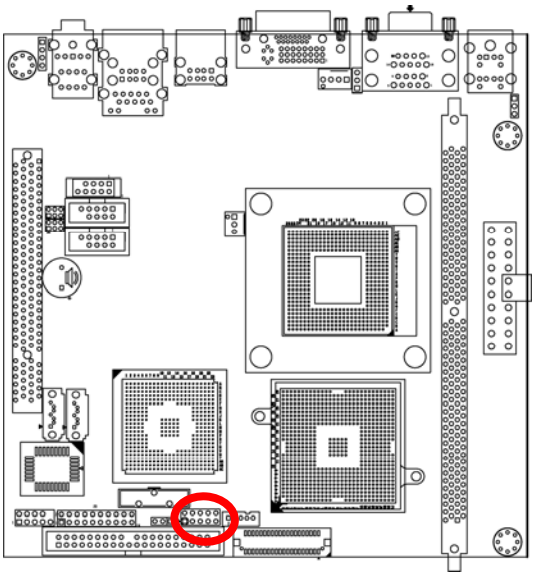


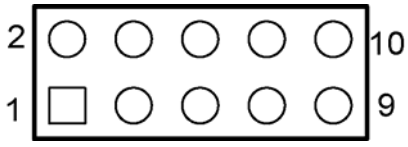
Signal	PIN	PIN	Signal
DIO0	1	2	DIO10
DIO1	3	4	DIO11
DIO2	5	6	DIO12
DIO3	7	8	DIO13
DIO4	9	10	DIO14
DIO5	11	12	DIO15
DIO6	13	14	DIO16
DIO7	15	16	DIO17
SMB_CLK_S	17	18	SMB_DATA_S
GND	19	20	+5V

2.4.15.1 Signal Description – Digital Input / Output Connector (JDIO1)

Signal	Signal Description
DI [0:17]	Digital Input/Output Data Bit 0 to Bit 17
SMB_CLK	Data input for I^2C input, 5V tolerant
SMB_DATA	Data input for I^2C serial input, 5V tolerant

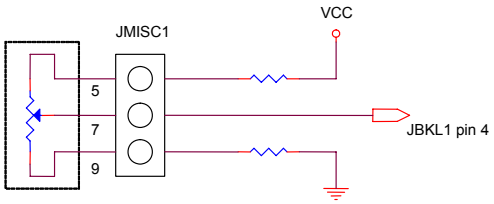
2.4.16 Miscellaneous Setting Connector (JMISC1)



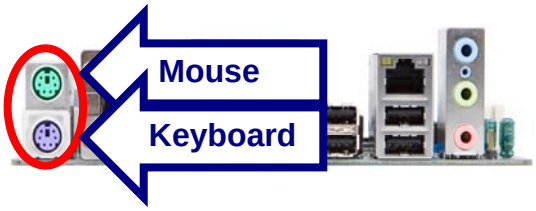


Signal	PIN	PIN	Signal
CASEOPEN#	1	2	VTIN3
GND	3	4	THRMDN
+5V	5	6	+5V
VR	7	8	#MASTER
GND	9	10	GND

2.4.16.1 Signal Description – Miscellaneous Setting Connecter (JMISC1)

PIN No.	Description
1, 3	Case open detection
5, 7, 9	LCD brightness setting  Variation Resistor (Recommended: 4.7KΩ, >1/16W)
2, 4	Thermal detection
6, 8, 10	CF Master/Slave setting 8-10 short (default: Master)

2.4.17 PS/2 Keyboard & Mouse Connector (KBMS1)

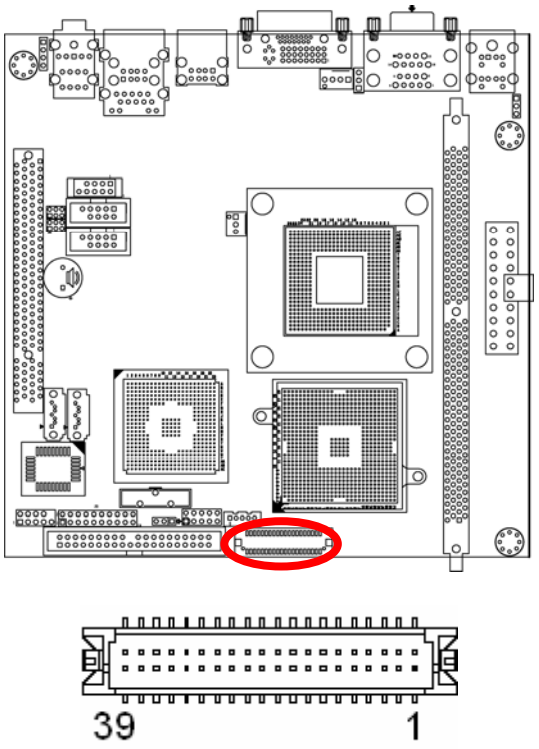


Port	Description
Mouse	PS/2 Mouse connector
Keyboard	PS/2 Keyboard connector

2.4.18 RJ-45 Ethernet / USB 0 & 1 Connectors (LANUSB34)

Port	Description
RJ-45	Allows connection to a Local Area Network (LAN) through a network hub.
USB 2.0	For connecting USB port 0, 1

2.4.19 LVDS Connector (LVDS1)

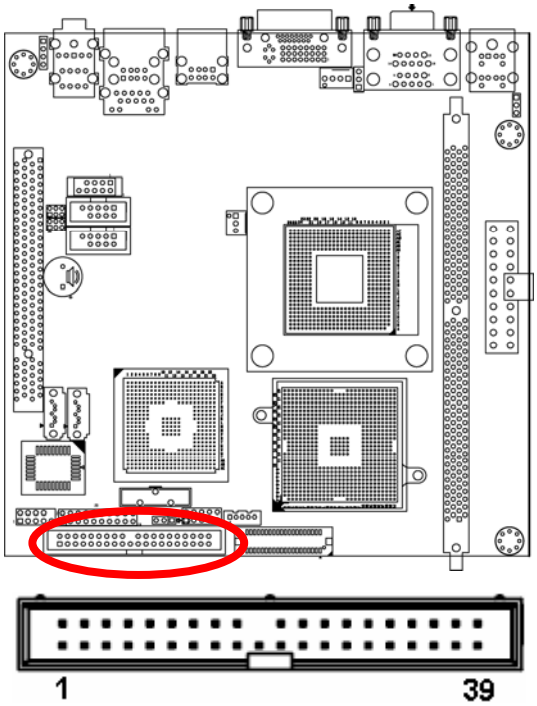


Signal	PIN	PIN	Signal
+5V	2	1	+3.3V
+5V	4	3	+3.3V
I^2C_DAT	6	5	I^2C_CLK
GND	8	7	GND
Txout0	10	9	Txout1
Txout0#	12	11	Txout1#
GND	14	13	GND
Txout2	16	15	Txout3
Txout2#	18	17	Txout3#
GND	20	19	GND
E_Txout0	22	21	E_Txout1
E_Txout0#	24	23	E_Txout1#
GND	26	25	GND
E_Txout2	28	27	E_Txout3
E_Txout2#	30	29	E_Txout3#
GND	32	31	GND
Txclk	34	33	E_Txclk
Txclk#	36	35	E_Txclk#
GND	38	37	GND
+12V	40	39	+12V

2.4.19.1 Signal Description – LVDS Connector (LVDS1)

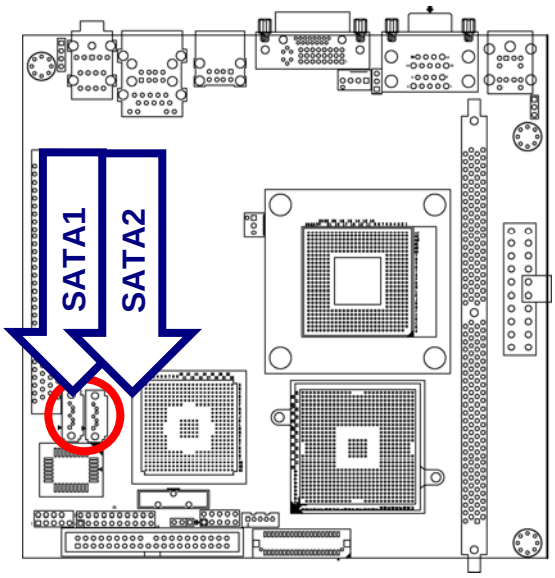
Signal	Signal Description
I^2C_DAT, I^2C_CLK	I^2C interface for panel parameter EEPROM. This EERPOM is mounted on the LVDS receiver. The data in the EEPROM allows the EXT module to automatically set the proper timing parameters for a specific LCD panel.

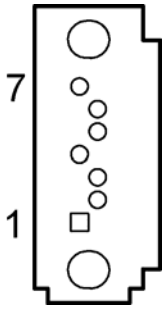
2.4.20 Primary IDE Connector (PRI_IDE1)



Signal	PIN	PIN	Signal
RESET#	1	2	GND
PDD7	3	4	PDD8
PDD6	5	6	PDD9
PDD5	7	8	PDD10
PDD4	9	10	PDD11
PDD3	11	12	PDD12
PDD2	13	14	PDD13
PDD1	15	16	PDD14
PDD0	17	18	PDD15
GND	19	20	NC
PDREQ	21	22	GND
PDIOW#	23	24	GND
PDIOR#	25	26	GND
PIORDY	27	28	GND
PDDACK#	29	30	GND
IRQ14	31	32	NC
PDA1	33	34	PATADET
PDA0	35	36	PDA2
PDCS1#	37	38	PDCS3#
IDEACTP#	39	40	GND

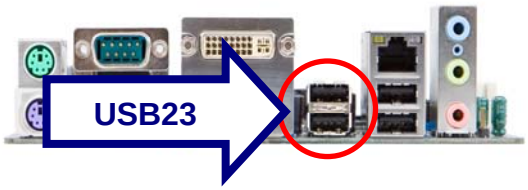
2.4.21 Serial ATA Connector (SATA1, SATA2)





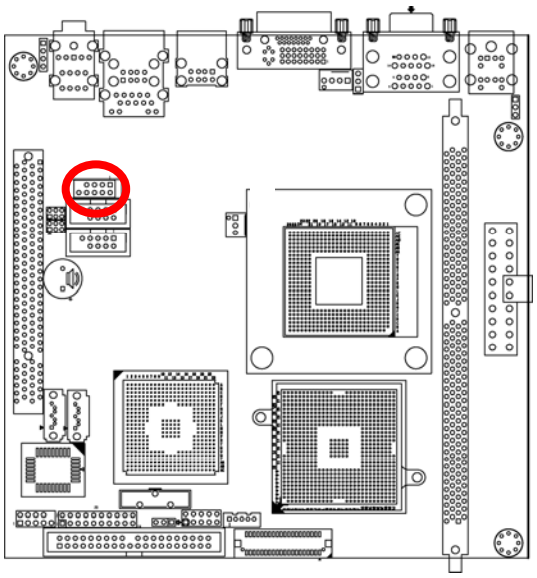
PIN	Signal
1	GND
2	SATA_TXP
3	SATA_TXN
4	GND
5	SATA_RXN
6	SATA_RXP
7	GND

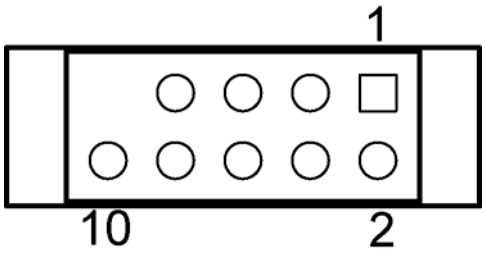
2.4.22 USB 2 & 3 Connectors (USB23)



Port	Description
USB 2.0	For connecting USB port 0, 1

2.4.23 USB Connector 4 & 5 (USB45)



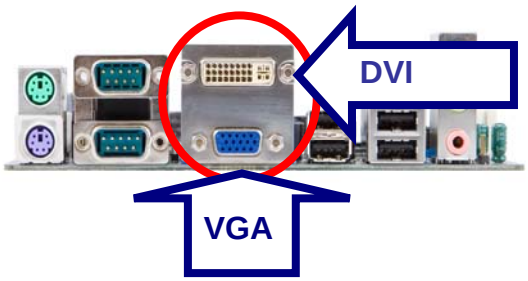


Signal	PIN	PIN	Signal
+5V	1	2	GND
D4-	3	4	GND
D4+	5	6	D5+
GND	7	8	D5-
		10	+5V

2.4.23.1 Signal Description – USB Connecter 4 & 5 (USB45)

Signal	Signal Description
D4+/D4-	Differential bi-directional data signal for USB channel 4. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
D5+/D5-	Differential bi-directional data signal for USB channel 5. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.

2.4.24 VGA Connector & DVI Connector (VGA_DVI-D1)



VGA

Signal	PIN			Signal
		6		GND
RED	1		11	NC
		7		GND
GREEN	2		12	DAT
		8		GND
BLUE	3		13	HSYNC
		9		VCC
NC	4		14	VSYNC
		10		GND
GND	5		15	DCK

DVI

PIN	Signal	PIN	Signal	PIN	Signal
1	D2-	16	HPDET	17	D0-
2	D2+	15	GND	18	D0+
3	GND	14	+5V	19	GND
4	D4-	13	D3+	20	D5-
5	D4+	12	D3-	21	D5+
6	DDCCLK	11	GND	22	GND
7	DDCDATA	10	D1+	23	Clock+
8	VSYNC	9	D1-	24	Clock-

C1	Red	C2	Green	C3	Blue	C4	VSYNC

2.4.24.1 Signal Description – VGA Connector (VGA_DVI-D1)

Signal	Signal Description
HSYNC	CRT horizontal synchronisation output.
VSYNC	CRT vertical synchronisation output.
DCK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red colour signal to the CRT. For 75 Ω cable impedance.
GREEN	Analog output carrying the green colour signal to the CRT. For 75 Ω cable impedance.
BLUE	Analog output carrying the blue colour signal to the CRT. For 75 Ω cable impedance.