

phyCORE-MPC5200B tiny

Hardware Manual

Edition September 2007

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Preface

This phyCORE-MPC5200B tiny Hardware Manual describes the board's design and functions. Precise specifications for the Freescale MPC5200B microcontroller series can be found in the enclosed MPC5200B microcontroller Data Sheet/User's Manual. If software is included please also refer to additional documentation for this software.

In this hardware manual and in the attached schematics, low active signals are denoted by a "/" in front of the signal name (i.e.: /RD). A "0" indicates a logic-zero or low-level signal, while a "1" represents a logic-one or high-level signal.

Declaration regarding Electro Magnetic Conformity of the PHYTEC phyCORE-MPC5200B tiny



PHYTEC Single Board Computers (henceforth products) are designed for installation in electrical appliances or as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

Note:

PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians and engineers) handle and/or operate these products. Moreover, PHYTEC products should not be operated without protection circuitry if connections to the product's pin header rows are longer than 3 m.

PHYTEC products fulfill the norms of the European Union's Directive for Electro Magnetic Conformity only in accordance to the descriptions and rules of usage indicated in this hardware manual (particularly in respect to the pin header rows or connectors, power connector and serial interface to a host-PC).

Implementation of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electro Magnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

The phyCORE-MPC5200B tiny is one of a series of PHYTEC Single Board Computers that can be populated with different controllers and, hence, offers various functions and configurations. PHYTEC supports common 8-, 16- and numerous 32-bit controllers on two types of Single Boards Computers:

- (1) as the basis for Rapid Development Kits which serve as a reference and evaluation platform
- (2) as insert-ready, fully functional phyCORE OEM modules, which can be embedded directly into the user's target design.

PHYTEC's microcontroller modules allow engineers to shorten development horizons, reduce design costs and speed project concepts from design to market.

1 Introduction

The phyCORE-MPC5200B tiny belongs to PHYTEC's phyCORE Single Board Computer module family. The phyCORE SBCs represent the continuous development of PHYTEC Single Board Computer technology. Like its mini-, micro- and nanoMODUL predecessors, the phyCORE boards integrate all core elements of a microcontroller system on a sub-miniature board and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

As independent research indicates that approximately 70 % of all EMI (Electro Magnetic Interference) problems stem from insufficient supply voltage grounding of electronic components in high frequency environments the phyCORE board design features an increased pin package. The increased pin package allows dedication of approximately 20 % of all pin header connectors on the phyCORE boards to Ground. This improves EMI and EMC characteristics and makes it easier to design complex applications meeting EMI and EMC guidelines using phyCORE boards even in high noise environments.

phyCORE boards achieve their small size through modern SMD technology and multi-layer design. In accordance with the complexity of the module, 0402-packaged SMD and laser-drilled Microvias components are used on the boards, providing phyCORE users with access to this cutting edge miniaturization technology for integration into their own design.

The phyCORE-MPC5200B tiny is a subminiature (53 x 57 mm) insert-ready Single Board Computer populated with Freescale's PowerPC MPC5200B microcontroller. Its universal design enables its insertion in a wide range of embedded applications. All controller signals and ports extend from the controller to high-density (0.635 mm) Molex pin header connectors aligning two sides of the board, allowing it to be plugged like a "big chip" into a target application.

Precise specifications for the controller populating the board can be found in the applicable controller User's Manual or Data Sheet. The descriptions in this manual are based on the MPC5200B controller. No description of compatible microcontroller derivative functions is included, as such functions are not relevant for the basic functioning of the phyCORE-MPC5200B tiny.

The phyCORE-MPC5200B tiny offers the following features:

- Single Board Computer in subminiature form factor (53 x 57 mm) according to phyCORE specifications
- all applicable controller and other logic signals extend to two high-density 100-pin Molex connectors
- processor: Freescale embedded PowerPC MPC5200B
- single 3.3 V (max. 1.2 A) supply voltage

Internal Features of the MPC5200B:

- e300 core
 - 760 MIPS at 400 MHz (-40 to +85 °C)
 - 16 k instruction cache, 16 k data cache
 - Double precision FPU
 - Instruction and data MMU
- SDRAM / DDR SDRAM memory Interface
 - up to 132 MHz operation
 - SDRAM and DDR SDRAM support
 - 256 MByte addressing range per CS, two CS available
- Flexible multi-function external bus interface
- Peripheral component interconnect (PCI) controller
- ATA controller
- BestComm DMA subsystem
- 6 programmable serial controllers (PSC), configurable for the following functions:

- Fast Ethernet controller (FEC)
 - Supports 100Mbps IEEE 802.3 MII, 10 Mbps IEEE 802.3 MII
- Universal serial bus controller (USB)
 - USB revision 1.1 host
- Two inter-integrated circuit interfaces (I²C)
- Serial peripheral interface (SPI)
- Dual CAN 2.0 A/B controller (MSCAN)
- J1850 byte data link controller (BDLC)
- Test/debug features
- JTAG (IEEE 1149.1 test access port)
- Common on-chip processor (COP) debug port

Memory Configuration¹:

- DDR SDRAM: 64 MByte to 128 MByte
- Flash: 16 MByte to 32 MByte Intel Strata Flash memory, 16-bit memory width, only asynchronous devices are supported
- I²C memory: 4 kByte EEPROM

Other Board-Level Features:

- Two UART ports, RS-232 interfaces (RxD/TxD)
- One 10/100Mbit Ethernet port via optional Micrel PHY
- I²C Real-Time Clock with calendar and alarm function
- Optional industrial temperature range (-40...+85°C)

¹: Please contact PHYTEC for more information about additional module configurations.

1.1 Block Diagram

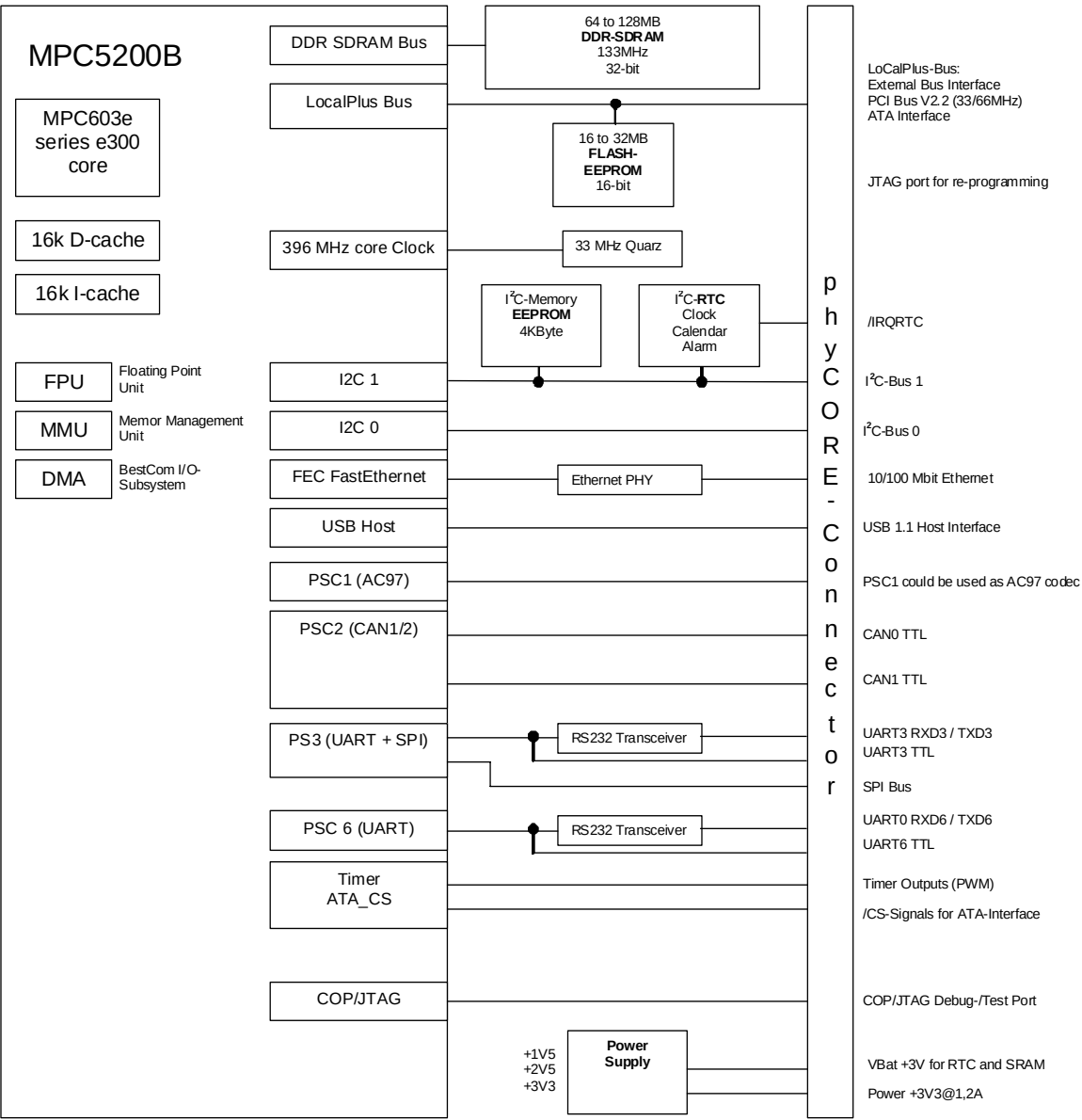


Figure 1: Block Diagram phyCORE-MPC5200B tiny

1.2 View of the phyCORE-MPC5200B tiny

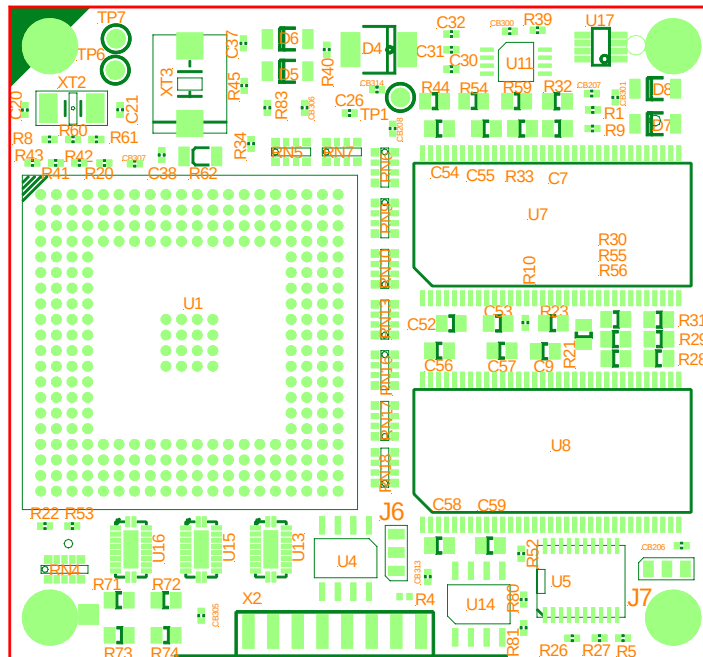


Figure 2: Top-View of the phyCORE-MPC5200B tiny PCB Rev. 1245.2

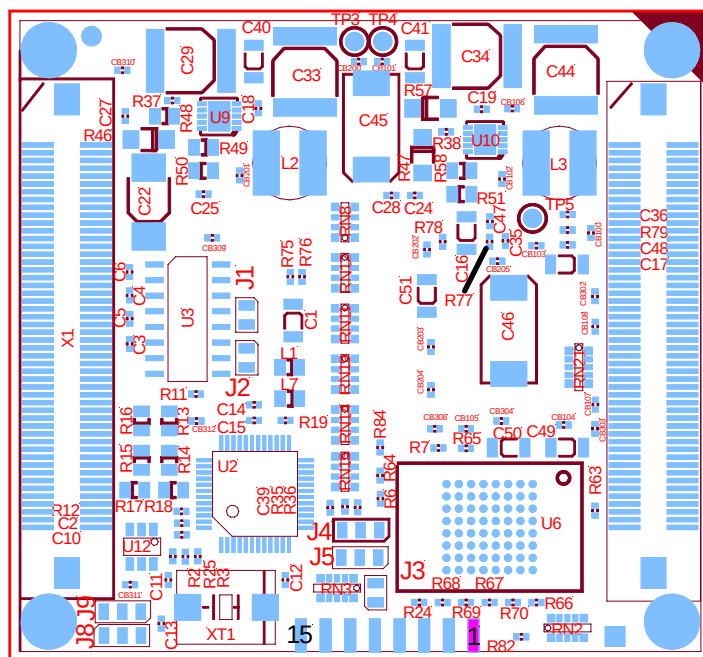


Figure 3: Bottom-View of the phyCORE-MPC5200B tiny PCB Rev. 1245.2

1.3 Minimum Requirements to Operate the phyCORE-MPC5200B tiny

Basic operation of the phyCORE-MPC5200B tiny only requires supply of a +3V3 input voltage and the corresponding GND connection.

These supply pins are located at the phyCORE-connector X1:

+3V3	X1	1C, 2C, 4C, 5C, 1D, 2D
GND	X1	3C, 3D, 7C, 9D, 12C, 14D

Caution:

We recommend connecting all available +3V3 input pins to the power supply system on a custom carrier board housing the phyCORE-MPC5200B tiny and at least the matching number of GND pins neighboring the +3 V3 pins.

In addition, proper implementation of the phyCORE module into a target application also requires connecting all GND pins neighboring signals that are being used in the application circuitry.

Please refer to section 4 for more information.

2 Pin Description

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller manuals/data sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

Many of the phyCORE-MPC5200B tiny pins offer alternative functions. These alternative functions must be activated by configuring the applicable controller registers prior to their use. Certain controller functions are pre-configured based on the module's design and are shown in *Table 1*. Signals that are routed directly from the CPU to the Molex connectors can be configured to any available alternative function desired by the user. In contrast, signals that are used on the phyCORE-MPC5200 tiny as listed in *Table 1* can only be used if a special module configuration was purchased (e.g. SBC version without on-board RS-232 transceivers. Please contact PHYTEC for more details.

Note:

The following sections of this manual assume use of the port pins according to configuration listed in *Table 1*.

CPU Port	Function	Port_conf Register Bits	Used on phyCORE SBC
PSC1	AC97_1	01x [29:31]	No
PSC2	CAN 1/2	001 [25:27]	No
PSC3	UART3/SPI	1100 [20:23]	Yes
USB	USB	01 [18:19]	No
Ethernet	Ethernet w/ MD	0101 [12:15]	Yes
Timer	ATA_CS	00_11 [2:3_6:7]	No
I2C	I2C1 / I2C2	default	Yes (I2C1 available)
PSC6	UART6	101 [9:11]	Yes

Table 1: Default Port Configuration

As *Figure 4* indicates, all controller signals extend to surface mount technology (SMT) connectors (0.635 mm) lining two sides of the module (referred to as phyCORE-connector; *refer to section 2*). This allows the phyCORE-MPC5200B tiny to be plugged into any target application like a "big chip".

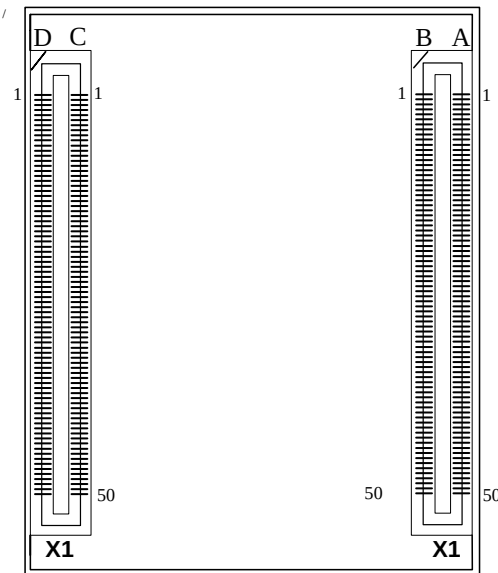


Figure 4: Pinout of the phyCORE-MPC5200B tiny (Bottom View)

Table 2 provides an overview of the pinout of the phyCORE-connector.

Please refer to the Freescale MPC5200B User Manual/Data Sheet for details on the functions and features of controller signals and port pins.

Pin Number	Signal	I/O	Comments
Pin Row X1A			
1A	NC	-	Not connected
2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A	GND	-	Ground 0 V
3A	/IRQ3	I	Interrupt input 3 of the processor.
4A	/IRQ0	I	Interrupt input 0 of the processor.
5A 6A 8A 29A 30A 31A	/LP_CS1 /LP_ALE /LP_RD#WR /LP_Ts /LP_Cs4 /LP_Cs6	O O O O O O	LocalPlus Bus control signals Chip Select 1 Address Latch Enable Read, not Write Transfer Start Chip Select 4 Chip Select 6 (PSC3 is UART3)
9A 10A 11A 13A 14A 15A 16A 18A 19A 20A 21A 23A 24A 25A 26A 28A	EXT_AD1 EXT_AD2 EXT_AD4 EXT_AD7 EXT_AD9 EXT_AD10 EXT_AD12 EXT_AD15 EXT_AD17 EXT_AD18 EXT_AD20 EXT_AD23 EXT_AD25 EXT_AD26 EXT_AD28 EXT_AD31	I/O	LocalPlus Address/Data Signals
33A	ETH_TXD3	O	Already used by the MII interface between CPU and Ethernet PHY. Could be used as J1850_TX signal, if the PHY is not populated or in "isolation mode". The pin state is latched by the CPU after reset and used as "byte lane swap" configuration. Refer to section 5, "System Start-Up Configuration". There is a 10kOhm pull-down resistor on this signal..
34A 35A 36A 38A 39A	ATA_CS_0 ATA_CS_1 ATA_IOCHRDY /ATA_IOR ATA_INTRQ	O O O O I	ATA Interface Signals Timer Port configured as ATA_CS (Timer0) Timer Port configured as ATA_CS (Timer1) ATA negated to extend transfer ATA read ATA interrupt request

Pin Number	Signal	I/O	Comments
			<i>Dedicated PCI Signals</i>
40A	/PCI_RESET	O	Reset output (open drain)
41A	/PCI_GNT	O	Bus grant
43A	/PCI_CBE_3	O	Command byte enable 3
44A	/PCI_CBE_2	O	Command byte enable 2
45A	/PCI_IRDY	O	Initiator (HOST) ready
46A	/PCI_DEVSEL	O	Device select
48A	/PCI_PERR	O	Parity error
49A	/PCI_SERR	O	System Error (open drain)
50A	/PCI_CBE_1	O	Command byte enable 1

Pin Number	Signal	I/O	Comments
Pin Row X1B			
1B	RTC_CLKOUT	O	Clock output of the I ² C RTC U5
2B	/IRQ1	I	Interrupt input 1 of the processor
3B	/IRQ2	I	Interrupt input 2 of the processor
4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 41B, 44B, 49B	GND		Ground 0 V
5B 6B 7B 28B 30B 31B	/LP_CS2 /LP_CS3 /LP_Oe LP_Ack /LP_CS5 /LP_CS7	O O O O O	LocalPlus Bus Signals Chip Select 2 Chip Select 3 Output Enable Acknowledge Chip Select 5 Chip Select 7 (PSC3 is UART3)
8B 10B 11B 12B 13B 15B 16B 17B 18B 20B 21B 22B 23B 25B 26B 27B	EXT_AD0 EXT_AD3 EXT_AD5 EXT_AD6 EXT_AD8 EXT_AD11 EXT_AD13 EXT_AD14 EXT_AD16 EXT_AD19 EXT_AD21 EXT_AD22 EXT_AD24 EXT_AD27 EXT_AD29 EXT_AD30	I/O	LocalPlus Address/Data Signals
32B	Test_Sel_1	I/O	Input in CPU production test. Can be configured as LocalPlus-Bus TSIZ bit <i>Refer to section 7.3.2.1.1 in the MPC5200 controller User's Manual.</i>
33B	ETH_RXD1	I	Already used by the MII interface between CPU and Ethernet PHY. Can be used as J1850_RX signal, if the PHY is not populated or in "isolation mode".
35B 36B 37B 38B	ATA_DRQ /ATA_IOW ATA_Isolation /ATA_DACK	I O O O	ATA Interface Signals ATA DMA request ATA write ATA write enable for PCI bus sharing ATA DMA acknowledge

Pin Number	Signal	I/O	Comments
			<i>Dedicated PCI Signals</i>
40B	PCI_CLOCK	O	PCI and external peripheral clock
42B	/PCI_REQ	O	PCI bus request
43B	PCI_IDSEL	O	Initial device select
45B	/PCI_FRAME	O	Frame start
46B	/PCI_TRDY	I	Target ready
47B	/PCI_STOP	O	Transition stop
48B	PCI_PAR	O	Bus parity
50B	/PCI_CBE_0	O	Command byte enable 0

Pin Number	Signal	I/O	Comments
Pin Row X1C			
1C, 2C, 4C, 5C	+3V3	I	Supply voltage +3.3 VDC
3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C	GND	-	Ground 0 V
6C	VBAT	I	Connection for external battery (+) 2.4 - 3.3 V to supply (backup) the RTC U5
8C	ETH_TXD1	O	Already used by the MII-Interface between CPU and Ethernet PHY. The pin state is latched by the CPU after reset and used as "boot high" configuration. Refer to section 5 "System Start-Up Configuration". A 10kOhm pull-up resistor is connected to this signal.
9C	GPIO_WKUP_6	I/O	Dedicated GPIO with wakeup capability Note: This is a 2.5V based GPIO!!!
10C	/SRESET	I/O	External SRESET is an open drain signal which is connected to a 10 kOhm pull-up resistor on the module. Assertion of SRESET causes assertion of the internal soft reset. Internal soft reset is actually an interrupt that takes the same exception vector as HRESET. In particular, this means that SRESET cannot abort a hung XLB operation, and no device should use SRESET in a way that interferes with any bus operation in progress. SRESET can also be asserted by internal sources. When SRESET is asserted internally, external SRESET is also asserted.
11C	/HRESET	I/O	HRESET is a bi-directional signal with a Schmitt-trigger input and an open drain output. The HRESET signal is connected a 10 kOhm pull-up resistor on the module. Assertion of external HRESET causes external HRESET and SRESET as well as internal hard and soft resets to be asserted for at least 4096 reference clock cycles. During PORRESET or HRESET the reset configuration word is sampled to establish the initial state of various vital internal MPC5200B functions. The reset configuration word is latched internally when PORRESET or HRESET is released.
13C 14C 15C 16C	AC97_1_RES AC97_1_SYNC AC97_1_BITCLK AC97_1_SDATA_IN	O O I I	AC97 Codec Signals (PSC1) Reset signal to the external AC97 device Frame sync, or start-of-frame (SOF) Driven by the external serial bit-clock Receiver serial data input
18C	CAN2_TX	O	CAN transmit output of the second CAN interface (PSC2)
19C	UART6_RXD_TTL	I	PSC6 receive data signal
20C	UART6_TXD_TTL	O	PSC6 transmit data signal

Pin Number	Signal	I/O	Comments
21C	RXD6_232	I	RxD input on the RS-232 transceiver for the MPC UART (PSC6)
23C	TXD6_232	O	TxD output on the RS-232 transceiver for the MPC UART (PSC6)
24C	/UART6_RTS_TTL	I	PSC6 request to send signal
25C	/UART6_CTS_TTL	O	PSC6 clear to send signal
26C 28C	I2C2_CLK I2C2_IO	I/O I/O	Second I²C Interface Clock (SCL) Data (SDA)
29C 30C	Timer4 Timer5	I/O I/O	Timer 4 signal of the MPC5200B Timer 5 signal of the MPC5200B
31C	I2C1_CLK	I/O	Clock for first I2C-Interface (SCL)
33C 34C 35C 36C 38C 41C	ETH_LINK ETH_SPEED ETH_RX- ETH_TX- /ETH_PD ET_NWAYEN	O O I O I O	10/100MBit TP Ethernet Interface (if on-board PHY is not populated, pins are NC) Link/Activity LED (L=link; toggle=act) Speed LED (H=10 Mbit/s, L=100 Mbit/s) Differential receive input Differential transmit output Power down Collision LED (H = no collision)
39C 40C	/COP_TRST CK_STOP	I O	JTAG Interface JTAG reset input. Via logic OR connected to /PORRESET resulting in /CPU_TRST signal. Scan enable, clock stop
43C	PSC2_4	I/O	Freely available GPIO with wakeup function
44C	Timer6	I/O	Timer 6 signal of the MPC5200B
45C 46C 48C 49C 50C	USB1_OVRCRNT USB1_SUSPEND USB1_RXN USB1_TXN /USB1_OE	I O I O O	USB1 (Host) Over current Suspend Receive negative Transmit negative Output enable

Pin Number	Signal	I/O	Comments
Pin Row X1D			
1D, 2D	+3V3	I	Supply voltage +3.3 VDC
3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D	GND	-	Ground 0 V
4D, 5D	NC	-	Not connected
6D	VCC_SRAM	O	VCC_SRAM supply voltage is generated by VBAT or +3V3 using a battery backup circuit (MAX6364). VCC_SRAM serves as supply voltage for the Real-Time Clock.
7D	RESOUT	O	Reset output of the voltage supervisor circuit
8D	/PHYReset	I	A low on this pin forces only the PHY into reset state
10D	/RESIN	I	Reset input signal of the MPC5200B tiny. It could be asserted via connection to a reset push button. Signal connected to +3V3 via 10 kOhm pull-up resistor.
11D	GPIO_WKUP_7	I/O	Dedicated GPIO with wakeup capability
12D	Timer2	I/O	Timer 2 signal of the MPC5200
13D	Timer3	I/O	Timer 3 signal of the MPC5200
15D	AC97_SDATA_OUT	O	AC97 codec signal (PSC1) Receiver serial data output
16D	UART3_RXD_TTL	I	PSC3 receive data signal
17D	UART3_TXD_TTL	O	PSC3 transmit data signal
18D	CAN2_RX	I	CAN receive of the second CAN interface (PSC2)
20D	CAN1_RX	I	CAN receive of the first CAN interface (PSC2)
21D	CAN1_TX	O	CAN transmit of the first CAN interface (PSC2)
22D	RXD3-232	I	RxD input on the RS-232 transceiver for UART3 (PSC3).
23D	TXD3-232	O	TxD output on the RS-232 transceiver for UART3 (PSC3).
25D	/UART3_RTS_TTL	I	PSC3 request to send signal
26D	/UART3_CTS_TTL	O	PSC3 clear to send signal
27D 28D 30D 31D	SPI_MOSI SPI_MISO SPI_CLK SPI_SS	I/O I/O I/O O	SPI Interface (PSC3) SPI master out slave in SPI master in slave out SPI clock SPI slave select
32D	I2C1_IO	I/O	Data line of first I2C interface (SDA)
33D	/IRQ_RTC	O	Interrupt from the on-board RTC U5. Interrupt can be programmed to occur to a specific time or date.

35D 36D 37D	ETH_RX+ ETH_TX+ /ETH_INT	I O O	10/100MBit TP Ethernet Interface (if on-board PHY is not populated, pins are NC0) Differential receive input Differential transmit output MII interface interrupt
38D 40D 41D 42D	CPU_TCK CPU_TDI CPU_TDO CPU_TMS	I I O I	MPC5200B JTAG interface Clock Data in Data out Mode select
43D	Timer7	I/O	Timer 7 signal of the MPC5200B
45D 46D 47D 48D 50D	USB1_PORTPWR USB1_SPEED USB1_RXD USB1_RXP USB1_TXP	O O I I O	USB1 (host) Enable/disable port power Speed select Receive data Receive positive Transmit positive

Table 2: Pinout of the phyCORE-Connector X1

3 Jumpers

For configuration purposes, the phyCORE-MPC5200B tiny has 10 solder jumpers, some of which have been installed prior to delivery. *Figure 5* illustrates the numbering of the jumper pads, while *Figure 6* indicates the location of the jumpers on the board.

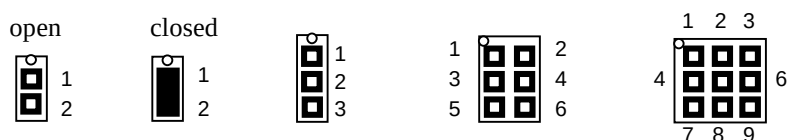


Figure 5: Numbering of the Jumper Pads

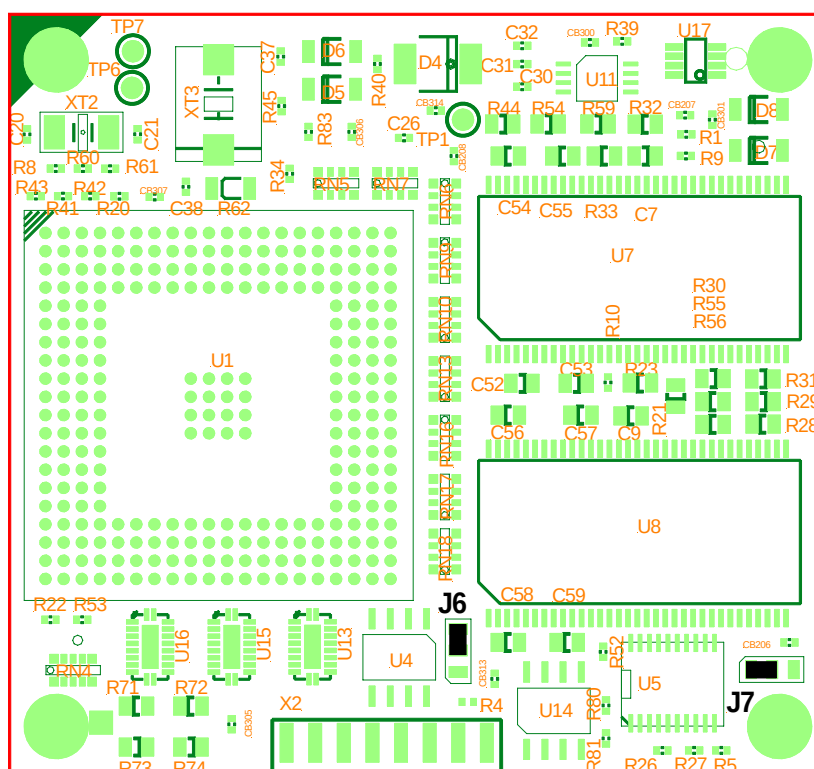


Figure 6: Location of the Jumpers (Controller Side)
(phyCORE-MPC5200B tiny Standard Version)

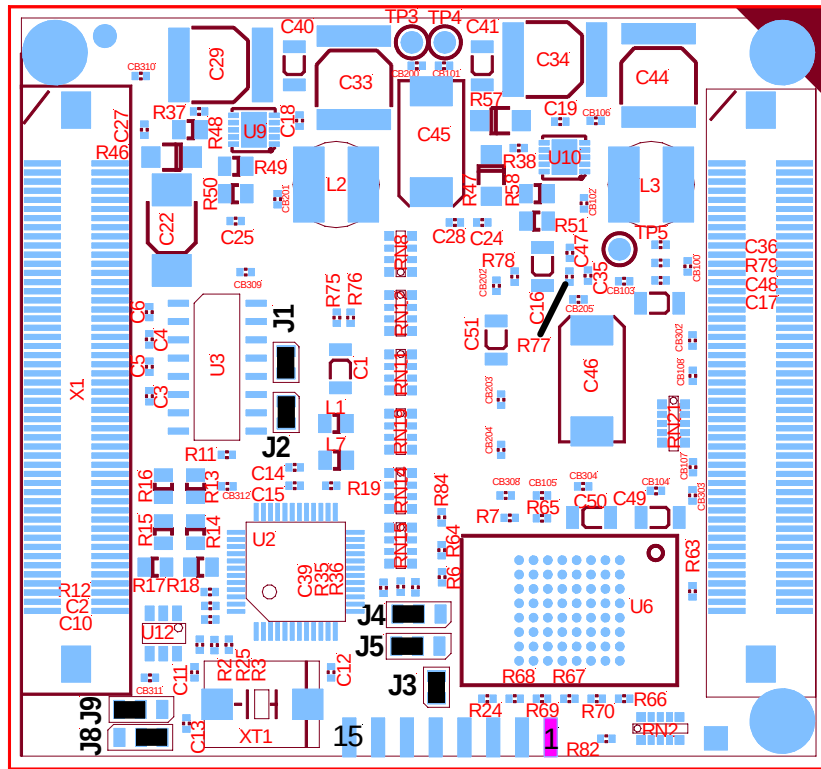


Figure 7 Location of the Jumpers (Bottom Side)
(phyCORE-MPC5200B tiny Standard Version)

The jumpers (J = solder jumper) have the following functions:

Jumper	Default	Comment
J1, J2		J1 and J2 disconnect the receive lines (UART3_RXD_TTL and UART6_RXD_TTL) of the MPC5200B PSC3 and PSC6 from the RS-232 transceiver at U3. This makes the controller's TTL signals available at pins X1D16 (UART3_RXD_TTL) and X1C19 (UART6_RXD_TTL). This is useful, for instance, for optical isolation of the RS-232 interface.
open		The UART receive signals UART3_RXD_TTL and UART6_RXD_TTL are disconnected from the RS-232 transceiver.
closed	X	The UART receive signals UART3_RXD_TTL and UART6_RXD_TTL are connected to the on-board RS-232 transceiver.
Package Type		0R in SMD 0805
J3		J3 connects pin 7 of the serial memory at U4 to 3V3. On many memory devices pin 7 enables the activation of a write protect function. It is not guaranteed that the standard serial memory populating the phyCORE-MPC5200B tiny will have this write protection function. <i>Please refer to the corresponding memory data sheet for more detailed information.</i>
open	X	
closed		
Package Type		0R in SMD 0805
J4, J5, J6		J4, J5 and J6 define the slave addresses (A0, A1 and A2) of the serial memory U4 on the I ² C bus. In the high-nibble of the address, I ² C memory devices have the slave ID 0xA. The low-nibble consists of A2, A1, A0, and the R/W bit. It must be noted that the RTC at U5 is also connected to the I ² C bus. The RTC has the address 0xA2/0xA3 which cannot be changed.
2+3, 2+3,2+3	X	A2= 0, A1= 1, A0= 0 (0xA4 / 0xA5) I ² C slave address 0xA0 for write operations and 0xA1 for read access.
Package Type		0R in SMD 0805

Jumper	Default	Comment		
J7	X	Enables or disables the clock output of the I ² C RTC U5 RTC clockout is connected to X1B1.		
1 + 2		RTC clockout disabled		
2 + 3		RTC clockout enabled		
Package Type		0R in SMD 0805		
J12 J13	X	Pll_cfg3 = 1	These jumpers define the core PLL configuration. <i>Refer to the "MPC5200B controller User's Guide"</i> . The default configuration 0x08 defines a bus-to-core clock ratio of 1:3.	
		Pll_cfg2 = 1		
1 + 2		Logic 1		
2 + 3		Logic 0		
Package Type	10 kOhm resistor in SMD 0805			
J8, J9	-	These jumpers are reserved for factory settings!		
		Do not change these jumper settings!		

Table 3: Jumper Settings

4 Power Requirements

The phyCORE-MPC5200B tiny must be supplied with one supply voltage only:

Supply voltage: +3.3 V $\pm 10\%$ with 1.2 A load

Caution:

Connect all +3V3 input pins to your power supply and at least the matching number of GND pins neighboring the +3V3 pins.

As a general design rule we recommend connecting all GND pins neighboring signals which are being used in the application circuitry

Optional Supply Input VBAT

VBAT is the input pin that supplies the Real-Time Clock (U5). The MAX6364 battery supervisor IC (U12) senses the 3.3 V main supply and VBAT and switches to the voltage with the higher level. VBAT should be supplied from a 3 V source (i.e. lithium battery).

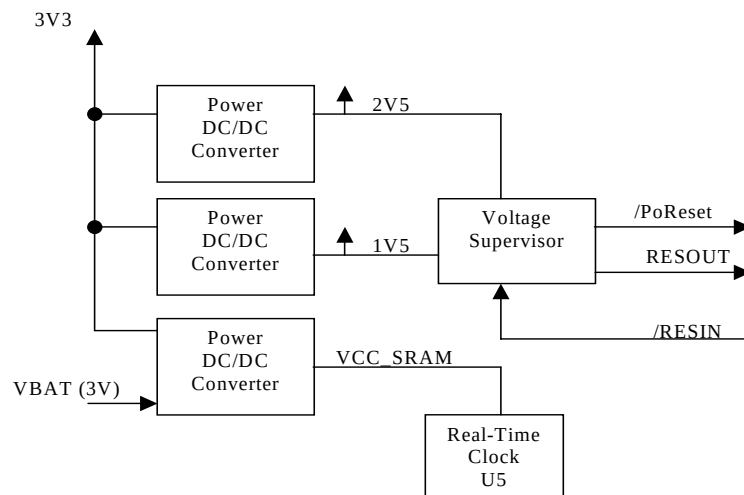


Figure 8: Power Supply Diagram

Internally generated voltages: 1V5, 2V5

- 3 V3 PowerPC I/O, Flash memory
- 2 V5 DDR SDRAM and Ethernet PHY
- 1 V5 PowerPC Core

4.1 Voltage Supervision and Reset

The input voltage 3V3 as well as the on-board generated operation voltages 2V5 and 1V5 are monitored by a voltage supervisor device at U11. This circuitry is responsible for generation of the system reset signal /PoReset. The voltage supervisor IC initiates a reset cycle if any operating voltage drops below its minimum threshold value. After all voltages reach their required value, the supervisor chip adds an additional 200 ms delay until the /PoReset line will be inactive (high). /PoReset connects to the processor reset input.

/PoReset is combined via the diodes D5 and D6 with /COP_TRST to a logic OR with /CPU_TSRT (JTAG controller reset) as output. This logic connection is used to ensure a proper reset of the CPU internal debug interface by /PoReset or by the COP signal /COP_TRST.

The voltage supervisor's master reset input /RESIN can be connected to an external signal or switch to release a asynchronous reset manually.

5 System Start-Up Configuration

During the reset cycle the MPC5200B processor reads the state of selected controller signals to determine the basic system configuration. The configuration circuitry (pull-up or pull-down resistors) is located on the phyCORE module.

The system start-up configuration includes:

- Clock configuration
- Basic LocalPlus characteristic for boot memory configuration

Note:

Since most of these signal lines are routed to the phyCORE connector care must be taken not to overwrite the startup configuration accidentally when connecting these signals to external devices.

-

The following default configuration is read by the processor with the rising edge of the reset line /PoReset. The logic level of the signals written in *italic style* could be configured via solder jumpers on-board (refer to section 3)

Signal Name	Register Bit	Logic Level	Description
/LP_Ale LP_RD/WR /ATA_low /ATA_lor /ATA_Dack	PPC_pll_cfg [0..4]	0 1 0 0 0	Bus clock ratio XLB: core clock = 1:3 132 MHz * 3 = 396 MHz
/LP_Ts	xl原因clk_sel	0	Bit=0: XLB_CLK = fsystem / 4 Bit=1: XLB_CLK = fsystem / 8
USB1_TXN	sys_pll_cfg0	0	Bit =0: fsystem = 16x SYS_XTAL_IN Bit =1: fsystem = 12x SYS_XTAL_IN
USB1_TXP	sys_pll_cfg1	0	Bit=0: fvcosys = fsystem Bit=1: fvcosys = 2 x fsystem
ETH_TXEN	boot_rom_mg	0	Bit=0: No boot in most graphics mode 1 Bit=1: Boot in most graphics mode
ETH_TXD1	ppc_msrip	1	Bit=0: 0000_0100 (hex) boot address Bit=1: FFF0_0100 (hex) boot address
ETH_TXD2	boot_rom_wait	1	Bit=0: 4 PCI bus clocks of wait state Bit=1: 48 PCI bus clocks of wait state
ETH_TXD3	boot_rom_swap	0	Bit=0: no byte lane swap, same endian ROM image Bit=1: byte lane swap, different endian ROM image
ETH_TXERR	boot_rom_size	0	Boot ROM address is max 25 significant bits during address tenure. Bit=0: 16-bit ROM data bus Bit=1: 32-bit ROM data bus
ETH_MDC	boot_rom_type	1	Bit=0: non-muxed boot ROM bus, single tenure transfer. 1 Bit=1: muxed boot ROM bus, with address and data tenures, ALE and TS active. 1
ETH_TXD0	large_flash_sel	0	Bit=0: No boot in large Flash mode 1 Bit=1: Boot in large Flash mode 1,3,4

Table 4: System Start-Up Configuration

6 System Memory

The system memory consist of Flash memory, DDR SDRAM (Double Data Rate Synchronous Dynamic Random Access Memory) and a small non-volatile memory device:

- 16 MByte Intel Strata Flash memory (1x 16-bit, multiplexed mode)
- 64 MByte DDR SDRAM (2x 16-bit)
- 4 kByte serial memory (EEPROM)

The Flash memory is connected to the PowerPC LocalPlus bus and is controlled by /CS0. This Chip-Select signal is used for boot operation.

The DDR SDRAM is connected to the special SDRAM interface of the MPC5200B processor and operates at the maximum frequency (132 MHz).

Communication to the small non-volatile memory device (EPROM) is established over the processor's I²C bus. This memory device holds the boot loader (U-Boot) environment variables in its first two kilobytes and can be used for parameter storage.

6.1 Flash Memory

Use of Flash as non-volatile memory on the phyCORE-MPC5200B tiny provides an easily reprogrammable means of code storage.

- 16 up to 32 MByte Intel Strata Flash memory
- 16-bit bus width
- Only asynchronous operation is possible

The Flash memory bank supports the following Intel memory devices:

Type	Size	Manufacturer	Device Code	Manufacturer Code
Asynchronous Devices				
28F128J3D	16 MByte	Intel	0x0018	0x0089
28F128P33-T	16 MByte	Intel	0x881E	0x0089
28F128P33-B	16 MByte	Intel	0x8821	0x0089
28F256P33-T	32 MByte	Intel	0x891F	0x0089
28F256P33-B	32 MByte	Intel	0x8922	0x0089

Table 5: Choice of Flash Memory Devices and Manufacturers¹

The organization of the Flash memory bank is 16-bit. The Flash memory bank is controlled by the processor Chip Select signal /CS0. This Chip Select signal is the dedicated control signal for boot purposes.

The MPC5200B's LocalPlus bus can be configured for many different bus modes. For /CS0 the 25-bit address / 16-bit data multiplexed mode was chosen because it offers the largest address space without interfering the ATA or PCI bus. With 25 address lines a total of 32 MByte of data/code can be addressed. It is possible to use different bus modes on other available Chip Select signals.

The Flash memory bank 0 starts at address 0x0000_0100 or 0xFFFF_0100 depending on the startup configuration and relative to the base address of the processor's Chip Select signal /CS0.

¹: Flash types in the shaded lines are the preferred parts for the phyCORE-MPC5200B tiny.

The access speed depends on the equipped memory device. The LocalPlus Bus clock cycle is determined by the PCI clock which is configured by the PCI clock divider. A typical configuration selects 33 MHz. The resulting basic cycle time is 30.30 ns.

The MPC5200B processor multiplexed read or write is divided into a address tenure and a data tenure. Because the Chip Select signal is generated with the start of the data tenure only this period is of interest for access time calculation.

The equation for access time calculation is: $(2+WS) * t_{PCICK} - 8.5 \text{ ns}$

To support all memory speed grades up to 85 ns at least 2 wait states must be added for /CS0.

- 2 wait state and 1 dead cycle for /CS0
(supports 33 MHz PCI clock)
- 5 wait states and 2 dead cycles for /CS0
(supports 66 MHz PCI clock)

No additional voltages are needed for in-system programming. As of the printing of this manual, Flash devices generally guarantee at least 100,000 erase/programming cycles. *Refer to the applicable INTEL data sheet for detailed description of the erasing and programming procedure.*

6.2 DDR SDRAM

The phyCORE-MPC5200B tiny is equipped with fast **Double Data Rate Synchronous Dynamic Random Access Memory** (DDR SDRAM) devices. This memory is connected to a dedicated SDRAM interface provided by the MPC5200B processor.

The DDR SDRAM memory bank consist of two 16-bit data port devices connected in parallel to support the 32-bit bus width of the processor. The memory bank is controlled by Chip Select signal /SD_CS0 of the processor's DDR SDRAM controller.

Table 6 shows all possible memory configurations.

Available Capacity	Device Organization	Devices (two)
32 MByte	128 MBit 2 MBit x 16 x 4 banks	MT46V8M16 TSOP66 packaging
64 MByte	256 MBit 4 MBit x 16 x 4 banks	MT46V16M16 TSOP66 packaging
128 MByte	512 MBit 8 MBit x 16 x 4 banks	MT46V32M16 TSOP66 packaging

Table 6: *DDR SDRAM Device Selection*

6.3 Serial Memory

The phyCORE-MPC5200B tiny features a non-volatile memory device (EEPROM) with a serial I²C interface. This memory can be used for storage of configuration data or operating parameters that must be maintained in the event of a power interruption. The available capacity is 4 kByte.

Note:

The first 2 kilobytes section of the EEPROM is already used for storing the boot manager (U-Boot) environment variables. This portion must not be used by user data.

The MPC5200B processor provides two on-chip I²C interfaces. The memory device is connected to I²C interface #2.

Table 7 gives an overview of the possible devices for use at U4 as of the printing of this manual.

Type	Size	I ² C Frequency	Address Pins	Write Cycles	Life of Data	Device	Manufacturer
EEPROM	4 kBytes	400 kHz	A2, A1, A0	1 000 000	100 yrs.	CAT24WC32	CATALYST

Table 7: Serial Memory Options for U4

It is important to note that the RTC U5 is also connected to the I²C #2 bus. The RTC can operate with a bus frequency up to 400 kHz. Therefore the use of high bus frequencies for accessing the serial memory is not recommended. The RTC has the I²C bus slave address 0xA2 / 0xA3. The slave address of the serial memory must be selected accordingly using solder jumpers J4 (A0), J5 (A1) and J6 (A2) to avoid bus collision.

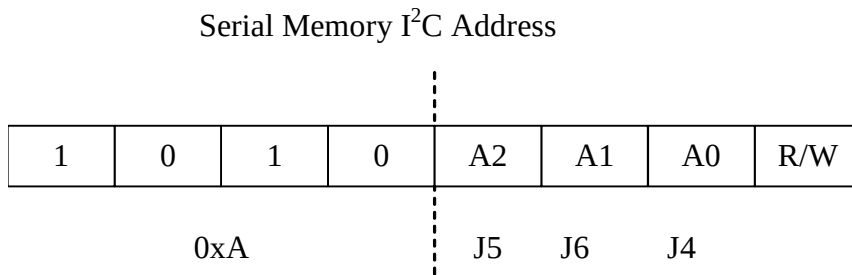


Figure 9: Serial Memory I²C Slave Address

Possible configuration options are shown below:

I ² C Address	J4 A0	J5 A1	J6 A2
0xA0 / 0xA1	2 + 3	1 + 2	2 + 3
0xA4 / 0xA5	2 + 3	2 + 3	2 + 3
0xA8 / 0xA9	2 + 3	1 + 2	1 + 2
0xAC / 0xAD	2 + 3	2 + 3	1 + 2

Table 8: Serial Memory I²C Address (Examples)

Address lines A1 and A2 are not always made available with certain serial memory types. This should be noted when configuring the I²C bus slave address.

7 Real-Time Clock RTC-8564 (U5)

For real-time or time-driven applications, the phyCORE-MPC5200B tiny is equipped with a RTC-8564 Real-Time Clock at U5. This RTC device provides the following features:

- Serial input/output bus (I²C), address 0xA2
- Power consumption
 - Bus active (400 kHz): < 1 mA
 - Bus inactive, CLKOUT inactive: < 1 μ A
- Clock function with four year calendar
- Century bit for year 2000-compliance
- Universal timer with alarm and overflow indication
- 24-hour format
- Automatic word address incrementing
- Programmable alarm, timer and interrupt functions

The Real-Time Clock is programmed via the I²C bus (address 0xA2 / 0xA3). Since the MPC5200B is equipped with an internal I²C controller, the I²C protocol is processed very effective without extensive processor action (*refer also to section 6.3*)

The Real-Time Clock also provides an interrupt output that extends to the /IRQRTC signal X1D33. An interrupt occurs in the event of a clock alarm, timer alarm, timer overflow and event counter alarm. It has to be cleared by software. With the interrupt function, the Real-Time Clock can be utilized in various applications.

If the RTC interrupt is to be used as a software interrupt via a corresponding interrupt input of the processor, the signal /IRQRTC must be connected externally with a processor interrupt input.

The RTC_CLKOUT signal can be programmed to various frequencies e.g. 1Hz. The RTC_CLKOUT output must be enabled via solder jumper J7.

For more information on the features of the RTC-8564, refer to the corresponding Data Sheet.

Note:

After connection of the supply voltage the Real-Time Clock generates **no** interrupt. The RTC must first be initialized (*see RTC Data Sheet for more information*).

8 Serial Interfaces

8.1 RS-232 Interface

A dual-channel RS-232 transceiver is located on the phyCORE-MPC5200B tiny at U3. This device adjusts the signal levels of the UART3_RXD/TXD_TTL and UART6_RXD/TXD_TTL lines (MPC5200B PSC3/PSC6). The RS-232 interface enables connection of the module to a COM port on a host-PC or other peripheral devices. In this instance, the RXD3-232 or RXD6-232 line (X1D22/X1C21) of the transceiver is connected to the corresponding TXD line of the COM port; while the TXD3-232 or TXD6-232 line (X1D23/X1C23) is connected to the RXD line of the COM port. The Ground circuitry of the phyCORE-MPC5200B tiny must also be connected to the applicable Ground pin on the COM port.

The processor's on-chip UART supports handshake signal communication. Use of an RS-232 signal level in support of handshake communication requires use of an external RS-232 transceiver not located on the module.

Furthermore it is possible to use the TTL signals of both of the UART channels externally. These signals are available at X1D16, X1D17 (UART3_RXD_TTL, UART3_TXD_TTL) and X1C19, X1C20 (UART6_RXD_TTL, UART6_TXD_TTL) on the phyCORE-connector. External connection of TTL signals is required for galvanic separation of the interface signals. Using solder jumpers J1 and J2, the TTL transceiver outputs of the on-board RS-232 transceiver devices can be disconnected from the receive lines UART3_RXD_TTL and UART6_RXD_TTL. This is required so that the external transceiver does not drive signals against the on-board transceiver. The transmit lines UART3_TXD_TTL / UART6_TXD_TTL can be connected parallel to the transceiver input without causing any signal conflicts.

8.2 Ethernet Interface

Connection of the phyCORE-MPC5200B tiny to the world wide web or a local network (LAN) is possible over the integrated FEC (Fast Ethernet Controller) of the Freescale processor. The FEC operates with a data transmission speed of 10 or 100 Mbit/s.

8.2.1 PHY Physical Layer Transceiver

The phyCORE-MPC5200B tiny has been designed for use in 10Base-T and 100Base-T networks. The 10/100Base-T interface with its LED monitoring signals extends to phyCORE-connector X1. In order to connect the module to an existing 10/100Base-T network some external circuitry is required. The required 49,9 Ohm +/-1% termination resistors on the analog signals (ETH_RX±, ETH_TX±) are already populated on the module.

If you are using the applicable Development Board for the phyCORE-MPC5200B tiny (part number PCM-973), the external circuitry mentioned above is already integrated on the board (*refer to section 14*).

The default PHY address configured with the boot-strapping option is 0x1.

Table 9 shows the interface signals for the Ethernet channel.

FEC Channel PHY U2	Pin Function	Location at phyCORE- Connector
ETH_RX+	Differential positive receive input signal	X1D35
ETH_RX-	Differential negative receive input signal	X1C35
ETH_TX+	Differential positive transmit output signal	X1D36
ETH_TX-	Differential negative transmit output signal	X1C36
ETH_LED0	Link/activity LED output "H"/LED off no link "L"/LED on link "toggle"/LED toggle activity	X1C33
ETH_LED1	Speed LED output "H"/LED off 10BT "L"/LED on 100BT	X1C34
ETH_LED3	Collision LED output "H"/LED off no collision "L"/LED on collisions	X1C41

Table 9: Signal Definition PHY Ethernet Port (U2)

8.2.2 MAC Address

In a computer network such as a local area network (LAN), the MAC (Media Access Control) address is a **unique** computer hardware number. For a connection to the Internet, a table is used to convert the assigned IP number to the hardware's MAC address.

In order to guarantee that the MAC address is unique, all addresses are managed in a central location. PHYTEC has acquired a pool of MAC addresses. The MAC address of the phyCORE-MPC5200B is located on the bar code sticker attached to the module. This number is a 12-position HEX value.

8.3 USB 1.1 Host Interface

The MPC5200B integrates a USB 1.1 compliant host interface with two ports. This interface supports full-speed (12 Mbit/s) transmission rates. The USB 1.1 controller is integrated in the MPC5200B processor. The physical layer transceiver unit must be connected externally, it is **not** populated on the phyCORE module.

For additional information of the USB 1.1 controller refer to the MPC5200B Reference Manual as well as the USB 1.1 bus specification provided by www.usb.org.

9 The U-Boot Boot Loader

"U-Boot" is a universal boot loader firmware based on GPL (Gnu Public License). Its main function is initializing the system hardware following a reset followed by starting application software such as an operating system.

Furthermore, U-Boot provides various functions to query system information and to change the start-up behavior of the target system. For example U-Boot allows to choose from different boot sources (such as Ethernet, etc.). It also provides functions to download application code into Flash.

The serial interface is used to communicate with U-Boot on the target system. The U-Boot for phyCORE-MPC5200B tiny uses PSC3 with 115,200 Baud, 8, N, 1. The U-Boot boot messages can be viewed within a terminal program running on a host PC using the above mentioned communication settings.

Note:

PHYTEC delivers all phyCORE-MPC5200B tiny modules with a pre-installed U-Boot allowing the user immediate startup. The U-Boot software project is subject to continuous maintenance and improvements. Firmware updates will occur without special notification. Should you require a specific version of U-Boot pre-installed at time of delivery please contact PHYTEC's sales department.

If U-Boot is used as boot loader firmware and basic component of the system software, the user should be familiar with the following topics in order to ensure proper function:

- U-Boot default system configuration
- system resources required by U-Boot
- modifying the U-Boot loader

9.1 U-Boot Default System Configuration

The U-Boot boot loader changes the following default settings to different than the reset values of the controller on the phyCORE-MPC5200B tiny:

Clock: Core = 396 MHz, IPB=132 MHz, PCI=33 MHz

Memory Base Address Register (MBAR): 0xF0000000

DDR-RAM: Automatic storage size detection; start address 0x0

Flash: Chip Select = /CSBoot, 16-bit data bus width, 25 address lines, multiplexed mode, 1 wait state; 16 MByte starting at address 0xFF000000

PSC2: CAN1&2

PSC3: UART, 115200 baud, 8,N,1 ; SPI

PCI: Enabled, 33MHz

Ethernet: 100 Mbit/s with MD

I²C_2: EEPROM at address 0x52, RTC at address 0x51

9.2 System Resources Required by U-Boot

U-Boot is located at address 0xFFFF0 0000 in the module's Flash and occupies two sectors (2x 128kByte). The boot loader itself makes sure that these sectors are protected using the Flash's "locked sector" mechanism. This makes accidental erasure of U-Boot almost impossible. Following a system start at address 0xFFFF0 0100 (high boot), U-Boot first initializes the DDR-RAM interface, then copies itself to the upper end of the RAM memory space and transfers program execution to this address. As a result U-Boot now runs out of RAM which allows for reprogramming itself in Flash (firmware update).

So called environment variables are used to configure U-Boot. Such variables define the IP number as well as the MAC address using Ethernet configuration as example. The variables are saved in the module's EEPROM (U4) and occupy the first 2 kByte.

When using the RAM memory, care should be taken to not overwrite the U-Boot code as well as the trap table which is located in the lower portion of the RAM. Among other factors, the size of the U-Boot stack determines how much memory at the upper end of the RAM memory range is occupied by U-Boot. As U-Boot is used the stack size is growing and more memory space is required. It is recommended to reserve a sufficient RAM portion to be used for the stack beginning at the stack start address.

9.2.1 The "Backup" U-Boot

In the event the "original" U-Boot at address 0xFFFF0 0000 becomes corrupted (e.g. by overwriting the loader with a wrong version) a second U-Boot loader at address 0xFF00 0000 is available as an "emergency" backup version providing the same functionality as the original copy. This backup U-Boot can be started by connecting a 4.7 kOhm pull down resistor at pin X1-8C during a hardware reset cycle.

Note:

When using the phyCORE-MPC5200B-tiny in conjunction with the applicable Carrier Board (part number PCM-973) the "Backup" U-Boot loader can be started by closing Jumper JP3 at position 1+2.

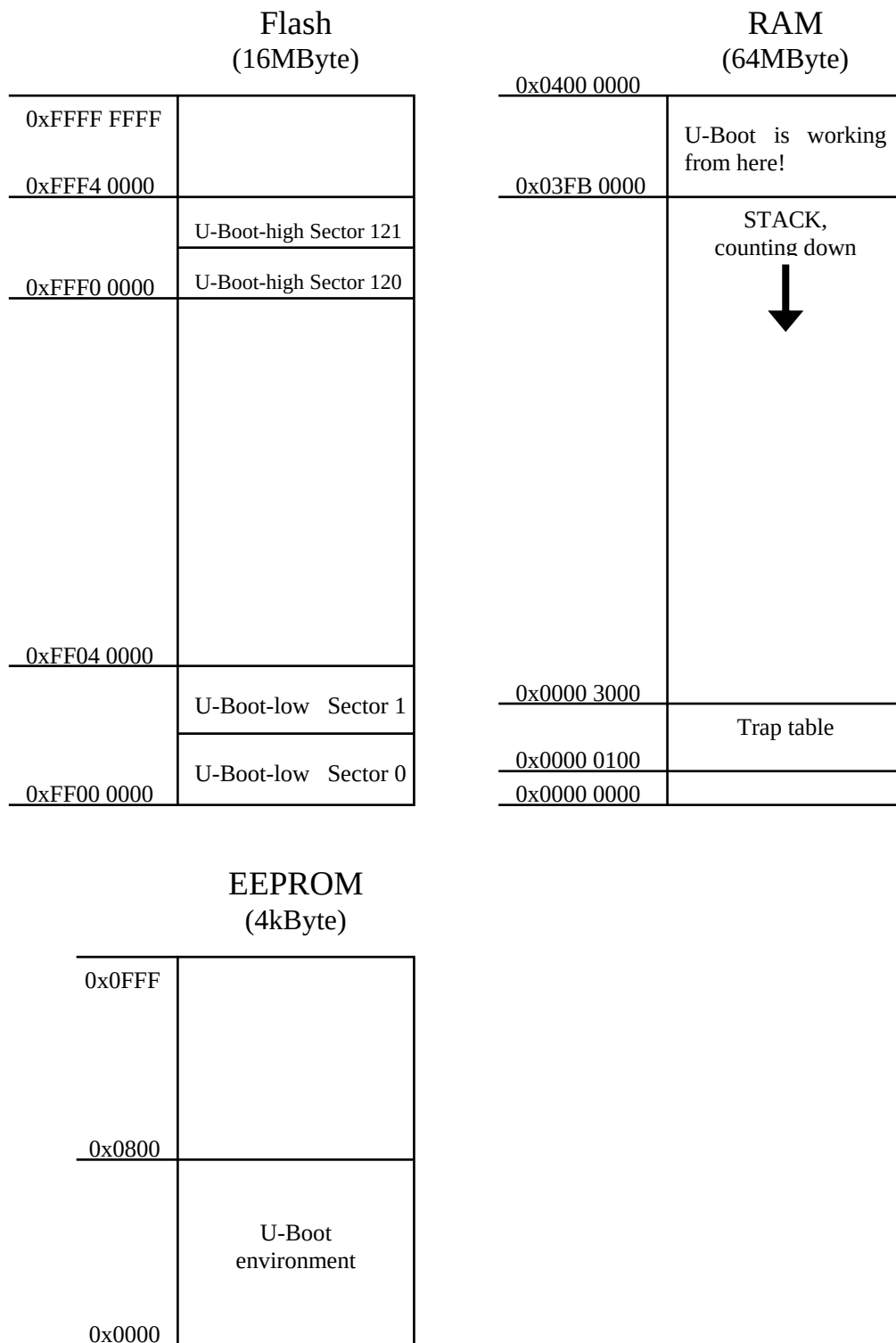


Figure 10: U-Boot Memory Map

9.3 Modifying the U-Boot Loader

Changing the U-Boot should always be compared to recompiling the program code and updating the Flash contents. A detailed description of each individual step would by far exceed the scope of this Hardware Manual. Please refer to the Application Note "Configuring and Updating the Boot Loader", document number LAN-044 for more details.

10 JTAG Interface

The MPC5200B CPU provides a JTAG interface for connecting to debuggers, emulators and boundary scan. The JTAG interface signals extend to the module's phyCORE-connector. Furthermore, there is an on-board JTAG connector (X2) located at the edge of the module, which has the standard COP-Interface pinout but uses a 2.0 mm pin pitch instead of 2.54 mm. The connector is not populated on the standard version of the phyCORE-MPC5200B. You can order a specific debug version of the module (denoted by the –D part number extension) or populate a 2*8-pin header connector at space X2. The numbering scheme is depicted on the phyCORE-MPC5200B. The pinout of the JTAG interface at X2 is described in the following table.

Signal	Pin Row		Signal
	Bottom	Top	
TDO	1	2	NC (quack)
TDI	3	4	/TRST
NC (/halted)	5	6	3V3
TCK	7	8	NC
TMS	9	10	NC
/SReset	11	12	GND
/HReset	13	14	NC (key)
CK_Stop	15	16	GND

Table 10: JTAG Interface

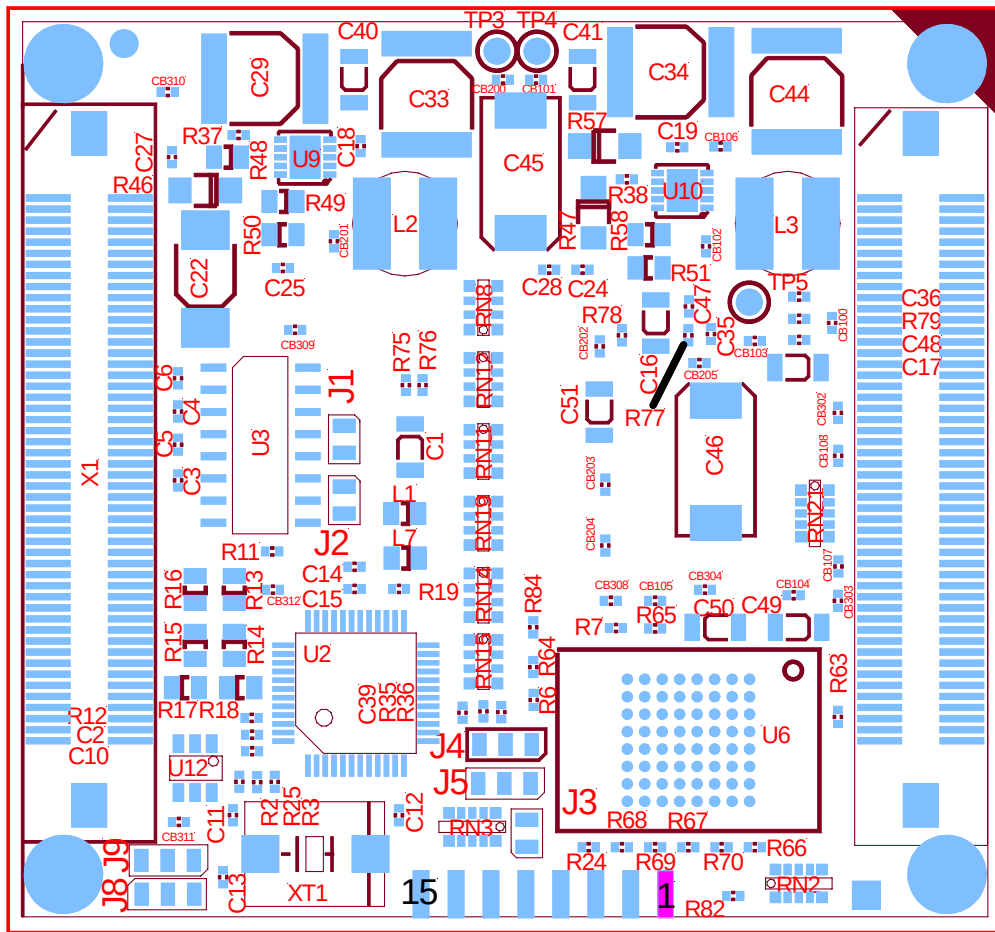


Figure 12:1245.2 component placement Bottom view

The height of all components on the top side of the PCB is ca. 2.5 mm. The PCB itself is approximately 1.6 mm thick. The Molex connector pins are located on the underside of the PCB, oriented parallel to its two long sides. The maximum height of components on the underside of the PCB is 2.5 mm.

Additional Technical Data:

Parameter	Condition	Characteristics
Dimensions		57 mm x 53 mm
Weight		approximately 25g with all optional components mounted on the circuit board
Storage Temp. Range		-40°C to +90°C
Operating Temp. Range:		
Extended		-25°C to +85°C
Humidity		max. 95 % r.F. not condensed
Operating voltages:		
Voltage 3.3V		3.3 V $\pm$ 5 %
Operating Power Consumption:	(depending on load)	
Voltage 3.3 V		Max. 4 watts

Table 11: Technical Data

These specifications describe the standard configuration of the phyCORE-MPC5200B tiny as of the printing of this manual.

Connectors on the phyCORE-MPC5200B tiny:

Manufacturer	Molex
Number of pins per contact rows	100 (2 rows of 50 pins each)
Molex part number (lead free)	52760-1009 (receptacle)

Two different heights are offered for the receptacle sockets that correspond to the connectors populating the underside of the phyCORE-PXA255. The given connector height indicates the distance between the two connected PCBs when the module is mounted on the corresponding carrier board. In order to get the exact spacing, the maximum component height (2,5 mm) on the underside of the phyCORE must be subtracted.

Component height 6 mm

Manufacturer	Molex
Number of pins per contact row	100 (2 rows of 50 pins each)
Molex part number (lead free)	55091-1079 (header)

Component height 10 mm

Manufacturer	Molex
Number of pins per contact row	160 (2 rows of 80 pins each)
Molex part number (lead free)	53553-1079 (header)

Please refer to the corresponding data sheets and mechanical specifications provided by Molex (www.molex.com).

13 Hints for Handling the Module

- **Modifications on the phyCORE Module**

Removal of various components, such as the microcontroller and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Carefully heat neighboring connections in pairs. After a few alternations, components can be removed with the solder-iron tip. Alternatively, a hot air gun can be used to heat and loosen the bonds.

Caution!

If any modifications to the module are performed, regardless of their nature, the manufacturer guarantee is voided.

- **Integrating the phyCORE-MPC5200B tiny into a Target Application**

Successful integration in user target circuitry greatly depends on the adherence to the layout design rules for the GND connections of the phyCORE module. For best results we recommend using a carrier board design with a full GND layer. It is important to make sure that the GND pins that have neighboring signals which are used in the application circuitry are connected. Just for the power supply of the module at least 6 GND pins that are located right next to the VCC pins must be connected

14 The phyCORE-MPC5200B tiny on the Carrier Board

PHYTEC Carrier Boards are fully equipped with all mechanical and electrical components necessary for the speedy and secure start-up and subsequent communication to and programming of applicable PHYTEC Single Board Computer (SBC) modules. Carrier Boards are designed for evaluation, testing and prototyping of PHYTEC Single Board Computers in laboratory environments prior to their use in customer designed applications.

14.1 Concept of the Carrier Board phyCORE-MPC5200B

The Carrier Board phyCORE-MPC5200B tiny provides a flexible development platform enabling quick and easy start-up and subsequent programming of the phyCORE-MPC5200B tiny Single Board Computer module. The Carrier Board design allows easy connection of additional expansion boards featuring various functions that support fast and convenient prototyping and software evaluation.

This modular development platform concept is depicted in Figure 14 and includes the following components:

- The actual **Carrier Board** (1), which offers all essential components and connectors for start-up including: a power socket enabling connection to an **external power adapter** (2) and **serial interfaces** (3) of the SBC module at DB-9 connectors.
- Most of the signals from the SBC module mounted on the Carrier Board extend to two mating receptacle connectors. The pin assignment of these **expansion bus** (4) depends entirely on the pinout of the SBC module mounted on the Carrier Board.

- As the physical layout of the expansion bus is standardized across all applicable PHYTEC Carrier Boards, we are able to offer various **expansion boards** (5) that attach to the Carrier Board at the expansion bus connectors. These modular expansion boards offer **supplemental I/O functions** (6) as well as peripheral support devices for specific functions offered by the controller populating the **SBC module** (9) mounted on the Carrier Board.
- All controller and on-board signals provided by the SBC module mounted on the Carrier Board are broken out 1:1 to the expansion board by means of its **patch field** (7). The required connections between SBC module / Carrier Board and the expansion board are made using **patch cables** (8) included with the expansion board.

Figure 14 illustrates the modular development platform concept:

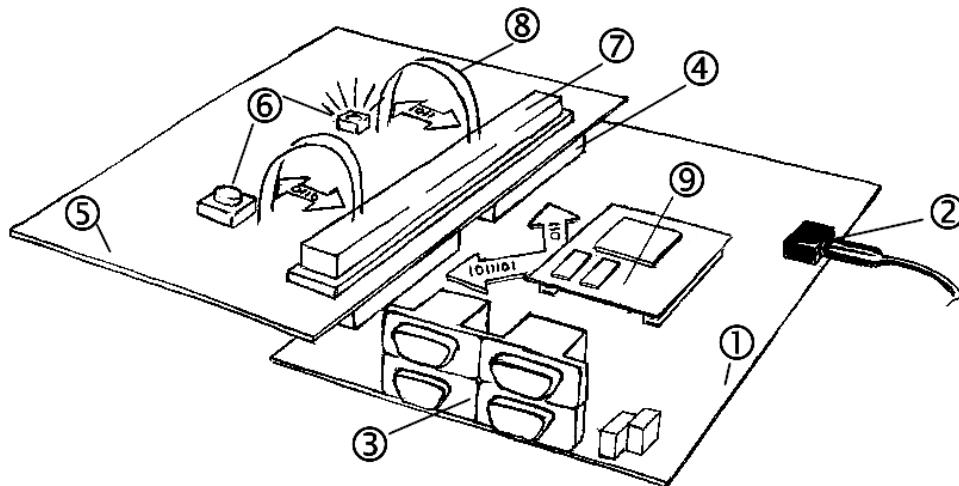


Figure 14: Modular Development and Expansion Board Concept with the phyCORE-MPC5200B tiny

The following sections contain specific information relevant to the operation of the phyCORE-MPC5200B tiny mounted on the Carrier Board phyCORE-MPC5200B tiny.

14.2 Carrier Board phyCORE-MPC5200B tiny Connectors and Jumpers

14.2.1 Connectors

As shown in Figure 15, the following connectors are available on the phyCORE Development Board PCM-973:

X1-	phyCORE-connector for phyCORE module with 400 pins (e.g. phyCORE-MPC5200B tiny)
X2-	phyCORE-connector for phyCORE module with 200 pins (e.g. phyCORE-MPC5200B-tiny)
X3-	400-pin mating receptacle for GPIO expansion board connectivity
X4-	PCI connector for compatible 3.3V PCI insert cards
X5-	JTAG pin header for PCI insert card connector X4
X6-	Connector for supply voltage 9 -14V
X7-	PE connection
X8-	JTAG pin header for FPGA
X9-	JTAG pin header for MPC5200B controller
X10-	Compact Flash card socket
X11-	IDE Interface connector
X12-	FPGA configuration interface
X15-	Base Speaker Interface of the WM9712 (U20)
X16-	Mono out from WM9712
X17-	Beeper out from WM9712
X18-	SPDIF out from WM9712
X19-	Differential output from WM9712
X20-	Auxiliary output from WM9712
P1-	RJ45 Interface for Ethernet connection 10/100MBit
P2-	dual DB-9 plugs for CAN interface connectivity
P3-	dual DB-9 sockets for serial RS232 interface connectivity
P4-	MIC input

- P5- Line in left/right
P6- Line out left/right
GND1 GND connector for measurement purposes

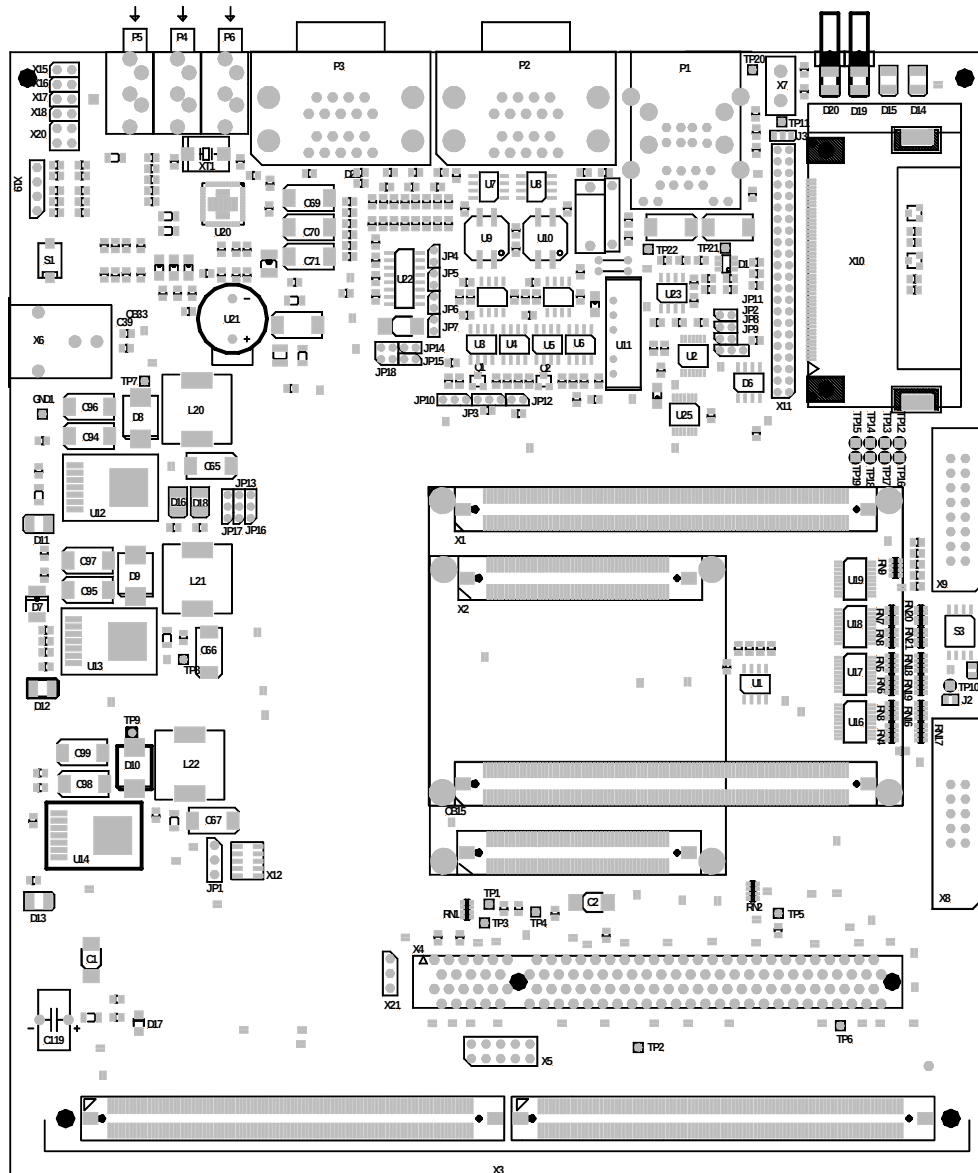


Figure 15: Location of Connectors on the phyCORE-MPC-5200B-tiny Carrier Board

Please note that all module connections are not to exceed their expressed maximum voltage or current. Maximum signal input values are indicated in the corresponding controller User's Manual/Data Sheets. As damage from improper connections varies according to use and application, it is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

14.2.2 Jumpers on the Carrier Board phyCORE-MPC5200B tiny

Peripheral components of the phyCORE-MPC5200B tiny Carrier Board can be connected to the signals of the phyCORE-MPC5200B tiny by setting the applicable jumpers.

The Carrier Board's peripheral components are configured for use with the phyCORE-MPC5200B tiny by means of removable jumpers. If no jumpers are set, no signals connect to the DB-9 connectors, the control and display units and the CAN transceivers. The Reset input on the phyCORE-MPC5200B tiny directly connects to the Reset button (S1). Figure 16 illustrates the numbering of the jumper pads, while Figure 17 indicates the location of additional jumpers on the Carrier Board.

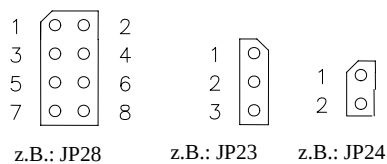


Figure 16: Numbering of Jumper Pads

0

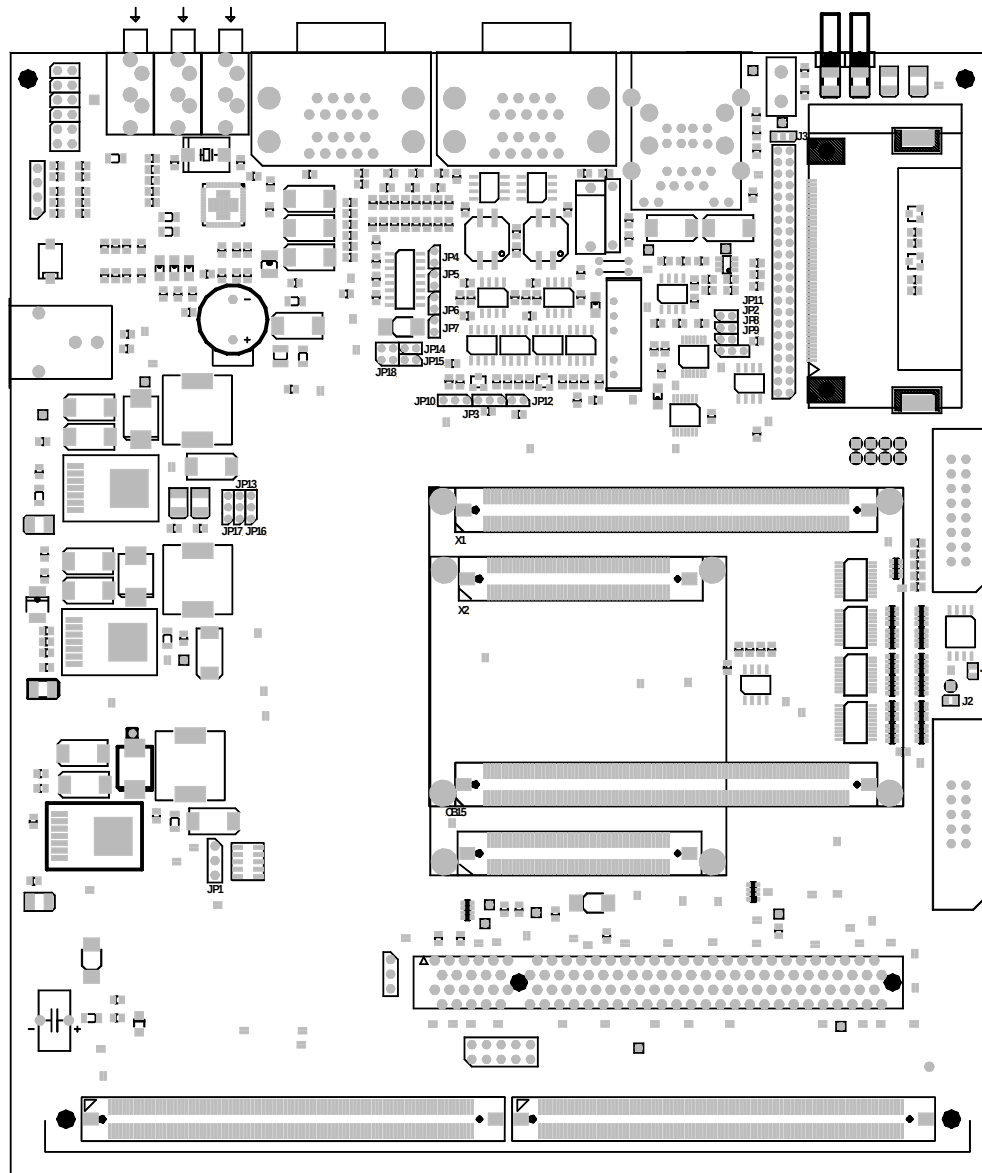


Figure 17: Location of the Jumpers (View of the Component Side)

Figure 18 shows the factory default jumper settings for operation of the phyCORE-MPC5200B tiny Carrier Board with the standard phyCORE-MPC5200B tiny (standard = MPC5200B controller, use of first and second RS-232, both CAN interfaces and LED D3 on the Carrier Board). Jumper settings for other functional configurations of the phyCORE-MPC5200B tiny module mounted on the Carrier Board are described in *section 14*.

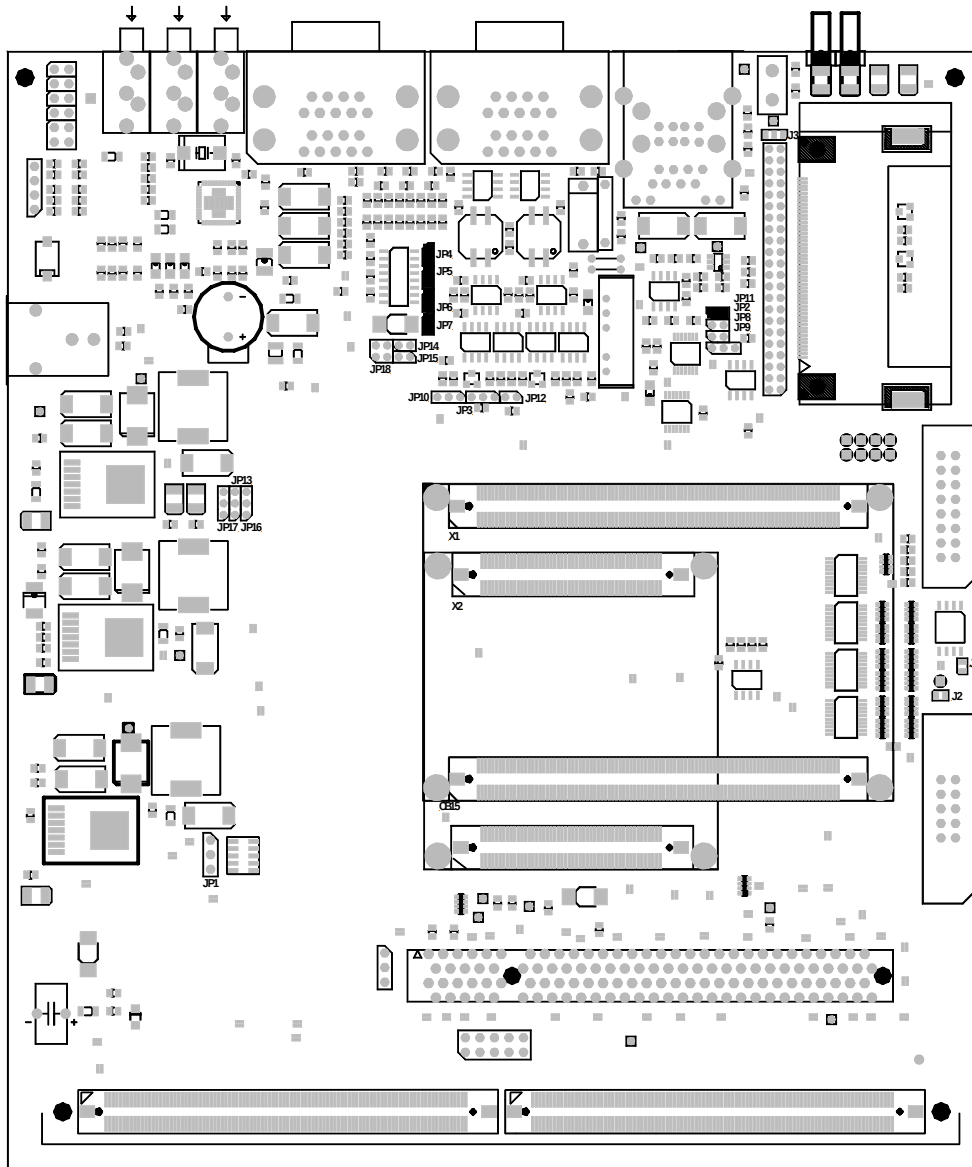


Figure 18: Default Jumper Settings of the phyCORE Development Board MPC5200B tiny with phyCORE-MPC5200B tiny

14.3 Functional Components on the phyCORE-MPC5200B tiny Carrier Board

This section describes the functional components of the phyCORE-MPC5200B tiny Carrier Board supported by the phyCORE-MPC5200B tiny and appropriate jumper settings to activate these components. Depending on the specific configuration of the phyCORE-MPC5200B tiny module, alternative jumper settings can be used. These jumper settings are different from the factory default settings as shown in Figure 18 and enable alternative or additional functions on the phyCORE-MPC5200B tiny Carrier Board depending on user needs.

14.3.1 Power Supply at X6

Caution:

Only use the included power adapter to supply power to the Carrier Board! Do not change modules or jumper settings while the Carrier Board is supplied with power!

Permissible input voltage: $\pm 9 - 14$ V DC unregulated.

The required current load capacity of the power supply depends on the specific configuration of the phyCORE-MPC5200B tiny mounted on the Carrier Board as well as whether an optional expansion board is connected to the Carrier Board. An adapter with a minimum supply of 1.2 A is recommended.

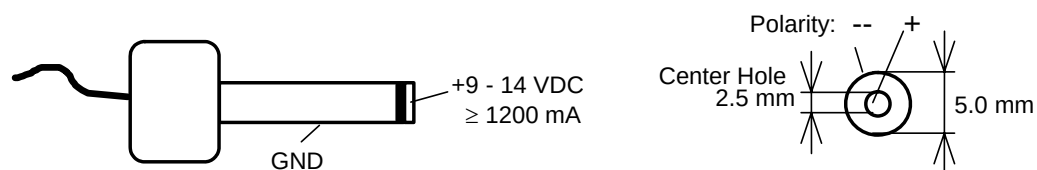


Figure 19: Connecting the Supply Voltage at X6

No jumper configuration is required in order to supply power to the phyCORE-MPC5200B tiny module!

14.3.2 First Serial Interface at Socket P3A

Socket P3A is the lower socket of the double DB-9 connector at P3. P3A is directly connected to the serial interface PSC3 of the phyCORE-MPC5200B tiny. The only signal configurable with Jumper JP18 is UART3_CTS_TTL coming from PSC3 on the MPC5200B.

Jumper	Setting	Description
JP18	3 + 4	Signal UART3_CTS_TTL is connected to the RS-232 transceiver U22 on the phyCORE-MPC5200B tiny Carrier Board, interface signals with RS-232 level are available at connector P3A
JP18	open	UART3_CTS_TTL signal is freely available

Table 12: Jumper Configuration for the First RS-232 Interface

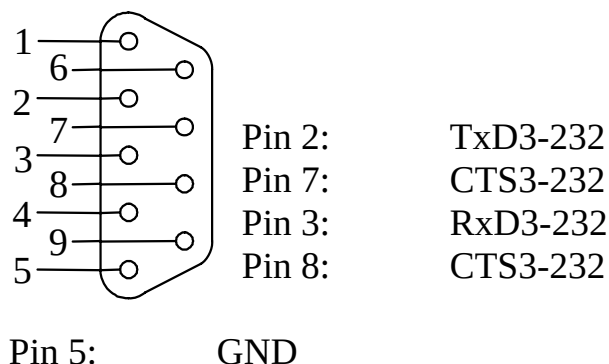


Figure 20: Pin Assignment of the DB-9 Socket P3A as RS-232 (PSC3) (Front View)

14.3.3 Second Serial Interface at Socket P3B

Socket P3B is the upper socket of the double DB-9 connector at P3. P3B is connected directly to the serial interface PSC6 of the phyCORE-MPC5200B tiny. The only signal configurable with Jumper JP18 is UART6_CTS_TTL coming from PSC6 on the MPC5200B.

Jumper	Setting	Description
JP18	1 + 2	Signal UART6_CTS_TTL is connected to the RS-232 transceiver U22 on the phyCORE-MPC5200B tiny Carrier Board, interface signals with RS-232 level are available at connector P3B
JP18	open	UART6_CTS_TTL signal is freely available

Table 13: Jumper Configuration of the DB-9 Socket P3B (PSC6)

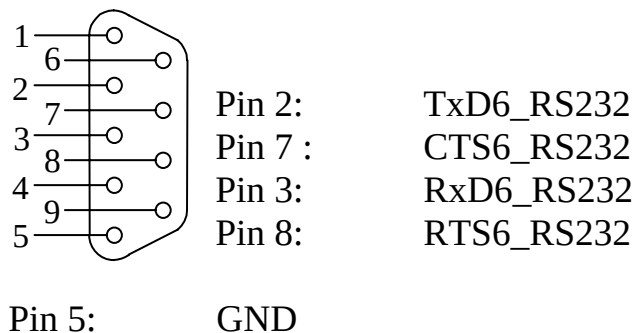


Figure 21: Pin Assignment of the DB-9 Socket P3B as Second RS-232 (Front View)

14.3.4 First CAN Interface at Plug P2A

Plug P2A is the lower plug of the double DB-9 connector at P2. P2A is connected to the first CAN interface (CAN1) of the phyCORE-MPC5200B tiny via jumpers. There are no CAN transceivers available on the phyCORE-MPC5200B tiny therefore the transceivers on the Carrier Board must be used. Depending on the configuration of the CAN transceivers and their power supply, the following configuration is possible:

1. CAN signals generated by the Carrier Board CAN transceiver (U9) extend to connector P2A **with galvanic separation**:

Jumper	Setting	Description
JP4	closed	Input at opto-coupler U3 on the Carrier Board connected to CAN1_TX signal from the phyCORE-MPC5200B tiny
JP5	closed	Output at opto-coupler U4 on the Carrier Board connected to CAN1_RX signal of the phyCORE-MPC5200B tiny

Table 14: Jumper Configuration for CAN Plug P2A using the CAN Transceiver on the Carrier Board

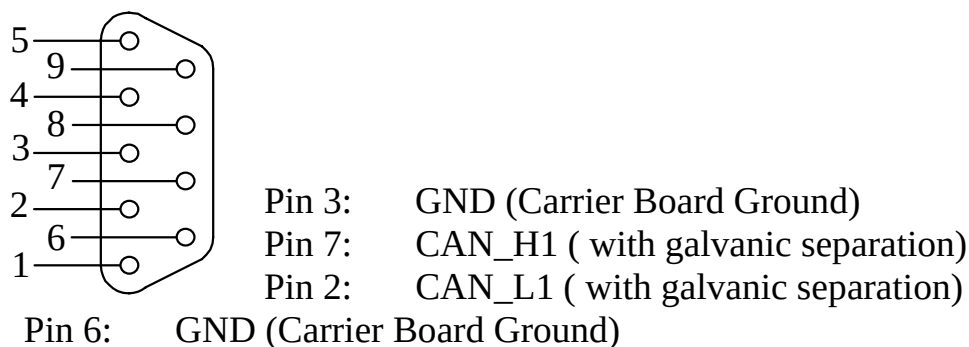


Figure 22: Pin Assignment of the DB-9 Plug P2A (CAN Transceiver on Carrier Board)

Caution:

When using the DB-9 connector P2A as CAN interface and the CAN transceiver on the Carrier Board the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP4	open	CAN1_TX signal not connected to transceiver, no CAN communication possible
JP5	open	CAN1_RX signal not connected to transceiver, no CAN communication possible

Table 15: *Improper Jumper Settings for the CAN Plug P2A (CAN Transceiver on the Carrier Board)*

14.3.5 Second CAN Interface at Plug P2B

Plug P2B is the upper plug of the double DB-9 connector at P2. P2B is connected to the second CAN interface (CAN2) of the phyCORE-MPC5200B tiny via jumpers. There are no CAN transceivers available on the phyCORE-MPC5200B tiny therefore the transceivers on the Carrier Board must be used. Depending on the configuration of the CAN transceivers and their power supply, the following configuration is possible:

- 1. CAN signals generated by the Carrier Board CAN transceiver (U10) extend to connector P2B **with galvanic separation**:

Jumper	Setting	Description
JP6	closed	Input at opto-coupler U5 on the Carrier Board connected to CAN2_TX signal from the phyCORE-MPC5200B tiny
JP7	closed	Output at opto-coupler U6 on the Carrier Board connected to CAN2_RX signal of the phyCORE-MPC5200B tiny

Table 16: Jumper Configuration for CAN Plug P2B using the CAN Transceiver on the Carrier Board

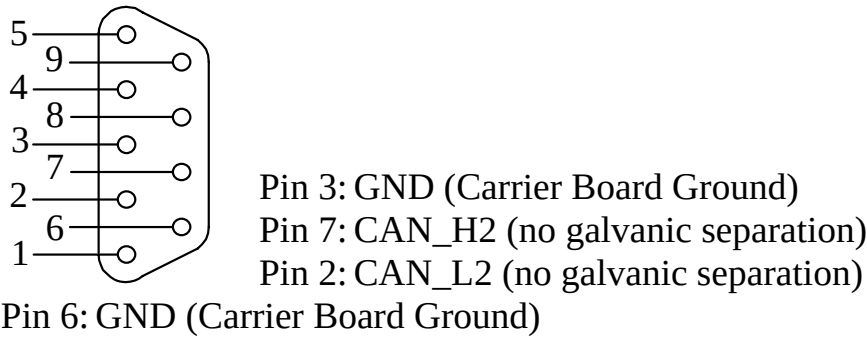


Figure 23: Pin Assignment of the DB-9 Plug P2B (CAN Transceiver on Carrier Board)

Caution:

When using the DB-9 connector P2B as second CAN interface and the CAN transceiver on the Carrier Board the following jumper settings are not functional and could damage the module:

Jumper	Setting	Description
JP6	open	CAN2_TX signal not connected to transceiver, no CAN communication possible
JP7	open	CAN2_RX signal not connected to transceiver, no CAN communication possible

Table 17: *Improper Jumper Settings for the CAN Plug P2B (CAN Transceiver on the Carrier Board)*

14.3.6 Programmable LED D16

The phyCORE Carrier Board MPC5200B tiny offers a programmable LED at D16 for user implementations. This LED can be connected to port pin Gpio_Wkup_7 (ball C12) or to the SPI_MOSI signal (ball B5) of the MPC5200B CPU. A low-level at applicable port pin causes the LED to illuminate, LED D16 remains off when writing a high-level.

Jumper	Setting	Description
JP13	1 + 2	Port pin SPI_MOSI of the MPC5200B controls LED D16 on the Carrier Board
JP13	2 + 3	Port pin Gpio_Wkup_7 of the MPC5200B controls LED D16 on the Carrier Board

Table 18: JP17 Configuration of the Programmable LED D3

14.3.7 Ethernet Interface P1A

The Ethernet interface of the phyCORE-MPC5200B tiny is accessible at an RJ45 connector (P1A) on the Carrier Board. Due to its characteristics this interface is hard-wired and can not be configured via jumpers. The LEDs for LINK and SPEED indication are integrated in the connector. Two additional LEDs at D19 and D20 are provided to allow display of other Ethernet transmission states. These LEDs can be used to indicate transmission type and possible collisions that may occur on the Ethernet network. Jumpers JP8 and JP9 allow configuration of additional Ethernet PHY interface signals. The following configuration options are possible:

Jumper	Setting	Description
JP8	open	/ETH_INT from PHY on the phyCORE-MPC5200B tiny not connected
	closed	/ETH_INT from PHY on the phyCORE-MPC5200B tiny connected to /IRQ1 on the phyCORE module
JP9	open	PHY transceiver /ETH_PD input on the phyCORE-MPC5200B tiny not connected
	1 + 2	PHY transceiver /ETH_PD input on the phyCORE-MPC5200B tiny connected to SPI_MISO signal on the phyCORE module
	2 + 3	PHY transceiver /ETH_PD input on the phyCORE-MPC5200B tiny connected to GPIO7 signal on the phyCORE module

Table 19: JP8, JP9 Ethernet Interface Configuration

14.3.8 USB Host Interface P1B

The USB Host interface of the phyCORE-MPC5200B tiny is accessible at connector P1B on the Carrier Board. This interface is compliant with USB version 1.1 and its mode can be configured with the help of Jumper JP2. The following configuration options are possible:

Jumper	Setting	Description
JP2	open	VMO mode selected
	closed	FSEO mode selected

Table 20: JP2 USB Host Interface Configuration

A second USB connector is provided at P1C. However, this connector does not carry any USB communication signals. Connector P1C can only be used to access the USB supply voltage.

14.3.9 Audio Interface

The AC97 interface on the phyCORE-MPC5200B tiny connects to a Wolfson WM9712 audio codec controller on the Carrier Board. A variety of signals generated by the WM9712 IC are available at the following connectors:

- Header X15 - Base Speaker
- Header X18 - SPDIF OUT
- Header X19 - Differential Output
- Header X20 - Auxiliary Output
- Socket P4 - MIC1/MIC2
- Socket P5 - LINE IN R/L
- Socket P6 - LINE OUT R/L

Jumpers JP14 and JP15 are available for configuration of interrupt signals generated by the WM9712 device. The following configuration options are possible:

Jumper	Setting	Description
JP14	open	AC_INT signal on WM9712 not used
	closed	AC_INT signal connected to /IRQ_2 on the phyCORE-MPC5200B tiny
JP15	open	PEN_INT signal from WM9712 not used
	closed	PEN_INT signal connected to /IRQ_3 on the phyCORE-MPC5200B tiny

Table 21: JP14, JP15 AC97 Audio Interface Configuration

14.3.10 Compact Flash Card Socket X10

The phyCORE-MPC5200B tiny Carrier Board provides a Compact Flash (CF) card socket at X10. CF cards used in this socket can only be operated in IDE mode. Activity on the CF card socket is indicated by LED D14. Jumpers J3 and JP11 are available for configuration of the Compact Flash card interface. The following configuration options are possible:

Jumper	Setting	Description
J3	open	<i>Not recommended!</i>
	1 + 2	Compact Flash card write protection active
	2 + 3	Compact Flash card write protection not active
JP11	open	Compact Flash slave mode selected
	closed	Compact Flash master mode selected

Table 22: J3, JP11 CF Card Interface Configuration

14.3.11 IDE Interface X11

The phyCORE-MPC5200B tiny Carrier Board provides an IDE interface header at X11 for connection to external 2.5" hard disks. The 44-pin header connector in 2.0 mm pin spacing allows easy and convenient connection to peripheral devices using a ribbon cable. Activity on the IDE socket is indicated by LED D15.

14.3.12 PCI Card Slot X4

The phyCORE-MPC5200B tiny Carrier Board provides a 3.3V PCI interface connector at X4. All common 3.3V PCI insert cards can be used in this slot allowing the user to add additional interface features to this hardware platform. Configuration of the PCI interface via jumpers is not necessary. Only the required interrupt sources can be configured via SMD resistors. Resistors R95-R98 on the Carrier Board connect the available interrupts. Only R95 is placed as the default configuration connecting /PCI_INTA with /IRQ_0. Additional interrupt sources can be made available by adding the corresponding resistor on the Carrier Board.

Note:

The current draw of the PCI application in combination with the power consumption of all other circuitry used at the same time must not exceed the allowed maximum current draw for the phyCORE-MPC5200B tiny and Carrier Board hardware combination.

14.3.13 Misc. Configuration Jumpers on the Carrier Board

The following table describes additional jumpers provided for configuration of the Carrier Board or the phyCORE-MPC5200B tiny operated on it:

Jumper	Setting	Description
JP3	open	Default Boot configuration of the connected phyCORE-MPC5200B tiny will be used
	1 + 2	Boot configuration of the inserted phyCORE-MPC5200B tiny will be overwritten by a LOW level
	2 + 3	Boot configuration of the inserted phyCORE-MPC5200B tiny will be overwritten by a HIGH level
JP10	open	This Jumper is not supported in conjunction with a phyCORE-MPC5200B tiny
JP12	open	This Jumper is not supported in conjunction with a phyCORE-MPC5200B tiny

Table 23: Misc. Configuration Jumpers JP3, JP10, JP12

14.3.14 FPGA JTAG Connector X8

Connector X8 provide access to the JTAG signals for the FPGA on the phyCORE-MPC5200B-I/O module:

Signal	Pin#	Pin#	Signal
FPGA_TCK	1	2	GND
FPGA_TDO	3	4	3.3V
FPGA_TMS	5	6	n.c. (default), J1 connects to 3.3V
n.c.	7	8	n.c.
FPGA_TDI	9	10	GND

Table 24: FPGA JTAG Connector X8 Pin Assignment

14.3.15 Pin Assignment Summary of the phyCORE, the Expansion Bus and the Patch Field

Most signals from the phyCORE-MPC5200B tiny extend to the Expansion Bus connector X3 on the Carrier Board. These signals, in turn, are routed in a similar manner to the patch field on an optional expansion board that mounts to the Carrier Board at X3.

Please note that, depending on the design and size of the expansion board, only a portion of the entire patch field is utilized under certain circumstances. When this is the case, certain signals described in the following section will not be available on the expansion board. However, the pin assignment scheme remains consistent.

A two dimensional numbering matrix similar to the one used for the pin layout of the phyCORE-connector is provided to identify signals on the Expansion Bus connector (X3 on the Carrier Board) as well as the patch field.

However, the numbering scheme for Expansion Bus connector and patch field matrices differs from that of the phyCORE-connector, as shown in the following two figures:

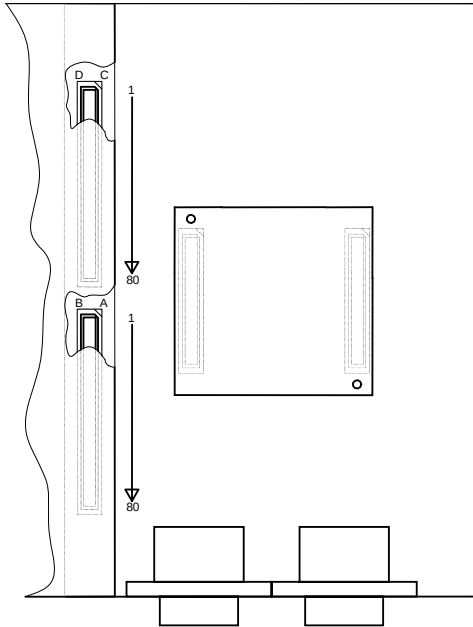


Figure 24: Pin Assignment Scheme of the Expansion Bus

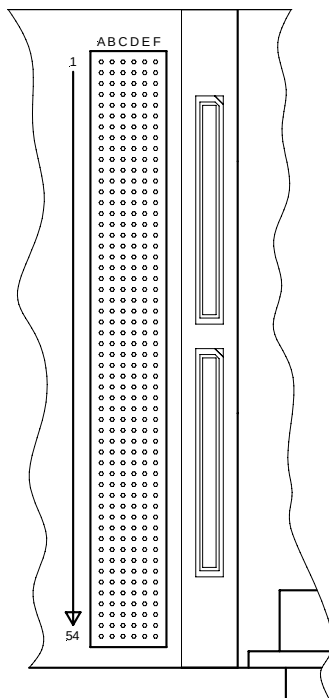


Figure 25: Pin Assignment Scheme of the Patch Field

The pin assignment on the phyCORE-MPC5200B tiny, in conjunction with the Expansion Bus (X3) on the Carrier Board and the patch field on an expansion board, is as follows:

Signal	phyCORE Module	Expansion Bus	Patch Field
Ext_AD0	8B	99A	X15-25
Ext_AD1	9A	98B	X13-25
Ext_AD2	10A	98A	X14-25
Ext_AD3	10B	97B	X12-25
Ext_AD4	11A	96A	X17-24
Ext_AD5	11B	96B	X11-25
Ext_AD6	12B	95A	X16-24
Ext_AD7	13A	95B	X10-25
Ext_AD8	13B	93B	X13-24
Ext_AD9	14A	93A	X15-24
Ext_AD10	15A	91B	X11-24
Ext_AD11	15B	91A	X17-22
Ext_AD12	16A	90B	X10-24
Ext_AD13	16B	90A	X16-22
Ext_AD14	17B	88B	X13-22
Ext_AD15	18A	89A	X15-22
Ext_AD16	18B	83A	X14-21
Ext_AD17	19A	78B	X14-20
Ext_AD18	20A	81A	X17-20
Ext_AD19	20B	77B	X12-20
Ext_AD20	21A	80A	X16-20
Ext_AD21	21B	76B	X11-20
Ext_AD22	22B	79A	X15-20
Ext_AD23	23A	75B	X10-20
Ext_AD24	23B	78A	X14-20
Ext_AD25	24A	72B	X12-19
Ext_AD26	25A	75A	X16-19
Ext_AD27	25B	71B	X11-19
Ext_AD28	26A	74A	X15-19
Ext_AD29	26B	70B	X10-19
Ext_AD30	27B	73A	X13-19

Ext_AD31	28A	68B	X13-17
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*Table 25: Pin Assignment Data/Address Bus for the
phyCORE-MPC5200B tiny / Carrier Board / Expansion Board*

Signal	phyCORE Module	Expansion Bus	Patch Field
/LP_CS1	5A	5A	X15-1
/LP_CS2	5B	35B	X10-10
/LP_CS3	6B	5B	X10-2
/LP_Cs4	30A	6B	X11-2
/LP_Cs5	30B	36B	X11-10
/LP_Cs6	31A	47B	X12-12
/LP_Cs7	31B	48B	X13-12
/LP_Ts	29A	33B	X13-9
LP_Ack	28B	34A	X15-9
/LP_Ale	6A	6A	X17-1
/LP_Oe	7B	8A	X14-2
LP_RD/WR	8A	7B	X12-2

Table 26: Pin Assignment Dedicated LocalPlus Control Signals
 phyCORE-MPC5200B tiny / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/Pci_Reset	40A	70A	X16-17
Pci_Clock	40B	66B	X11-17
/Pci_Gnt	41A	71A	X17-17
/Pci_Req	42B	67B	X12-17
/Pci_Cbe_3	43A	73A	X14-19
Pci_Idsel	43B	76A	X17-19
/Pci_Cbe_2	44A	80B	X10-21
/Pci_Irdy	45A	81B	X11-21
/Pci_Frame	45B	84A	X15-21
/Pci_Devsel	46A	82B	X12-21
/Pci_Trdy	46B	85A	X16-21
/Pci_Stop	47B	86A	X17-21
/Pci_Perr	48A	85B	X10-22
Pci_Par	48B	88A	X14-22
/Pci_Serr	49A	86B	X11-22
/Pci_Cbe_1	50A	87B	X12-22
/Pci_Cbe_0	50B	94A	X15-24

Table 27: Pin Assignment PCI dedicated signals
phyCORE-MPC5200B tiny / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
ATA_Isolation	37B	61B	X11-16
/ATA_Ior	38A	65A	X16-16
/ATA_Dack	38B	62B	X12-16
ATA_intrq	39A	66A	X17-16
ATA_Cs1	35A	63A	X14-16
ATA_Drq	35B	58B	X13-15
ATA_Cs0	34A	61A	X17-15
ATA_Iochrdy	36A	64A	X15-16
/ATA_Iow	36B	60B	X10-16

Table 28: Pin Assignment Dedicated ATA /IDE Interface Signals
 phyCORE-MPC5200B tiny / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
AC97_1_Sdata_In	16C	-	-
AC97_1_Sdata_O	15D	-	-
AC97_1_Res	13C	-	-
AC97_1_Sync	14C	-	-
AC97_1_Bitclk	15C	-	-
TXD6-232	23C	23C	X5-6
RXD6-232	21C	21C	X2-6
UART6_TXD_TL	20C	20C	X8-5
UART6_RXD_TL	19C	19C	X7-5
UART6_RTS_TL	24C	-	-
UART6_CTS_TL	25C	-	-
RXD3-232	22D	22D	X4-6
TXD3-232	23D	23D	X6-6
UART3_TXD_TL	17D	17D	X4-5
UART3_RXD_TL	16D	16D	X3-5
UART3_RTS_TL	25D	25D	X9-6
UART3_CTS_TL	26D	26D	X3-7
CAN1_TX	21D	21D	X3-6
CAN1_RX	20D	20D	X9-5
CAN2_TX	18C	18C	X5-5
CAN2_RX	18D	18D	X6-5
I2C1_Clk	31C	31C	X2-9
I2C1_Io	32D	32D	X4-9
I2C2_Clk	26C	26C	X2-7
I2C2_Io	28C	28C	X4-7

SPI_Mosi	27D	27D	X4-7
SPI_Miso	28D	28D	X6-7
SPI_Clk	30D	30D	X9-7
SPI_Ss	31D	31D	X3-9
ETH_RX-	35C	-	-
ETH_RX+	35D	-	-
ETH_TX-	36C	-	-
ETH_TX+	36D	-	-
/ETH_INT	37D	-	-
ETH_LINK	33C	-	-
ETH_SPEED	34C	-	-
/ETH_PD	38C	-	-
USB1_Oe	50C	-	-
USB1_TXP	50D	-	-
USB1_TXN	49C	-	-
USB1_RXD	47D	-	-
USB1_RXP	48D	-	-
USB1_RXN	48C	-	-
USB1_Suspend	46C	-	-
USB1_PortPwr	45D	-	-
USB1_Overcnt	45C	-	-
USB1_Speed	46D	-	-

Table 29: Pin Assignment Interfaces for the phyCORE-MPC5200B tiny /
Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
CPU_TCK	38D	-	-
/COP_TRST	39C	-	-
CPU_TDI	40D	-	-
CPU_TDO	41D	-	-
CPU_TMS	42D	-	-
CK_STOP	40C	-	-

Table 30: Pin Assignment COP Interface Signals for the
phyCORE-MPC5200B tiny /Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
/IRQ_0	4A	4A	X15-1
/IRQ_1	2B	2B	X12-1
/IRQ_2	3B	3B	X13-1
/IRQ_3	3A	3A	X14-1
Timer2	12D	12D	X4-4
Timer3	13D	13D	X6-4
Timer4	29C	61C	X2-16
Timer5	30C	44C	X7-11
Timer6	44C	60C	X8-15
Timer7	43D	36A	X17-9
/RESIN	10D	10D	X2-4
/HReset	11C	11C	X9-2
/SReset	10C	10C	X9-1
/PWR_GOOD	-	7D	X7-1
/FL_WP	-	9C	X8-2
GPIO7	11D	11D	X3-4
RTC_CLKOUT	1B	1B	X11-1
/IRQRTC	33D	33D	X6-9
PSC2_4	43C	43C	X5-11
ETH_TXD3	33A	58D	X6-15
ETH_TXD2	-	59C	X7-15
ETH_TXD1	8C	60D	X9-15
ETH_TXD0	-	61D	X3-16
ETH_RXD3	-	51C	X2-14
ETH_RXD2	-	52D	X4-14
ETH_RXD1	33B	53C	X5-14
ETH_RXD0	-	54C	X7-14
ETH_CRS	-	50D	X9-12
ETH_RXERR	-	51D	X3-14
ETH_TXCLK	-	53D	X6-14
ETH_RXCLK	-	55D	X9-14
ETH_MDIO	-	56D	X3-15
ETH_MDC	-	57D	X4-15
ETH_TXEN	-	62D	X4-16
ETH_TXERR	-	58C	X5-15

ETH_RXDV	-	56C	X2-15
ETH_COL	-	55C	X8-14
Test_Sel_1	32B	35A	X16-9
ETH_NWAYEN	41C	30C	X8-7
ETH_DUPLEX	-	29C	X7-7
WDI	-	8D	X7-2
/WDO	-	8C	X8-1

Table 31: Pin Assignment Misc. Control Signals for the
phyCORE-MPC5200B tiny /Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
FPGA_TDO	-	-	-
FPGA_TMS	-	-	-
FPGA_TDI	-	-	-
FPGA_TCK	-	-	-
FPGA_B1_C1	-	31B	X11-9
FPGA_B1_C2	-	32B	X12-9
FPGA_B1_D1	-	33A	X14-9
FPGA_B1_D2	-	37B	X12-10
FPGA_B1_D3	-	38A	X14-10
FPGA_B1_D4	-	38B	X13-10
FPGA_B1_D5	-	39A	X15-10
FPGA_B1_E1	-	40A	X16-10
FPGA_B1_E2	-	40B	X10-11
FPGA_B1_E3	-	41A	X17-10
FPGA_B1_E4	-	41B	X11-11
FPGA_B1_E5	-	42B	X12-11
FPGA_B1_F3	-	43A	X14-11
FPGA_B1_F5	-	43B	X13-11
FPGA_B1_G4	-	44A	X15-11
FPGA_B1_H1	-	45A	X16-11
FPGA_B1_H6	-	45B	X10-12
FPGA_B1_J1	-	46A	X17-11
FPGA_B1_J2	-	46B	X11-12
FPGA_B1_J4	-	48A	X14-12
FPGA_B1_J6	-	49A	X15-12
FPGA_B1_K1	-	50A	X16-12
FPGA_B1_K2	-	50B	X10-14
FPGA_B1_K4	-	51A	X17-12
FPGA_B1_K5	-	51B	X11-14
FPGA_B1_L1	-	52B	X12-14
FPGA_B1_L2	-	53A	X14-14
FPGA_B1_L3	-	53B	X13-14
FPGA_B1_L4	-	54A	X15-14
FPGA_B1_M1	-	55A	X16-14
FPGA_B1_M2	-	55B	X10-15

FPGA_B1_M3	-	56A	X17-14
FPGA_B1_M4	-	56B	X11-15
FPGA_B1_N1	-	57B	X12-15
FPGA_B1_N2	-	58A	X14-15
FPGA_B1_N3	-	58B	X13-15
FPGA_B1_N4	-	59A	X15-15
FPGA_B1_P1	-	60A	X16-15
FPGA_B1_P2	-	60B	X10-16
FPGA_B1_P3	-	61B	X11-16
FPGA_B2_C11	-	8B	X13-2
FPGA_B2_D8	-	9A	X15-2
FPGA_B2_G11	-	10A	X16-2
FPGA_B2_F10	-	10B	X10-4
FPGA_B2_G10	-	11A	X17-2
FPGA_B2_F9	-	11B	X11-4
FPGA_B2_D11	-	12B	X12-4
FPGA_B2_B11	-	13A	X14-4
FPGA_B2_D10	-	13B	X13-4
FPGA_B2_A11	-	14A	X15-4
FPGA_B2_B9	-	15A	X16-4
FPGA_B2_B10	-	15B	X10-5
FPGA_B2_A9	-	16A	X17-4
FPGA_B2_A10	-	16B	X11-5
FPGA_B2_B8	-	17B	X12-5
FPGA_B2_F8	-	18A	X14-5
FPGA_B2_A8	-	18B	X13-5
FPGA_B2_F7	-	19A	X15-5
FPGA_B2_A7	-	20A	X16-5
FPGA_B2_G7	-	20B	X10-6
FPGA_B2_B7	-	21A	X17-5
FPGA_B2_G6	-	21B	X11-6
FPGA_B2_F6	-	22B	X12-6
FPGA_B2_D6	-	23A	X14-6
FPGA_B2_E6	-	23B	X13-6
FPGA_B2_C6	-	24A	X15-6
FPGA_B2_A6	-	25A	X16-6
FPGA_B2_C5	-	25B	X10-7

FPGA_B2_B6	-	26A	X17-6
FPGA_B2_C4	-	26B	X11-7
FPGA_B2_A5	-	27B	X12-7
FPGA_B2_A4	-	28A	X14-7
FPGA_B2_B5	-	28B	X13-7
FPGA_B2_B4	-	29A	X15-7
FPGA_B2_A3	-	30A	X16-7
FPGA_B2_D9	-	30B	X10-9
FPGA_B2_B3	-	31A	X17-7
FPGA_B2_A12	-	63C	X5-16
FPGA_B2_B12	-	64C	X7-16
FPGA_B2_A14	-	65C	X8-16
FPGA_B2_C12	-	65D	X9-16
FPGA_B2_B14	-	66C	X2-17
FPGA_B2_C13	-	66D	X3-17
FPGA_B2_A13	-	67D	X4-17
FPGA_B2_B13	-	68C	X5-17
FPGA_B2_A12	-	68D	X6-17
FPGA_B3_C14	-	69C	X7-17
FPGA_B3_C15	-	70C	X8-17
FPGA_B3_C16	-	70D	X9-17
FPGA_B3_D13	-	71C	X2-19
FPGA_B3_D14	-	71D	X3-19
FPGA_B3_D15	-	72D	X4-19
FPGA_B3_D16	-	73C	X5-19
FPGA_B3_E13	-	73D	X6-19
FPGA_B3_E14	-	74C	X7-19
FPGA_B3_E15	-	75C	X8-17
FPGA_B3_E16	-	75D	X9-19
FPGA_B3_F13	-	76C	X2-20
FPGA_B3_F14	-	76D	X3-20
FPGA_B3_F15	-	77D	X4-20
FPGA_B3_F16	-	78C	X5-20
FPGA_B3_G12	-	78D	X6-20
FPGA_B3_G13	-	79C	X7-20
FPGA_B3_G15	-	80C	X8-20
FPGA_B3_G16	-	80D	X9-20

FPGA_B3_H11	-	81C	X2-21
FPGA_B3_H12	-	81D	X3-21
FPGA_B3_H13	-	82D	X4-21
FPGA_B3_H15	-	83C	X5-21
FPGA_B3_J11	-	83D	X6-21
FPGA_B3_J12	-	84C	X7-21
FPGA_B3_J15	-	85C	X8-21
FPGA_B3_J16	-	85D	X9-21
FPGA_B3_K13	-	86C	X2-22
FPGA_B3_K15	-	86D	X3-22
FPGA_B3_K16	-	87D	X4-22
FPGA_B3_L12	-	88C	X5-22
FPGA_B3_L14	-	88D	X6-22
FPGA_B3_L15	-	89C	X7-22
FPGA_B3_L16	-	90C	X8-22
FPGA_B3_M12	-	90D	X9-22
FPGA_B3_M14	-	91C	X2-24
FPGA_B3_M15	-	91D	X3-24
FPGA_B3_M16	-	92D	X4-24
FPGA_B3_N12	-	93C	X5-24
FPGA_B3_N15	-	93D	X6-24
FPGA_B3_N16	-	94C	X7-24
FPGA_B3_P14	-	95C	X8-24
FPGA_B3_P15	-	95D	X9-24
FPGA_B3_P16	-	96C	X2-25
FPGA_B4_K6	-	96D	X3-25
FPGA_B4_K7	-	97D	X4-25
FPGA_B4_N6	-	98C	X5-25
FPGA_B4_N7	-	98D	X6-25
FPGA_B4_P6	-	99C	X7-25
FPGA_B4_R6	-	100C	X8-25

Table 32: Pin Assignment FPGA Signals for the
phyCORE-MPC5200B tiny /Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
3V3	1C, 2C, 4C, 5C, 1D, 2D	1C, 2C, 4C, 5C, 1D, 2D	X2-1, X2-2, X3- 1, X3-2
VCC_SRAM	6D	6D	X6-2
VBAT	6C	6C	X6-1
GND	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 41B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 82C, 87C, 92C, 97C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D, 84D, 89D, 94D, 99D	2A, 7A, 12A, 17A, 22A, 27A, 32A, 37A, 42A, 47A, 52A, 57A, 62A, 67A, 72A, 77A, 82A, 87A, 92A, 97A, 4B, 9B, 14B, 19B, 24B, 29B, 34B, 39B, 44B, 49B, 54B, 59B, 64B, 69B, 74B, 79B, 84B, 89B, 94B, 99B, 3C, 7C, 12C, 17C, 22C, 27C, 32C, 37C, 42C, 47C, 52C, 57C, 62C, 67C, 72C, 77C, 82C, 87C, 92C, 97C, 3D, 9D, 14D, 19D, 24D, 29D, 34D, 39D, 44D, 49D, 54D, 59D, 64D, 69D, 74D, 79D, 84D, 89D, 94D, 99D	X2-3, X2-8, X2- 13, X2-18, X2- 23 X3-3, X3-8, X3-13, X3-18, X3-23 X4-3, X4-8, X4-13, X4-18, X4-23 X5-3, X5-8, X- 13, X5-18, X5- 23 X6-3, X6-8, X6-13, X6-18, X6-23 X7-3, X7-8, X7-13, X7-18, X7-23 X8-3, X8-8, X8- 13, X8-18, X8- 23 X9-3, X9-8, X9-13, X9-18, X9-23, X10-3, X10-8, X10-13, X10-18, X10-23 X11-3, X11-8, X11-13, X11- 18, X11-23 X12-3, X12-8, X12-13, X12- 18, X12-23 X13-3, X13-8, X-13, X13-18, X13-23 X14-3, X14-8, X14-13, X14-18, X14-23 X15-3, X15-8,

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Table 33: Pin Assignment Power Supply for the phyCORE-MPC5200B tiny / Carrier Board / Expansion Board

Signal	phyCORE Module	Expansion Bus	Patch Field
N.C.	4D, 5D, 1A, 100D	50A, 51A, 53A, 54A, 55A, 56A, 58A, 59A, 60A, 61A, 63A, 64A, 65A, 66A, 68A, 69A, 70A, 71A, 73A, 74A, 75A, 76A, 78A, 79A, 80A 51B, 53B, 54B, 55B, 56B, 58B, 59B, 60B, 61B, 63B, 64B, 65B, 66B, 68B, 69B, 70B, 71B, 73B, 74B, 75B, 76B, 78B, 79B, 80B 51C, 53C, 54C, 55C, 56C, 58C, 59C, 60C, 61C, 63C, 64C, 65C, 66C, 68C, 69C, 70C, 71C, 73C, 74C, 75C, 76C, 78C, 79C, 80C 4D, 5D, 7D, 8D, 51D, 53D, 54D, 55D, 56D, 58D, 59D, 60D, 61D, 63D, 64D, 65D, 66D, 68D, 69D, 70D, 71D, 73D, 74D, 75D, 76D, 78D, 79D, 80D	18A, 19A, 20A, 21A, 22A, 23A 24A, 25A, 26A, 27A, 45A, 46A, 47A, 48A, 49A, 50A, 51A, 52A, 53A, 54A 17B, 18B, 19B, 20B, 21B, 22B, 23B, 24B, 25B, 26B, 27B, 45B, 46B, 47B, 48B, 49B, 50B, 51B, 52B, 53B, 54B 20C, 21C, 25C, 26C, 47C, 48C, 52C, 53C 17D, 18D, 22D, 23D, 27D, 44D 45D, 49D, 50D, 54D 18E, 19E, 20E, 21E, 22E, 23E, 24E, 25E, 26E, 27E, 45E, 46E, 47E, 48E, 49E, 50E, 51E, 52E, 53E, 54E 17F, 18F, 19F, 20F, 21F, 22F, 23F, 24F, 25F, 26F, 27F, 44F, 45F, 46F, 47F, 48F, 49F, 50F, 51F, 52F, 53F, 54F

Table 34: Unused Pins on the phyCORE-MPC5200B tiny /
Carrier Board / Expansion Board

14.3.16 Gold CAP Connector C119

The mounting space C119 (see *PCB stencil*) is provided for connection of a gold cap that buffers the RTC on the phyCORE-MPC5200B tiny. In the event of a VCC operating voltage failure the RTC is automatically supplied with power from the connected gold cap. The optional gold cap required for the RTC is available through PHYTEC (order code CG-002).

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A Appendix

A.1 Release Notes

The following section contains information about deviations to the description in this manual. Revisions to previous manuals are also listed.

Date	Version numbers	Changes in this manual
18-Jan-2006	Manual L-678e_0 PCM-030 PCB# 1245.0 PCM-997-V2 PCB# 1179.5/6	First draft, Preliminary documentation. phyCORE-MPC5200B tiny in "Prototype" state
05-Sep-2006	Manual L-678e_1 PCM-030 PCB# 1245.1 PCM-997-V2 PCB# 1179.5	Second draft, Preliminary documentation. phyCORE-MPC5200B tiny in "Prototype" state New Ethernet signals added. New U-Boot section started, still under construction.
06-Dec-2006	Manual L-678e_2 PCM-030 PCB# 1245.1 PCM-997-V2 PCB# 1179.5	First Release U-Boot section finished.
26-September-2007	Manual L-678e_3 PCM-030 PCB# 1245.2 PCM-973 PCB# 1260.1	Second Release Development Board Section changed to new Board

Document: phyCORE-MPC5200B tiny
Document number: L-678e_3, June 2007

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