TI-DM3730-EM CORE BOARD

User Manual

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Catalogue

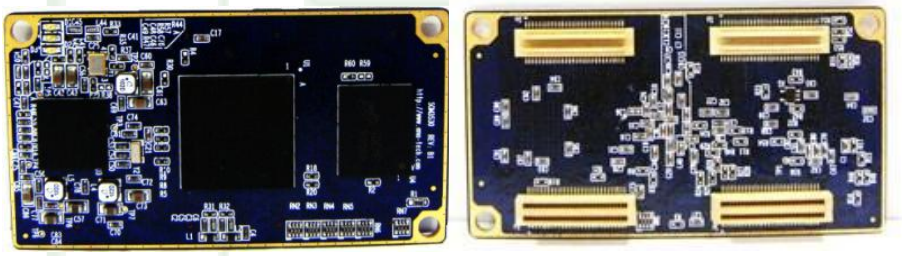
1 Introduction

1.1 Product Overview

The SOM35x module based on TI's OMAP35x processor family is a compact, product-ready hardware and software solution that fast forwards embedded designs. The SOM35x provides high-performance and low-power within tight space constraints for applications. SOM35x support Linux-2.6.31、WinCE6.0、Android and other embedded operating system. SOM35x provides a mass of software resources such as DVSDK, OpenGL ES2.0, OGRE and etc.

The SOM35x is an off-the-shelf solution that reduces development risks associated with the complex design and manufacturing details of the OMAP3 processor, that Speed Time-to-Market.

The compact SOM35x is an ideal off-the-shelf solution for applications that include medical devices, barcode readers, mobile Internet devices, Image Capture Machine, GPS and 3D Game machine. The SOM35x allows for powerful versatility, compact designs, and long-life products.



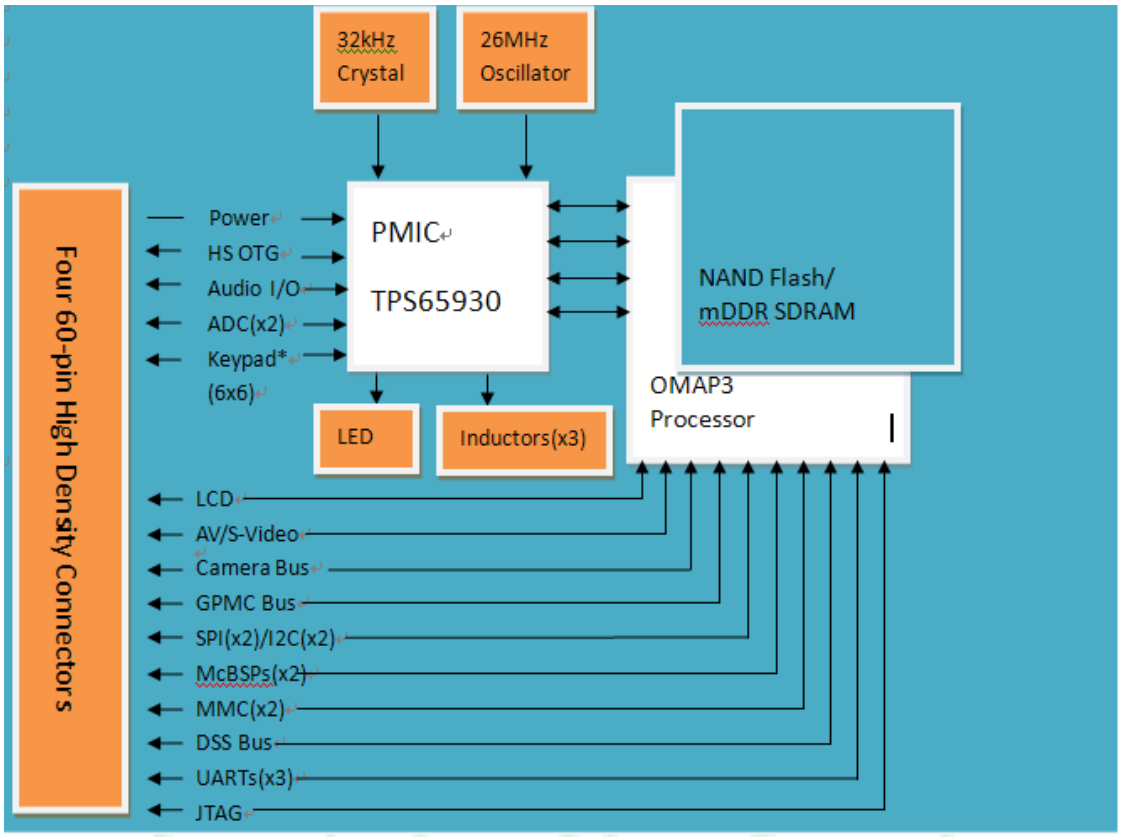
Picture 1.1 TI-DM3730-EM CORE BOARD

1.2 Acronyms

ADC	Analog to Digital Converter
BSP	Board Support Package
BTB	Board-to-board
DDR	Double Data Rate (RAM)
DMA	Direct Memory Access

ESD	Electrostatic Discharge
FIFO	First In First Out
GPIO	General Purpose Input Output
GPMC	General Purpose Memory Controller
GPO	General Purpose Output
IC	Integrated Circuit
I/O	Input/Output
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LDO	Low Dropout (Regulator)
McBSP	Multi-channel Buffered Serial port
PCB	Printed Circuit Board
PCMCIA	Personal Computer Memory Card International Association (PC Cards)
PHY	Physical Layer
PLL	Phase lock loop
PWM	Pulse Width Modulation
RTC	Real Time Clock
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SOM	System on Module
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
STN	Super-Twisted Nematic(LCD)
TFT	Thin Film Transistor(LCD)
TI	Texas Instruments
TSC	Touch Screen Controller
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit

1.3 TI-DM3730-EM CORE BOARD Block diagram



Picture 1.2 TI-DM3730-EM CORE BOARD Block diagram

2 Electrical Specification

2.1 Hardware

Processor	TI OMAP3530	ARM Cortex-A8 Core up to 720MHz NEON™ SIMD Co-processor 430MHz TMS320C64x+ DSP POWERVR SG™ 2D/3D graphic Acceleration
RAM	128MByte/256MByte/512MByte DDR	
Flash	256MByte/512MByte/1GByte Nand Flash	
LED	1x Power LED	
	2x Programmable LED	
SOM interface	4x 0.5mm 60Pin B2B interface	
Interface resource	1x OMAP3 GPMC 总线（full signal output）	

	1x OMAP3 DSS bus（full signal output）
	1x AV/S-Video output
	1x Camera bus（full signal output）
	2x SPI bus（1 route multiplex with 1 route HSUSB）
	3x 4 cable UART（RX、TX、CTS、RTS）
	2x MCBSP bus（1 route multiplex with 2 route UART）
	2x MMC bus（full signal output）
	1x HSUSB OTG
	2x HSUSB ULPI bus（full signal output）
	2x I2C bus
	1x OneWire bus
	1x TI standard JTAG
	1x stereo headphone output（Dual Channel）
	1x Mono Channel microphone input
	1x Mono Channel Audio output
	6x extra GPIO（Power Management IC derivation，include 2 route PWM）
	2x ADC input
	5x boot selection signal
	5x Power management signal(2 route system Reset ;1 route rouse ;2 route external power control)
	6x6 matrix scanning keyboard

2.2 Operating conditions

Condition	Minimum	Normal	Maximum
Power supply	3.3V 80mA（*1）	3.3V 200mA（*2）	3.3V 500mA（*3）
Power Consumption	264mW（*1）	660mW（*2）	1650mW（*3）
Temperature(Commercial)	0℃	/	70℃
Temperature(Industrial)	-40℃	/	80℃

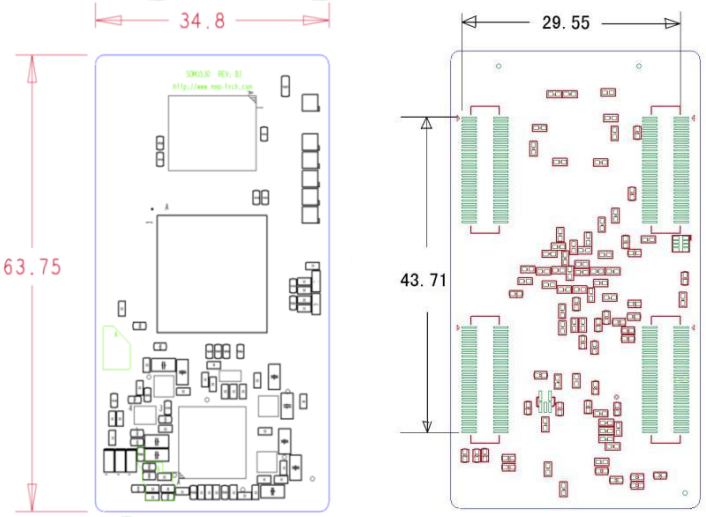
*1、Power Consumption Condition：SOM53x work in a low power consumption state and cut down all external power supply.

*2：Power Consumption Condition：SOM53x work in high speed and all the external power supply network normally (supply current is the half of the maximum value)

*3：Power Consumption Condition：SOM53x work in maximum speed and the external power supply in maximum current speed.

2.3 Mechanical data

Primary Purpose	OMAP35XSystem on Module
PCB size	1.37 x 2.51 inch（34.8 x 63.75mm）
Set hole	3



picture2.1 TI-DM3730-EM CORE BOARD PCB size diagram

2.4 Processor

2.4.1 OMAP35x Processor

The TI-DM3730-EM CORE BOARD uses TI's high-performance OMAP35x Applications Processor. This device features the Superscalar ARM® Cortex™-A8 RISC core and provides many integrated on-chip peripherals, including:

- Superscalar ARM ® Cortex™- A8 RISC core
  - Vectored floating point unit
  - 16 Kbytes instruction L1 cache
  - 16 Kbytes data L1 cache
  - 64 Kbyte RAM
  - 32Kbyte ROM
- Integrated LCD Controller
- 3 UART
- I2S codec interface
- One high-speed USB 2.0 On-the-Go(OTG) interface and one high-speed USB 2.0 host interface
- Many general purpose I/O GPIO signals
- Programmable timers
- Real time clock (RTC)
- Low power modes

See TI's OMAP35x TRM and Data Sheet for additional information; the documents are available from TI's website.

2.4.2 OMAP35x Processor Block Diagram

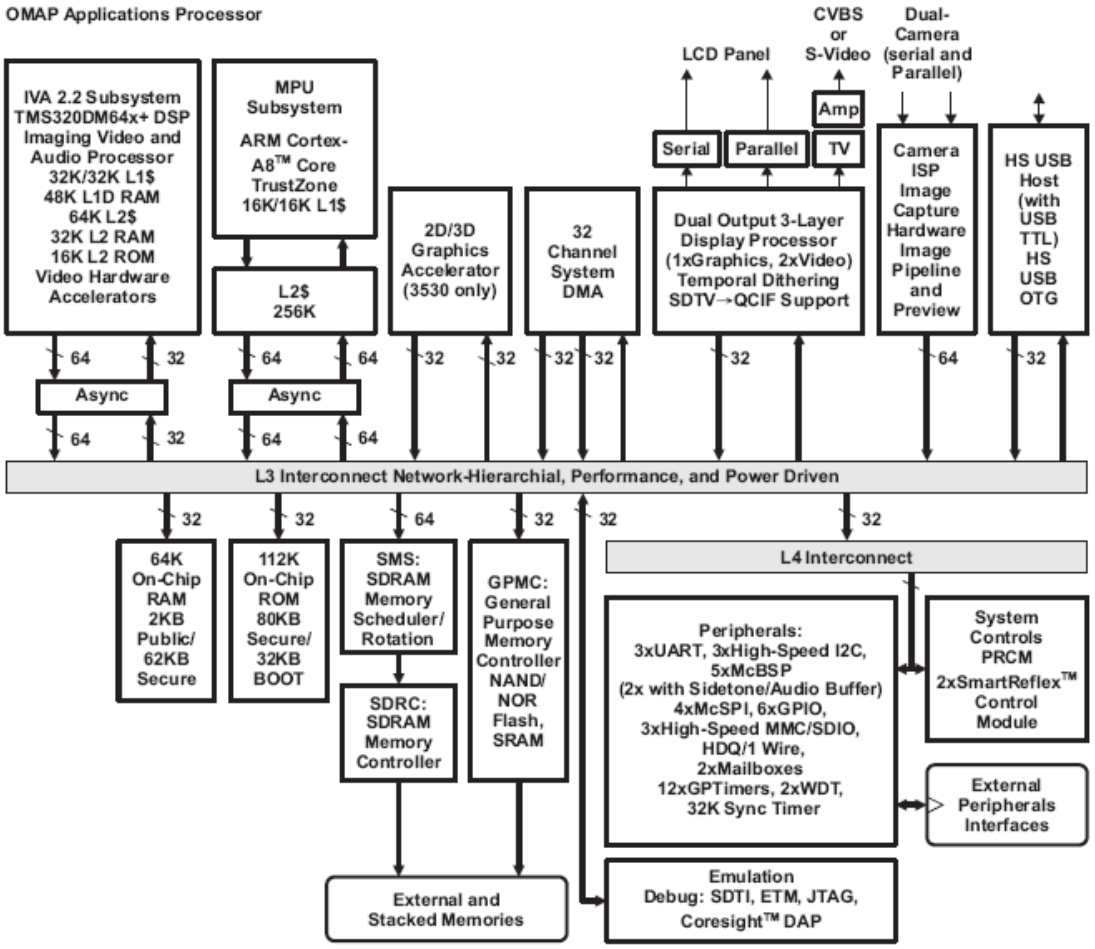


Figure 2.1：OMAP35x Processor Block Diagram

NOTE: The block diagram pictured above comes from TI's OMAP3530/25 Applications Processor Data Sheet.

2.5 Clocks

The OMAP35x requires an oscillator and crystal to enable proper internal timing. A 26.000 MHz oscillator is used to generate many of the processor's internal clocks via a series of Phase Lock Loops (PLLs) and signal dividers. To generate the core CPU clock, the 26.000 MHz signal is run through a Digital PLL controlled by the PRCM registers. Divisors are used to divide down the internal bus frequency to set the LCD, memory controller, camera interface, etc.

The second required crystal runs at 32.768 kHz and is connected directly to the TPS65950. The 32.768 kHz clock is used for PMIC and CPU start up and as a reference clock for the Real

Time Clock (RTC) Module.

The CPU's microcontroller core clock speed is initialized by software on the Torpedo SOM. The DDR SDRAM bus speed is set at 166 MHz in LogicLoader. Other clock speeds, such as core speed and specific serial baud rates, can be supported and modified in software for specific user applications.

The TI-DM3730-EM CORE BOARD provides an external bus clock, uP_BUS_CLK. This clock is driven by the

GPMC_CLK pin.

OMAP35x Microcontroller Signal Name	TI-DM3730-EM CORE BOARD Net Name	Default Software Value in X-Loader
CORE	N/A	Up to 600 MHz
SDRC_CLK	N/A	166 MHz
GPMC_CLK	uP_BUS_CLK	Not configured

IMPORTANT NOTE: Please see TI's OMAP35x TRM for additional information about processor clocking.

2.6 Memory

2.6.1 Mobile DDR and NAND

The OMAP35x uses a 32-bit memory bus to interface to mobile DDR SDRAM and a 16-bit memory bus to interface to NAND. At the time of publication, it can be ordered in three density options：

- 128 MB Mobile DDR and 128 MB NAND
- 256MB Mobile DDR and 256 MB NAND
- 512MB Mobile DDR and 512 MB NAND

In TI-DM3730-EM CORE BOARD , the default memory configuration is designated as 256MB Mobile DDR

and 256MB NAND.

2.6.2 External Memory

It is possible to expand the system's non-volatile storage capability by adding external flash ICs, SD memory, Compact Flash, or NAND flash.

2.7 Audio Codec

The OMAP35x processor has multiple Multi-channel Buffered Serial Port (McBSP) interfaces that support PCM and I2S formats. Both PCM and I2S serial paths drive the built-in TPS65950 audio codec. From the TPS65950, the outputs are CODEC_OUTL and CODEC_OUTR; these signals are available from the expansion connectors.

The codec in the TPS65950 performs up to full-duplex codec functions and supports variable sample rates from 8–96k samples per second.

2.8 Display Interface

The OMAP35x has a built-in LCD controller supporting STN, color STN, and TFT panels at a resolution of up to XGA 1024 x 768 x 24-bit color. See TI's OMAP35x TRM for further information on the integrated LCD controller. The signals from the OMAP35x LCD controller are organized by bit and color and can be interfaced through the expansion connectors.
PardazeshSabz provide 4.3-inch (resolution is 480x272) and 7-inch (resolution is 800x480) TFT touch screen panel.

IMPORTANT NOTE: Using the internal graphics controller will affect processor performance. Selecting display resolutions and color bits per pixel will vary processor busload.

2.9 Serial Interfaces

The TI-DM3730-EM CORE BOARD comes with the following serial channels :

UART1, UART2, UART3, three SPI ports, two MCBSP, and two I2C ports. If additional serial channels are required, please contact PardazeshSabz. Please see TI-DM3730-EM User Manual for further information regarding serial communications.

2.9.1 UART1

UART1 has been configured as the main SOM35x serial port based on the processor. It is an asynchronous 16C750-compatible UART. This UART provides a high-speed serial interface that uses 64 byte First In / First Out (FIFO) and is capable of sending and receiving serial data simultaneously. The signals from the Torpedo SOM are 1.8V Transistor-Transistor Logic (TTL) level signals, not RS232 level signals. The end-product design must provide an external RS232 transceiver for RS232 applications. When choosing an RS232 transceiver, the designer should keep in mind cost, availability, ESD protection, and data rates. The UARTA baud rate is set to a default 115.2 Kbits/sec, though it supports most common serial baud rates.

2.9.2 UART2

Serial Port UART3 is an asynchronous 16C750-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously.

The signals from the Torpedo SOM are 1.8V TTL level signals, not RS232 level signals. The UART2 baud rate can also be set to most common serial baud rates.

2.9.3 UART3

Serial port UART3 is an asynchronous 16C750-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the TI-DM3730-EM CORE BOARD are 1.8V TTL level signals, not RS232 level signals . The UARTC baud rate can also be set to most common serial baud rates.

2.9.4 MsSPI

The Torpedo SOM provides three external SPI ports with multiple chip selects. Additional SPI ports are available through different resistor populations. Please see Table 5.1 for more information.

2.9.5 I2C

The TI-DM3730-EM CORE BOARD supports two dedicated external I2C ports. The clock and data signals for the I2C2 port have 4.7K ohm pull-up resistors; the clock and data signals for the I2C3 port have
470 ohm pull-up resistors. Please see TI's OMAP35x TRM for further information.

2.9.6 Reserved I2C Addresses

The OMAP35x Torpedo SOM contains a product ID chip that connects to the I2C bus. PardazeshSabz software uses this product ID chip to determine hardware version information. As a result, the 7-bit I2C addresses listed below are used by the product ID chip and must be avoided in custom designs:

101 1000

101 1001

101 1010

101 1011

101 1100

101 1101

2.10 USB Interface

The TI-DM3730-EM CORE BOARD supports one USB 2.0 OTG port, which can function as a host or device/client. The port can operate at up to 480 Mbit/sec. For more information on using the OTG

interfaces, please see TI's OMAP35x TRM.

IMPORTANT NOTE: In order to correctly implement USB on the SOM3530-B2, additional impedance matching circuitry may be required on the USB2_D+ and USB2_D- signals before they can be used. USB 2.0 requirements specify the signals must be routed as differential pairs with 90 ohm differential impedance. Refer to the USB 2.0 Specification for detailed information.

2.11 GPIO

PardazsehSabz designed the TI-DM3730-EM CORE BOARD to be flexible and provide multiple options for analog and digital GPIO. There are numerous digital GPIO pins on the Torpedo SOM that interface to the OMAP35x processor and TPS65930 PMIC; see Section 5 –Pin Descriptions & Functions‖ for more information. If certain peripherals are not desired, such as the LCD controller, chip selects, IRQs, or UARTs, then more GPIO pins become available.

2.12 Expansion/Feature Options

The TI-DM3730-EM CORE BOARD was designed for expansion and a variable feature set, providing all the necessary control signals and bus signals to expand the user's design. It is possible for a user to expand the TI-DM3730-EM CORE BOARD 's functionality even further by adding host bus or ISA bus devices. Some features that are implemented on the OMAP35x, but are not discussed herein, include: RTC, pulse width modulation (PWM), Secure Digital, MMC cards, SDIO cards, graphics accelerator, DSP codecs, Image Processing Unit, 1wire interface, and the debug module.

3 System Integration

3.1 Configuration

OMAP35x TI-DM3730-EM CORE BOARD was designed to meet multiple applications for users with specific design and budget requirements. As a result, this TI-DM3730-EM CORE BOARD supports a variety of embedded operating systems and hardware configurations. Please contact PardazeshSabz Sales for additional hardware configurations to meet your application needs.

3.2 Reset

TI-DM3730-EM CORE BOARD has a reset input (SYS_nRESPWRON) and a reset output (SYS_nRESWARM).External devices can drive MSTR_nRST low to assert reset to the product.TI-DM3730-EM CORE BOARD uses SYS_nRESWARM to indicate to other devices that the Torpedo SOM is in reset.

3.2.1 Master Reset（SYS_nRESPWRON）——Reset Input

TheMSTR_nRST triggers a power-on-reset event to the OMAP35x processor and resets the entire CPU.

IMPORTANT NOTE: MSTR_nRST does not reset the TPS65930; the TPS65930 is only reset by removing power from the SOM.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition.

Low Pulse on SYS_nRESPWRON Signal：

A low pulse on the MSTR_nRST signal, asserted by an external source（for example, the reset button on the custom design application), will bring SYS_nRESPWRON low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external

SYS_nRESPWRON signal source, so the custom design must ensure that the assertion time is sufficient for all related.

3.2.2 TI-DM3730-EM CORE BOARD Reset（SYS_nRESWARM）——Reset output

All hardware peripherals should connect their hardware-reset pin to the SYS_nRESWARM signal on the expansion connector. Internally, all Torpedo SOM peripheral hardware reset pins areconnected to the SYS_nRESWARM net.

3.3 Interrupts

The OMAP35x incorporates the ARM Cortex-A8 interrupt controller which provides many intersystem. Most external GPIO signals can also be configured as interrupt inputs by configuring their pin control registers. PardazeshSabz BSP's setup and process all onboard systern and external TI-DM3730-EM CORE BOARD interrupt sources. Refer to TI's OMAP35x TRM for further information on using interrupts.

3.4 JTAG Debugger Interface

The JTAG connection on the OMAP35x allows recovery of corrupted flash memory, real-time application debug, and DSP development. There are several third-party JTAG debuggers available for TI microcontrollers. The following signals make up the JTAG interface to the OMAP35x processor: TDI, TMS, TCK, TDO, nTRST, RTCK, EMU0, and EMU1.

When laying out the 20-pin connector, realize that it may not be numbered as a standard 20-pin 0.1‖ insulation displacement connector (IDC) through-hole connector. Each JTAG tool vendor may define the 20-pin IDC connector pin-out differently.

3.5 Power Management

3.5.1 System Power Supplies

In order to ensure a flexible design, the Torpedo SOM has the following power areas: VDD_SOM and VDD_RTC。All power areas are inputs to the TI-DM3730-EM CORE BOARD 。The module

also provides VIO_1V8 as a reference voltage. It may be used to supply up to 200 mA of power, but it is recommended to use an external supply.

1) VDD_SOM

The VDD_SOM input is the main source of power for the TI-DM3730-EM CORE BOARD . This input expects a voltage within typical single lithium-ion battery limits which generally operate from 2.7V to

4.2V. If a lithium-ion battery is not used as the main power source, it is recommended to supply a fixed 3.3 V supply. The TPS65930 power management controller takes the VDD_SOM rail input and creates all onboard voltages. If the design is required to maintain RAM contents in a critical power situation (e.g., low battery, loss of power), the VDD_SOM supply should be maintained above the minimum level at all costs. we suggest using the Standby mode to prepare the system for a critical power condition. In this way, the DDR SDRAM is placed into self-refresh and the processor is placed into the Standby state.

2) VDD_RTC

The VDD_RTC power rail for power supply board TPS65930。Power management state machine, and RTC circuit when VDD_SOM is not present. A lithium-ion coin cell typically supplies power to this rail. The TPS65930 overrides this input when VDD_SOM is applied.

3.5.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power

supply selection (efficiency), clocking design, IC and component selection, etc.

On the OMAP35x there are many different software configurations that drastically affect power consumption: microcontroller core clock frequency, bus clock frequency, peripheral clocks, bus modes, power management states; peripheral power states and modes; product user scenarios; interrupt handling; and display settings (resolution, backlight, refresh, bits per pixel, etc). These settings are typically initialized in the startup software routines and may be modified later in the operating system and application software.

T2_REGEN is an open drain output from the TPS65930. It can be used to control power for external power ICs or LDOs. Please see the TPS65930 TRM for more information.

3.5.3 Microcontroller

The OMAP35x processor's power management scheme was designed for the cellular handset market, which means the static and dynamic power consumption has very flexible controls allowing designers to tweak the processor to minimize end-product power consumption.

1) Run State

The OMAP35x can enter Run mode from any state. A Standby-to-Run transition occurs on any valid wakeup event, such as the assertion or any enabled interrupt signal. All required power supplies are active in this state.

2) Suspend State

Suspend is the hardware power-down state for the SOM.,allowing for lower power consumption. The Suspend state is designed to reduce power consumption while the OMAP35x is waiting for an event, such as a keyboard input. In BSPs, All power supplies remain active and system context is retained. An internal or external wakeup event can cause the processor to transition back to Run mode.

3) Standby State

Standby is the lowest power state for the SOM. This state is entered in ParcazeshSabz BSPs through software commands. The OMAP35x processor is put into the lowest power state and all clocks are

stopped. The VDD_SOM power rail should be maintained if the low-power DDR SDRAM contents wish to be retained. Internal or external wakeup events can cause a return to the Run state.

3.6 Boot Modes

The OMAP35x provides the option of booting from multiple sources. The boot mode is controlled by the SYS_BOOT pins of the processor. SYS_BOOT0 and SYS_BOOT5 are available off-board through the expansion connectors.

OMAP35x Processor Pins	Boot Method
Default SYS_BOOT[6:0]=1101111	USB, UART3, MMC1, NAND
Alternate SYS_BOOT[6:0]=1001111	NAND, USB, UART3, MMC1
Alternate SYS_BOOT[6:0]=1001110	XIPwait, DOC, USB, UART3, MMC1
Alternate SYS_BOOT[6:0]=1000110	MMC1 USB

3.7 ESD Considerations

The TI-DM3730-EM CORE BOARD was designed to interface to a customer's peoard, while remaining low cost and adaptable to many different applications. The TI-DM3730-EM CORE BOARD does not provide any onboard ESD protection circuitry—this must be provided by the product it is used in.

4 Memory & I/O Mapping

On the OMAP35x microcontroller, all address mapping for the GPMC chip select signals is listed below. Mapped –Chip Select‖ signals for the OMAP are available as outputs from the microcontroller and are assigned as follows:

Chip select	Device/Feature	Notes
nCS0	uP_nCS0	For NandFlash
nCS1	uP_nCS1	Non Available
nCS2	uP_nCS2	Non Available
nCS3	uP_nCS3	Available for use by an off-board external
nCS4	uP_nCS4	Available for use by an off-board external
nCS5	uP_nCS5	Available for use by an off-board external
nCS6	uP_nCS6	Available for use by an off-board external
nCS7	uP_nCS7	Available for use by an off-board external

NOTE：Memory addresses for chip selects on the OMAP35x are configurable by software; Therefore , precise address locations cannot be provided.

5 Connector description and function

IMPORTANT NOTE：The following pin descriptions and states are provided by the default pin usage. the signal of defined in the connection table ,lots of that can be configured as input or output—---- Most of the OMAP35x processors can be configured as GPIO input or output of other ------- and have different functions。It is essential to review the final design (including electrical and software) all the signals, to verify the necessary configuration（external pull-ups/pull-downs）.

IMPORTANT NOTE：Please pay special attention to the reference voltage of the OMAP35x used to power each signal in the table below, especially when used as a GPIO. Not all power rails coming out of the TPS65930 are on by default and may need to be enabled through software.

5.1 Connector Descriptions

Connector list

Connector No.	Connector description	Remark
J1	SOM connector	0.5mm 60Pin B2B Male
J2	SOM connector	0.5mm 60Pin B2B Female
J3	SOM connector	0.5mm 60Pin B2B Male
J4	SOM connector	0.5mm 60Pin B2B Female

LED list

LED No.	LED description	Remark
D1	Programmable LED	T2.LEDB
D2	Programmable LED	T2.LEDA
D3	Power LED	

Power List

Power network	Voltage	Max	Direction	Remark
VDD_SOM	3.3V	1A	Input	Power Input of SOM35x
VDD_IO	1.8V	500mA	Output	I/O reference voltage output
VDD_MMC1	1.8V/3V	220mA	Output	MMC1 power output
VBUS_HSUSB0	5V	100mA	Output	USB OTG power output
VDD_RTC	3V		Input	RTC battery input
VDD_AUX2	1.8V	100mA	Output	Controllable 1.8V power output

Test Point list

Label	circuit	Key
TP1	T2.HFCLKOUT	1.8V 26MHz
TP2	VDD_MPU	1.2V
TP3	VDD_PLL	1.8V
TP4	VDD_DAC	1.8V
TP5	VDD_MMC1	3V
TP6	VDD_AUX2	1.8V
TP7	VDD_CORE	1.2V
TP8	VDD_IO	1.8V

5.2 Pin Descriptions & Functions

J1 Connector Pin Descriptions

Pin	Signal Name	GPIO No.	I/O Voltage	Remark
1	GND	/	/	Ground
3	GPMC_A 10	43	1.8V	
5	GPMC_A9	42	1.8V	
7	GPMC_A8	41	1.8V	
9	GPMC_A7	40	1.8V	
11	GPMC_A6	39	1.8V	
13	GPMC_A5	38	1.8V	
15	GPMC_A4	37	1.8V	
17	GPMC_A3	36	1.8V	
19	GPMC_A2	35	1.8V	
21	GPMC_A1	34	1.8V	
23	GND	/	/	Ground
25	GPMC_D0	/	1.8V	
27	GPMC_D1	/	1.8V	
29	GPMC_D2	/	1.8V	
31	GPMC_D3	/	1.8V	
33	GPMC_D4	/	1.8V	
35	GPMC_D5	/	1.8V	
37	GPMC_D6	/	1.8V	
39	GPMC_D7	/	1.8V	
41	GPMC_D8	44	1.8V	
43	GPMC_D9	45	1.8V	
45	GPMC_D10	46	1.8V	
47	GPMC_D11	47	1.8V	
49	GPMC_D12	48	1.8V	

51	GPMC_D13	49	1.8V	
53	GPMC_D14	50	1.8V	
55	GPMC_D15	51	1.8V	
57	GND	/	/	Ground
59	GND	/	/	Ground
Pin	**Signal Name**	**GPIO No.**	**I/O Voltage**	**Remark**
2	GND	/	/	Ground
4	GPMC_nWE	/	1.8V	
6	GPMC_nOE	/	1.8V	
8	GPMC_nCS3	54	1.8V	
10	GPMC_nCS4	55	1.8V	
12	GPMC_nCS5	56	1.8V	
14	GPMC_nCS6	57	1.8V	
16	GPMC_nCS7	58	1.8V	
18	GPMC_nBE0_CLE	60	1.8V	
20	GPMC_nBE1	61	1.8V	
22	GPMC_nADV_ALE	/	1.8V	
24	GPMC_nWP	62	1.8V	
26	GPMC_WAIT3	65	1.8V	
28	GPMC_CLK	59	1.8V	
30	GND	/	/	Ground
32	MCSPI1_CLK	171	1.8V	
34	MCSPI1_SIMO	172	1.8V	
36	MCSPI1_SOMI	173	1.8V	
38	MCSPI1_CS0	174	1.8V	
40	MCBSP3_FSX/UART2_RX	143	1.8V	
42	MSBSP3_DX/UART2_CTS	140	1.8V	
44	MCBSP3_DR/UART2_RTS	141	1.8V	
46	MCBSP3_CLKX/UART2_TX	142	1.8V	
48	UART1_TX	148	1.8V	
50	UART1_RTS	149	1.8V	
52	UART1_CTS	150	1.8V	
54	UART1_EX	151	1.8V	
56	GND	/	/	Ground
58	SYS_CLKOUT1/GPIO10	10	1.8V	
60	SYS_CLKOUT2/GPIO186	186	1.8V	

J2 Connector Pin Description

Pin	Signal Name	GPIO No.	I/O Voltage	Remark
1	GND	/	/	Ground
3	DSS_VSYNC	68	1.8V	
5	DSS_HSYNC	67	1.8V	
7	DSS_ACBIAS	69	1.8V	
9	DSS_PCLK	66	1.8V	
11	GND	/	/	Ground
13	DSS_D23	93	1.8V	
15	DSS_D22	92	1.8V	
17	DSS_D21	91	1.8V	
19	DSS_D20	90	1.8V	
21	DSS_D19	89	1.8V	
23	DSS_D18	88	1.8V	
25	DSS_D17	87	1.8V	
27	DSS_D16	86	1.8V	
29	DSS_D15	85	1.8V	
31	DSS_D14	84	1.8V	
33	DSS_D13	83	1.8V	
35	DSS_D12	82	1.8V	
37	DSS_D11	81	1.8V	
39	DSS_D10	80	1.8V	
41	DSS_D9	79	1.8V	
43	DSS_D8	78	1.8V	
45	DSS_D7	77	1.8V	
47	DSS_D6	76	1.8V	
49	DSS_D5	75	1.8V	
51	DSS_D4	74	1.8V	
53	DSS_D3	73	1.8V	
55	DSS_D2	72	1.8V	
57	DSS_D1	71	1.8V	
59	DSS_D0	70	1.8V	
Pin	**Signal Name**	**GPIO No.**	**I/O Voltage**	**Remark**
2	GND	/	/	Ground
4	HDQ_SIO/GPIO170	170	1.8V	
6	UART3_CTS_RCTX	163	1.8V	
8	UART3_RTS_SD	164	1.8V	
10	UART3_RX_IRRX	165	1.8V	
12	UART3_TX_IRTX	166	1.8V	
14	GND	/	/	Ground

16	CAM_PCLK	97	1.8V	
18	CAM_HS	94	1.8V	
20	CAM_VS	95	1.8V	
22	CAM_XCLKA	96	1.8V	
24	CAM_XCLKB	111	1.8V	
26	CAM_FLD	98	1.8V	
28	CAM_WEN	167	1.8V	
30	CAM_STROBE	126	1.8V	
32	CAM_D0	99	1.8V	
34	CAM_D1	100	1.8V	
36	CAM_D2	101	1.8V	
38	CAM_D3	102	1.8V	
40	CAM_D4	103	1.8V	
42	CAM_D5	104	1.8V	
44	CAM_D6	105	1.8V	
46	CAM_D7	106	1.8V	
48	CAM_D8	107	1.8V	
50	CAM_D9	108	1.8V	
52	CAM_D10	109	1.8V	
54	CAM_D11	110	1.8V	
56	GND	/	/	Ground
58	AV/SVIDEO_Y	/	/	CVBS output/S-Video output Y channel
60	SVIDEO_C	/	/	S-Video output C channel

J3 Connector Pin Descriptions

Pin	Signal Name	GPIO No.	I/O Voltage	Remark
1	MMC2_DAT7	139	1.8V	
3	MMC2_DAT6	138	1.8V	
5	MMC2_DAT5	137	1.8V	
7	MMC2_DAT4	136	1.8V	
9	MMC2_DAT3	135	1.8V	
11	MMC2_DAT2	134	1.8V	
13	MMC2_DAT1	133	1.8V	
15	MMC2_DAT0	132	1.8V	
17	MMC2_CLK	130	1.8V	
19	MMC2_CMD	131	1.8V	
21	GND	/	/	Ground
23	HSUSB2_D7	178	1.8V	
25	HSUSB2_D6	181	1.8V	
27	HSUSB2_D5	180	1.8V	

29	HSUSB2_D4	179	1.8V	
31	HSUSB2_D3	182	1.8V	
33	HSUSB2_D2	177	1.8V	
35	HSUSB2_D1	29	1.8V	
37	HSUSB2_D0	28	1.8V	
39	HSUSB2_NXT	27	1.8V	
41	HSUSB2_DIR	26	1.8V	
43	HSUSB2_STP	25	1.8V	
45	HSUSB2_CLK	24	1.8V	
47	GND	/	/	Ground
49	PREDRIV.RIGHT	/	/	Right audio output
51	PREDRIV.LEFT	/	/	Left audio output
53	GND	/	/	Ground
55	GND	/	/	Ground
57	VDD_IO	/	/	1.8V IO output
59	VDD_IO	/	/	1.8V IO output

Pin	Signal Name	GPIO No.	I/O Voltage	Remark
2	HSUSB2_CLK/GPIO13	13	1.8V	
4	HSUSB2_STP/GPIO12	12	1.8V	
6	HSUSB2_DIR/SYS_DRM_MSECURE/GPIO22	22	1.8V	
8	HSUSB2_NXT/GPIO23	23	1.8V	
10	HSUSB2_D0/MCSPI3_SIMO/GPIO14	14	1.8V	
12	HSUSB2_D1/MCSPI3_SOMI/GPIO15	15	1.8V	
14	HSUSB2_D2/MCSPI3_CS0/GPIO16	16	1.8V	
16	HSUSB2_D3/GPIO21	21	1.8V	
18	HSUSB2_D4/GPIO18	18	1.8V	
20	HSUSB2_D5/GPIO19	19	1.8V	
22	HSUSB2_D6/GPIO20	20	1.8V	
24	HSUSB2_D7/MCSPI3_CLK/GPIO17	17	1.8V	
26	GND	/	/	Ground
28	SYS_nRESPWRON	/	1.8V	Power on signal
30	SYS_nRESWARM	/	1.8V	Warm reset signal
32	GND	/	/	Ground
34	T2.LEDSYNC/T2.GPIO.13	/	1.8V	
36	T2.PWR_ON	/	1.8V	POWERON signal
38	T2.REGEN	/	1.8V	REGEN signal
40	T2.SYSEN	/	1.8V	SYSEN signal

42	MICIN	/	/	Mic input
44	MICGND	/	/	Mic GND
46	AUXR	/	/	Audio Input
48	GND	/	/	Ground
50	T2.KPD_C0	/	1.8V	Square Scan Key C0
52	T2.KPD_C1	/	1.8V	Square Scan Key C 1
54	T2.KPD_C2	/	1.8V	Square Scan Key C 2
56	T2.KPD_C3	/	1.8V	Square Scan Key C 3
58	T2.KPD_C4	/	1.8V	Square Scan Key C 4
60	T2.KPD_C5	/	1.8V	Square Scan Key C 5

J4 Connector Pin Descriptions

Pin	Signal Name	GPIO No.	I/O Voltage	Remark
1	VDD_MMC1	/	/	MMC1 Power
3	MMC1_CMD	121	VDD_MMC1	
5	MMC1_CLK	120	VDD_MMC1	
7	MMC1_DAT0	122	VDD_MMC1	
9	MMC1_DAT1	123	VDD_MMC1	
11	MMC1_DAT2	124	VDD_MMC1	
13	MMC1_DAT3	125	VDD_MMC1	
15	MMC1_DAT4	126	VDD_MMC1	
17	MMC1_DAT5	127	VDD_MMC1	
19	MMC1_DAT6	128	VDD_MMC1	
21	MMC1_DAT7	129	VDD_MMC1	
23	T2.MMC1_CD/T2.GPIO0	/	1.8V	MMC1 check
25	GND	/	/	Ground
27	HSUSB0_ID	/	3V	USB OTG ID
29	HSUSB0_DN	/	3V	USB OTG DN
31	HSUSB0_DP	/	3V	USB OTG DP
33	VBUS_HSUSB0	/	/	USB OTG Power
35	T2.GPIO1	/	1.8V	
37	T2.GPIO2	/	1.8V	
39	T2.GPIO6/T2.PWM0	/	1.8V	
41	T2.GPIO7/T2.PWM1	/	1.8V	
43	T2.GPIO15	/	1.8V	
45	T2.ADCIN0	/	/	0V~1.5V
47	T2.ADCIN2	/	/	0V~2.5V
49	VDD_AUX2	/	/	
51	VDD_RTC	/	/	RTC Power Input
53	GND	/	/	Ground
55	GND	/	/	Ground

57	VDD_SOM	/	/	SOM Power Input
59	VDD_SOM	/	/	SOM Power Input
Pin	**Signal Name**	**GPIO No.**	**I/O Voltage**	**Remark**
2	MCBSP1_CLKR/GPIO156	156	1.8V	
4	MCBSP1_FSR/GPIO157	157	1.8V	
6	MCBSP1_DX/GPIO158	158	1.8V	
8	MCBSP1_DR/GPIO159	159	1.8V	
10	MCBSP1_FSX/GPIO161	161	1.8V	
12	MCBSP1_CLKX/GPIO162	162	1.8V	
14	SYS_BOOT5	7	1.8V	Don’t using as GPIO
16	SYS_BOOT4	6	1.8V	Don’t using as GPIO
18	SYS_BOOT3	5	1.8V	Don’t using as GPIO
20	SYS_BOOT2	4	1.8V	Don’t using as GPIO
22	SYS_BOOT1	3	1.8V	Don’t using as GPIO
24	SYS_BOOT0	2	1.8V	Don’t using as GPIO
26	I2C3_SCL	184	1.8V	
28	I2C3_SDA	185	1.8V	
30	I2C2_SCL	168	1.8V	
32	I2C2_SDA	183	1.8V	
34	JTAG_TDO	/	1.8V	
36	JTAG_nTRST	/	1.8V	
38	JTAG_TMS	/	1.8V	
40	JTAG_TDI	/	1.8V	
42	JTAG_TCK	/	1.8V	
44	JTAG_RTCK	/	1.8V	
46	JTAG_EMU0	11	1.8V	
48	JTAG_EMU1	31	1.8V	
50	T2.KPD_R0	/	1.8V	Square Scan Key R0
52	T2.KPD_R1	/	1.8V	Square Scan Key R1
54	T2.KPD_R2	/	1.8V	Square Scan Key R2
56	T2.KPD_R3	/	1.8V	Square Scan Key R3
58	T2.KPD_R4	/	1.8V	Square Scan Key R4
60	T2.KPD_R5	/	1.8V	Square Scan Key R5